“Characterization of depleted monolithic active pixel sensors with a column-drain read-out architecture in CMOS technologies”

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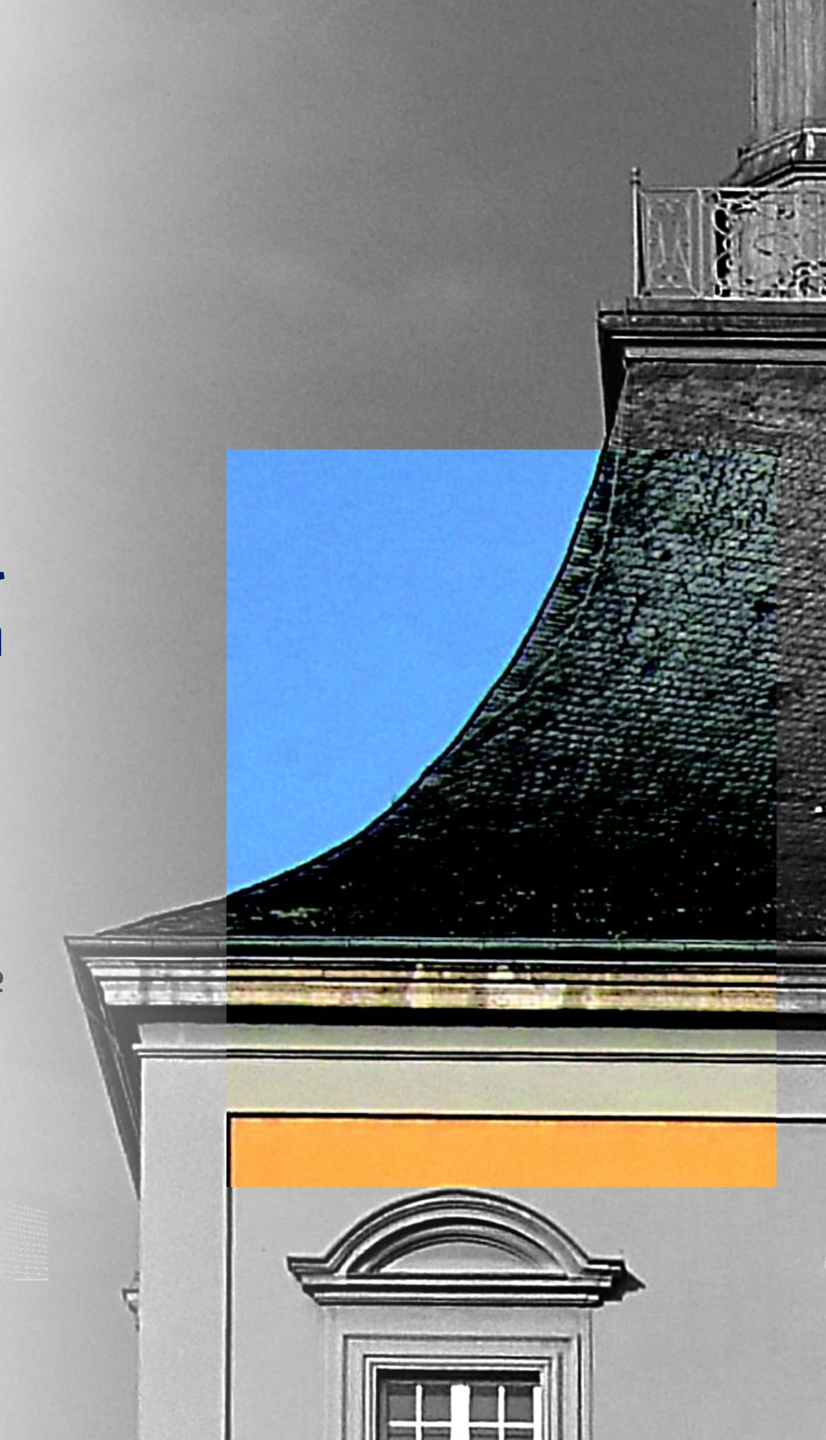

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STREAM

European Commission

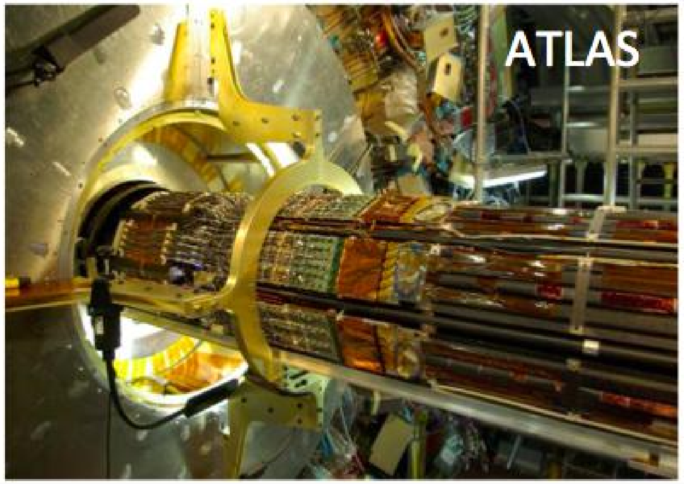
ATLAS INNER TRACKER UPGRADE FOR THE HL-LHC

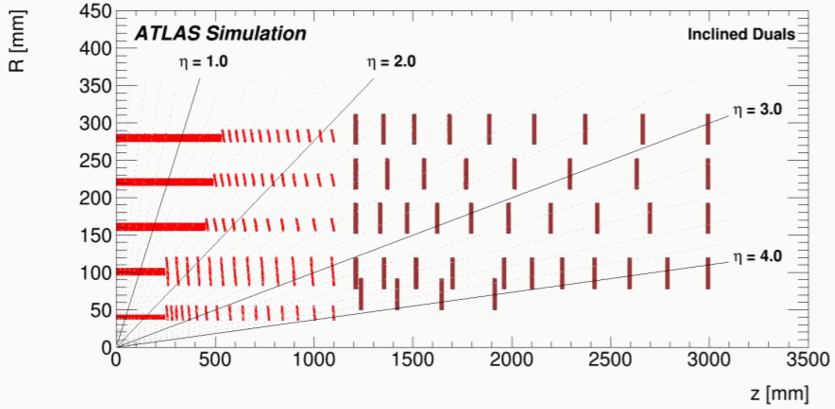
The ATLAS experiment will upgrade its inner tracker system for the HL-LHC

Max. instantaneous luminosity: of 7.5 x 10^{34} cm^{-2} s^{-1}
(~200 interactions per bunch crossing)

	Inner layer	Outer Layer
Occupancy	30 MHz/mm^2	1 MHz/mm^2
NIEL	10^{16} n_{eq}/cm^2	10^{15} n_{eq}/cm^2
TID	1 Grad	80 Mrad
Area	$O(1m^2)$	$O(10m^2)$

+ Fast R/O architecture with 25 ns precision





ATLAS ITK Pixel Layout
(CERN-LHCC-2017-021 / ATLAS-TDR-030)

Radiation-hard hybrid pixel sensors will remain as the baseline (RD-53):
- Significant material budget (3% Xo per layer).
- Complex (and expensive) module production.

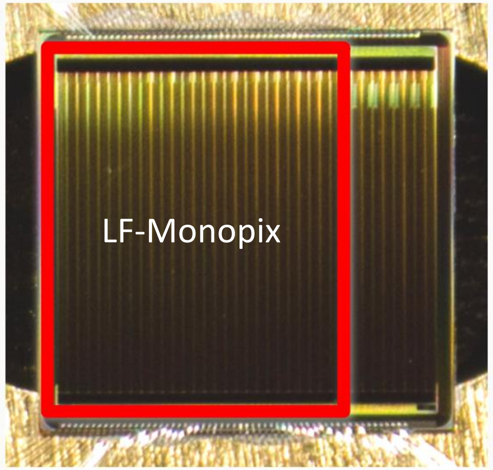
A complementary option for the outer layer?
Depleted monolithic sensors in CMOS technology

THE MONOPIX CHIPS

DMAPS with an integrated column-drain read-out architecture
(fast synchronous read-out architecture)

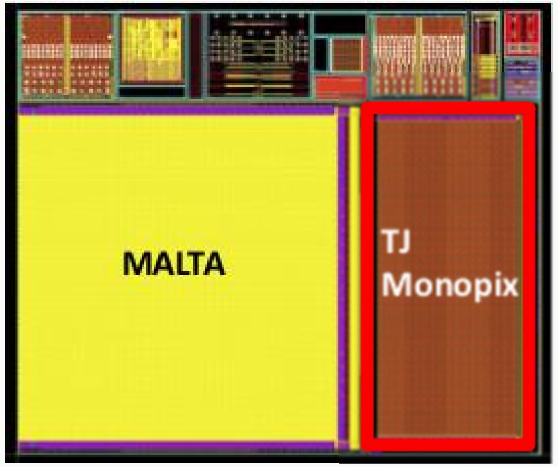
LF-MONOPIX01
(March 2017)

Large fill-factor design in **LFoundry 150 nm CMOS** technology



T. Wang, et al.
DOI: 10.1088/1748-0221/12/01/C01039
P. Rymaszewski et al.
DOI: http://doi.org/10.22323/1.313.0045
T. Hirono, et al.
DOI: 10.1016/j.nima.2018.10.059

TJ-MONOPIX01
(February 2018)

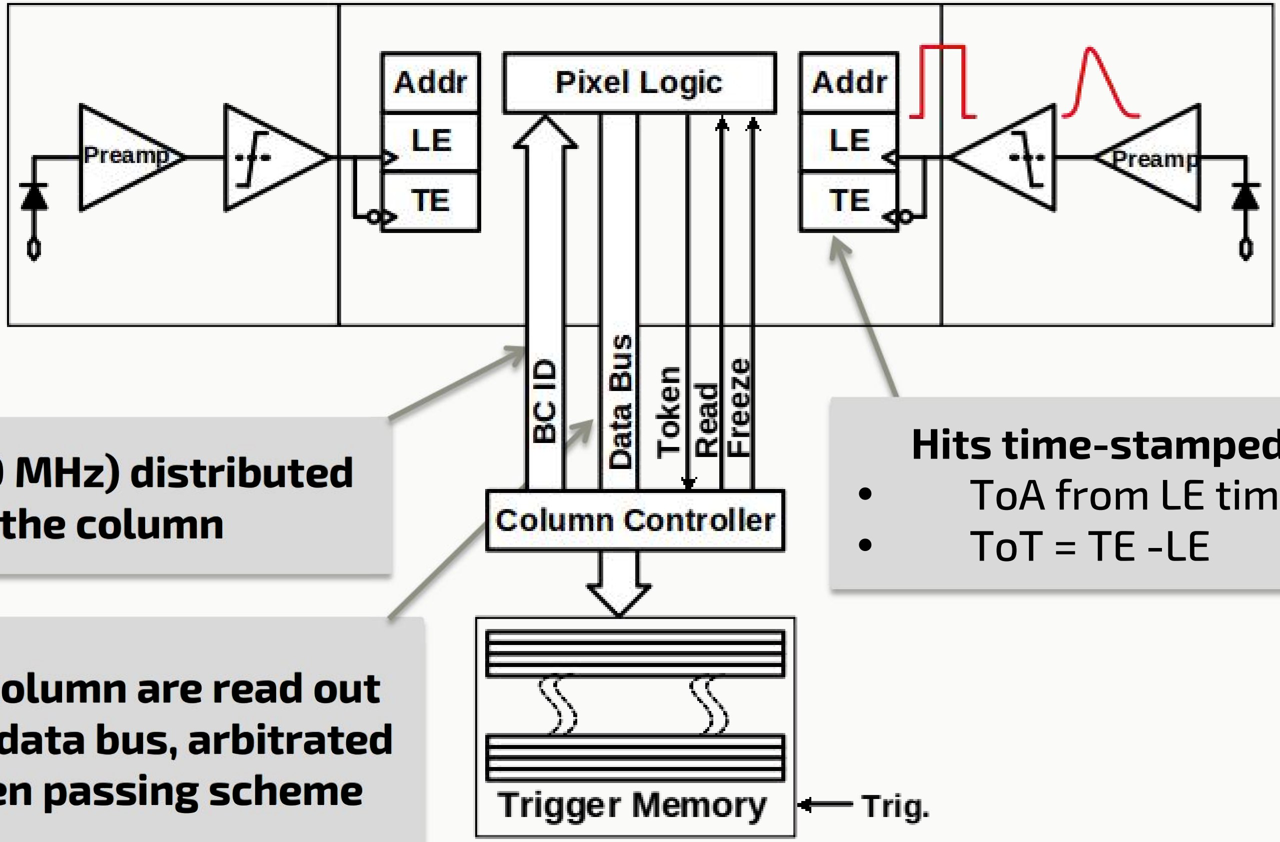


T. Wang, et al.
DOI: 10.1088/1748-0221/13/03/C03039
K. Moustakas, et al.
DOI: 10.1016/j.nima.2018.09.100

Small fill-factor design in **Towerjazz 180 nm CMOS** technology with a process modification

COLUMN-DRAIN R/O ARCHITECTURE

Why? Sufficient rate capability with affordable in-pixel logic density for CMOS pixels



BC ID (40 MHz) distributed in the column

Hits in the column are read out on a shared data bus, arbitrated by the token passing scheme

Hits time-stamped in pixel

- ToA from LE time stamp
- ToT = TE -LE

Column-drain has already proven to be capable to handle the hit rates of the current inner ATLAS pixel layers (FE-I3)

☑

Simulation studies for the outmost HL-LHC pixel layers agree

☑

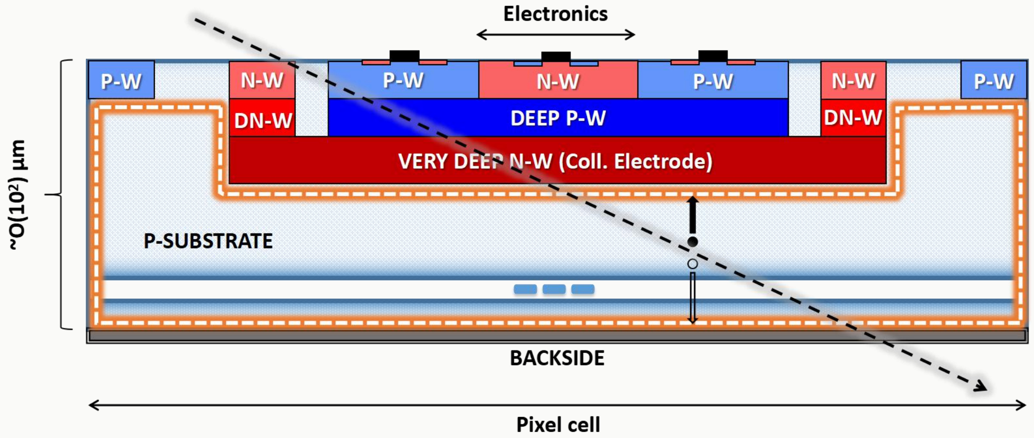
DEPLETED MONOLITHIC ACTIVE PIXEL SENSORS (DMAPS)

DMAPS in CMOS technology are suitable candidates for the outmost pixel layers

Commercial process, no hybridization (Reduced material budget and costs), considerable depleted regions in high-resistive substrates, fast charge collection by drift, multiple wells for shielding, scalable.

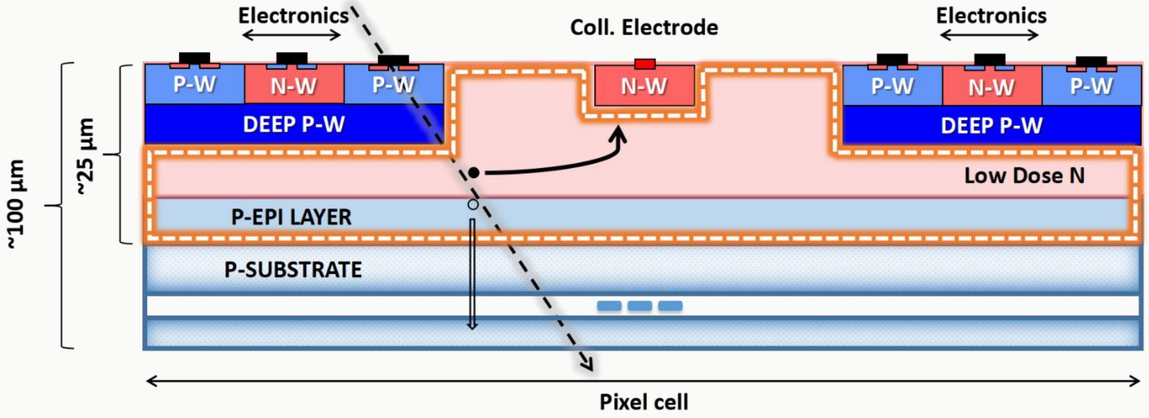
Two approaches:

"Large electrode design"
Collecting well containing all the electronics



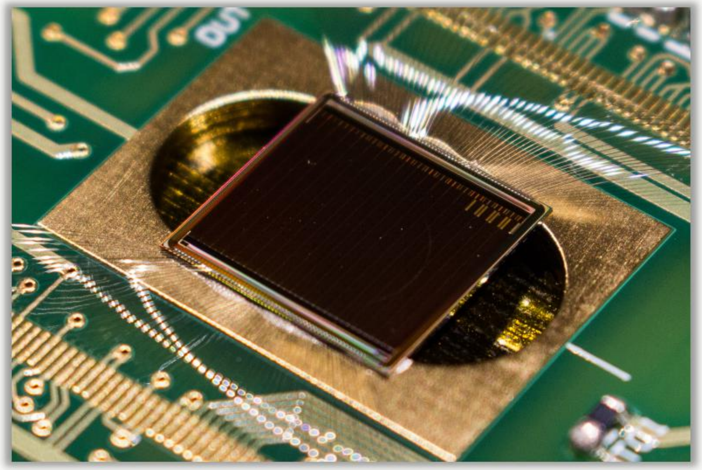
PROS: Short drift distances, strong E-field (Rad-hard)
CONS: Large sensor capacitance (Compromise on timing and noise), higher analog power.

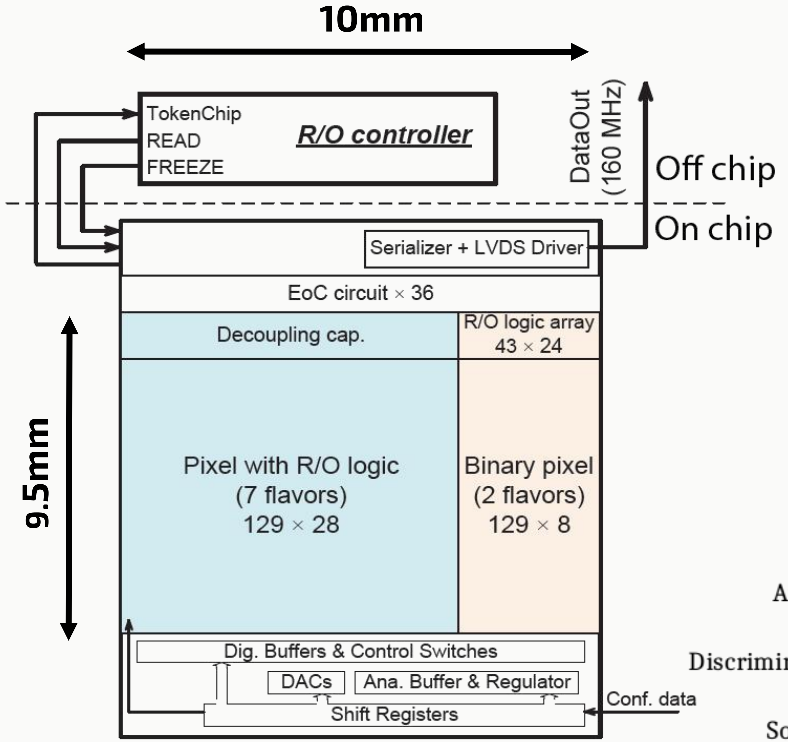
"Small electrode design"
Collecting well separate from the electronics

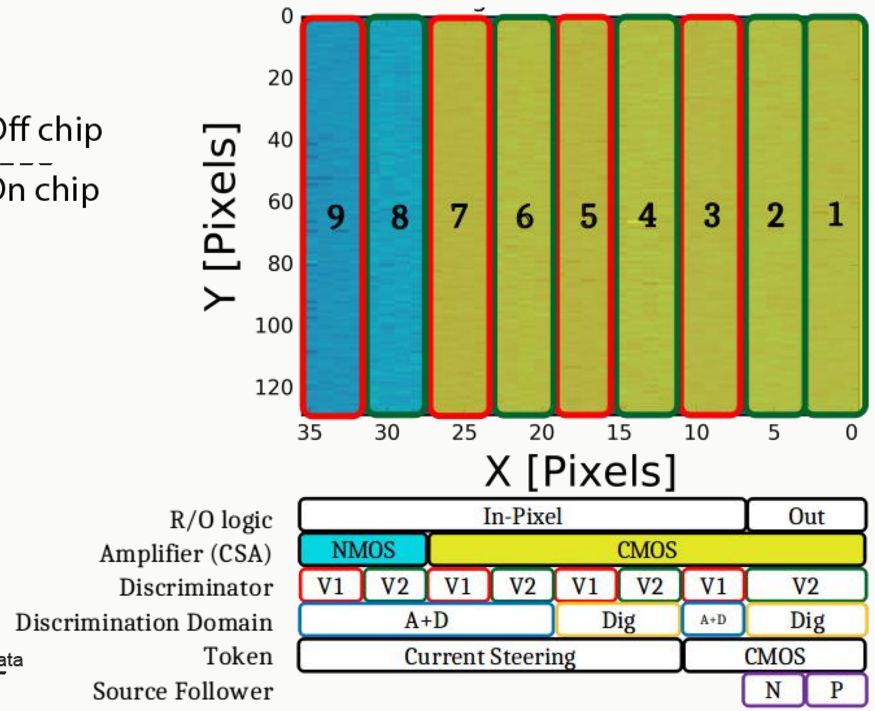


PROS: Very small sensor capacitance
CONS: Long drift distances, compromised rad-hardness

LF-MONOPIX01







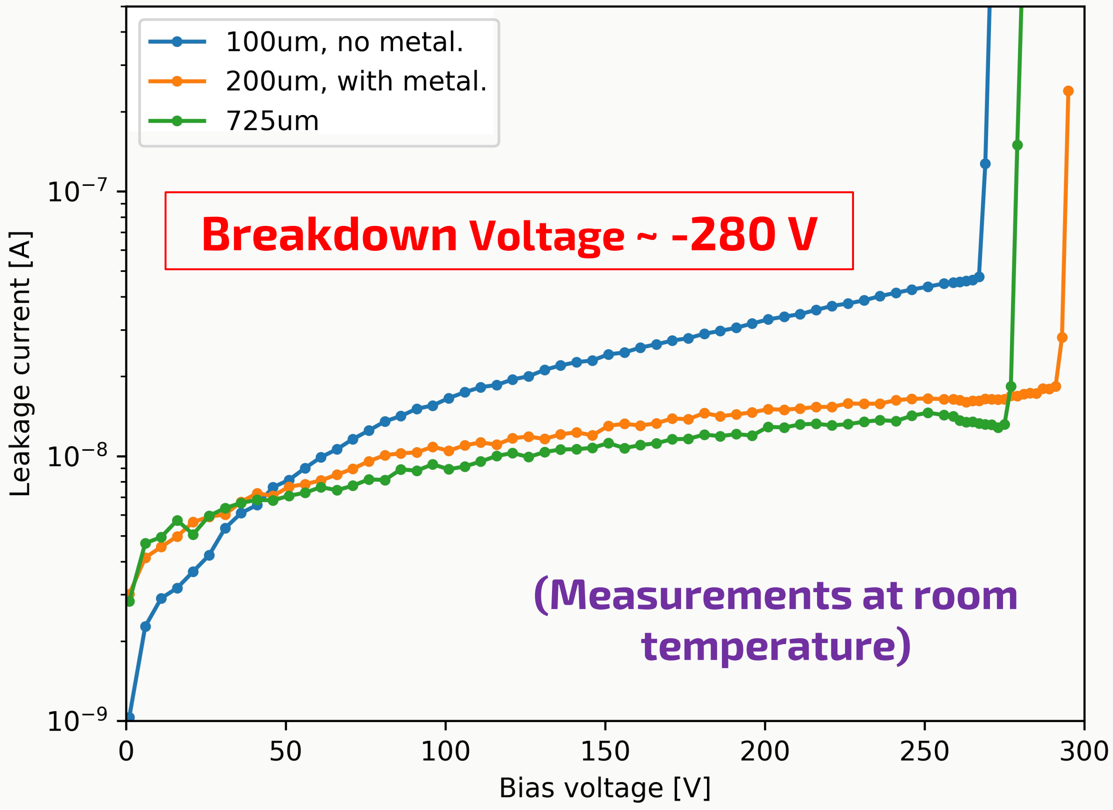
- **Fully functional synchronous column-drain read-out architecture.**
- High resistive substrate (**>2 kOhm-cm**)
- Large **50 x 250 µm²** pixel array (**129 x 36**)
- Bunch-crossing clock frequency (**40MHz clock**)
- 40 MHz (up to **160MHz** by design) LVDS serial output
- Charge sampling: **8-bit LE/TE time stamps (ToT)**
- Power: **55 µW/pixel (~1.7W/cm²)**

Radiation-hardness and sensor layout optimized in previous prototypes ☑

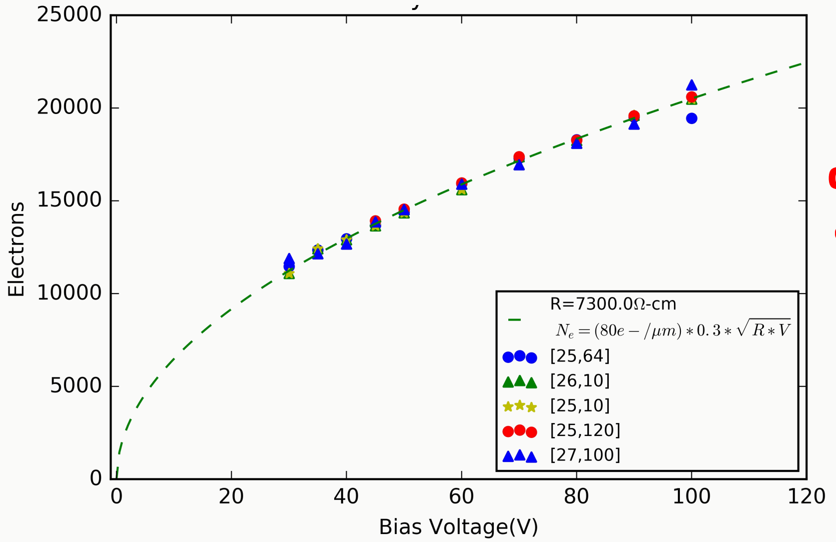
Succesful design efforts for cross-talk mitigation in digital lines ☑

Fast and low-power CSA and discriminator implementations ☑

BREAKDOWN AND DEPLETION

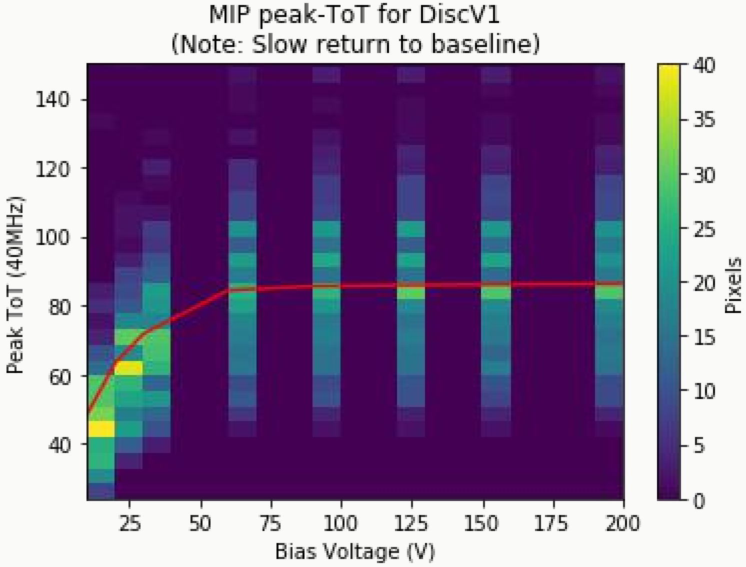


Most Probable Value for MIPs measured in LF-MONOPIX



Large collected charge (~10⁴ e-) in a highly resistive (>2 kOhm-cm) substrate.

☑

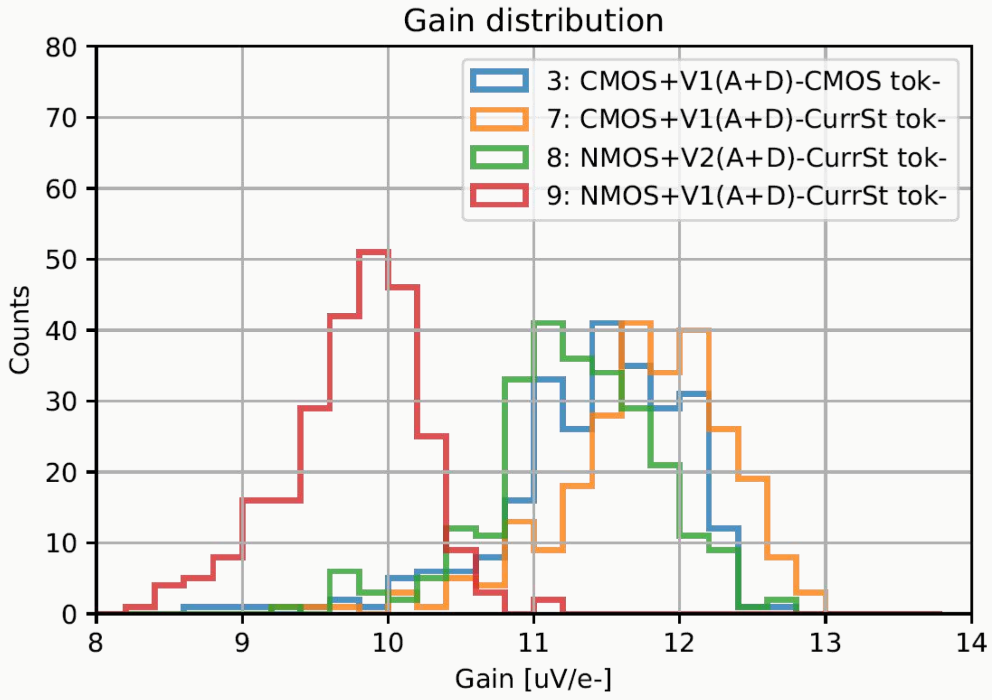


200μm thick chip fully depleted at ~60V

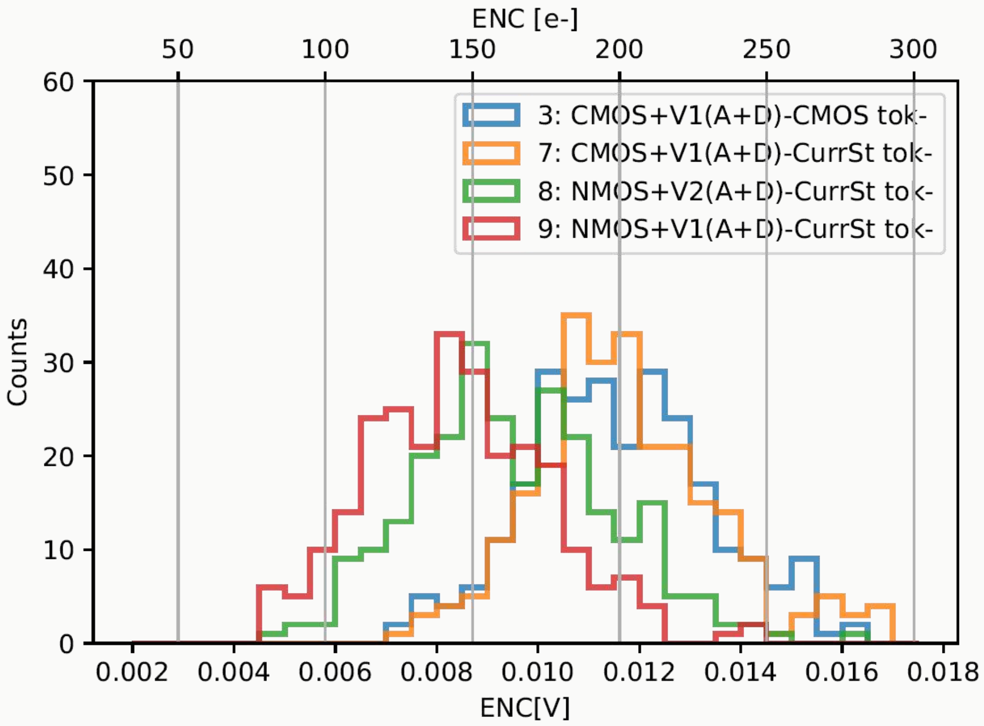
☑

GAIN AND NOISE

Gain within **10-12 µV/e-**
(Depending on the flavour implementation)



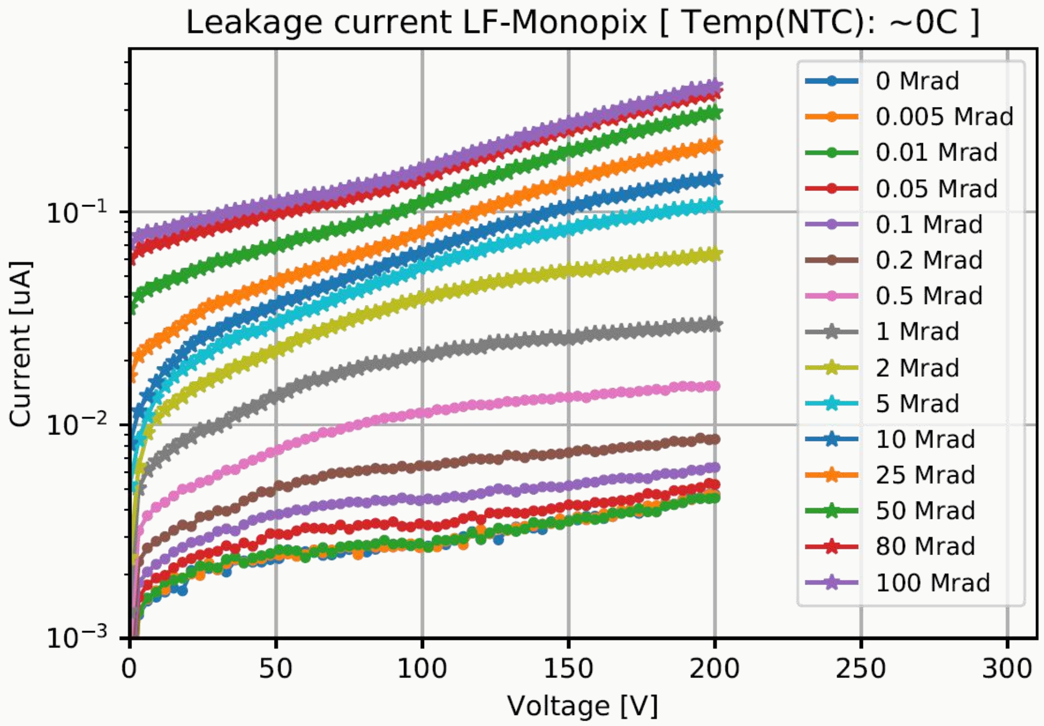
ENC within **140-210 e-**, with a **dispersion between 30 to 70 e-.**



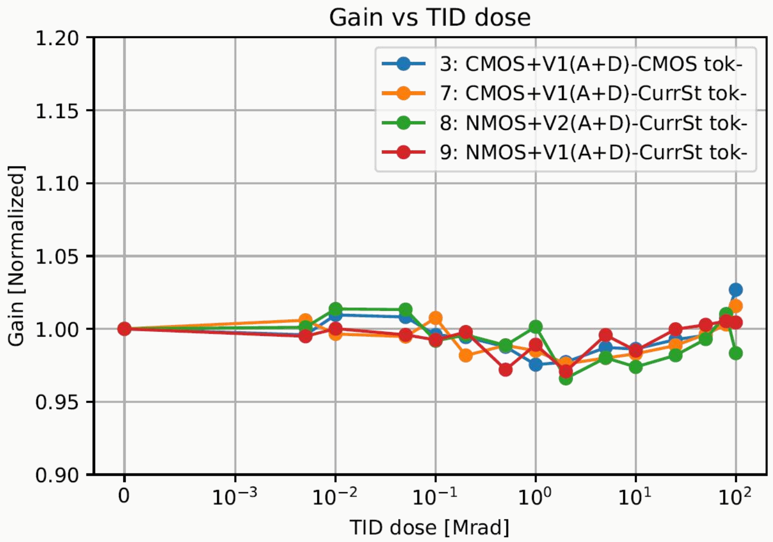
TID (X-RAY) EFFECTS

➢ Up to 100 Mrad (~0±2C temperature)

Leakage current increase of
~2 orders of magnitude



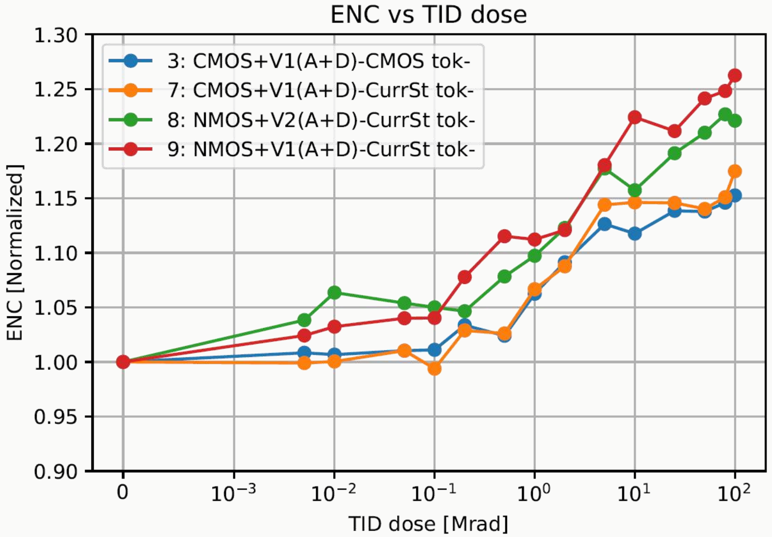
Relative gain fluctuations up to 3%



Relative ENC increase up to 25%

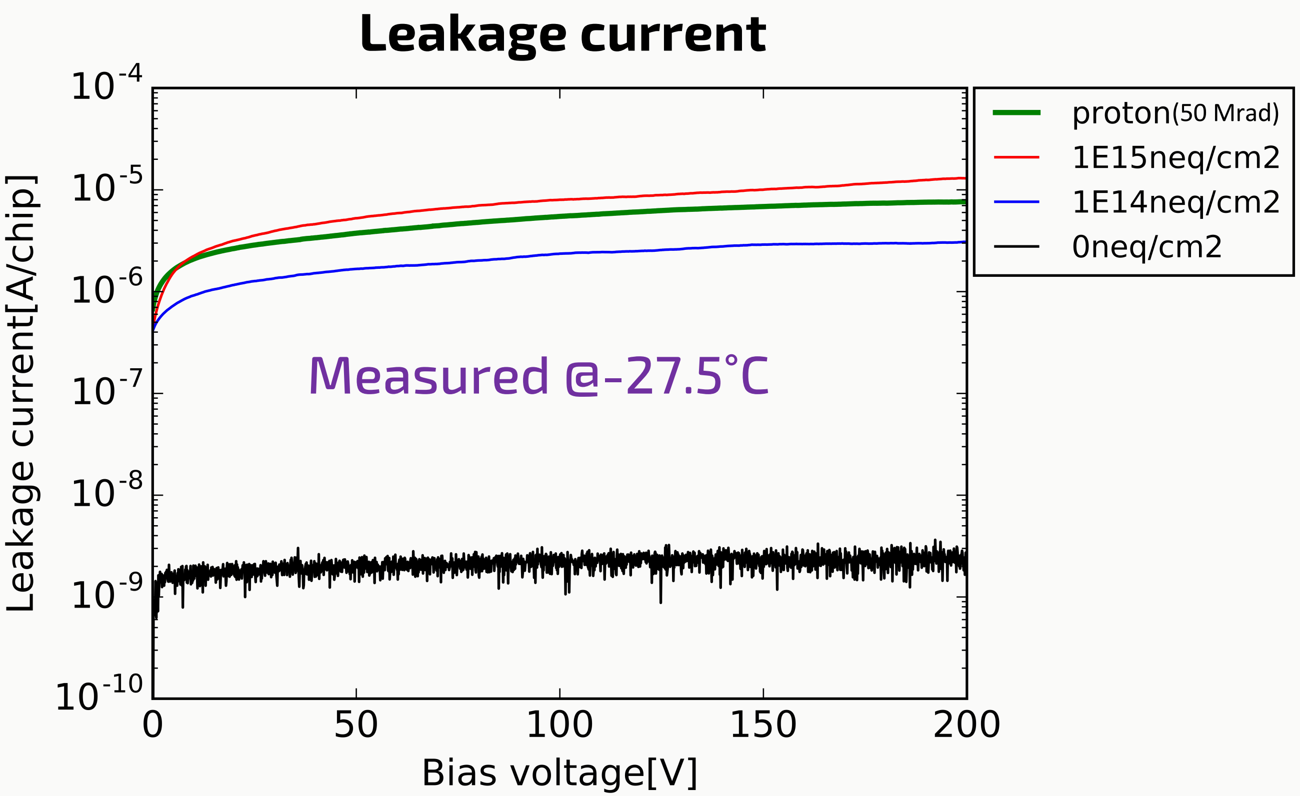
Note:

$ENC_{NMOS} < ENC_{CMOS}$



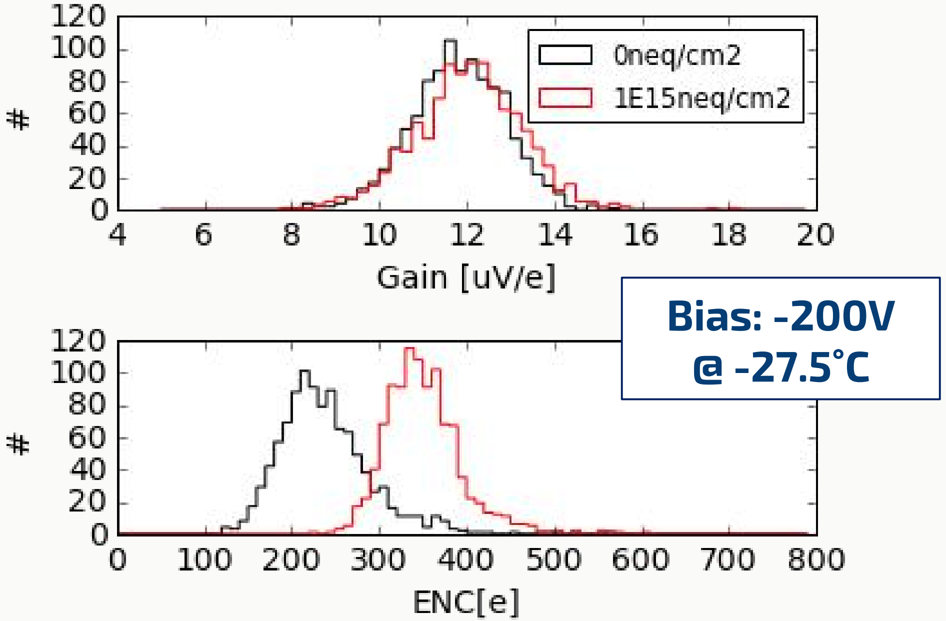
NIEL DAMAGE EFFECTS

** Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*



- **Breakdown voltage still > 200V** after 1 x $10^{15}n_{eq}/cm^2$ NIEL

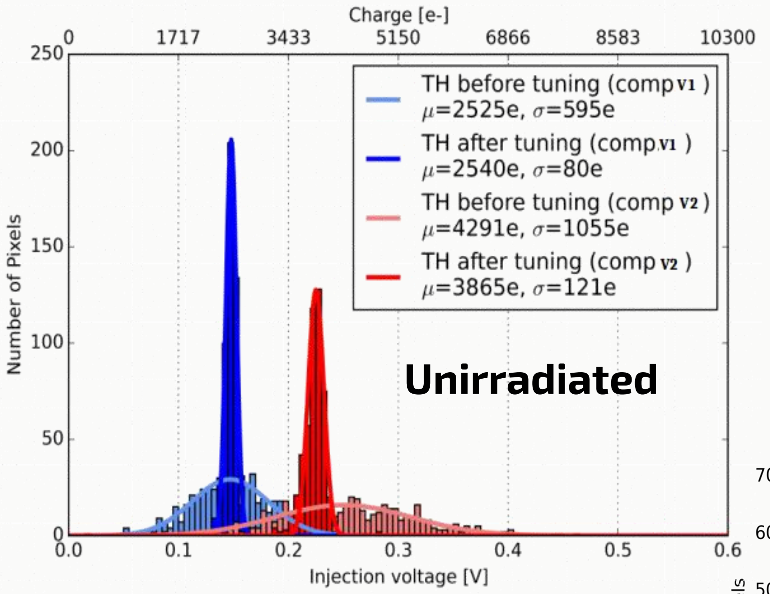
Performance after NIEL irradiation to $1x10^{15}n_{eq}/cm^2$



- **No loss in gain** after NIEL irradiation
- **Up to 150 e- noise increase** due to TID background in JSI

TUNING OF THRESHOLD DISTRIBUTIONS

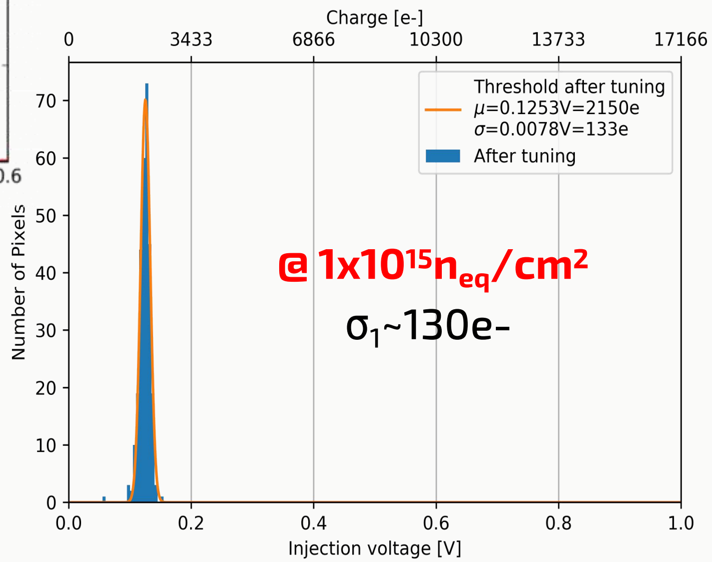
Injection tuning: *Fix global threshold*
+ *Binary search for optimal local threshold tuning*



→

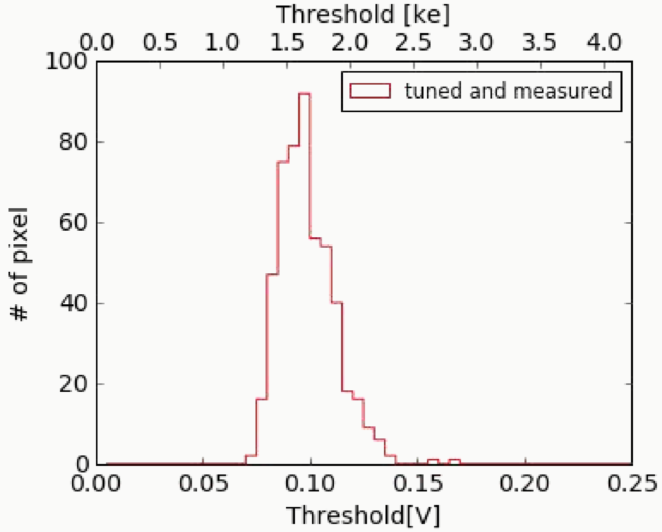
Before tuning:
$\sigma_2 >> \sigma_1$ (~600e-)
After tuning:
$\sigma_2 \sim \sigma_1$ (~100e-)

Threshold still tuneable after neutron irradiation →



@ $1x10^{15} n_{eq}/cm^2$
σ_1~130e-

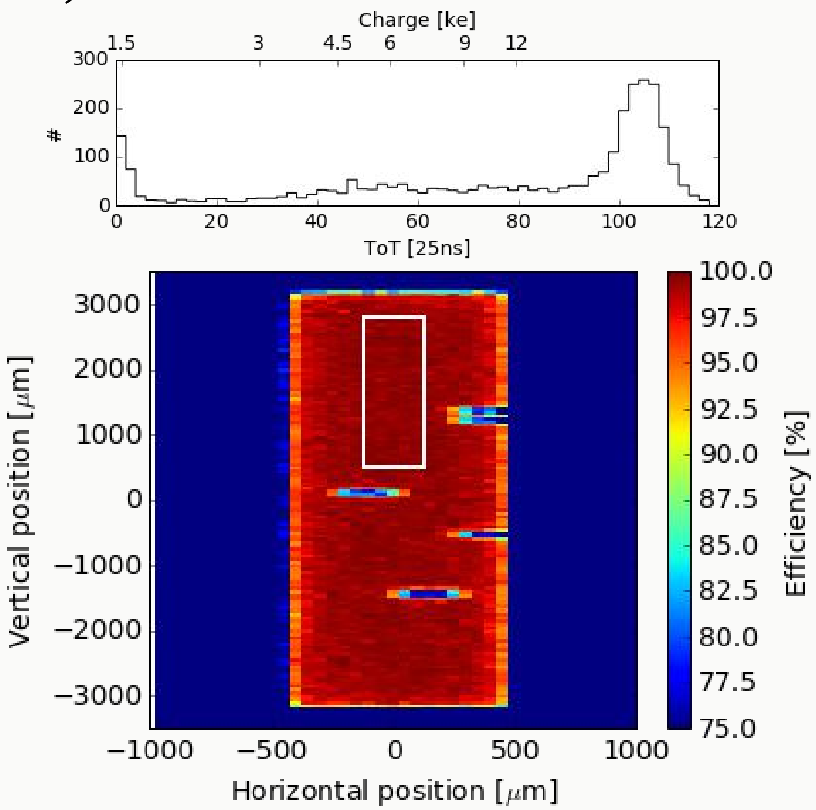
Baseline tuning: Lower global threshold close to baseline
+ *Tune local threshold according to noise hits*



- **Threshold tunable** down to **~1400e-** (Noise occ. < 10^{-7} hits/BX)
- Tuned threshold **dispersion ~100e-**

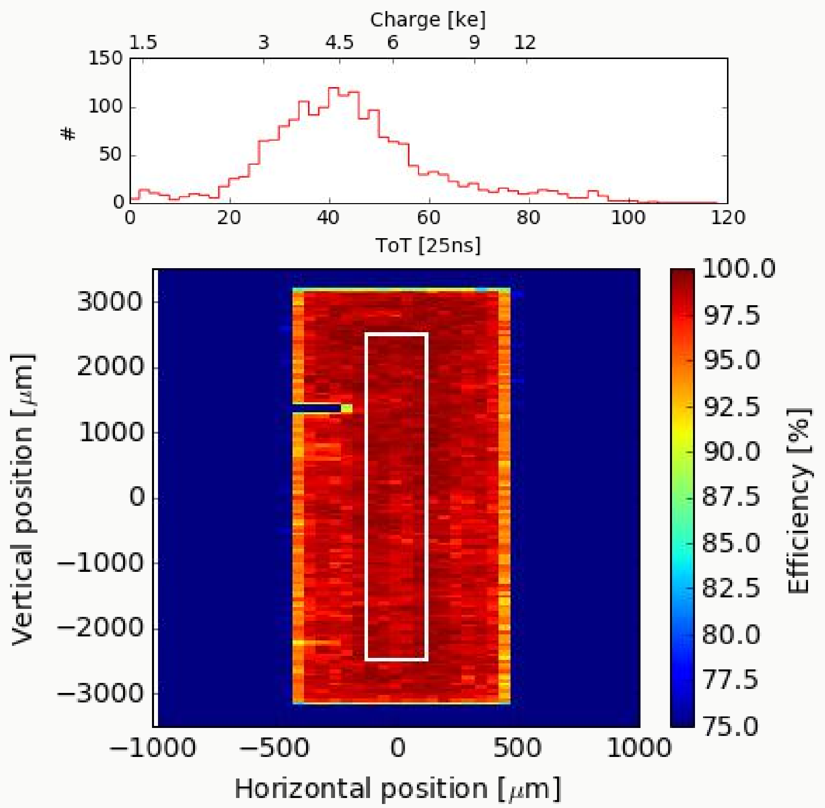
TB WITH 2.5 GEV ELECTRONS: HIT EFFICIENCY

– **Non-irradiated**
  - Hit efficiency **@ Noise occ. << 10^{-7} , TH~1700e- (<10^{-7} @ 1400e-)**
  - 1% masked pixels from noise tuning (not broken).



99.6% @ -200V

– **Neutron irradiated (1 x $10^{15} n_{eq}/cm^2$)**
  - Hit efficiency **@ Noise occ. < 10^{-8}, TH~1700e-**
  - < 0.2% masked pixels from noise tuning.
  - Efficiency loss between pixels, as expected.

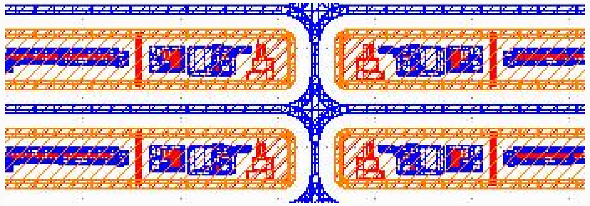


98.9% @-130V

(Voltage limited due to technical issues)

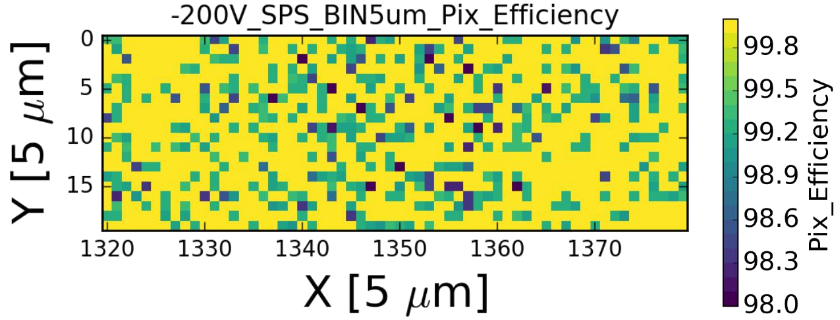
TB WITH 180 GEV PIONS: IN-PIXEL EFFICIENCY

- Deep N-well (Collecting electrode...)
- P-well (Inter-pixel region, isolation of electronics...)
- N-well (R/O electronics...)



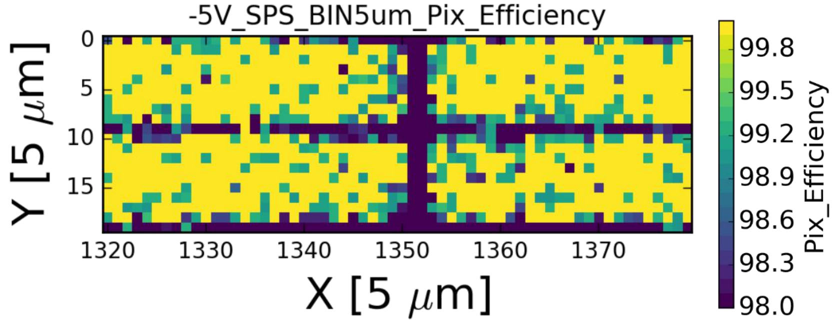
5 µm*5 µm bins

Uniform efficiency



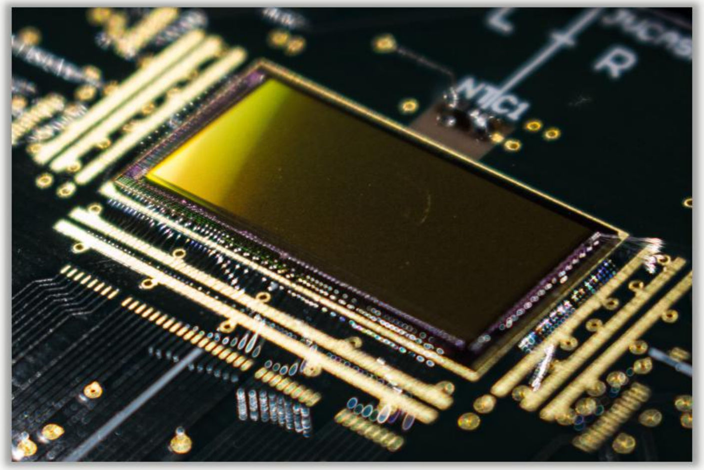
99.7% @ -200V

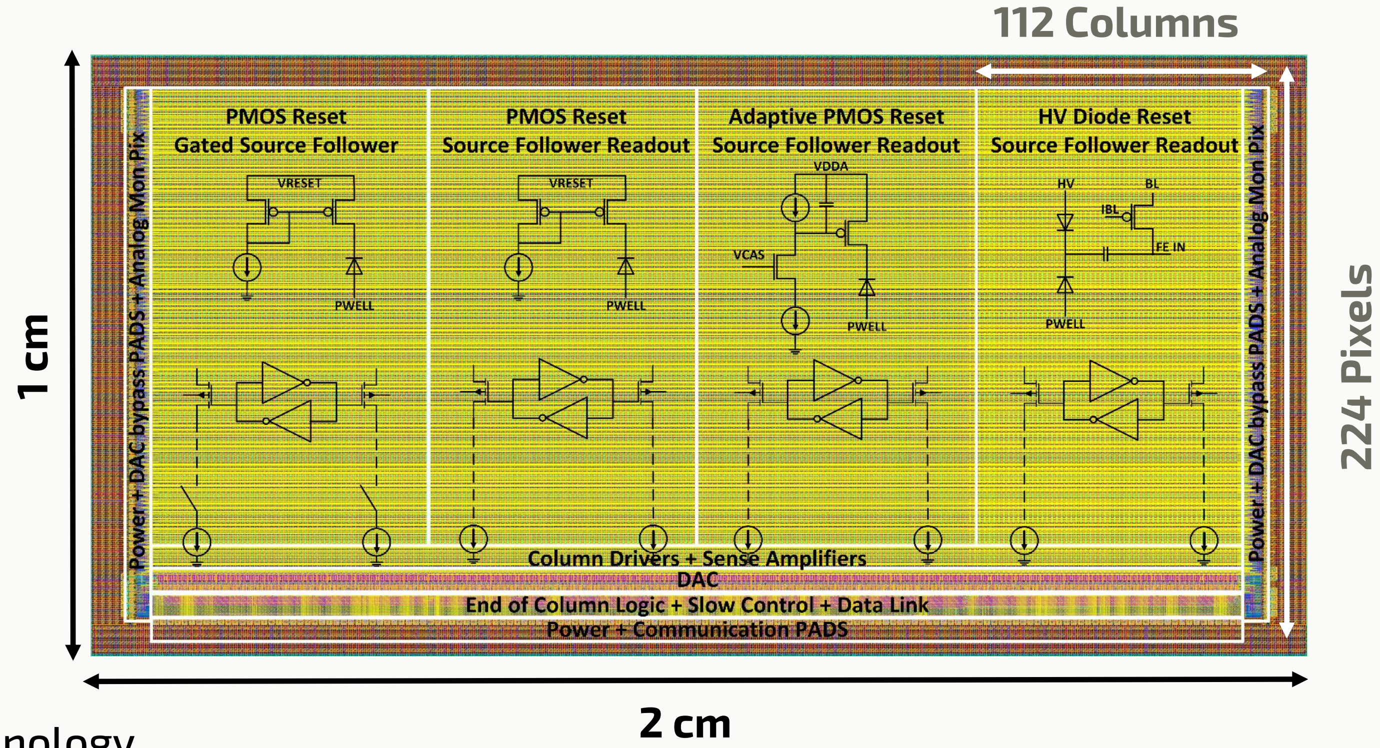
Efficiency drop only between pixels at VERY low bias voltage



98.8% @ -5V

TJ-MONOPIX01





- **Small fill-factor** design in **TJ 180 nm CMOS** technology
- Highly resistive p-epitaxial layer(**1 kOhm-cm**) with a process modification (additional n-type planar layer)
- Large **36 x 40 µm²** pixel array (**224 x 448**)
- Bunch-crossing clock frequency (**40MHz clock**)
- 40 MHz CMOS serial output per flavour
- Charge sampling: **6-bit LE/TE time stamps (ToT)**
- Power: **3 µW/pixel (~0.18 W/cm²)**

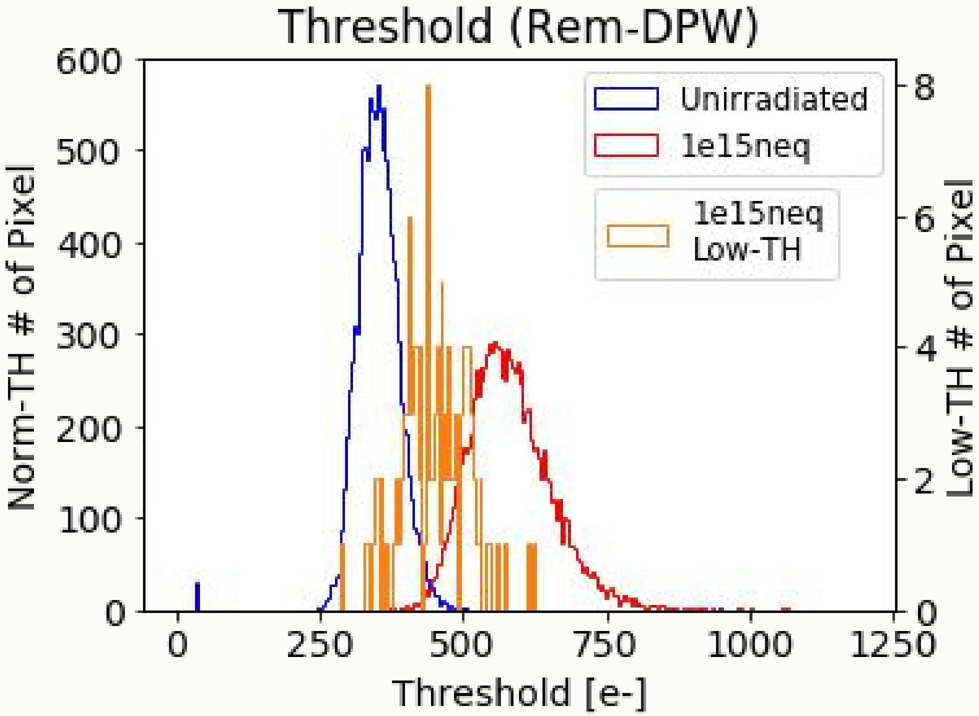
Fully integrated electronics in a small pixel volume ☑

Increased radiation tolerance with a modified process ☑

Low-noise and low-power analog front-end ☑

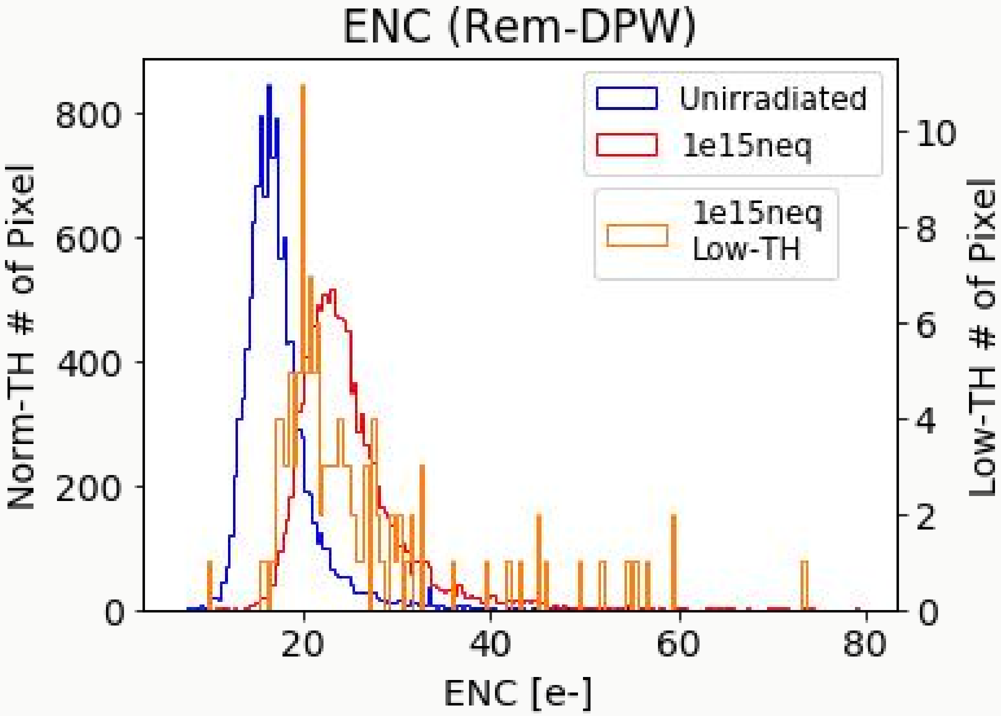
THRESHOLD AND NOISE

** Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*



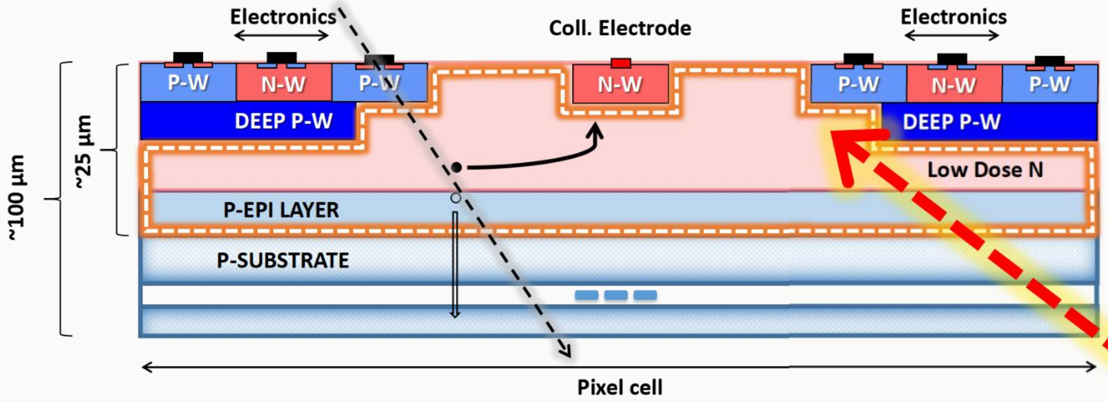
Unirradiated: μ= 349e-, σ=34e-

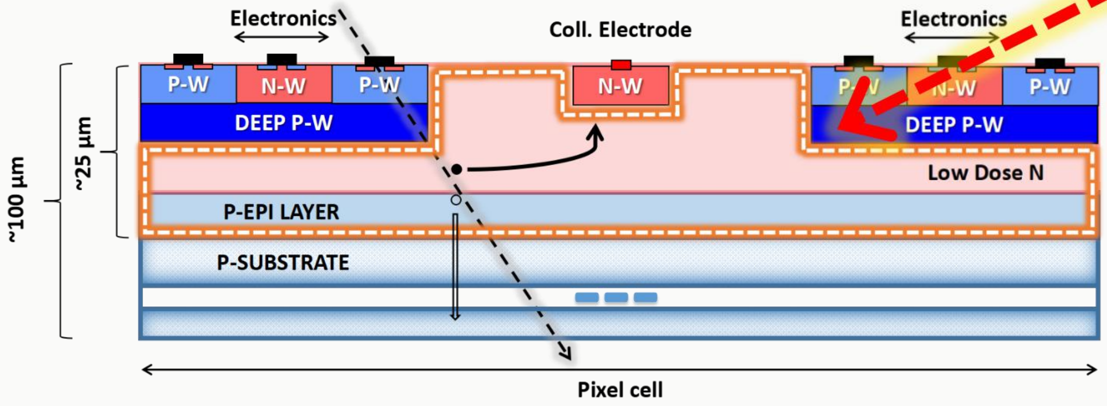
$1x10^{15}$ Irradiated: μ= 569e-, σ=66e-



ENC increased by ~10e- after $1x10^{15}\ n_{eq}/cm^2$ (Probably due to TID bckg)

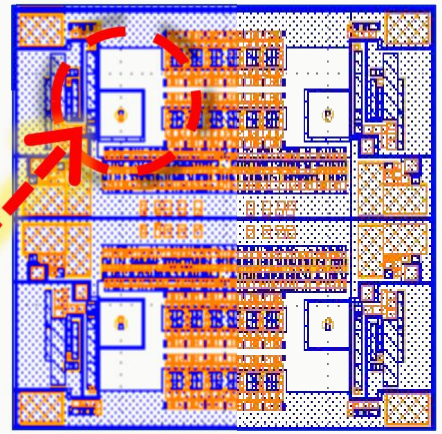
PIXEL LAYOUT AND P-WELL COVERAGE

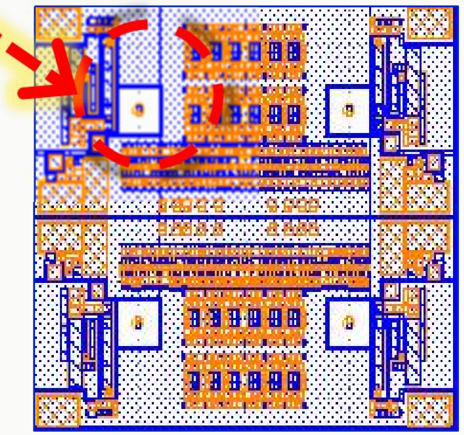




Different P-well coverage on top and bottom column regions

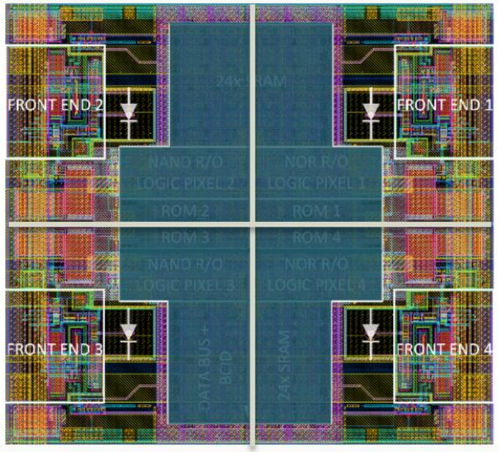
2x2 pixel array (Top view)

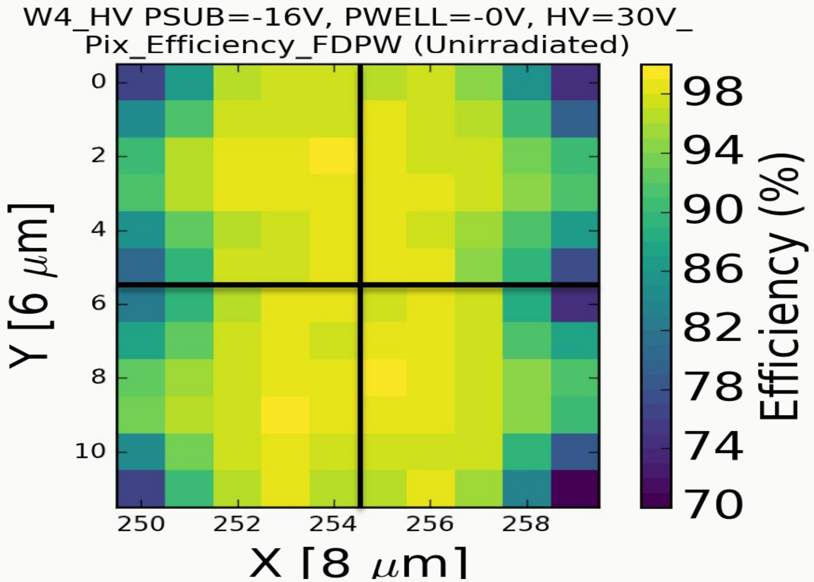


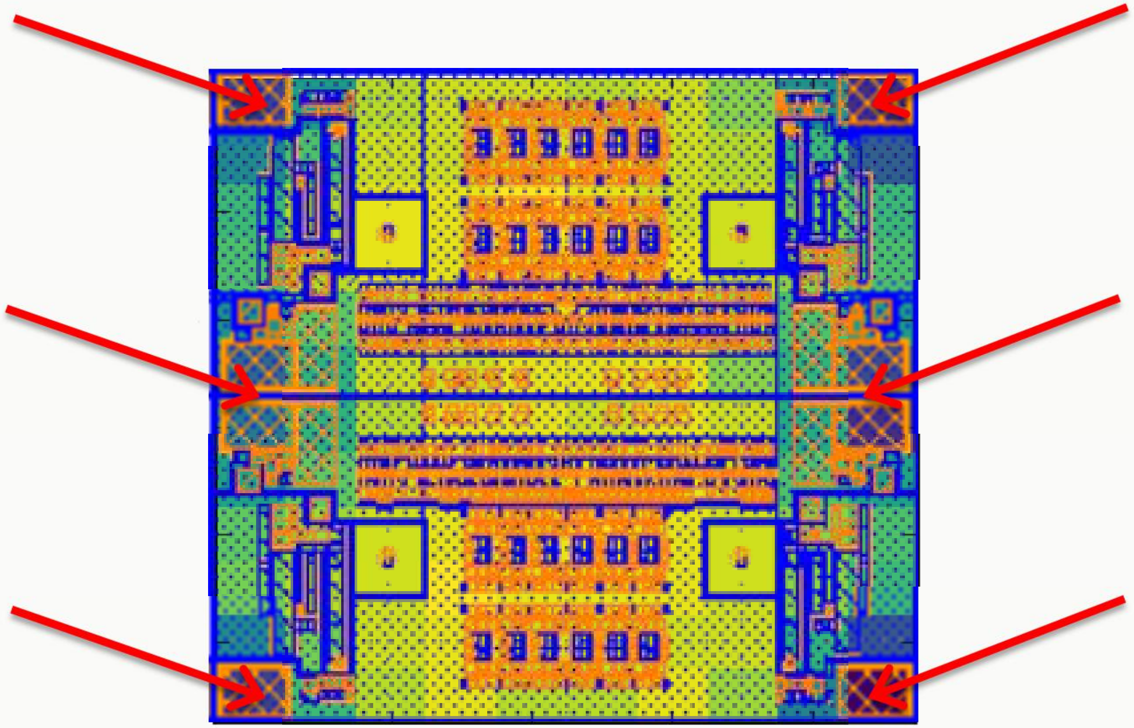


IN-PIXEL EFFICIENCY (UNIRRADIATED)

2x2 Pixel Array







Low efficiency "corners" correlated with **large active areas** used for decoupling capacitors

---> Design layout to be optimized in future designs

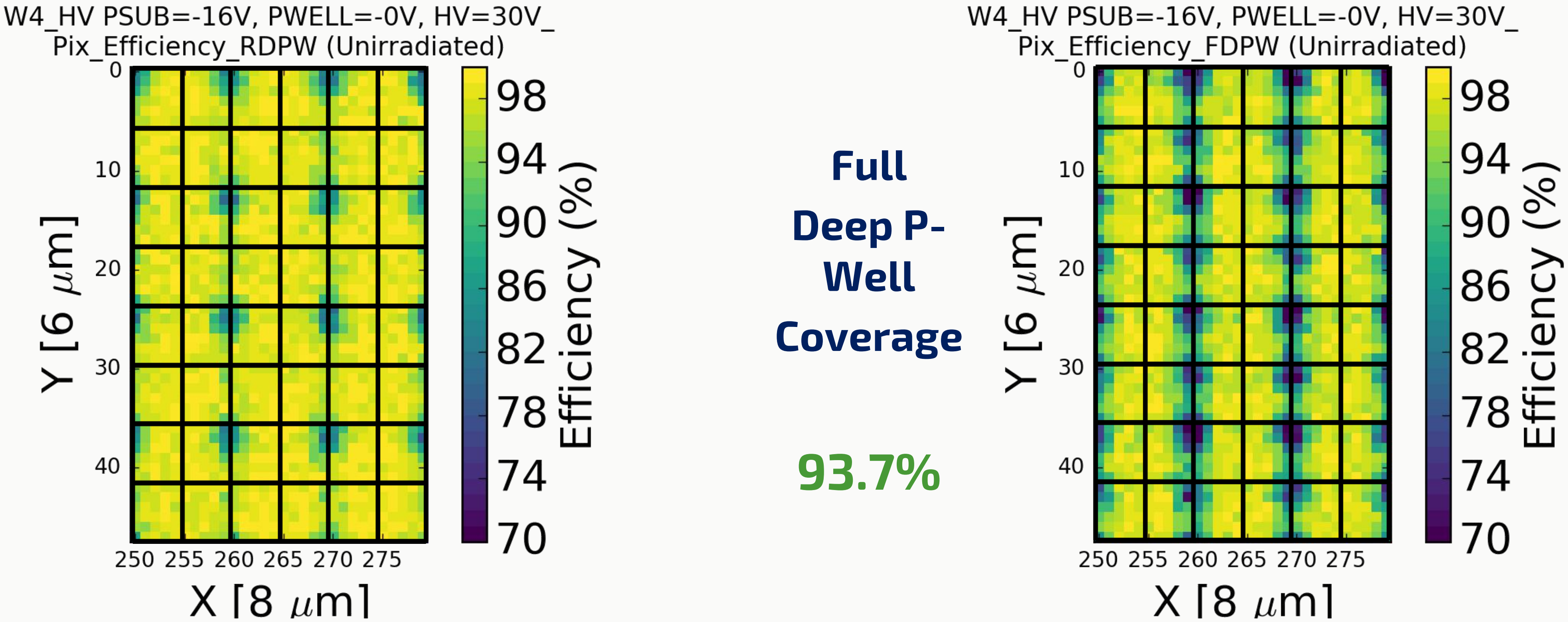
MEAN HIT EFFICIENCY VS DEEP P-WELL COVERAGE

Removed Deep P-Well Coverage

97.1%

Full Deep P-Well Coverage

93.7%



- Lower efficiencies in Full DP-Well regions (Bottom) than in Removed DP-Well (Top) ones.

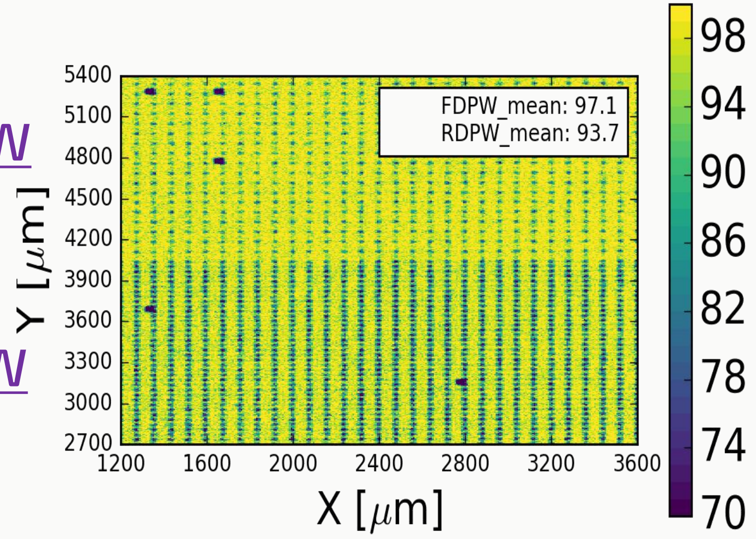
MEAN HIT EFFICIENCY AFTER IRRADIATION

In MALTA
(very similar front-end and pixel pitch)

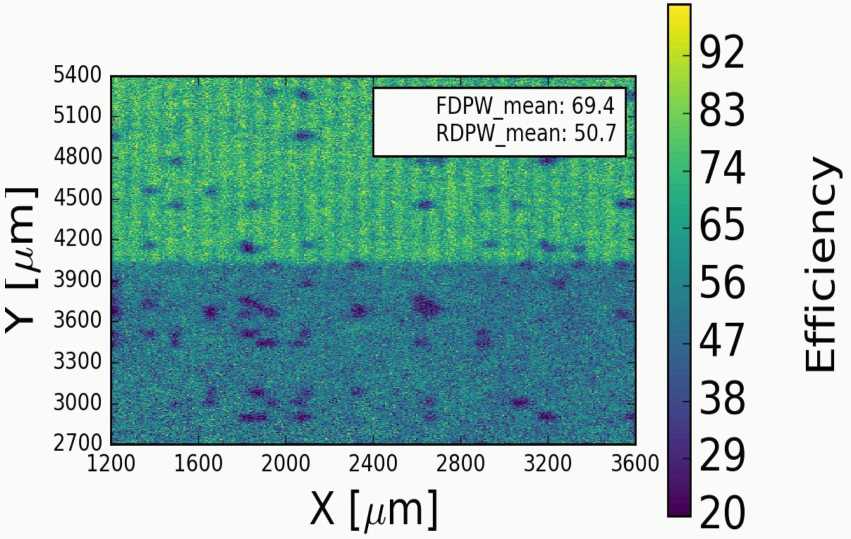
R-DPW

F-DPW

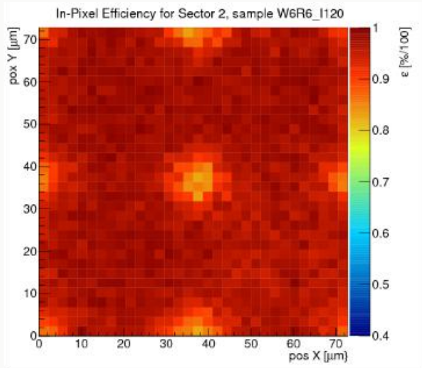
UNIRRADIATED



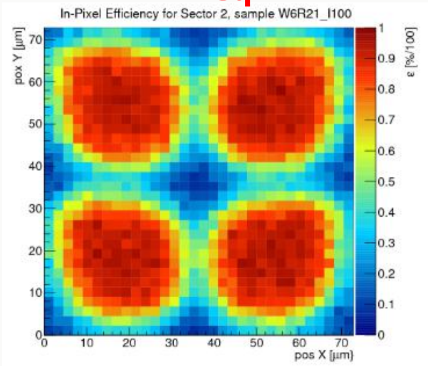
$1x10^{15}$ n_{eq}/cm^2



UNIRRADIATED



$5x10^{14}$ n_{eq}/cm^2



As discussed in MALTA related presentations

Large efficiency drop (30-50%) after $1x10^{15}$ n_{eq}/cm^2 neutron irradiation.

---> Fixes to the TJ modified process in pixel corners to enhance E-Field

(M. Munker, DOI: 10.1088/1748-0221/14/05/C05013)

CONCLUSIONS

Two fully monolithic CMOS pixel detectors in both small and large fill factor designs with an **operational column-drain read-out architecture** were characterized.

	LF-MONOPIX01		TJ-MONOPIX01	
DMAPS type	*Large electrode design (150nm CMOS | LFoundry)*		*Small electrode design (180nm CMOS, mod. | Towerjazz)*	
Dimensions	1 x 1 cm²		2 x 1 cm²	
Pixel size	250 x 50 µm²		40 x 36 µm²	
	Non-Irrad	$10^{15} n_{eq}/cm^2$	Non-Irrad	$10^{15} n_{eq}/cm^2$
Signal MPV	~23.3ke- (@130V)	~4.6ke- (@130V)	~1.6ke-	~1.4ke-
ENC	~200±50e	~350±50e	~15±2e	~25±3e
Threshold	>1400±100e	>1700e±130e	>350e±35e	>570e±65e
Mean Effic.	99.6%	98.9%	97.1%	69.4%

WHAT'S NEXT?

LF-MONOPIX02 (end 2019)

- Next iteration with CSA and discriminator with the best performance (noise, timing-wise) and radiation hardness.
- Full-size-like columns (~2cm length)
  ---> Requires design effort regarding long column effects.
- Smaller pixel size (~150x50 μm^2) to reduce detector capacitance.
- Optimization of the read-out logic

	LF-Monopix02	RD53 outer layer
Pixel size	50 × 150 μm^2	50 × 50 μm^2
Analog power	16 - 20 μA/pixel	3 - 4 μA/pixel
Digital power	4 - 5 μA/pixel	2 - 3 μA/pixel
In-time thres.	1500 - 2000 e$^-$	1500 e$^-$
Min. detectable charge	1000 - 1500 e$^-$	1000 e$^-$

TJ-MONOPIX02 (end 2019)

- Details discussed in K. Moustakas (ESR5) presentation.

MAIN ESR6 OUTPUT

STREAM Deliverables

- “D-3.1 Layouts for event driven pixel sensors as hybrid and monolithic sensor”. July, 2017.
- “M.S.7 Charge collection optimization of radiation hard designs”. December, 2017.
- “D-3.2 Implementation of ITK-relevant readout architecture to CMOS sensor”. December, 2018.

Presentations

- Talks at the annual meeting of the German Physics Society (DPG). 2017, 2018, 2019.
- **“Characterization of a Depleted Monolithic Active Pixel Sensor prototype in a 150 nm CMOS process for operation in harsh radiation environments”** Oral presentation at the IEEE NSS-MIC Conference. Atlanta, USA. October 21-28, 2017.
- ***“The Monopix chips: Depleted monolithic active pixel sensors with a column-drain read-out architecture for the ATLAS Inner Tracker upgrade”.*** Oral presentation at the PIXEL2018 Workshop. Taipei. December 10-14, 2018.

Publications

- Co-Author in 10 publications related to the CMOS monolithic developments.
- Main author of the PIXEL 2018 conference record publication (Details in “Presentations”)

Others

- *STREAM trainings (project management, entrepeneurship, etc.)*
- Presentations at the ITk-Week and CMOS weekly meetings.

Thank you to everybody who made STREAM possible.

Q&A Time!

This research project received funding from the European Union's Horizon 2020 Research and Innovation programme under Grant Agreement no. 654168.

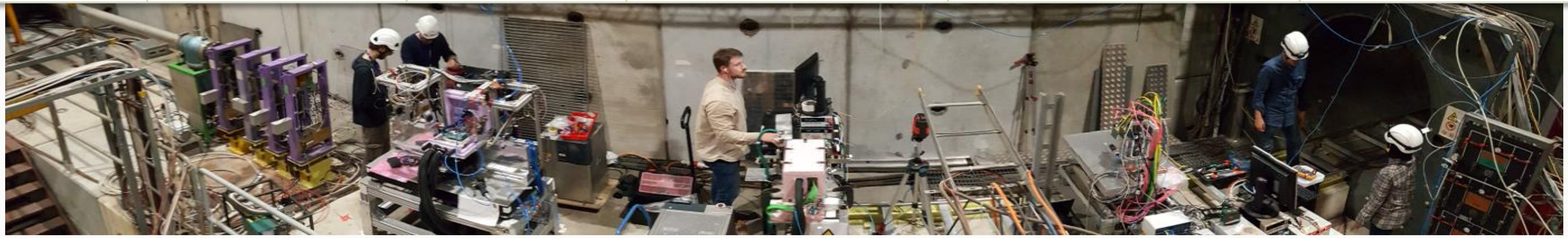
Moreover, it has been supported by a Marie Skłodowska-Curie Innovative Training Network Fellowship of the European Union's Horizon 2020 Research and Innovation Programme under grant agreement 675587-STREAM.

CMOS DEMONSTRATOR PROGRAM

A collaborative R&D effort within ATLAS focused on DMAPS prototypes with fast read-out architectures in different CMOS processes.

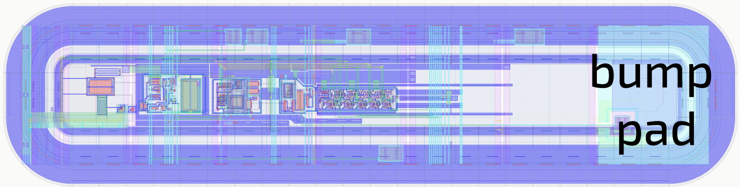
Previous iterations of these prototypes (passive sensors, or active ones with a first stage of the Front-End within the pixel) allowed to optimize the designs and improve radiation-hardness.

Chip name	Technology	Fill factor	Pixel size [μm²]	R/O architecture	Status
ATLASpix	Foundry 1 180nm	Large	56 x 56	Asynchronous	Measurements
MALTA	Foundry 2 180nm	Small	36 x 36	Asynchronous	Measurements
TJ Monopix		Small	36 x 40	Synchronous	
Coolpix		Large	50 x 250	Synchronous	
LF Monopix	Foundry 3 150 nm	Large	50 x 250	Synchronous	Measurements
LF2		Large	50 x 50	Synchronous	



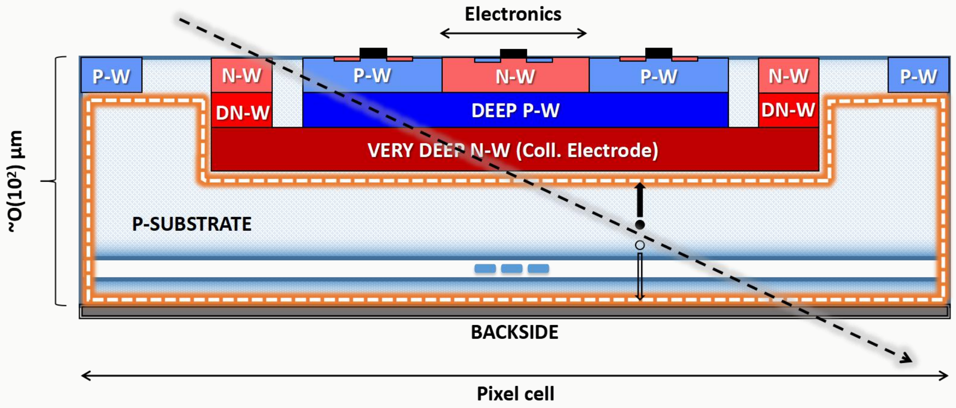
FROM LF-CPIX TO LF-MONOPIX

LF-CPIX Demonstrator (50 x 250 μm²)



LF-MONOPIX01 (50 x 250 μm²)

Large fill factor design. C_d~ 400fF



An increase in detector capacitance has implications on **timing** and **noise**

$$\tau_{CSA} \propto \frac{1}{g_m}\frac{C_d}{C_f} \qquad ENC^2_{thermal} \propto \frac{4}{3}\frac{kT}{g_m}\frac{C_d^2}{\tau}$$

Electronics are directly coupled to the collecting node through C_{pw}

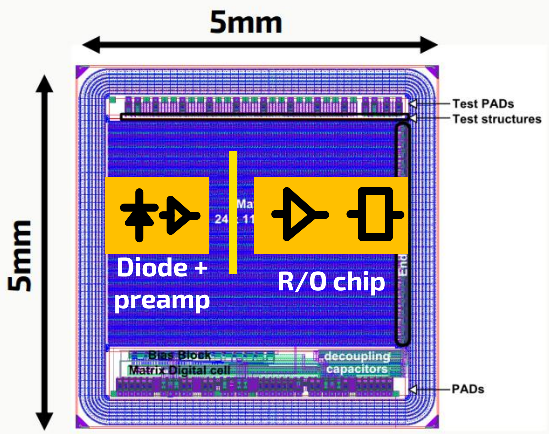
- Special efforts on design to minimize cross-talk with digital signals
- Increase of minimum operational threshold

PROTOTYPE DEVELOPMENT LINE

KIT — Karlsruhe Institute of Technology

CCPD_LF

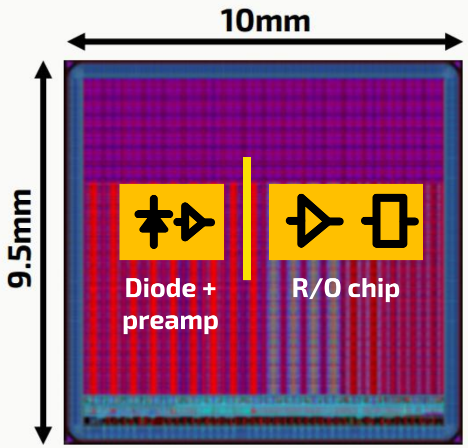
- Subm. in Sep. 2014
- 33 x 125 µm² pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test



Irfu - CEA Saclay — Institut de recherche sur les lois fondamentales de l'Univers

LF-CPIX (DEMO)

- Subm. in Mar. 2016
- **CPIX Demonstrator in LF**
- 50 x 250 µm² pixels
- Fast R/O coupled to FE-I4
- Standalone R/O for test



Irradiated without substantial performance loss

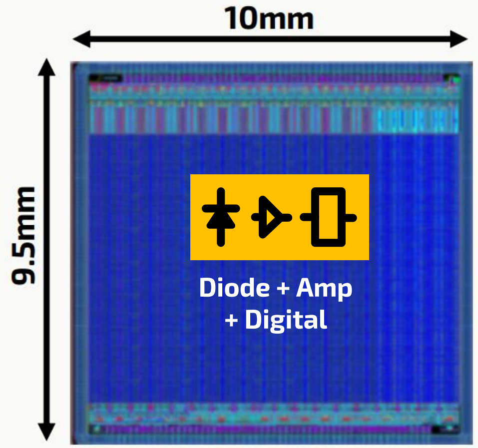
LF-MONOPIX01 (Monolithic)

Irfu - CEA Saclay — Institut de recherche sur les lois fondamentales de l'Univers

- Subm. in Aug. 2016

(Back: End of Mar. 2017)

- "Demonstrator size"
- 50 x 250 µm² pixels
- 150 nm CMOS
- **Fast (Col. Drain) standalone R/O**

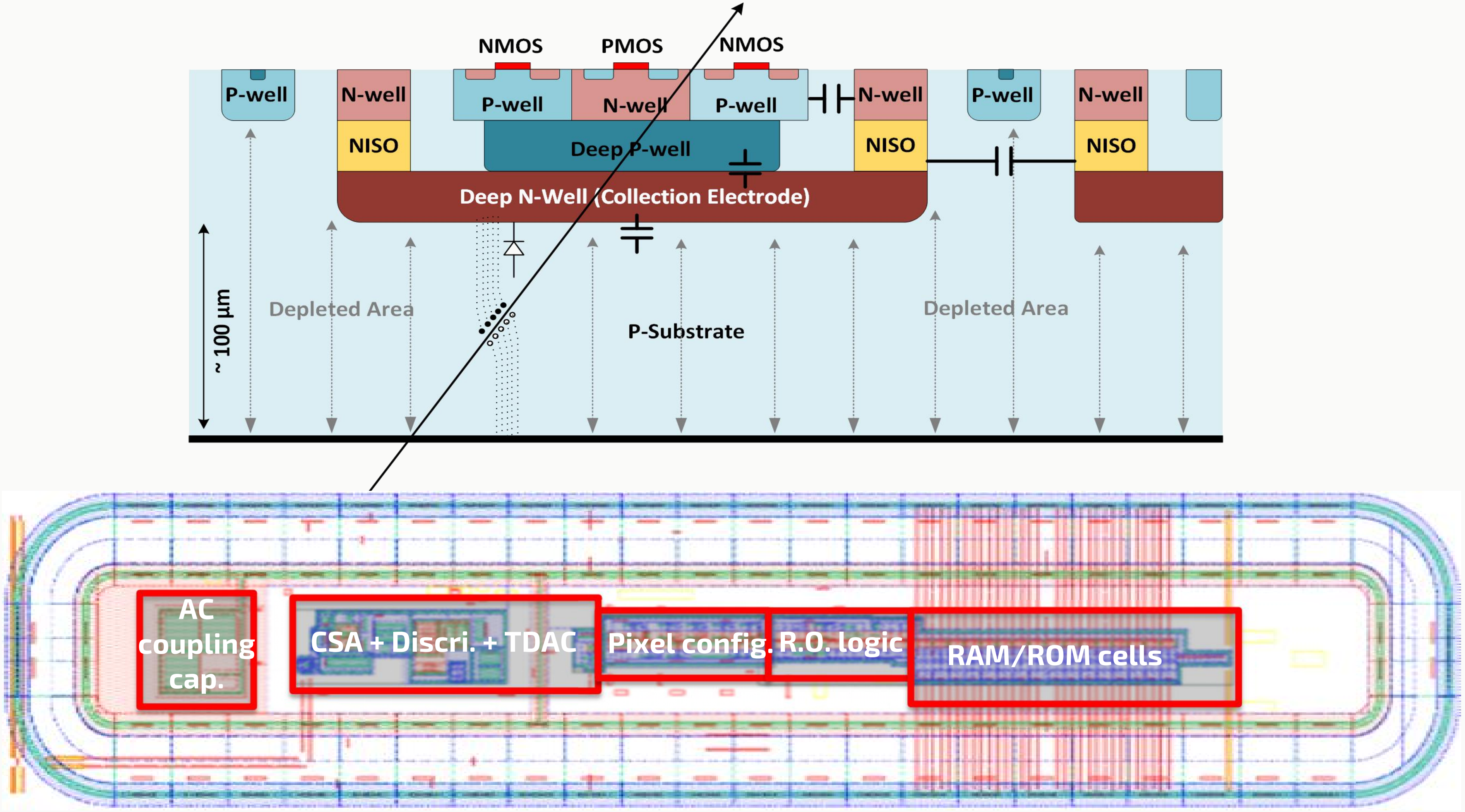


Fully integrated Speed and digital R/O

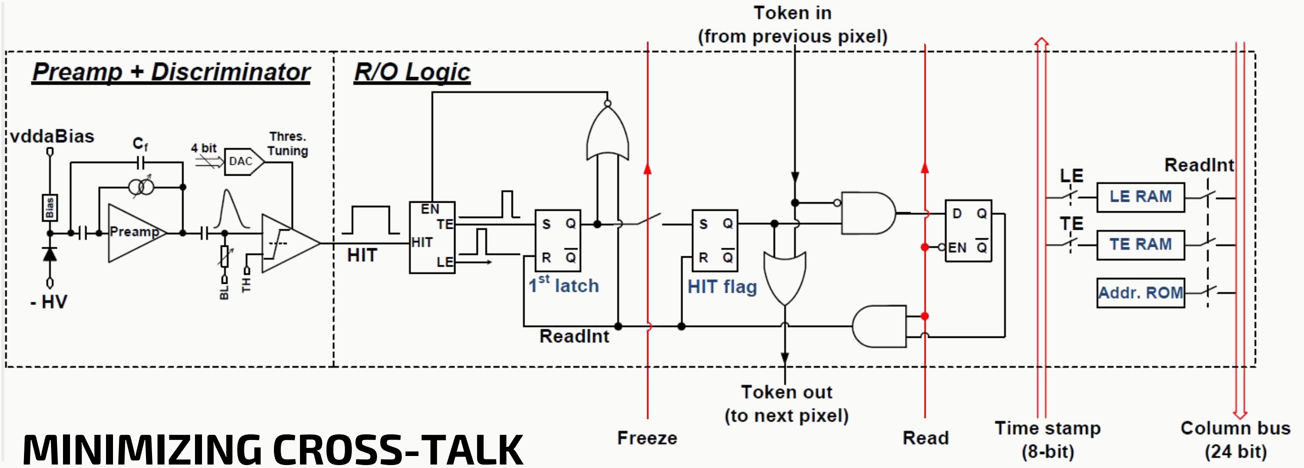
SI LAB Silizium Labor Bonn

CENTRE DE PHYSIQUE DES PARTICULES DE MARSEILLE CPPM

PIXEL LAYOUT IN LF-MONOPIX01

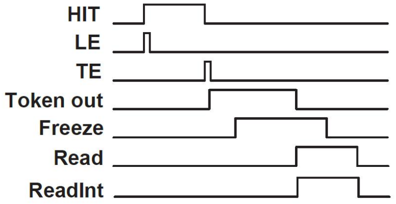


DESIGN CHALLENGES



MINIMIZING CROSS-TALK

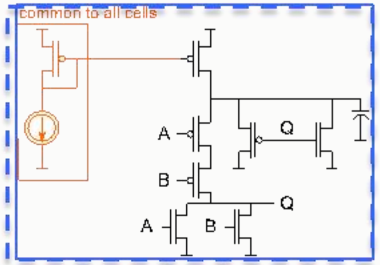
Column-drain R/O logic

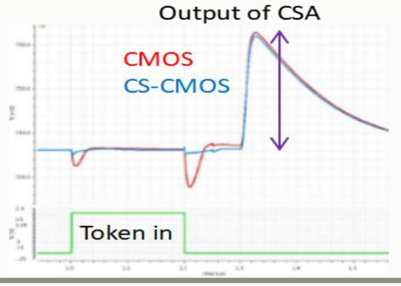


8-bit LE/TE time-stamps (ToT) + Address

In Token propagation:

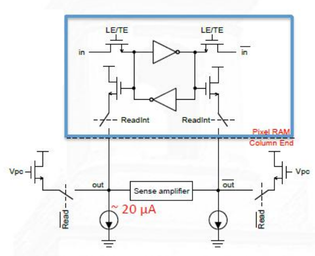
“Current steering logic”
-> Limit the current to avoid glitches

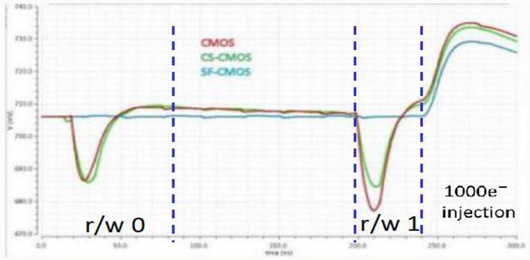




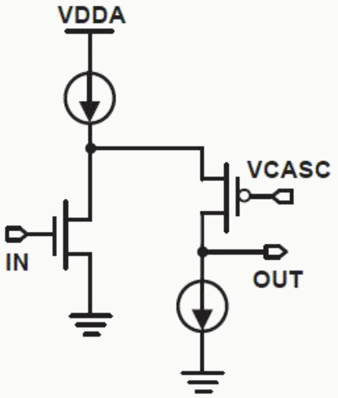
In Data R/O (LE/TE, address):

Differential lines + Source followers
-> Avoids current injection into the PW when switching from high to low





PREAMPLIFIERS AND DISCRIMINATORS



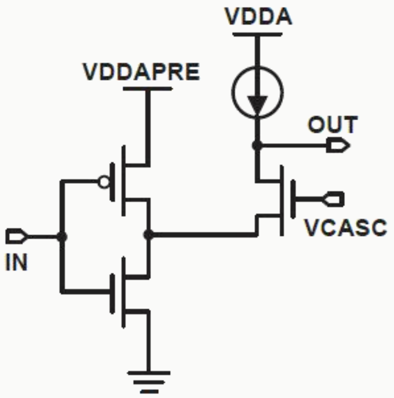
NMOS input pre-amp.

Bias I ~ 17 µA

Peak time ~20 ns (4ke- signal)

ENC (Simulation) ~ 170 e-

Faster



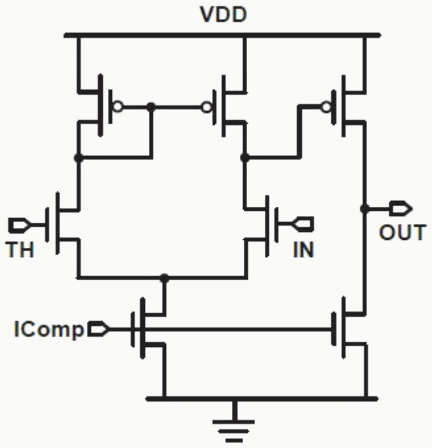
CMOS input pre-amp.

Bias I ~ 15 µA

Peak time ~25 ns (4ke- signal)

ENC (Simulation)~ 135 e-

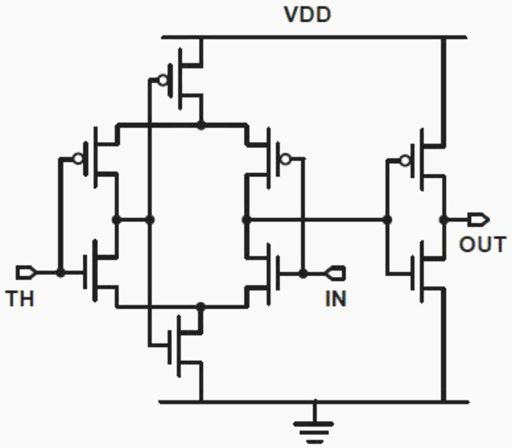
(Analog power from periphery)



Discriminator V1

Bias I ~ 4.5 µA

Two-stage open loop structure

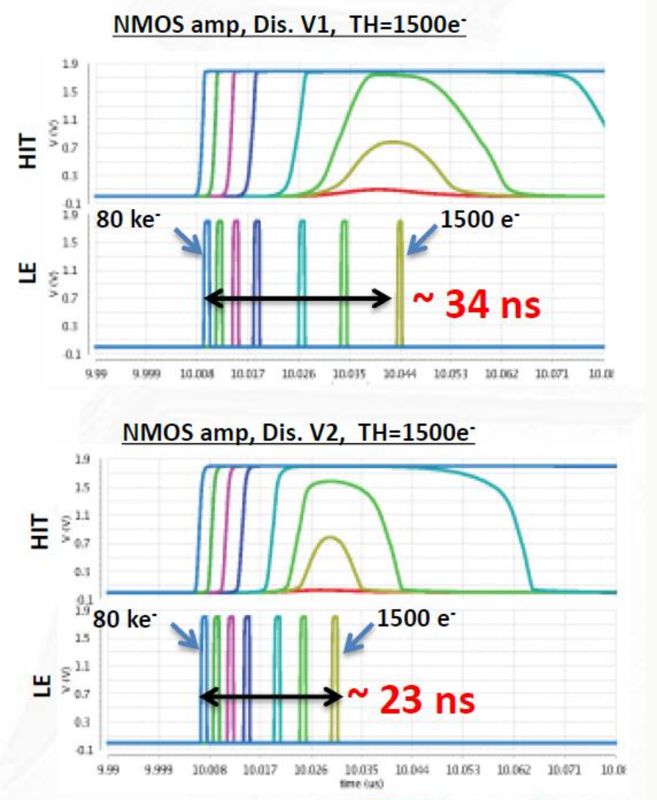


Discriminator V2

Self-bias < 4 µA

Self-biased differential amplifier + CMOS inverter

Faster



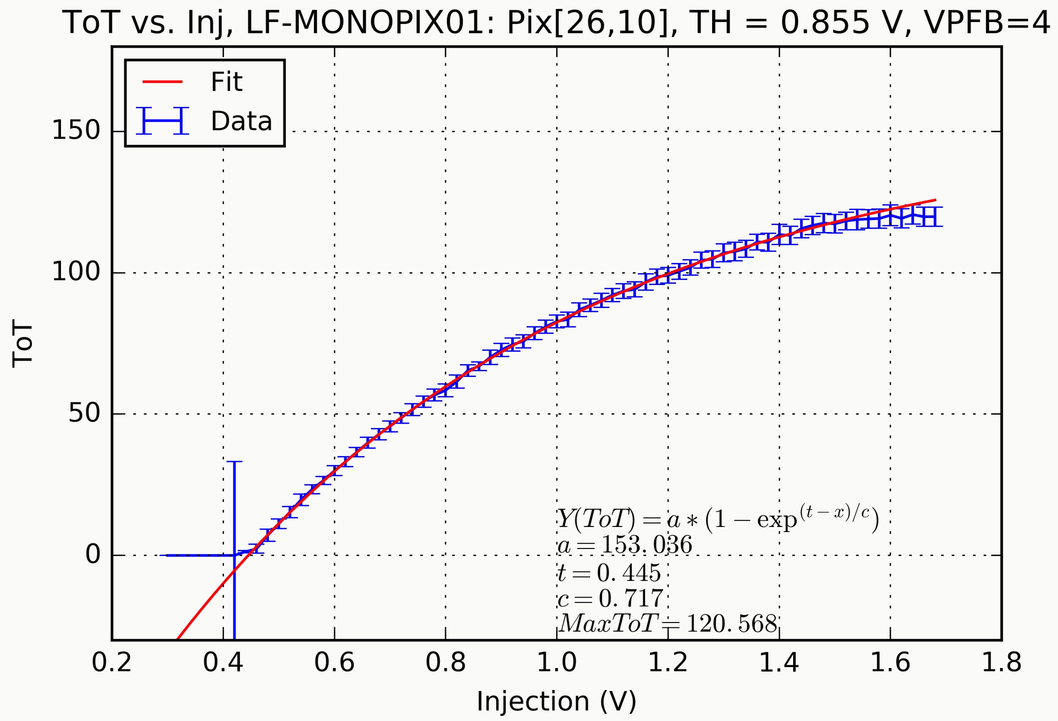
T. Wang, Bonn

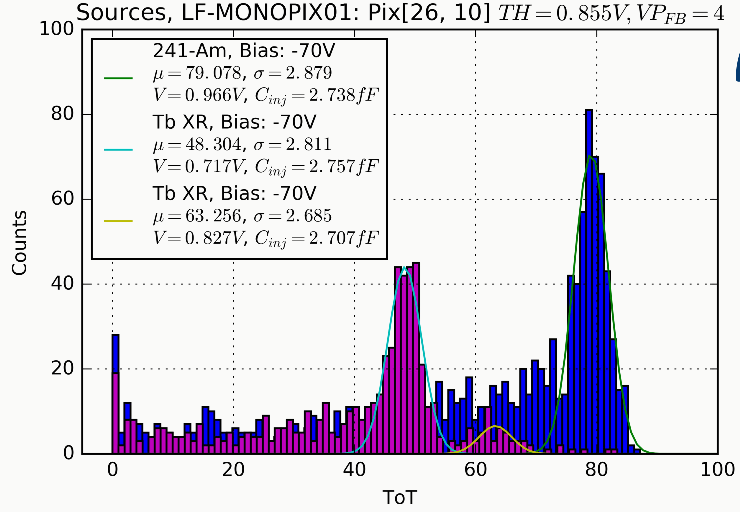
TOT RESPONSE AND INJECTION CAPACITANCE

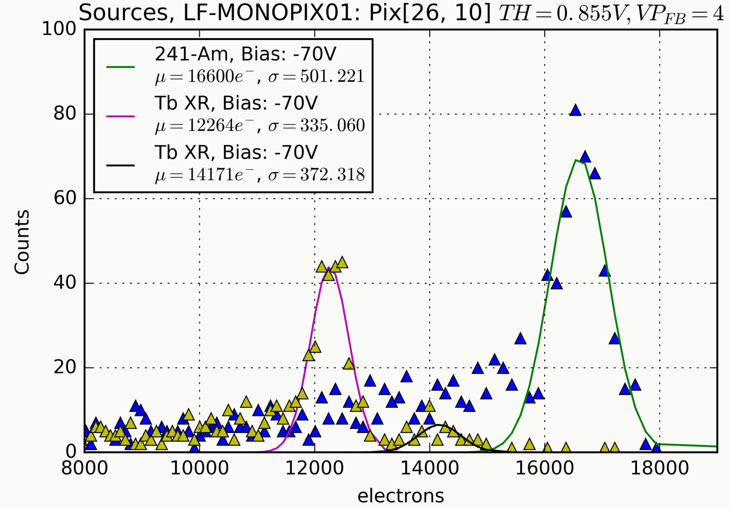
-> Injecting charge directly to the pre-amplifier.

+ Low feedback voltage (VPFB): Longer ToT

(sampling with **higher resolution**)







(Assuming 3.6 eV/e-)

^{241}Am:

16539 e-

Tb X-rays:

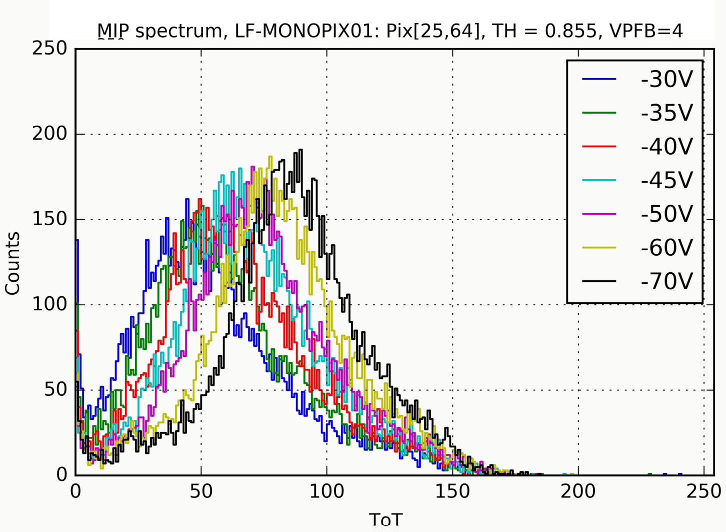
K_α	12353 e-
K_β	13997 e-

C_{inj} = Q / V ~ 2.7 fF

ToT can also be used for event differentiation or time-walk corrections.

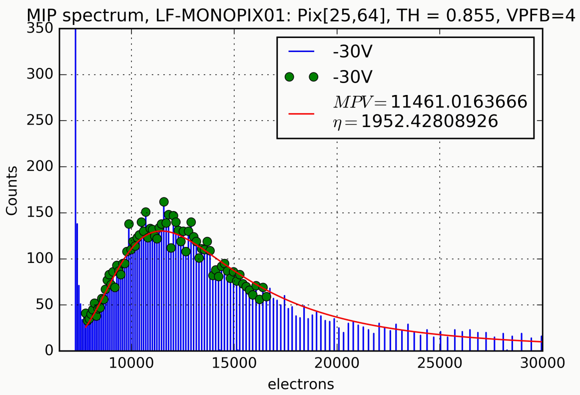
TOT RESPONSE AND CALIBRATION

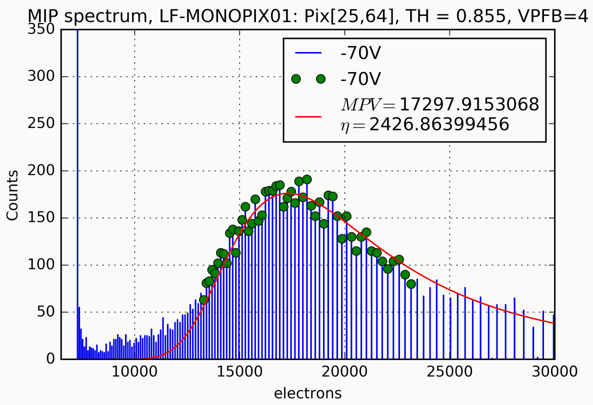
Data from energy loss by 2.5 GeV electrons (MIPs) in silicon for different bias voltages (without cluster size selection)

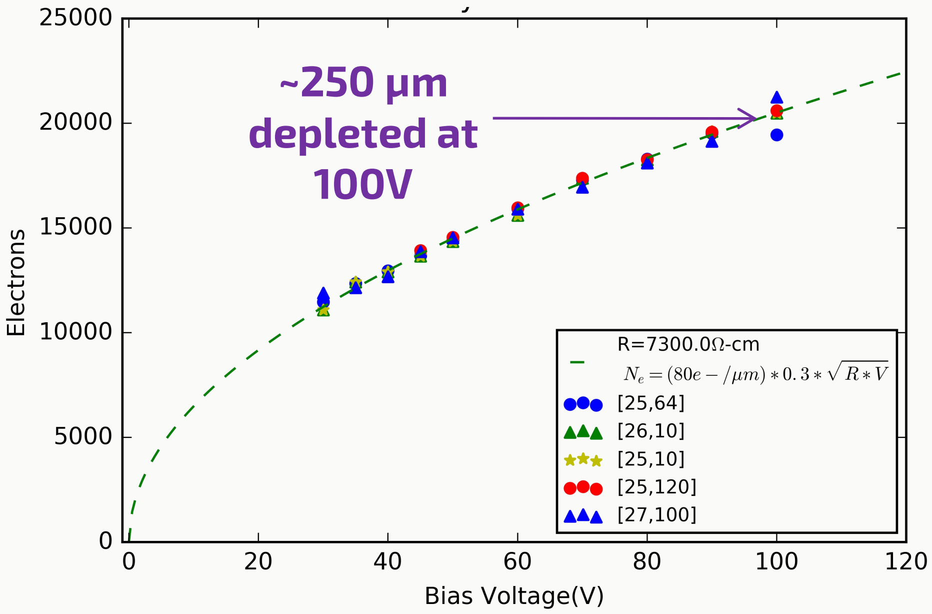


Landau+Gaussian convolution fit to describe every calibrated distribution.

Applying per-pixel calibration



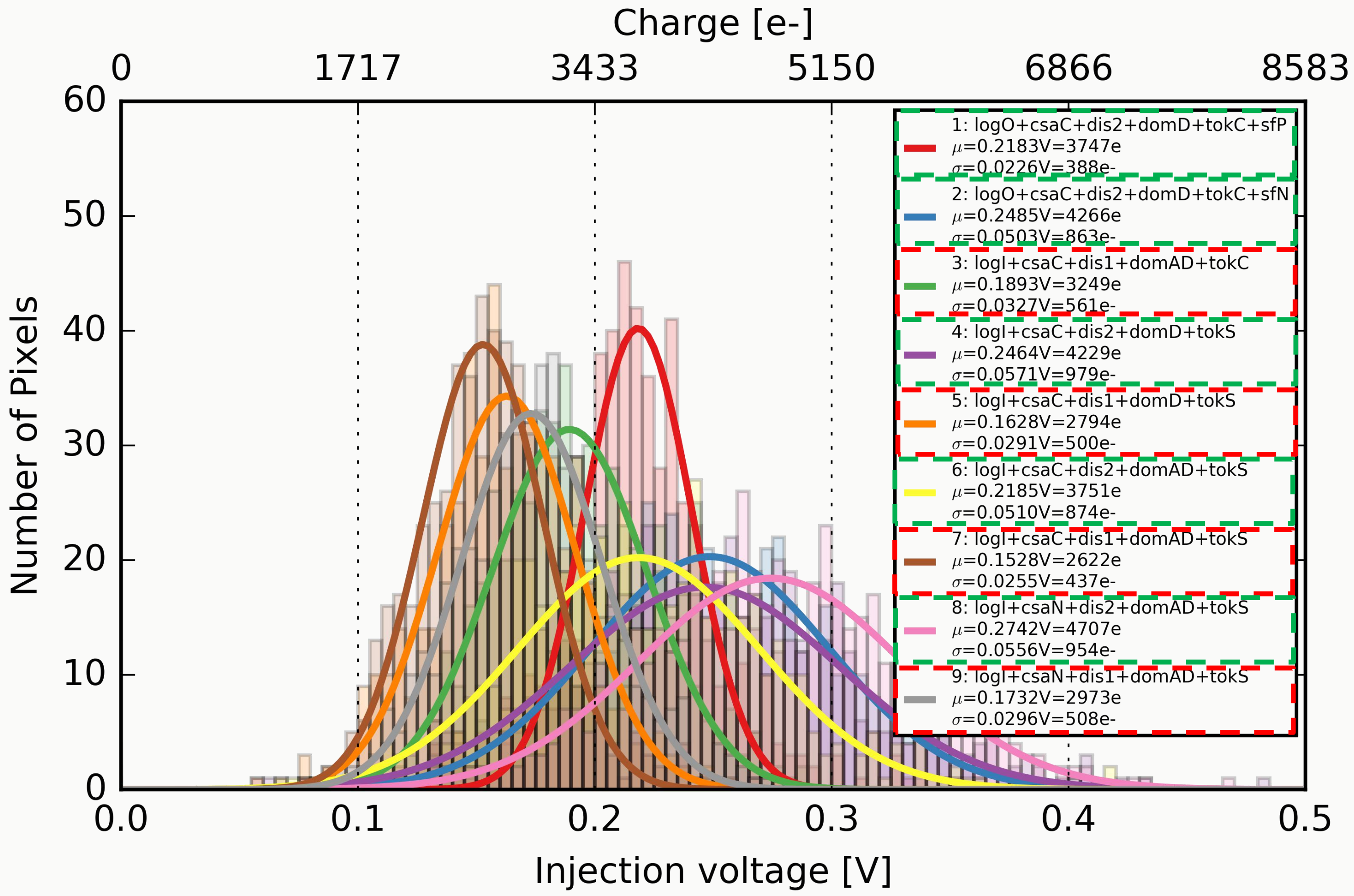




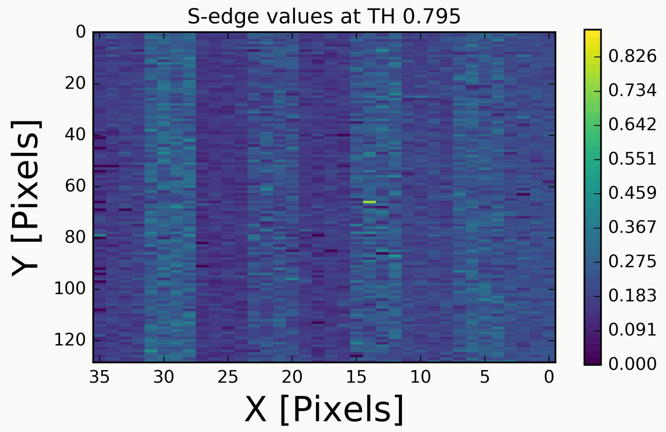
R ~ 7.3 kOhm-cm

> 2 kOhm-cm, but also higher than previous measurements in other wafers from the same foundry (3.5 and 5.5 kOhm-cm)

UNTUNED THRESHOLD DISTRIBUTIONS



Untuned threshold dispersion for flavours with the **V1** discriminator **~400-600 e-** (**plus 350-400 e-** for those with integrated pixel R/O logic and the **V2** discriminator)



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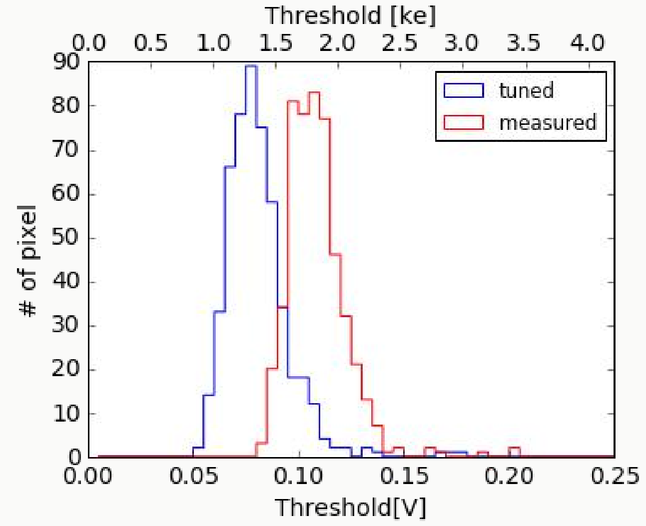
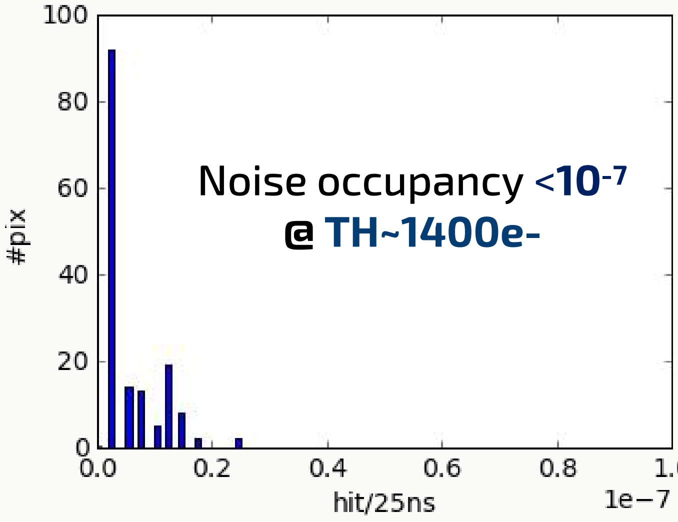
BONN

STREAM

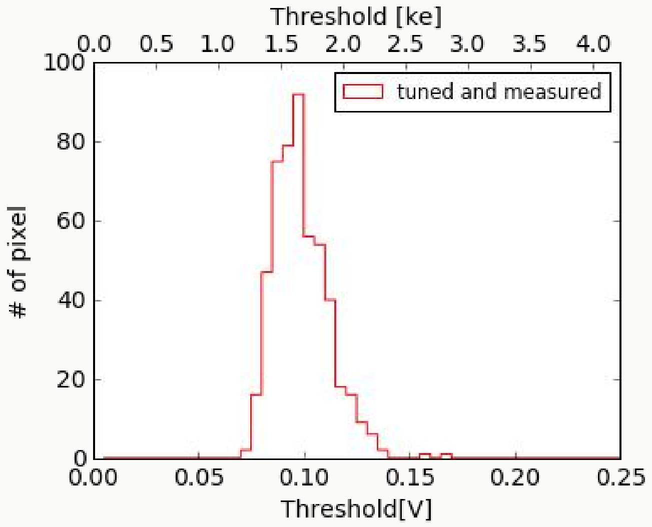
NOISE OCCUPANCY AT LOW THRESHOLD

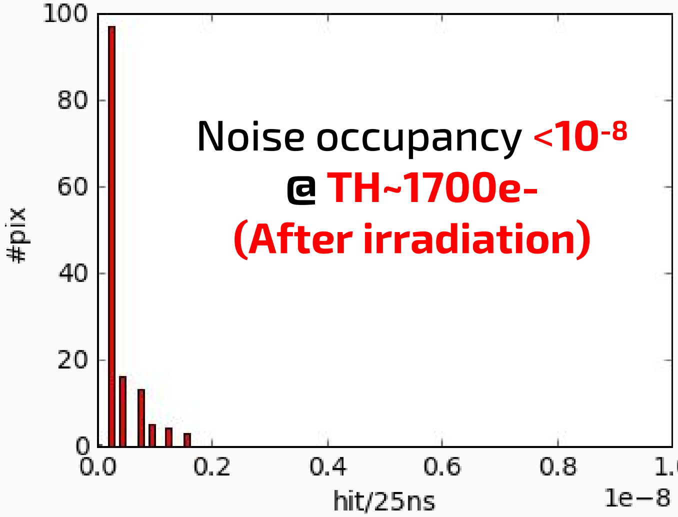
- **Non-irradiated**
  - Threshold: **1400 e-**
  - Dispersion due to noise baseline tuning
  - Bias V: -200V
  - Cooled with dry ice.



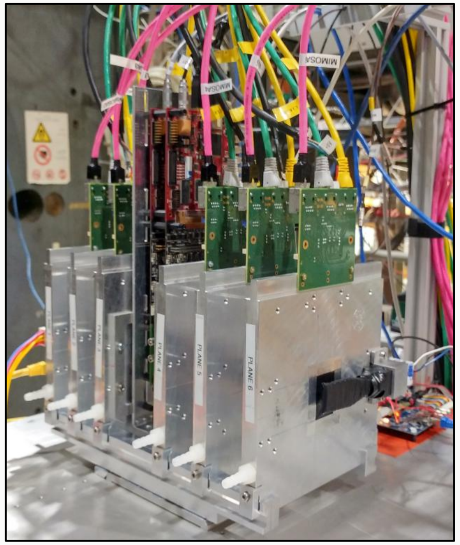


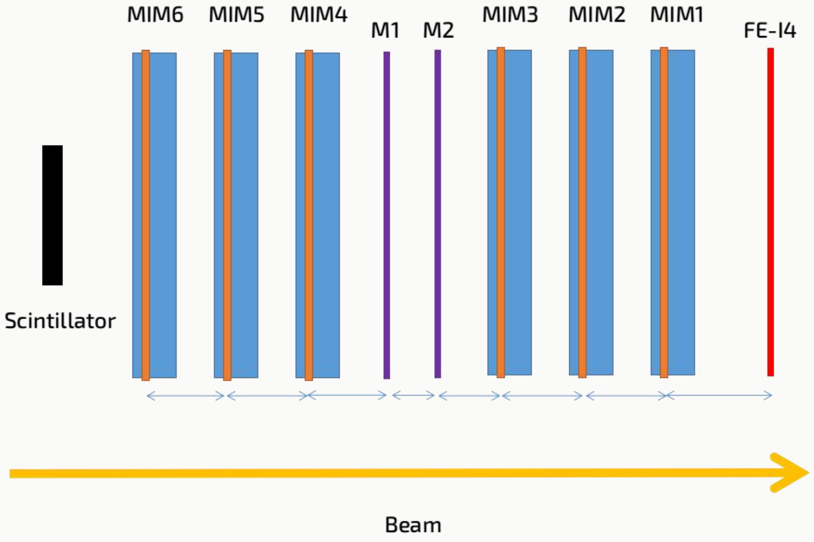
- **Neutron irradiated ($1 \times 10^{15} n_{eq}/cm^2$)**
  - Threshold: **1700 e-**
  - Bias V: -130V (due to technical issues)
  - Cooled with dry ice.





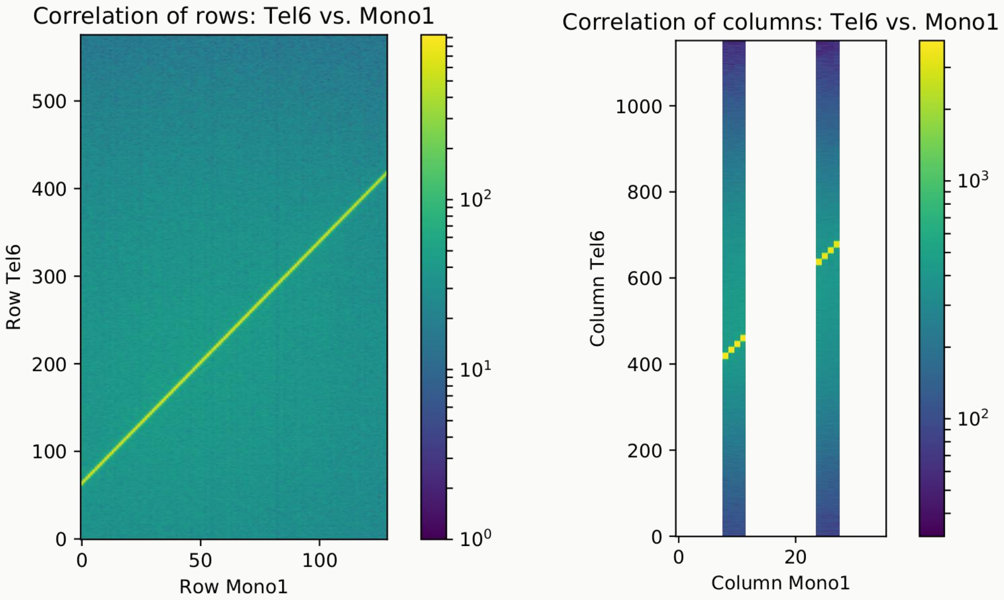
TEST BEAM CAMPAIGNS





LF-MONOPIX (unirradiated and neutron-irradiated samples) exposed to MIPs at ELSA (2.5 GeV e-) and the H8 line of CERN's SPS (180 GeV pions)

Sample of event correlation (@SPS) MONOPIX <-> MIM26 (6)

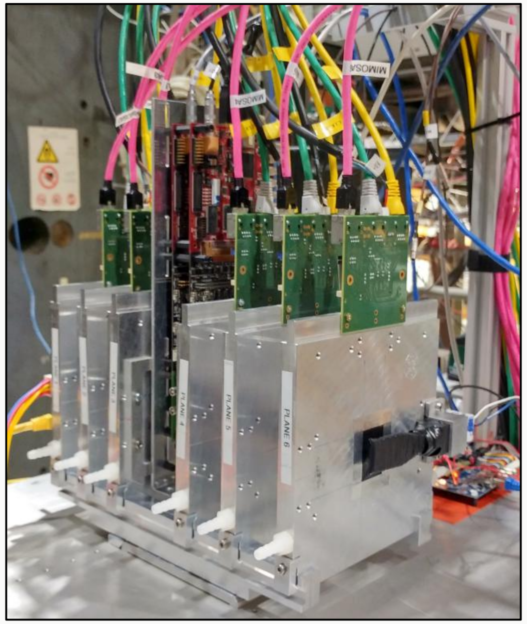


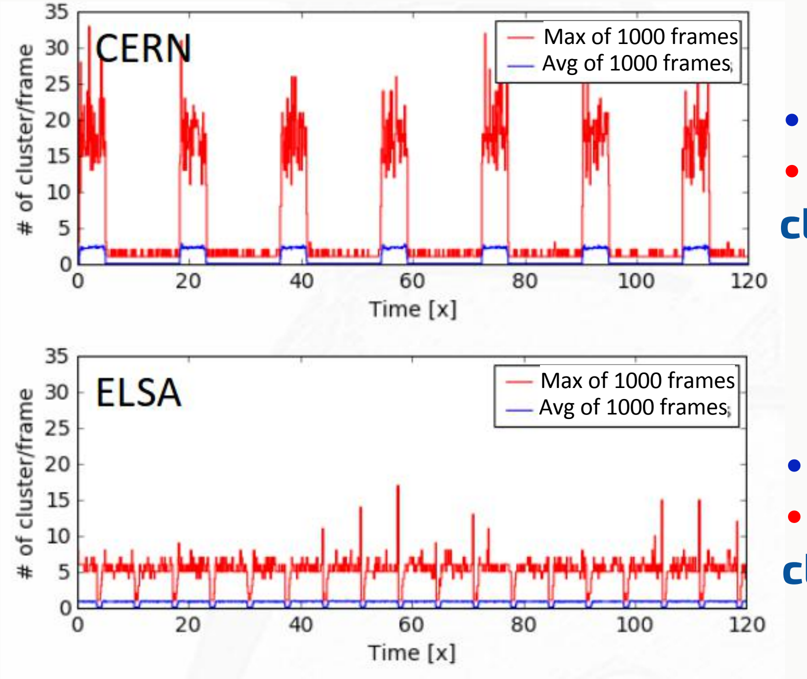
- **MIMOSA26 x 6**
  - Pixel size: 18.2 μm x 18.2μm
  - 1152 μs/frame (rolling shutter)
- **FE-I4 x 1**
  - Pixel size: 250 μm x 50 μm
  - Timing resolution: 25ns (trig. by scintillator + TLU)

TEST BEAM CAMPAIGNS

MONOPIX planes (unirradiated and neutron-irradiated samples) exposed to MIPs at ELSA (2.5 GeV e-) and the H8 line of CERN's SPS (180 GeV pions):

Measurements for different bias and threshold settings.





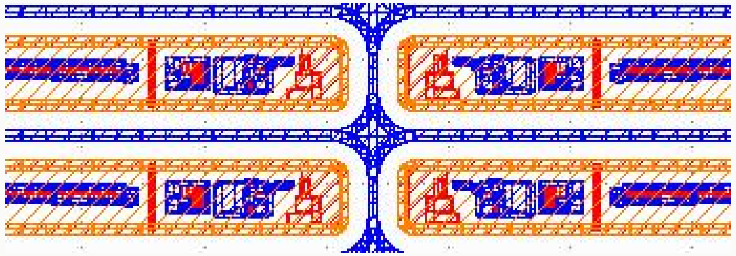
- Avg: 2.2
- Max: ~20

clust/frame

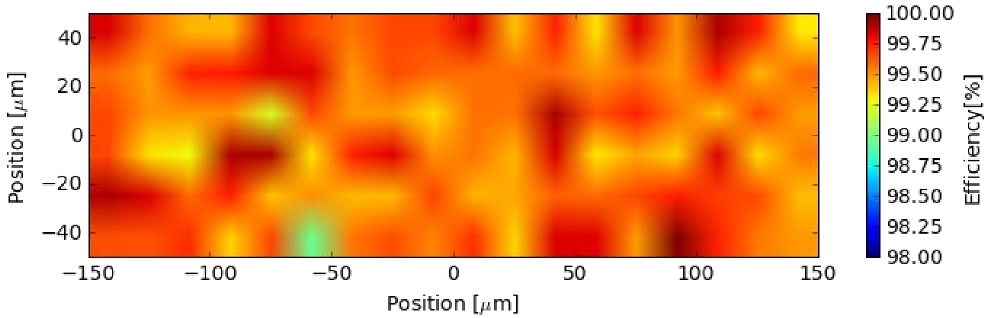
- Avg: 0.8
- Max: ~6

clust/frame

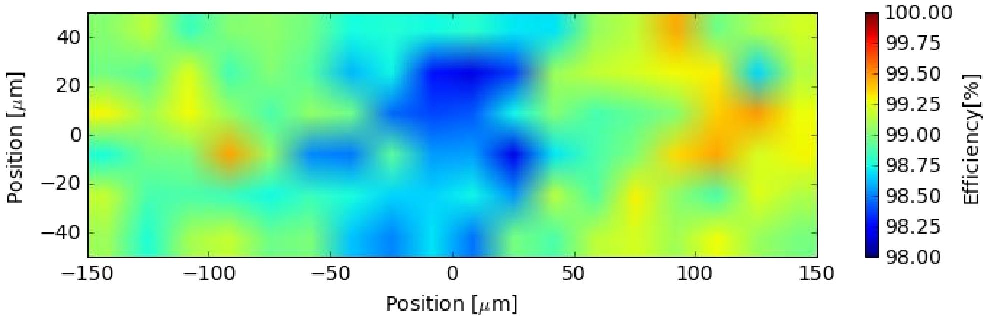
TB @ ELSA: IN-PIXEL EFFICIENCY



Deep N-well (Collecting electrode…)
P-well (Inter-pixel region, isolation of electronics…)
N-well (R/O electronics…)



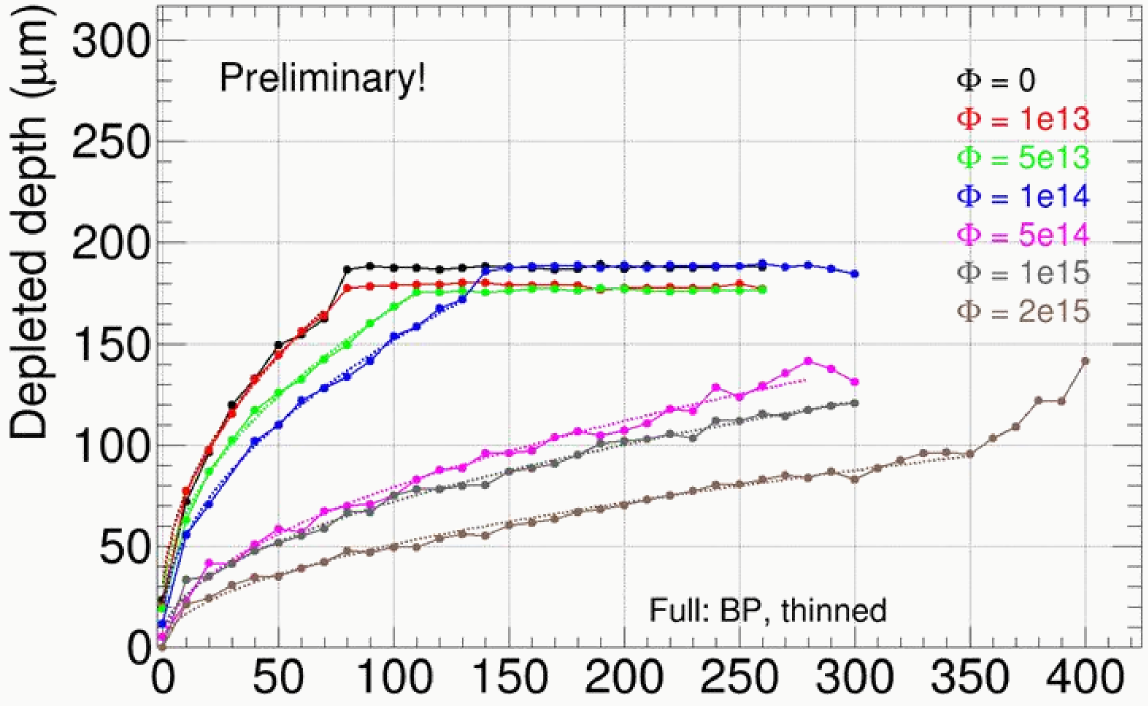
Non-irradiated
@ -200V:
Uniform efficiency



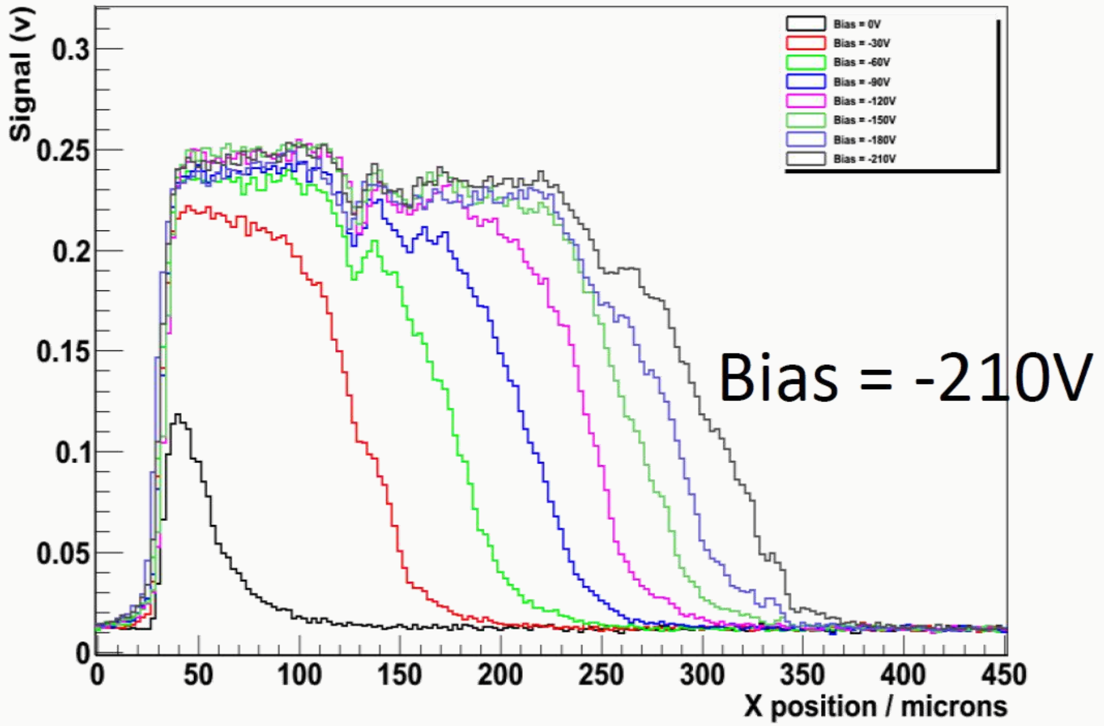
Neutron irradiated (1 x $10^{15} n_{eq}/cm^2$)
@-130V
Observed efficiency loss between pixels

E-TCT MEASUREMENTS

** Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*



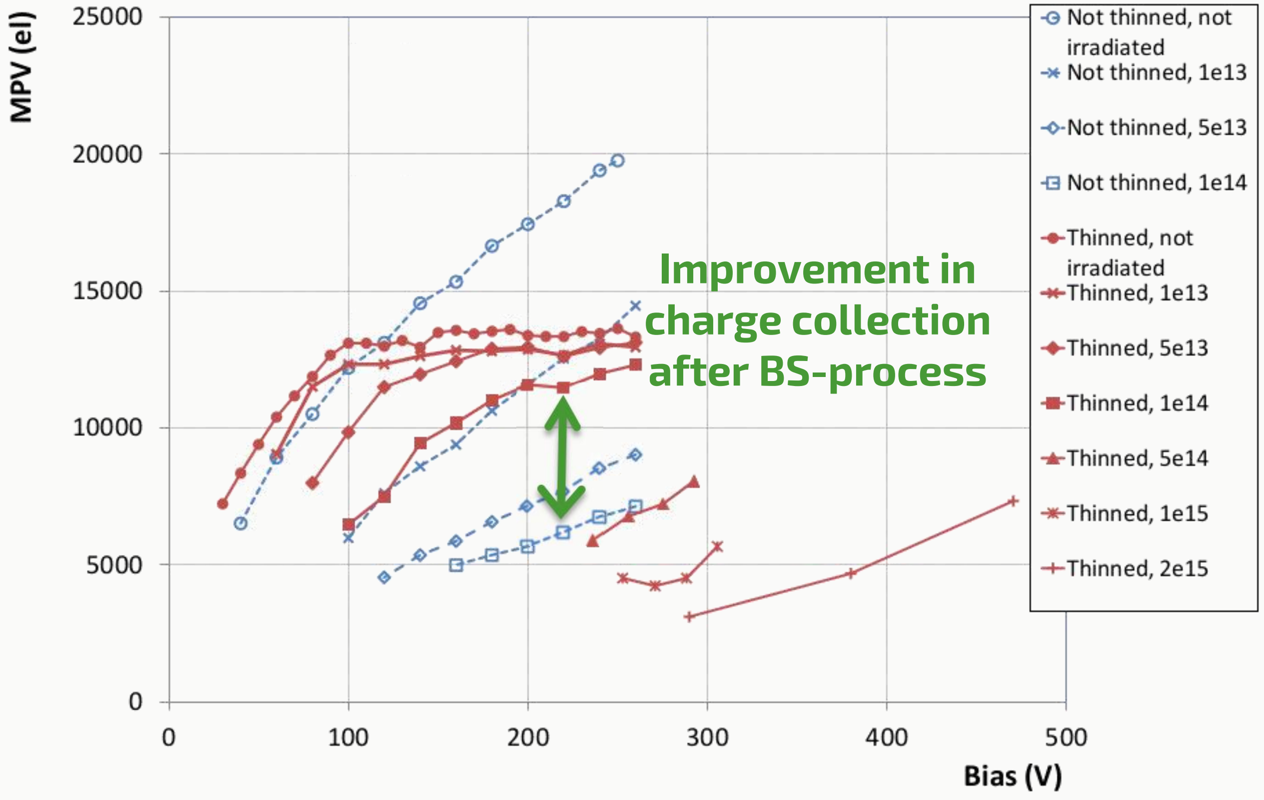
E-TCT measurement on LF test structures thinned to 200µm
I. Mandić, RD50 workshop 2017



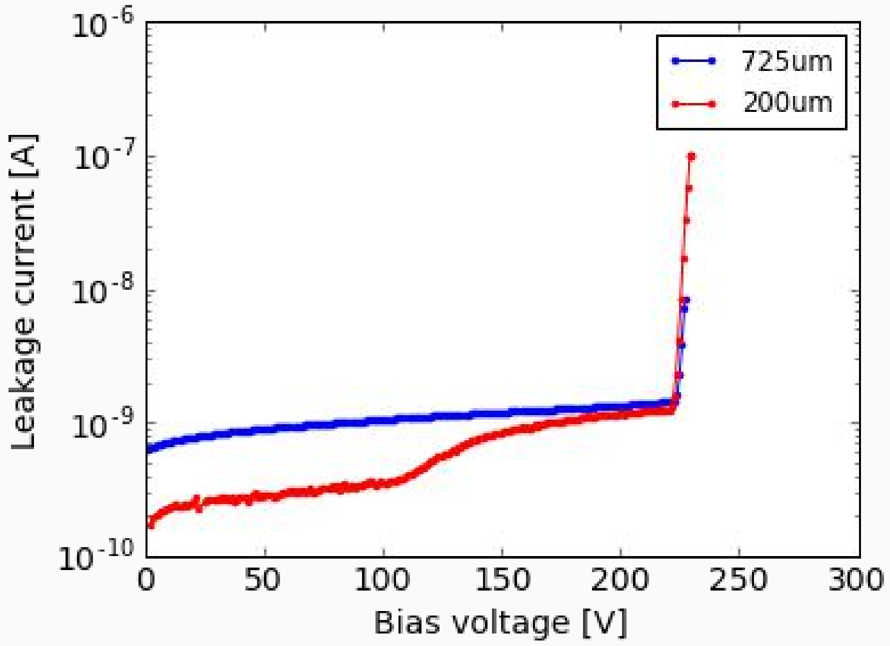
E-TCT measurement on LF-MONOPIX (775µm thick)
L. Vigani. University of Oxford.

IMPROVEMENT AFTER BACKSIDE-PROCESS

** Neutron irradiation in Lubljana (JSI), samples annealed for 80 mins at 60°C*



E-TCT measurement on LF test structures thinned and Backside-processsed to 200µm
I. Mandić, RD50 workshop 2017

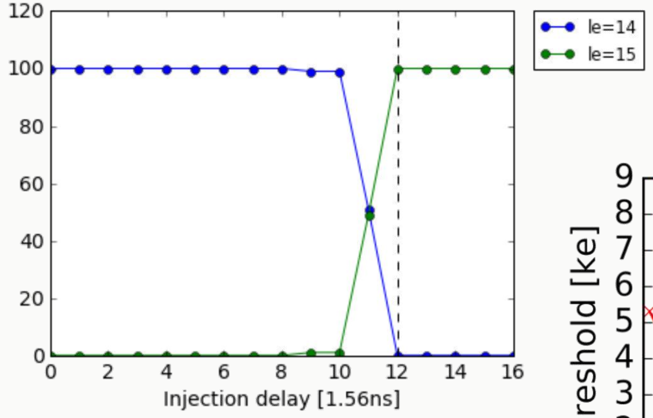


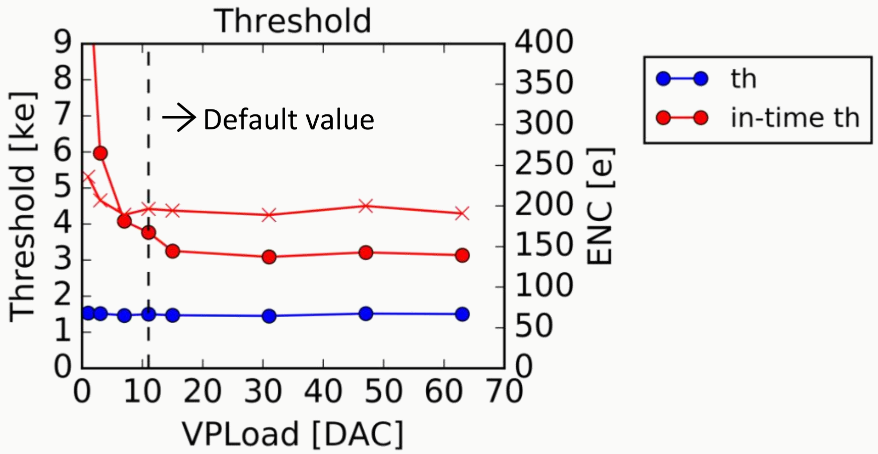
Reduction in leakage current after thinning and BS-process

TIMING OPTIMIZATION AND OVERDRIVE

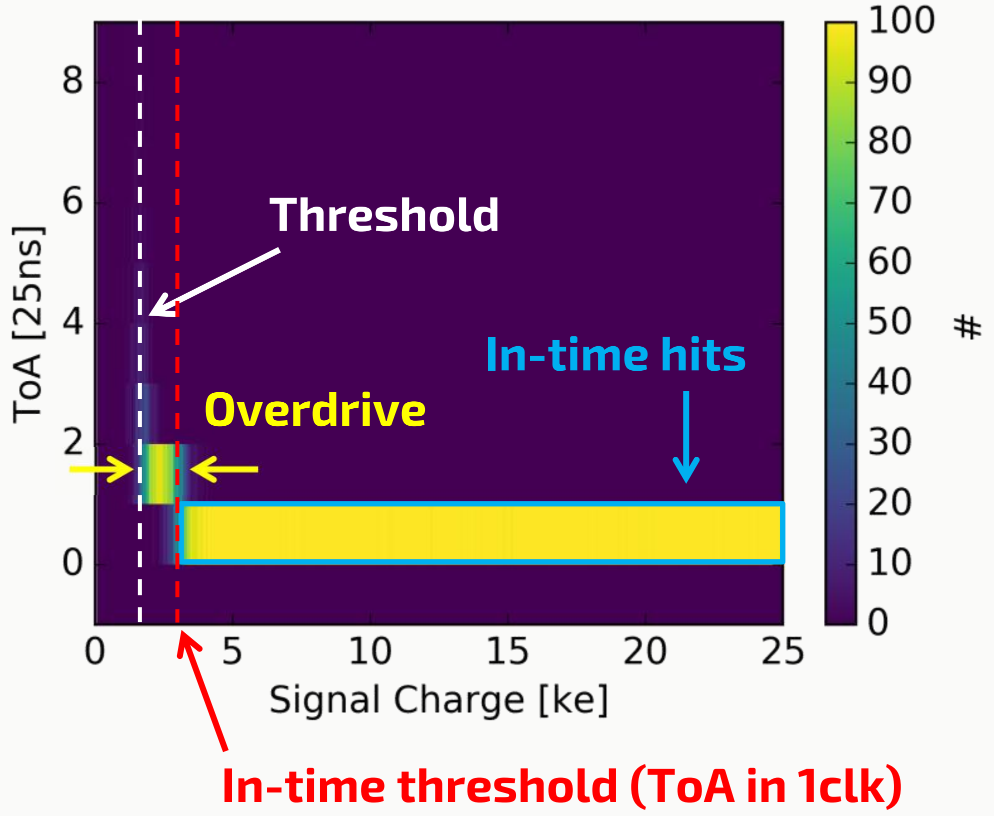
To measure timing performance:

- Injection delay (Difference between INJ and LE) optimized to measure all data from a 20ke- signal at the start of a single 40MHz clock cycle.
- DACs optimized from default values for good timing.



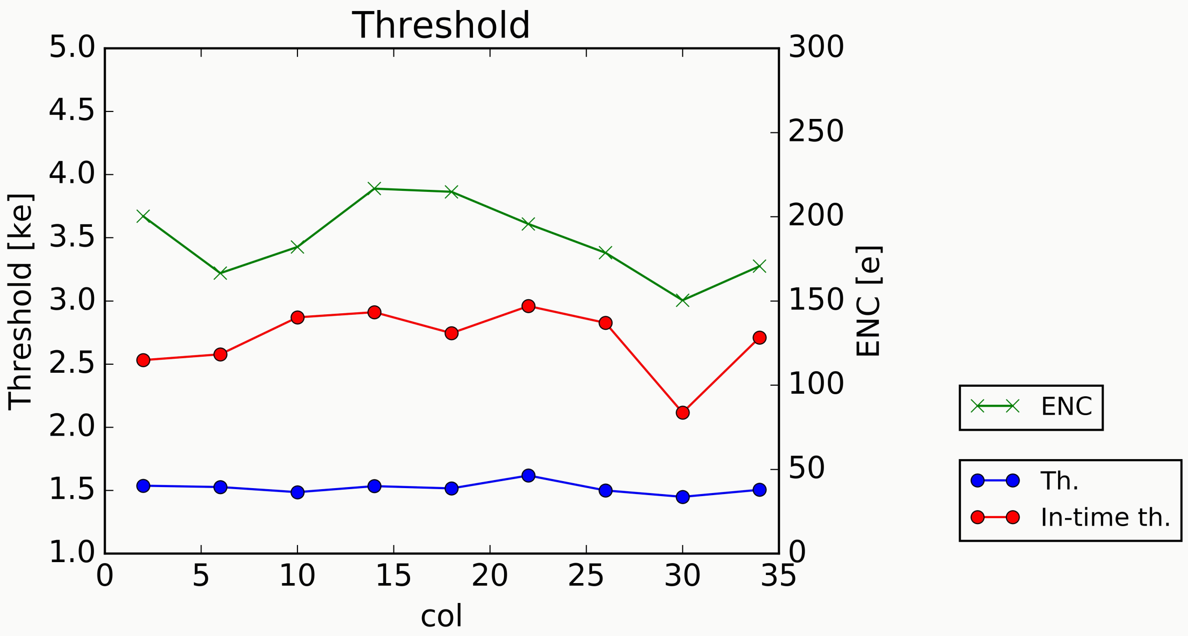


Overdrive and in-time hits

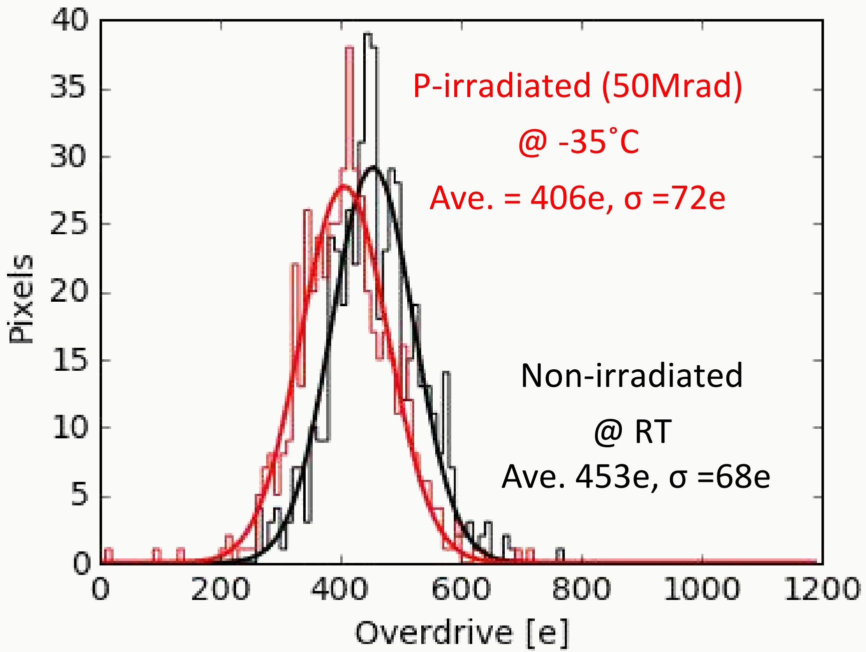


IN-TIME THRESHOLD IN LF-MONOPIX01

In-time thresholds (1 pixel per flavour)



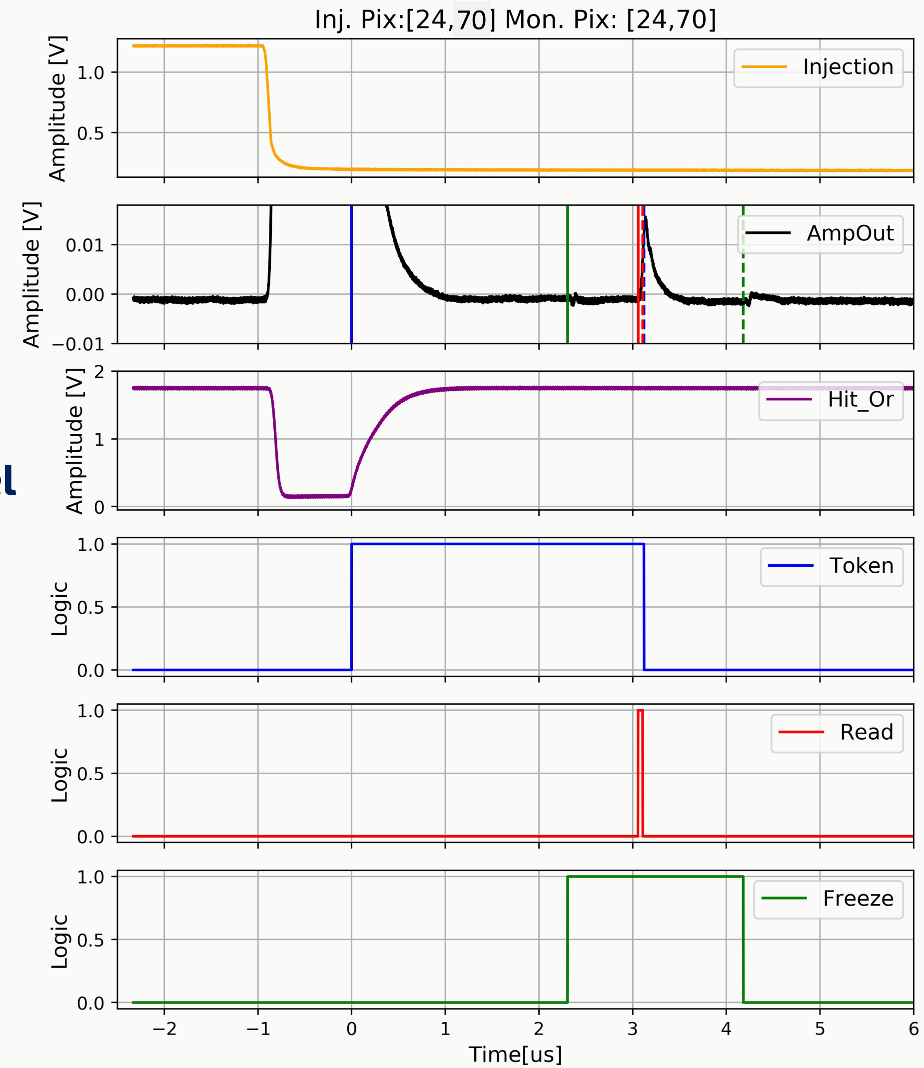
Overdrive distribution before/after irradiation (Full flavour)



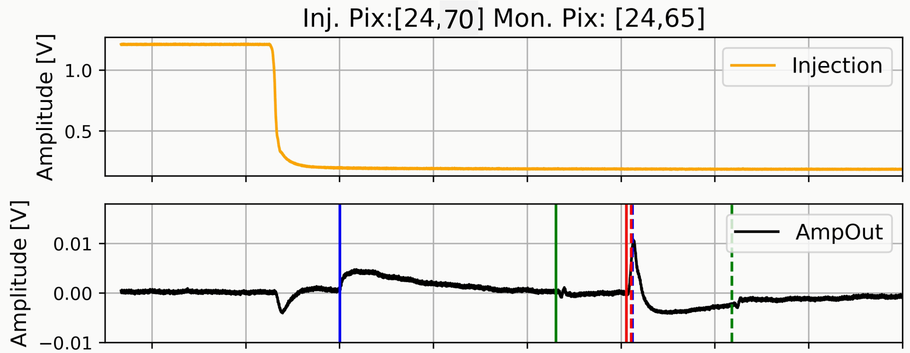
- **Overdrive variations in different implementations**
- **Timing performance not affected after irradiation**

COUPLING IN NON-INJECTED PIXELS (EVEN VS ODD ROWS)

Injected pixel [24,70]



Odd pixel [24,65]

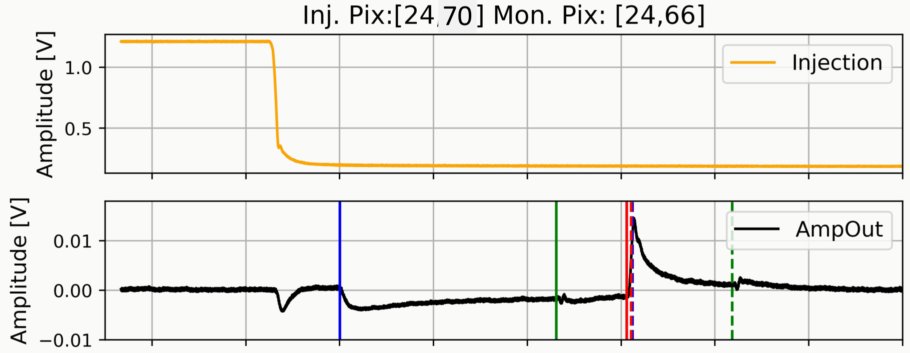


Token↑ Freeze↑ Freeze↓

Read↑↓

Token↓

Even pixel [24,66]



- **Token coupling inverted every double column**

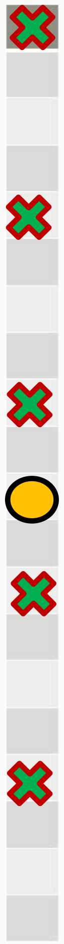
COUPLING ACROSS THE COLUMN

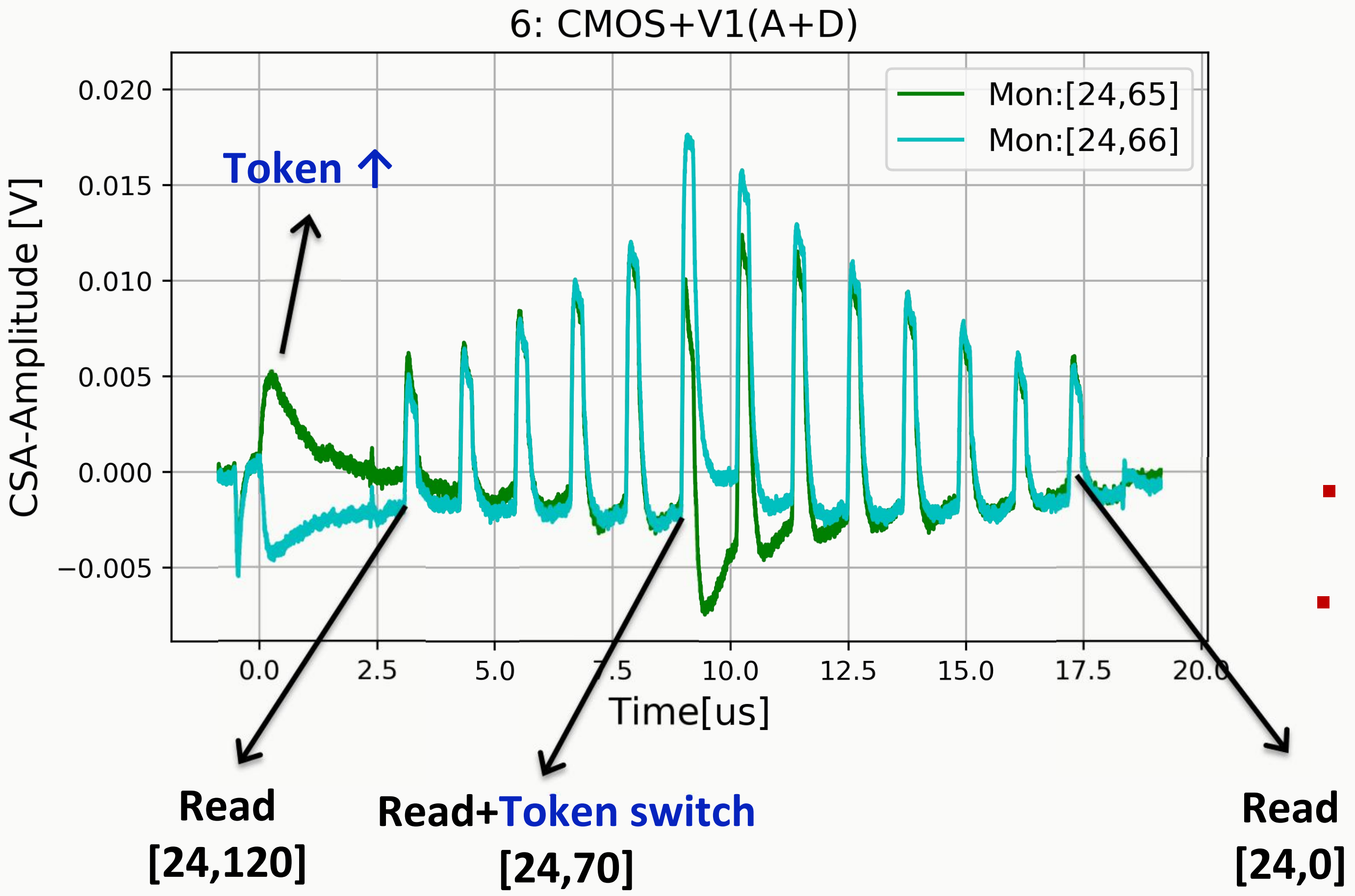
Injecting 1 pixel every 10 rows (0,10,20…120) and monitoring rows 65 and 66

(Remember our READ priority goes from largest to lowest row number!)

EoC

(row 0)





What does a pixel "see"?:

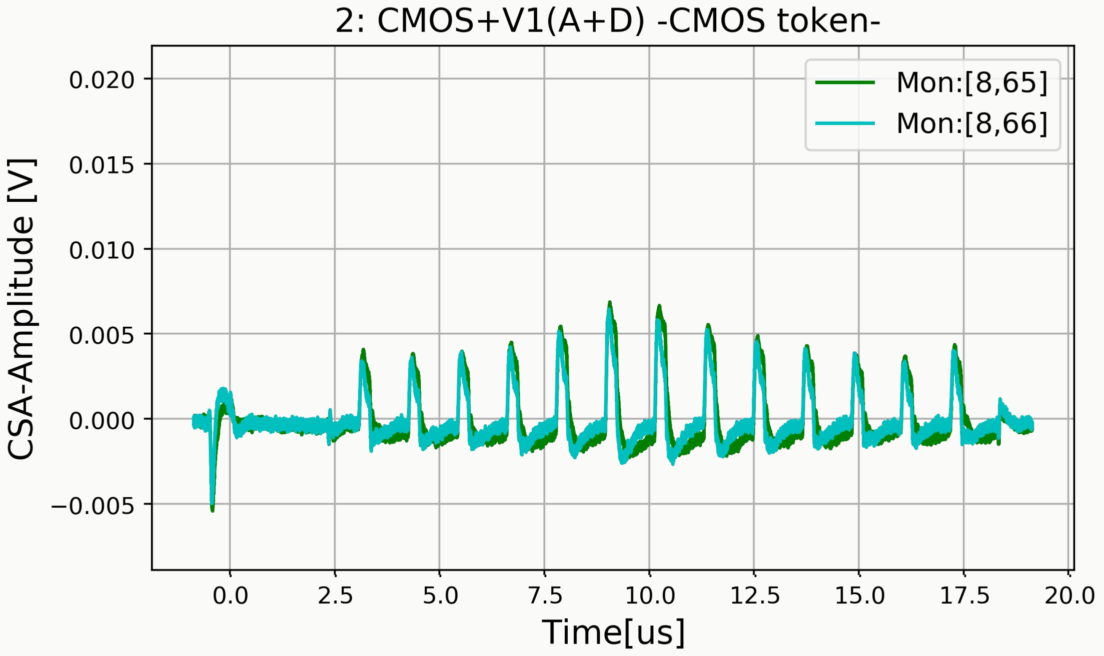
"Read" coupling:

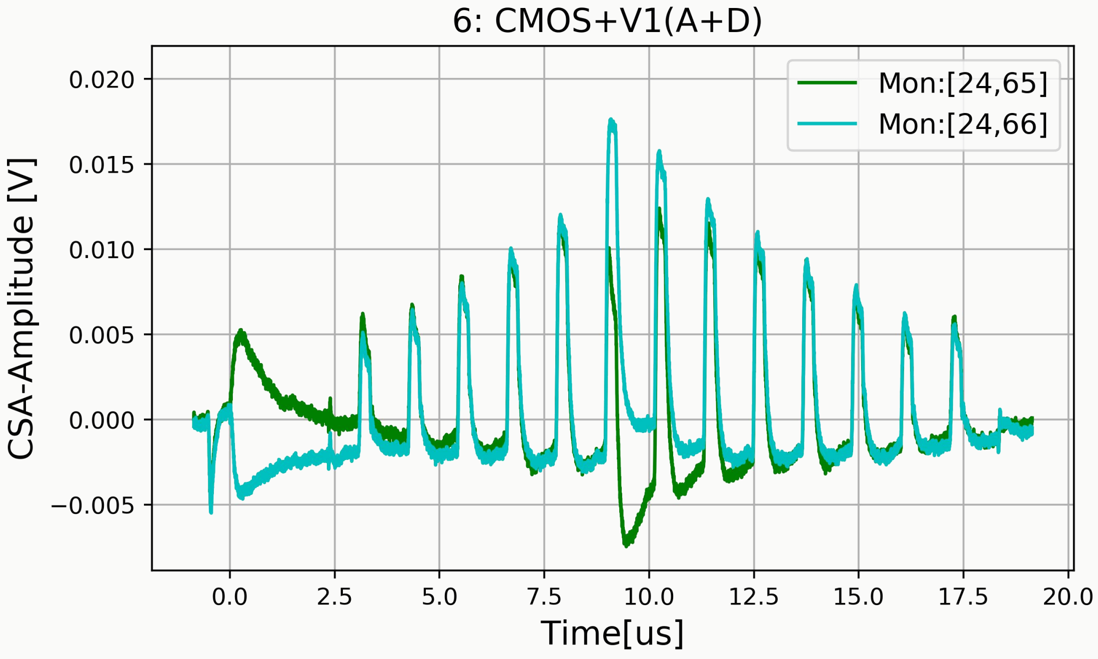
- As long as "Read" is high.
- Amplitude dependent on the distance in rows to the hit pixel

- "Token" coupling:

- Inverse polarity of rising and falling edge.
- Observation of the falling edge from the closest hit pixel with higher priority (higher row number)

"CMOS" VS "CURRENT STEERING" TOKEN



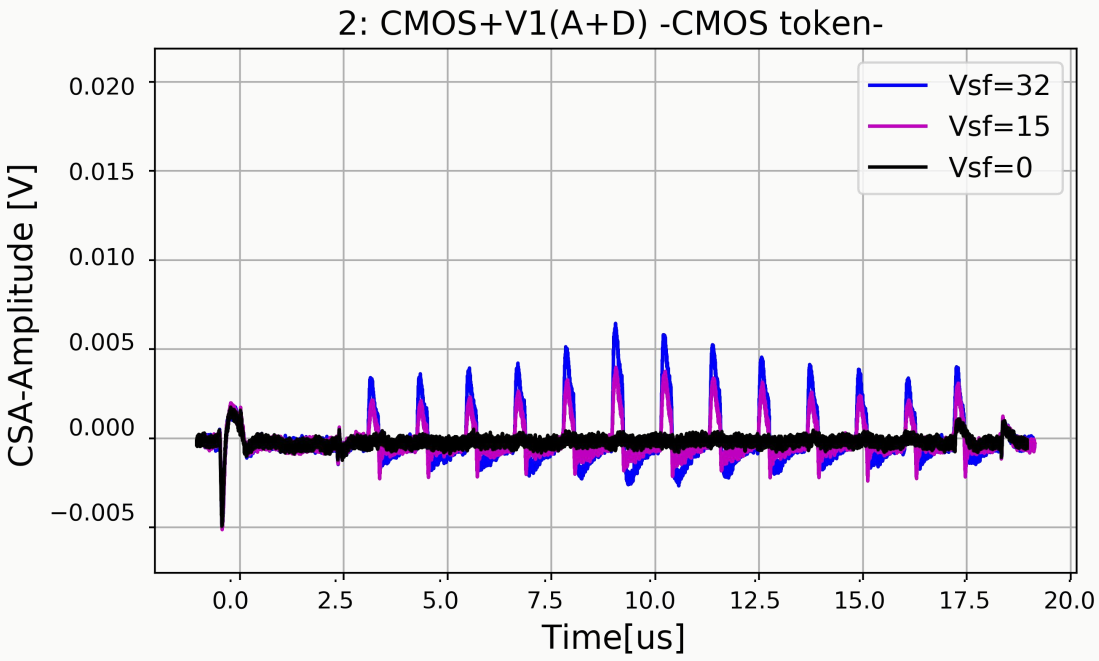


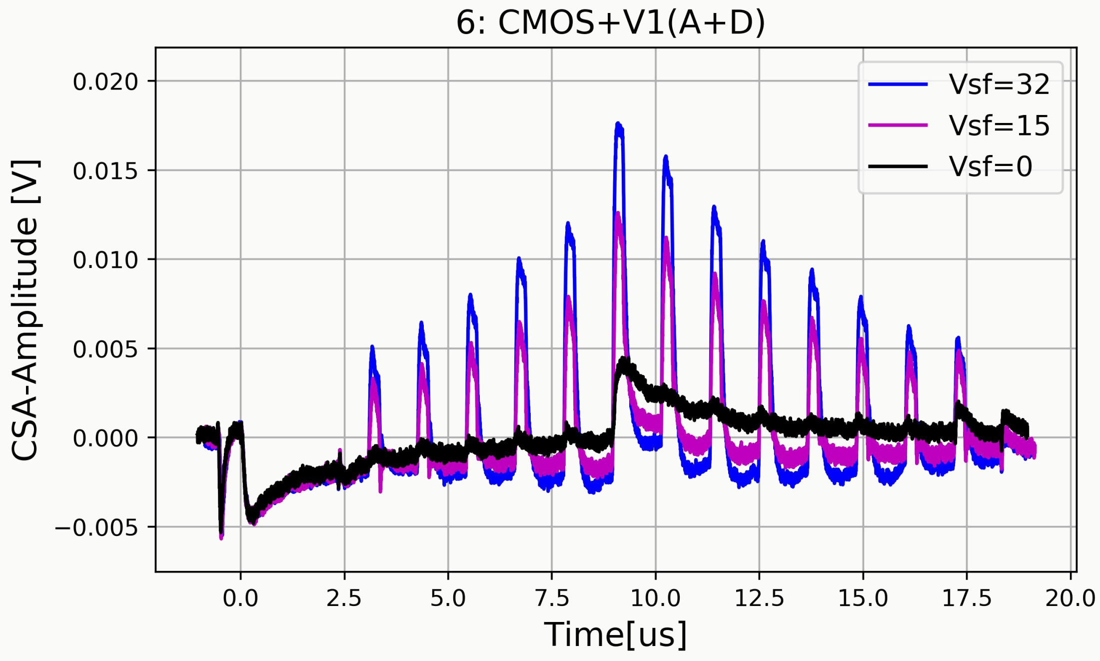
In the flavour with CMOS token:

- The amplitude of "Read" coupling is smaller
- There is not a noticeable coupling from "Token"

(unexpected!---> To be simulated and understood)

EFFECT OF VSF





By reducing the Vsf:

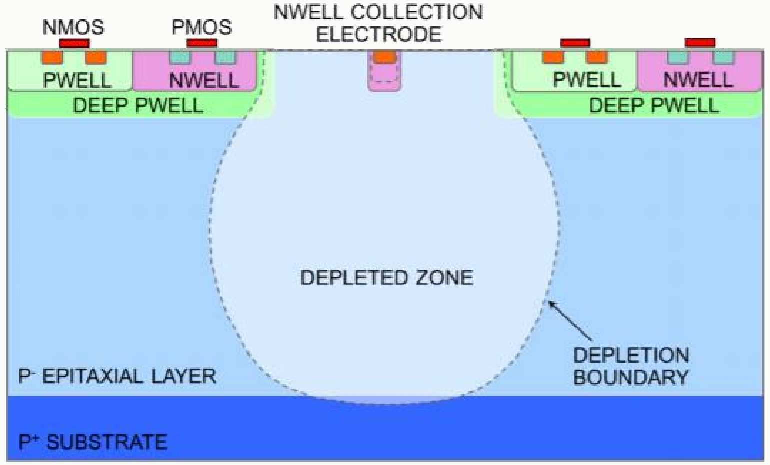
- The amplitude of "Read" coupling is reduced (gone for Vsf=0) →
- Only the signal coupling from "Token" remains noticeable in CS flavours

(We can still optimize the "Read" coupling in Lf-Monopix01)

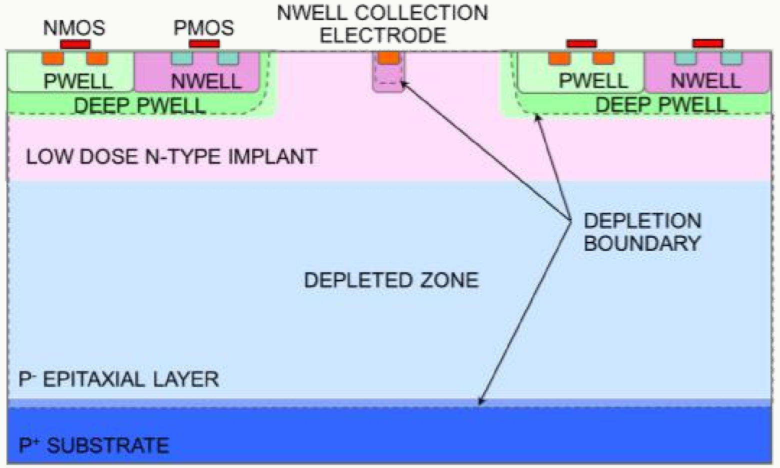
Enabling the data bus is linked to the "Read" digital coupling

PROCESS MODIFICATION IN TOWERJAZZ 180NM

Standard Process

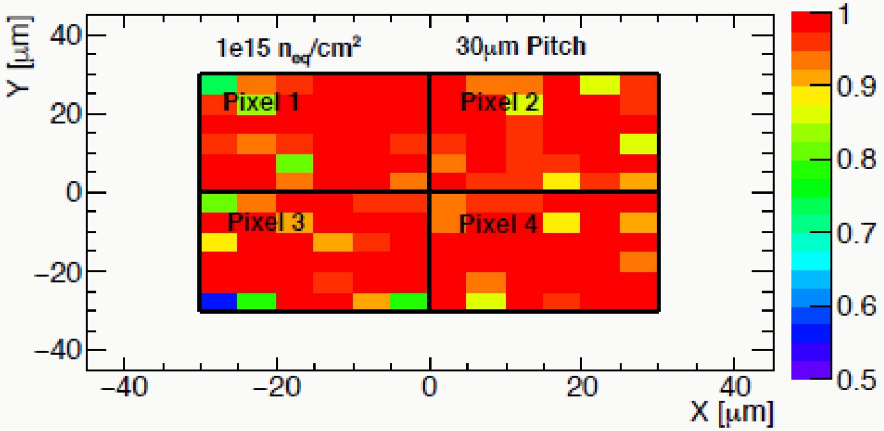


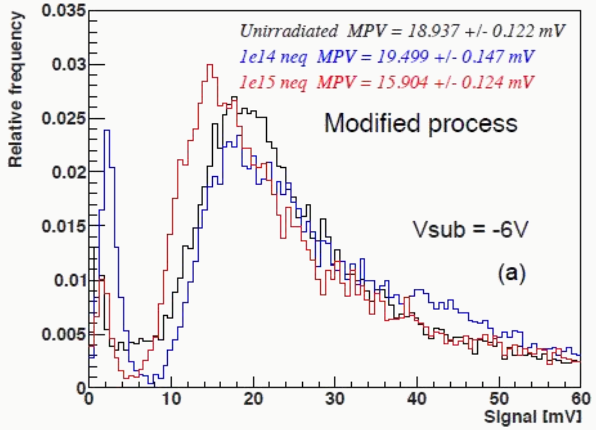
Modified Process



W. Snoeys et al.
DOI: 10.1016/j.nima.2017.07.046

Rad-hard modified process tested on an "Investigator" chip

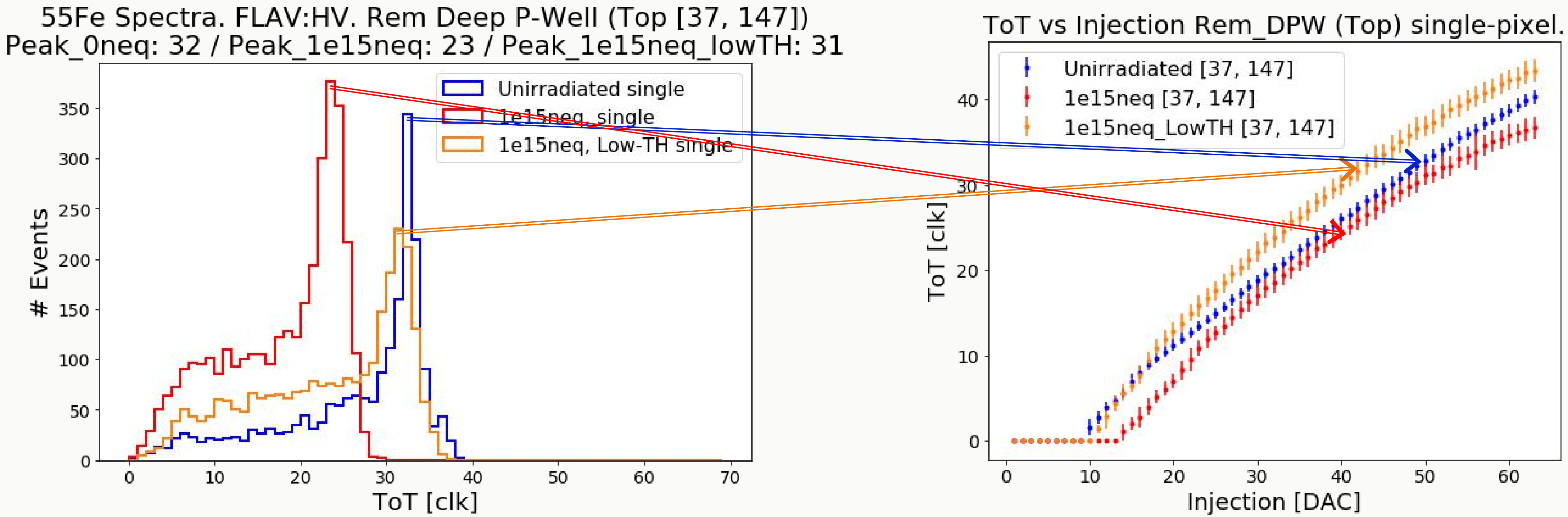




97% efficiency after $1x10^{15}$ n_{eq}/cm^2
(100e- threshold, 30 μm square pixel)

H. Pernegger, et al.
DOI: 10.1088/1748-0221/12/06/P06008

CALIBRATION OF THE INJECTION CIRCUIT

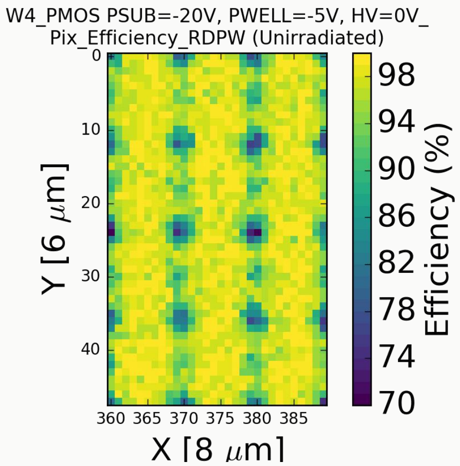


- Calibration values are similar in "Top" and "Bottom", but different for unirradiated and irradiated samples:

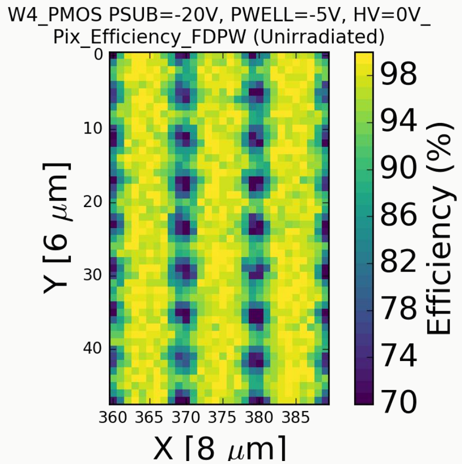
Unirradiated: ~33e-/DAC **$1x10^{15}$ Irradiated:** ~42e-/DAC

IN-PIXEL EFFICIENCY (UNIRRADIATED PMOS VS HV)

PMOS

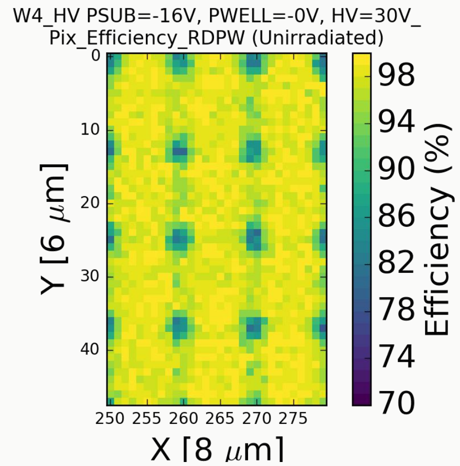


95.9%

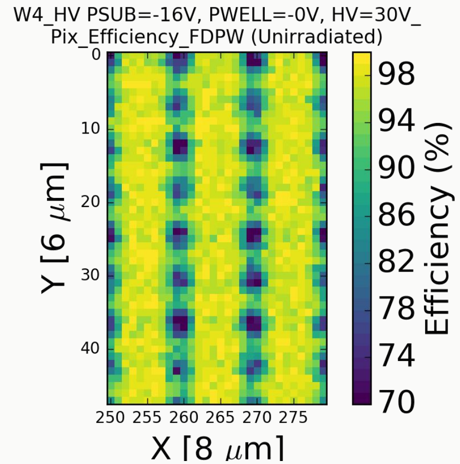


93.5%

HV

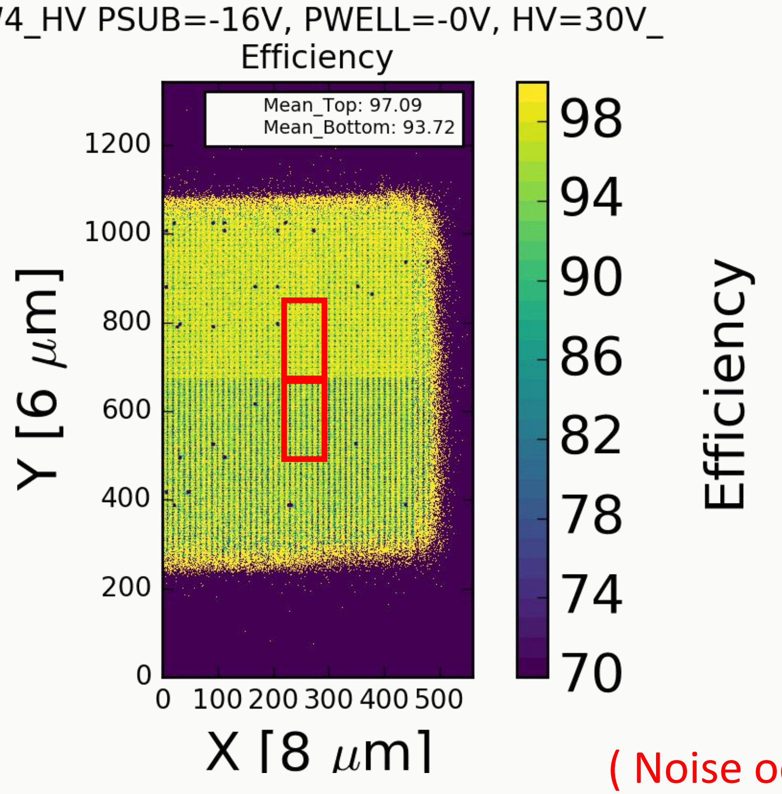


97.1%



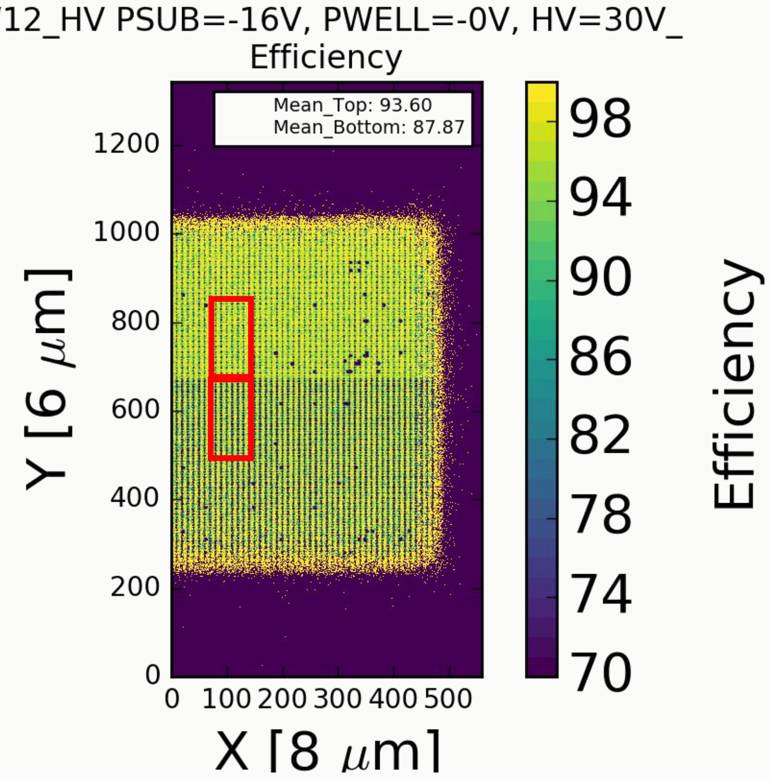
93.7%

DIFFERENCES DUE TO N-LAYER DOPING



W04 (HV): UNIRRADIATED

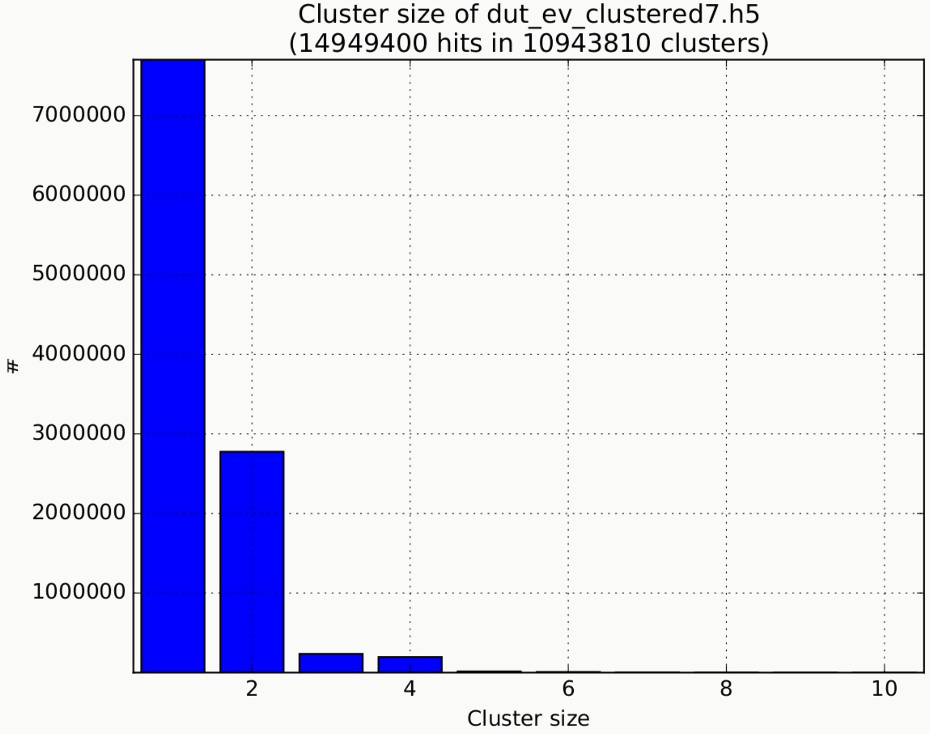
(Noise occupancy < 10 Hz/pixel)

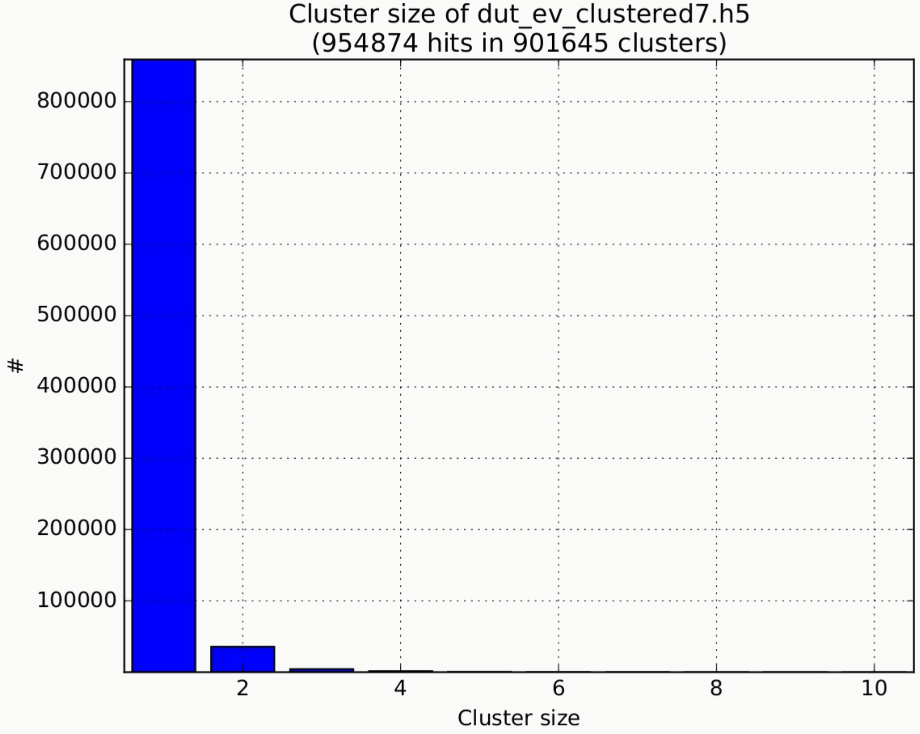


W12 (HV): UNIRRADIATED

- Mean efficiency larger for unirradiated W4 than for W12

CLUSTER SIZE FROM TEST BEAM (TJ-MONOPIX)



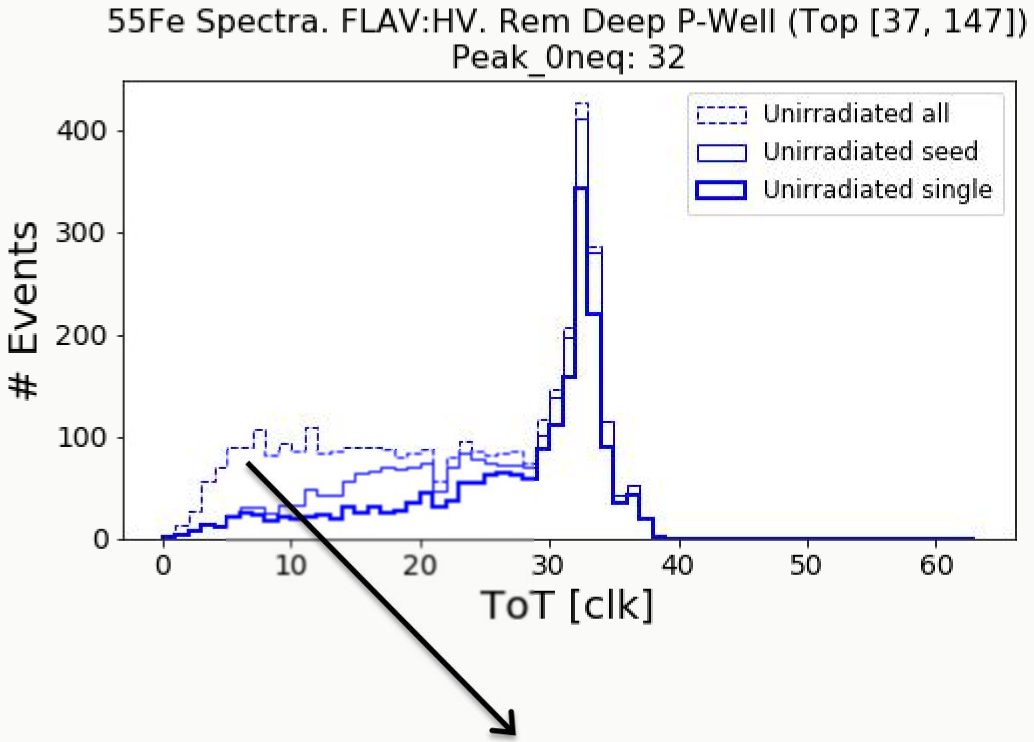


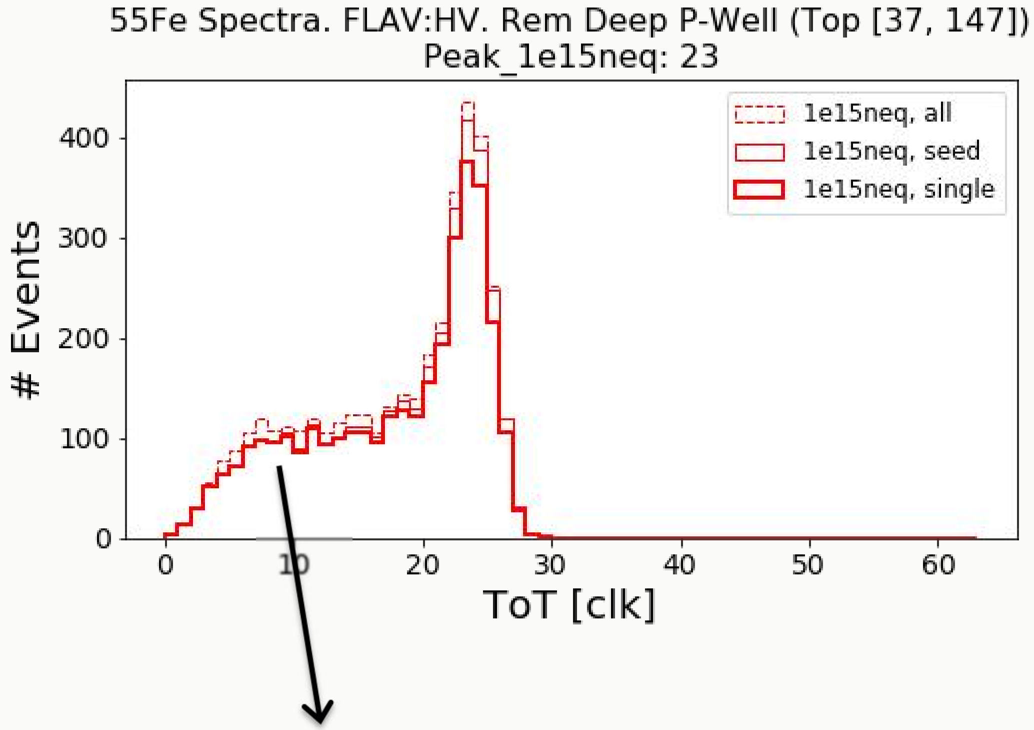
W04 (HV): UNIRRADIATED

W04 (HV): $1x10^{15}\ n_{eq}/cm^2$

- The cluster size decreases after irradiation ---> Less charge sharing.

55-FE SPECTRA BEFORE AND AFTER IRRADIATION





- We observe charge sharing in the unirradiated sample, but not after irradiation

(This observation agrees with the cluster size measurement during test beam)