Advances on Integration of Monolithic Silicon Sensors in Pixel Trackers

Roberto Cardella
ESR 9
Sv. Petra Riedler (CERN)
Sv. Heidi Sandaker (UiO)
CERN EP-DT-DD
Outline

1. MALTA and MiniMALTA sensors
   - From Assembly to Efficiency
   - Rad Hardness studies
   - Improvements and MiniMalta

2. A large area CMOS module

3. Chip To Chip Communication

4. Buried Microchannel in CMOS Devices

5. High Speed Data Transmission in Trackers
   - LAPA testchip Results

6. Conclusions
The 512x512 pixel $36.4 \mu m^2$ - 8 sectors

- Small collection electrode sensor (shared with MONOPIX)
- Low-power front-end (shared with MONOPIX)
- Novel Asynchronous Readout architecture

For more details see presentation of I.Berdalovic and F.Piro
Collection Efficiency Characterization - MALTA

ELSA-BONN Exposed MALTA to a 2.5 GeV electron beam during 3 days

SPS- CERN Down to in-pixel efficiency

Target Efficiency

>97% after $1 \times 10^{15} n_eq cm^{-2}$
Decreasing threshold from ~600 e\textsuperscript{-} to ~250 e\textsuperscript{-} (unirrad.)

\textbf{Unirradiated:} lowering the threshold gives full efficiency

Cannot go lower with threshold because of RTS noise and masking issue

See I. Berdalovic presentation
Collection Efficiency Characterization - MALTA

Unirradiated: lowering the threshold gives full efficiency

Decreasing threshold from ~600 e⁻ to ~250 e⁻ (unirrad.)/350 e⁻ (irrad.)

Neutron irradiated

Could not reach lower threshold (RTS + MASKING ISSUE)

inefficiency in pixel corners due to low lateral electric field
Efficiency vs. deep p-well coverage
Efficiency vs. deep p-well coverage

- Deep p-well only needed under n-wells of PMOS transistors
- In-pixel efficiency can be correlated to deep p-well coverage around the collection electrode
- Removed deep p-well results in higher overall efficiency due to higher lateral electric field
Pixel design improvements

Additional “extra-deep p-well” layer
• Already known by TowerJazz: no process R&D needed

Gap in the n-layer
• requires only a change of the existing mask for the n-layer

After irradiation simulated current pulse

Magdalena Munker
Mini MALTA pixel matrix

- Pixel size: 36.4 μm x 36.4 μm
- 64x16 pixel matrix includes 8 sectors with splits on analogue front-end design, reset mechanism and process

MiniMALTA with synchronization and fixes for improved charge collection
Testbeam campaigns

EUDAQ DURANTA telescope in DESY

MALTA telescope in ELSA
Before Irradiation

<table>
<thead>
<tr>
<th>Sector ID</th>
<th>Front-End</th>
<th>Sensor</th>
<th>Reset Mechanism</th>
</tr>
</thead>
<tbody>
<tr>
<td>S0</td>
<td>Enlarged</td>
<td>Standard</td>
<td>Diode</td>
</tr>
<tr>
<td>S1</td>
<td>Enlarged</td>
<td>Extra Deep p-well</td>
<td>Diode</td>
</tr>
<tr>
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<td>PMOS</td>
</tr>
<tr>
<td>S3</td>
<td>Enlarged</td>
<td>n^- Fap</td>
<td>Diode</td>
</tr>
<tr>
<td>S4</td>
<td>Standard</td>
<td>Standard</td>
<td>Diode</td>
</tr>
<tr>
<td>S5</td>
<td>Standard</td>
<td>Extra Deep p-well</td>
<td>Diode</td>
</tr>
<tr>
<td>S6</td>
<td>Standard</td>
<td>Standard</td>
<td>PMOS</td>
</tr>
<tr>
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<td>Standard</td>
<td>n^- Gap</td>
<td>Diode</td>
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<tr>
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<th>Efficiency (enlarged trans. region) [%] / threshold [e^-]</th>
<th>Efficiency (standard trans. region) [%] / threshold [e^-]</th>
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<tbody>
<tr>
<td>n-gap</td>
<td>99.6 ± 0.1 / 200e^-</td>
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Neutron Irradiated

\[ 1 \times 10^{15} n_{eq} cm^{-2} \]

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Matching ATLAS ITk requirements!
CMOS development for the ATLAS ITk

Outermost layer of ITk Pixel Barrel
- 2016 quad modules
- 3m² (~45% of outer barrel layers)

Monolithic CMOS sensors were considered as option for the outermost layer
- Saves bump bonding for ~45% of outer barrel system
- Substantial cost reduction and reduced module assembly time
- Requires “Drop-In” module compatibility to hybrid module
Integrating a CMOS Module in a Tracker

Module Design

Dead Area Minimization

Sensor cooling

Data Transmission
Pixels operated at -30 °C to avoid thermal runaway

Critical Parameters

- Good thermal conductivity
- Low thermal expansion mismatch between parts
- Integration with mechanics

Embedding the channels in the sensor!
Could improve all the three parameters

Buried Channels Technology (BCT)

J. Bronuzzi, R. Callegari, R. Cardella, C. Lipp, A. Mapelli, P. Riedler
BCT Process

Processed at the CMI – EPFL, Lausanne

DRIE of 30 µm deep trenches (3 x 10 µm)

XeF$_2$ etching of microchannels (diam. 40 µm)

Trenches filled with Parylene (5 µm)
MALTA with BCT
MALTA with BCT
MALTA with BCT – Functional Test

**55Fe source scan**

- Peaks fit comparable
- Distance of the peaks within the gain dispersion of MALTA
MALTA with BCT – Functional Test

55Fe source scan
• Peaks fit comparable
• Distance of the peaks within the gain dispersion of MALTA

Collection Efficiency
• Readout issue reduced the efficiency of ALL detectors to ~70%
• Comparable efficiency for the different ROIs
**MALTA with BCT – Functional Test**

**55Fe source scan**
- Peaks fit comparable
- Distance of the peaks within the gain dispersion of MALTA

**Collection Efficiency**
- Readout issue reduced the efficiency of ALL detectors to ~70%
- Comparable efficiency for the different BCTs

---

BCT process does not change the device performance!
BCT Thermal Test - No Cooling

Hot area about 29°C
5ml/min -> 10 ml/min

Hot area from 29°C to 24°C, using “fresh” water
Data Transmission from Module

Several solutions to transmit data from a module to the readout

**Master/Slaves configuration:**
- Avoid large number of output connections
- Could simplify flex design
- Only one sensor transmits data over a long distance

![Diagram of Master/Slaves configuration]
**Chip 2 Chip Communication**

**Wirebond connection**

MALTA can transmit power and data asynchronously to a neighboring chip (via CMOS pad), merging the data of multiple pixel matrix in just one parallel output.

**Flip chip connection**

Connection between neighboring chips using flip chip:
- Better for assembling
- Allow additional electronics in the flipchip
MALTA can transmit power and data asynchronously to a neighboring chip (via CMOS pad), merging the data of multiple pixel matrix in just one parallel output.

Connection between neighboring chips using flip chip:
- Better for assembling
- Allow additional electronics in the flipchip

Can save Power and Reduce the Material Budget!
MALTA Chip2Chip data transmission
MALTA Chip to Chip Data Transmission

$^{90}$Sr source

Compatible results in both directions
LAPA: pseudo-LVDS for the ATLAS Pixel Apparatus

- 280 X 240µm² (2 pad pixel pitch)
- Tunable DC current (7x 0.8mA)
- Modular capacitive coupled pre-emphasis: 16 blocks driving 25fF each.
- Vcm feedback control at 0.8V.
- External 100 Ω differential termination
- 40 drivers integrated in MALTA (up to 2Gb/s)

5Gb/s

Dedicated testchip
LAPA Receiver

5Gb/s

- 320 X 240 (2 pad pixel pitch) $\mu$m\(^2\)
- Internal selectable 100 $\Omega$ termination resistor

<table>
<thead>
<tr>
<th>SPEC</th>
<th>Min</th>
<th>Max</th>
<th>Tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCM</td>
<td>0.7 V</td>
<td>1 V</td>
<td>0.75 V</td>
</tr>
<tr>
<td>Vdiff</td>
<td>0.3 V</td>
<td>-</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Term Res</td>
<td>-</td>
<td>-</td>
<td>100 $\Omega$</td>
</tr>
<tr>
<td>Bit rate</td>
<td>-</td>
<td>-</td>
<td>5 Gbit/s</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power</th>
<th>Current [mA]</th>
<th>Power [mW]</th>
<th>Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static</td>
<td>2.69</td>
<td>4.84 V</td>
<td>-</td>
</tr>
<tr>
<td>Dynamic</td>
<td>-</td>
<td>0.44</td>
<td>5 Gb/s</td>
</tr>
<tr>
<td>Total</td>
<td>-</td>
<td>5.28</td>
<td>5 Gb/s</td>
</tr>
<tr>
<td>Bias Static</td>
<td>0.94</td>
<td>1.7 V</td>
<td>-</td>
</tr>
<tr>
<td>RX+Bias</td>
<td>-</td>
<td>6.98</td>
<td>5 Gb/s</td>
</tr>
</tbody>
</table>
LAPA eye diagram measurement

5Gb/s

1.28Gb/s (ITk specification)

Jitter_{p-p} = 71ps

Jitter_{p-p} = 38ps
LAPA @1.28 Gbit/s on FLEX ITk prototype

Flex for data transmission out of the ITk system (length~5m)
Conclusions

The small collection electrode shows a collection efficiency >97% after neutron irradiation to \(1 \times 10^{15} n_{eq} cm^{-2}\).

- The first version of the sensor (MALTA), suffers from degraded efficiency in the pixel corners after irradiation.
- Two process modifications have been developed using technology simulations, promising to improve the sensor radiation-hardness.
- The two new versions of the pixel have been implemented in the MiniMALTA sensor, which confirmed the results of the simulations, achieving the target radiation hardness, matching the ATLAS ITk outermost layer requirements. However, the collaboration has chosen to use Hybrid Pixel as baseline solution for the detector upgrade.

Several R&D towards the integration of CMOS pixel sensors have been carried on.

- A CMOS compatible microchannel fabrication process, has been successfully performed with the MALTA sensor. The sensor test demonstrate that the chip performance are not degraded after processing. The preliminary cooling tests demonstrate that this approach could be use in future applications.
- The data transmission in the tracker has been addressed with the development of a chip to chip communication schema and the design of a 5Gb\s low-power LVDS driver and receiver (LAPA). Both are promising to reduce power consumption, hence the overall material budget.
- Studies on a CMOS module have been performed, aiming to define the constrains for the future CMOS sensor design, and minimize the dead area.
My Year

Guiding in ATLAS cavern

ELSA-TESTBEAM

PIXEL2019 Taipei

University of Glasgow

Exam @ UiO

IMEC - COURSE
My Year

Guiding in ATLAS cavern

ELSA-TESTBEAM

PIXEL2019 Taipei

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Thank you for the attention
7 HBRIDGE blocks of 0.8mA - max: total 6mA
16 BLOCKS driving 25fF coupled with the output pad
Pre Emphasis Simulations

Simulations of the LVDS OUTPUT

<table>
<thead>
<tr>
<th>PRE</th>
<th>PwSH [mW]</th>
<th>PwDig [mW]</th>
<th>PwToT [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>8</td>
<td>7.2</td>
<td>18.6</td>
<td>26.8</td>
</tr>
<tr>
<td>16 (max)</td>
<td>7.2</td>
<td>25.4</td>
<td>33.6</td>
</tr>
</tbody>
</table>
2.5GHz LVDS IN – LVDS OUT. 100Ω termination. 1pF load.

Simulated jitter=45ps
## Preliminary power consumption

### Expected static power consumption

<table>
<thead>
<tr>
<th>Static</th>
<th>Current [mA]</th>
<th>Power [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 Hbridge</td>
<td>4</td>
<td>7.2</td>
</tr>
<tr>
<td>7 Hbridge</td>
<td>5.2</td>
<td>10</td>
</tr>
</tbody>
</table>

### Measurements on test chip

<table>
<thead>
<tr>
<th>Static+Dynamic 1.28Gb/s</th>
<th>Current [mA]</th>
<th>Power [mW]</th>
</tr>
</thead>
<tbody>
<tr>
<td>5 Hbridge</td>
<td>6</td>
<td>10.8</td>
</tr>
<tr>
<td>7 Hbridge</td>
<td>8</td>
<td>14.4</td>
</tr>
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First signs of life from MALTA

ANALOG pixel output

MALTA (not the one under test)

Digital signal from read-out
First signs of life from MALTA

Happy Designers

ANALOG pixel output

MALTA (not the one under test)

Digital signal from read-out