Design and characterization in Depleted CMOS technology for particle physics pixel detector

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ESR-02

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Outline

- ATLAS inner detector upgrade for the HL-LHC
- Depleted CMOS Sensor developments
  - Design and measurements of Single Event Upset (SEU) tolerant memories
  - Developments towards Serial Powering
- Conclusions

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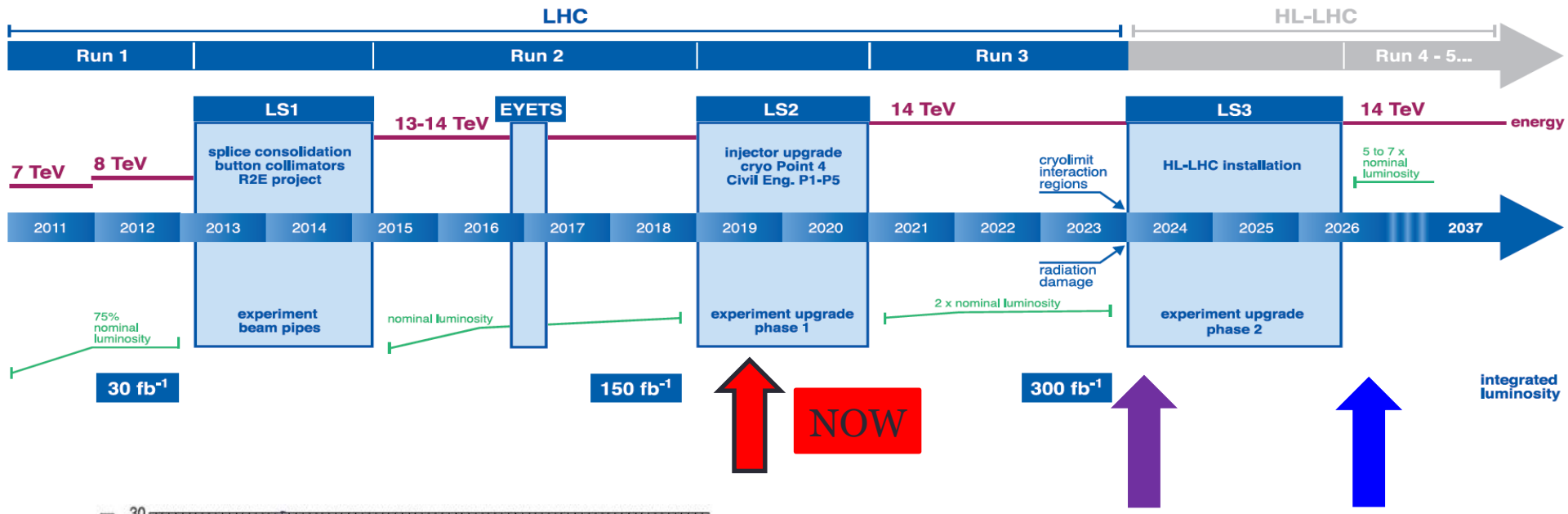
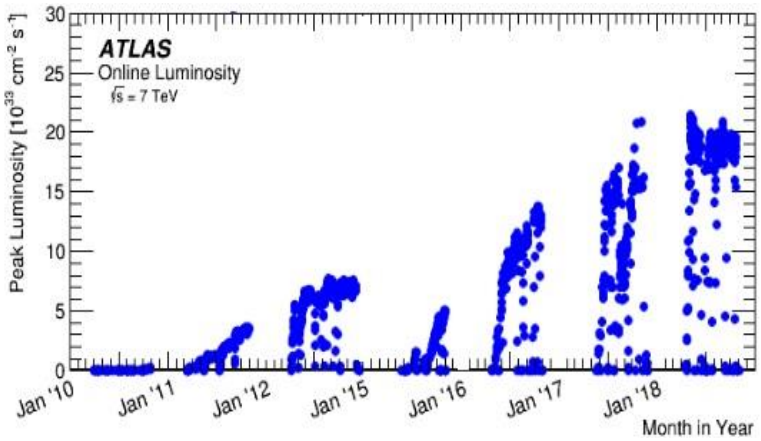
The HL-LHC upgrade

LHC / HL-LHC Plan

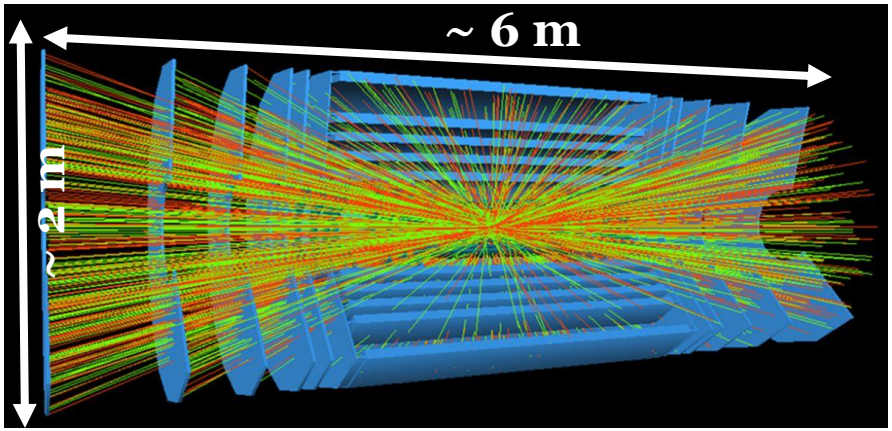


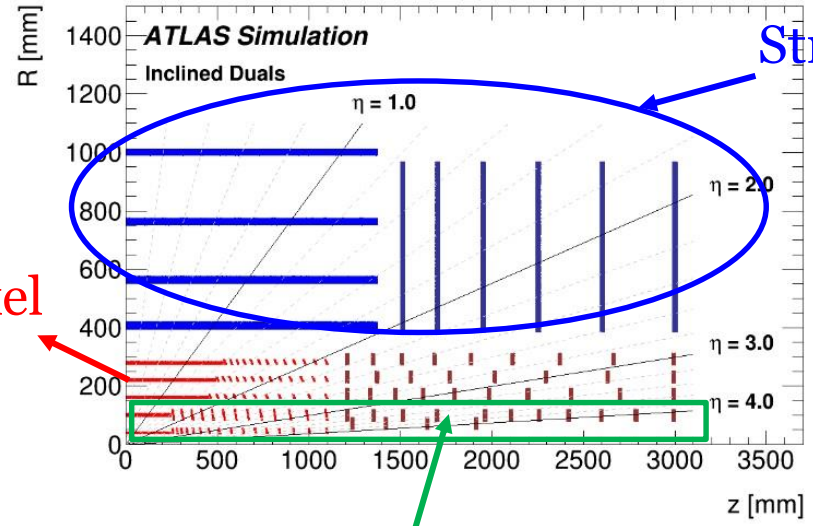


Pixel detector
$L = 2 \times 10^{34}$ cm^{-2} s^{-1}
$\int L\,dt = 500$ fb^{-1}

ITk pixel detector
$L = 7.5 \times 10^{34}$ cm^{-2} s^{-1}
$\int L\,dt = 4000$ fb^{-1}

The new ITk





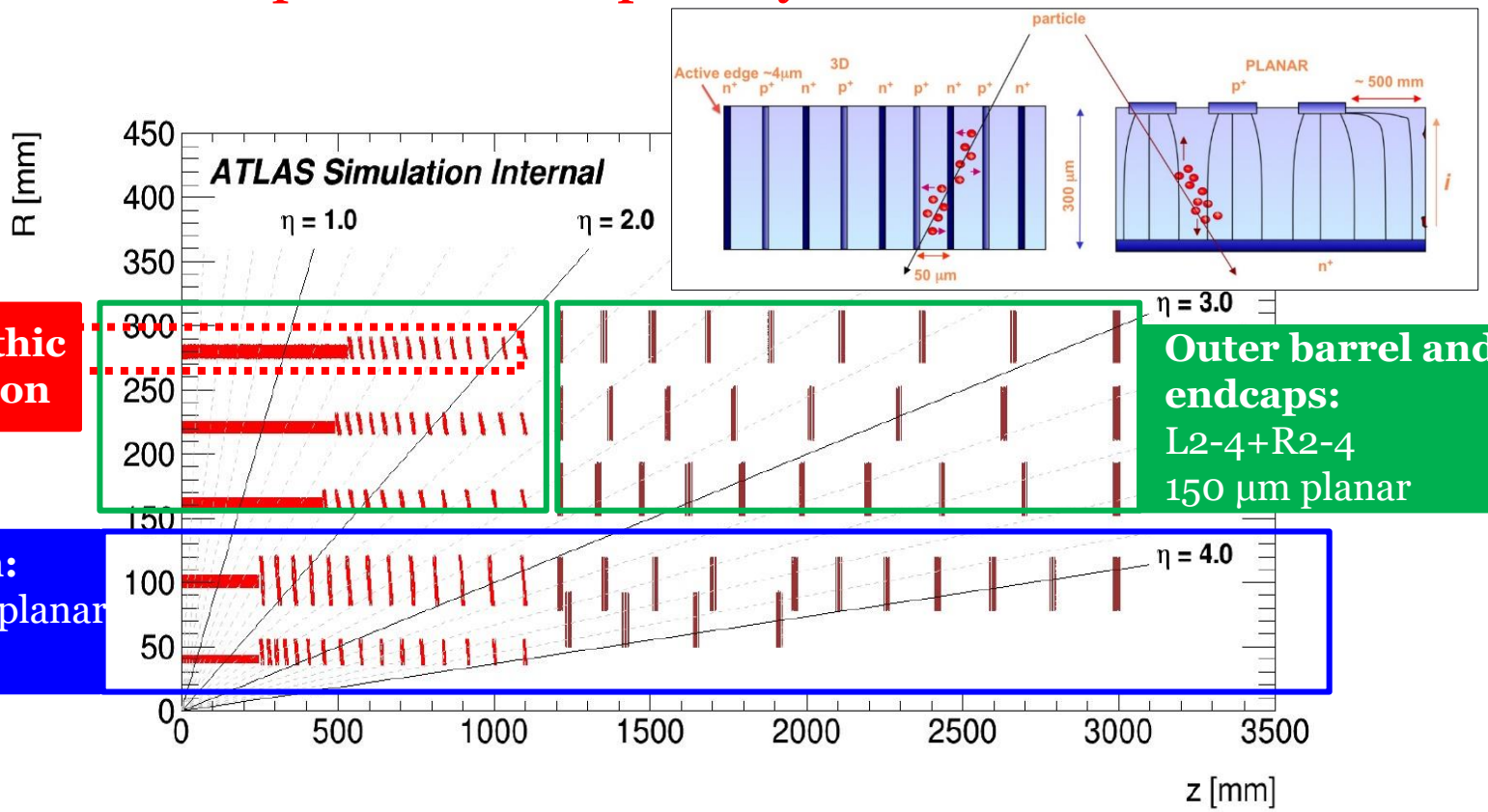
- Strips at outer radii, pixels near to the interaction region.
- **Pixel detector : (R<35cm)**
  - 12.7 m², 5×10⁹ channels
  - 5 barrel layers
  - Inner 2: 3D/planar
  - Outer 3: planar/CMOS
  - 50×50 µm² or 25×100 µm²
  - inclined modules

  → minimize material and maximize resolution while keeping full coverage.

	ATLAS-HL-LHC	
	Outer	Inner
Required Time Res. [ns]	25	25
Particle Rate [kHz/mm²]	1000	10 000
Fluence [n_{eq}/cm²]	10^{15}	10^{16}
Ion. Dose [Mrad]	80	1000

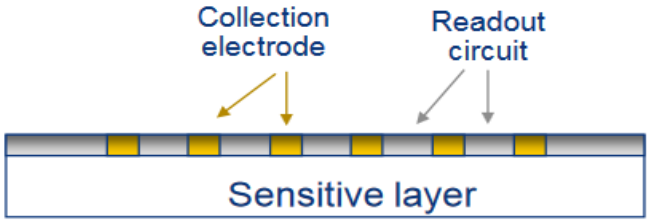
Sensor technologies

- One CMOS IC technology for whole ATLAS & CMS pixel detectors:
  - RD53 collaboration: joint ATLAS and CMS effort on common 65 nm design.
  - Requirements given by the innermost layers
- Sensor technology baseline optimized according to radiation hardness, cost and foundries production capability.



Depleted Monolithic Active Pixel Sensor

Integrate the sensor and electronics on a single entity!

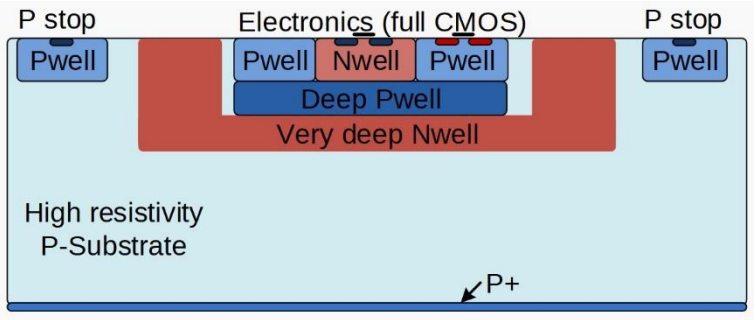


Advantages: Commercial process, no hybridization (reduced material budget, cost and procurement), considerable depleted regions in high-resistive substrates, fast charge collection by drift, multiple wells for shielding, etc...

Two Approaches:

"Large sensor electrode"

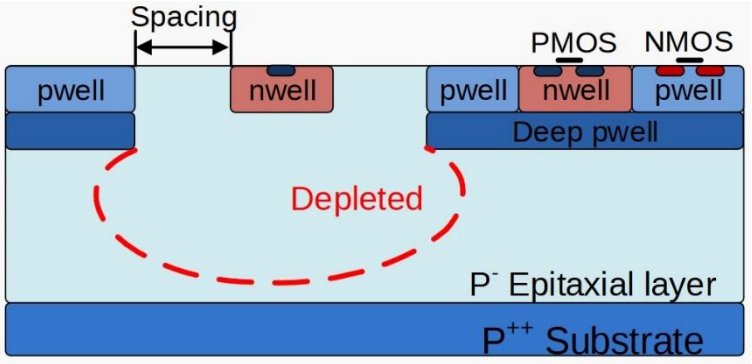
Large collecting well containing the electronics



PROS: Short-drift distances, Rad-hard
CONS: Large sensor capacitance (compromise on timing and noise), higher analog power.

"Small sensor electrode"

Small collecting well, separate from the electronics



PROS: Very small sensor capacitance
CONS: Long drift distances, compromised rad-hardness.

Depleted Monolithic Active Pixel Sensor

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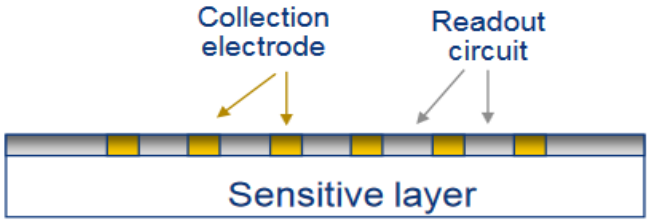

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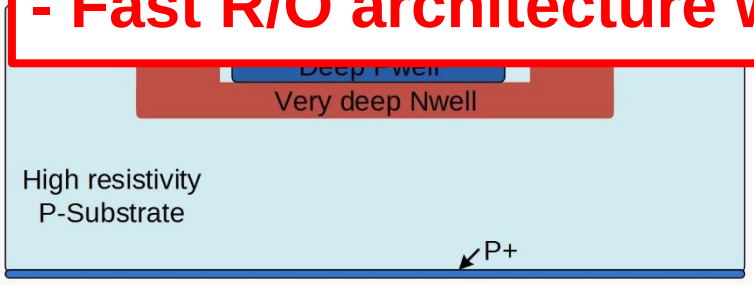
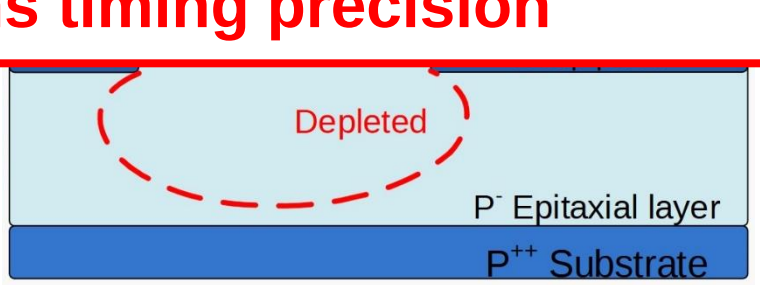
Two main challenges for 5th layer pixel ITk:

- **Rad-hard: 80 MRad & 1.5×10^{15} n_{eq}/cm^2**
- **Fast R/O architecture with 25 ns timing precision**





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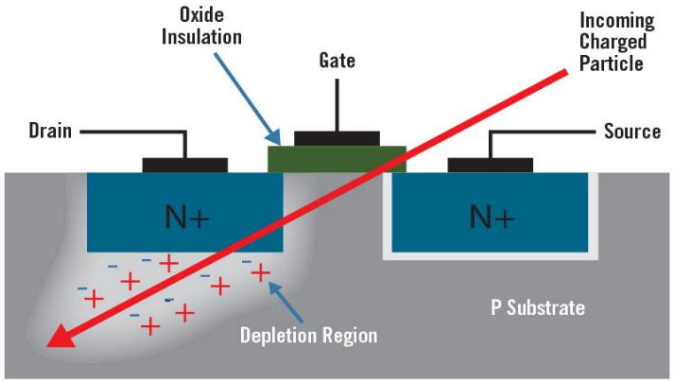
Single Event Upset (SEU) mechanism

- Energetic particle strikes ⟶ Creates ionization path with free e^- and holes



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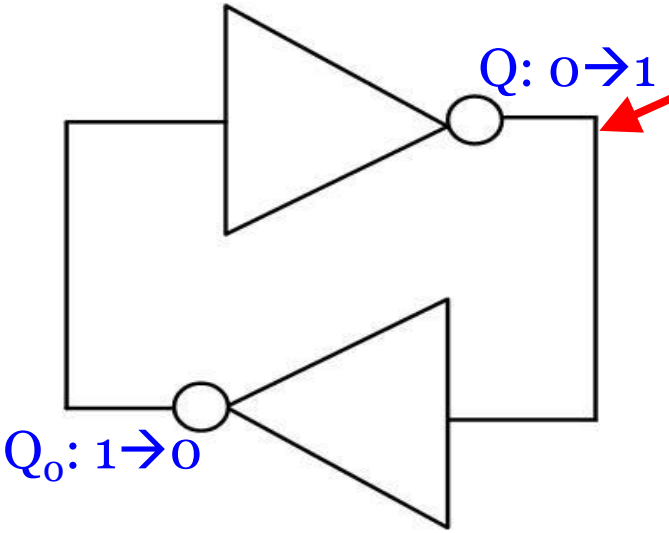
Single Event Effect (SEE)

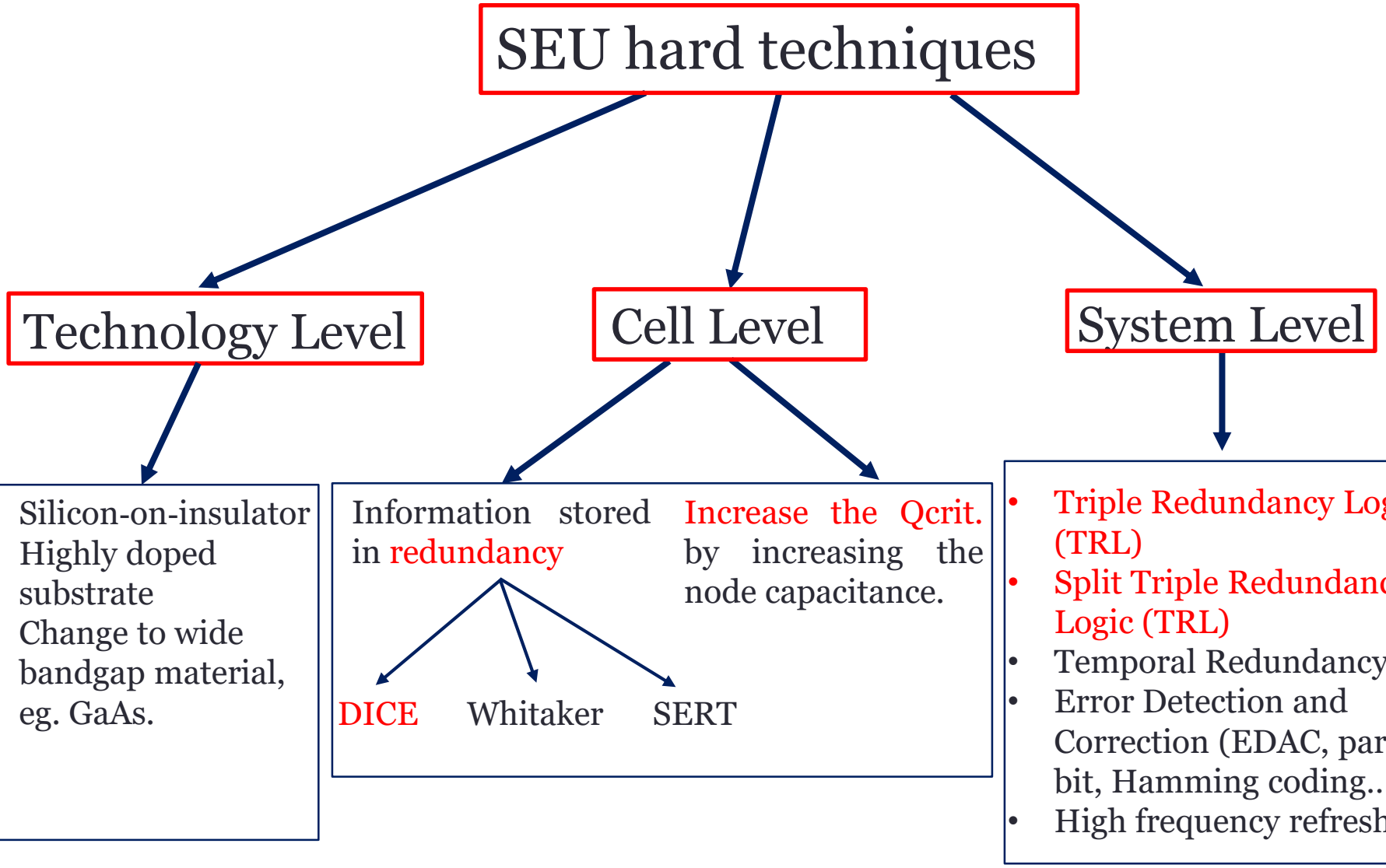
A particle strike
Bit Flip !!!



https://www.lanl.gov/science/NSS/issue1_2012/story4full.shtml

SEUs occur in memories (SRAMS,SDRAMS) and sequential logics!

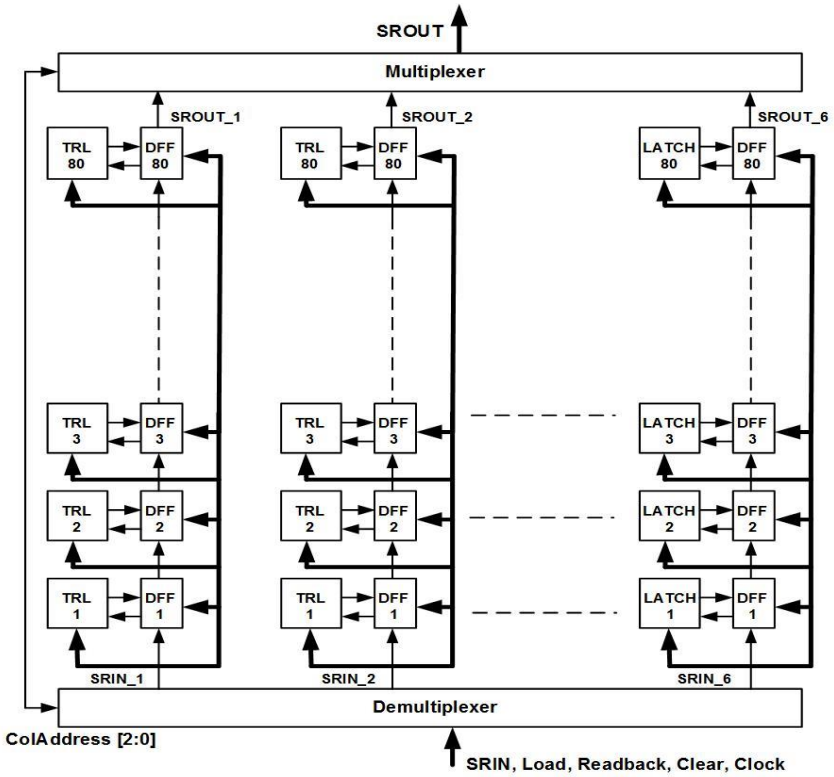
SEU Hardening techniques



SEU tolerant test chips

- 3 SEU tolerant chips in 3 different technologies designed and allow to collect all data from latches and directly compare their behavior during irradiation tests.

- The SEU chip is sub-divided in several columns
  - Typically 80 cells per kind of memories
- Custom patterns are written and read through a shift register in synchronization with the beam.



- **Sequence:**

→ Put data into SR
→ Write into memory
→ Wait for the beam
→ Data back into SR
→ Read through the SR
→ Cal. # of errors

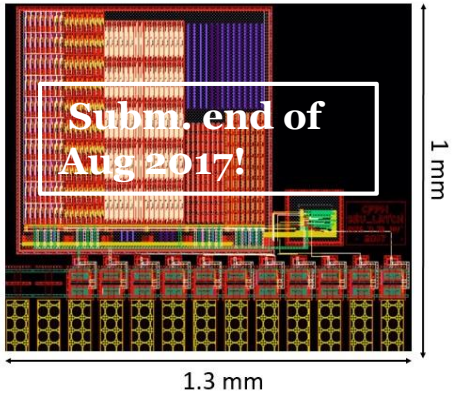
SEU tolerant memories

Different flavors of memories:

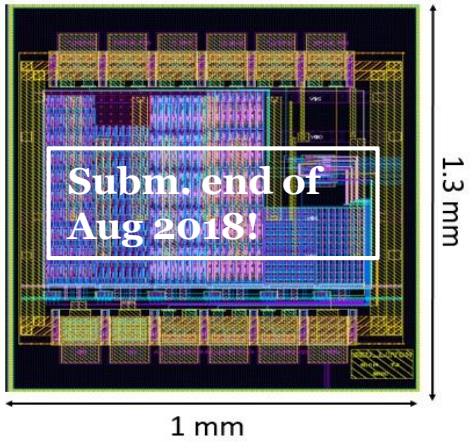
- Col1 : SRAM
- Col2 : Standard Cells
- Col3 : DICE Latch "Dual Interlocked Storage Cell"
- Col4 : Enhanced DICE Latch
- Col5 : Split Triple redundancy with standard cells
- Col6 : Split Triple redundancy with DICE cells
- Col7 : Triple redundancy standard cells
- Col8 : Triple redundancy DICE latch

- **Additional Functions**
  - Columns selector
  - Digital buffer output
  - DeepNwell and HV

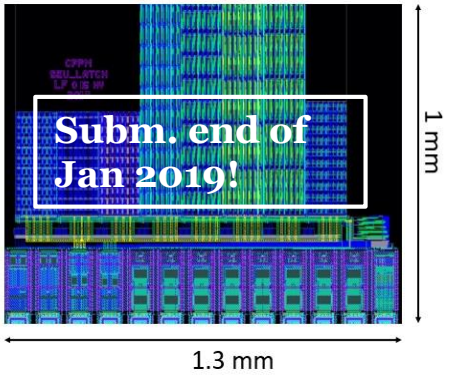
AMS



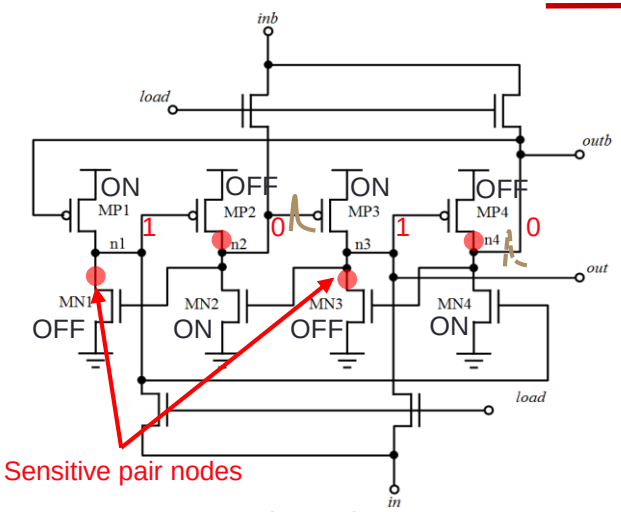
TJ



LF

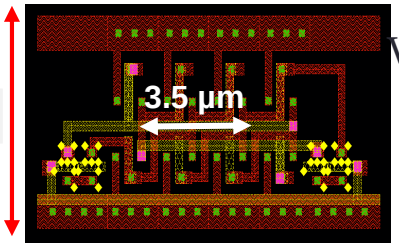


SEU-robustness: DICE Versions

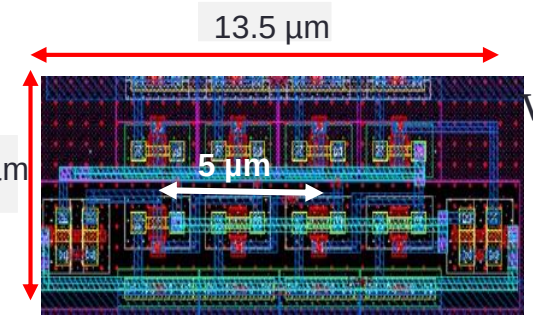


DICE schematic
(example of a stored data = 1)

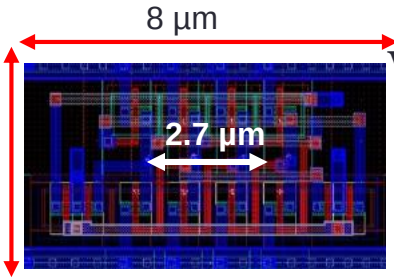
- DICE latch structure is based on the conventional cross coupled inverters:
  - The charges deposited by a ionising particle striking one node can't be propagated due to the stability of this architecture.
  - If 2 sensitive nodes are affected simultaneously, the immunity is lost and the DICE latch is upset.
- 4 versions have been submitted:



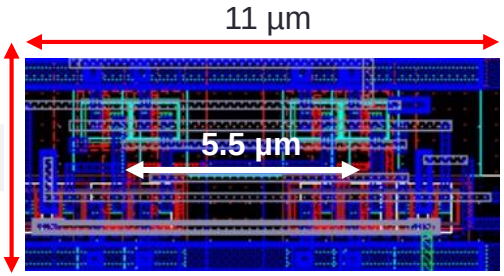
Version 1 (AMS)
DICE structure
W_{PMOS}/L_{PMOS}=220nm/260nm
W_{NMOS}/L_{NMOS}=220nm/260nm
D_{2N} = 3.5 µm



Version 2 (TowerJazz)
DICE structure
W_{PMOS}/L_{PMOS}=220nm/500nm
W_{NMOS}/L_{NMOS}=220nm/500nm
D_{2N} = 5 µm

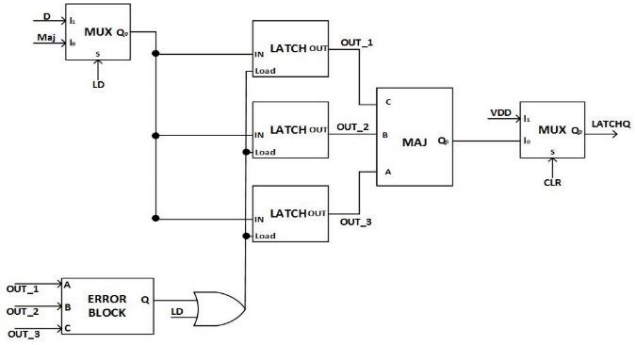


Version 3 (LFoundry)
DICE structure
W_{PMOS}/L_{PMOS}=450nm/150nm
W_{NMOS}/L_{NMOS}=320nm/150nm
D_{2N} = 2.7 µm

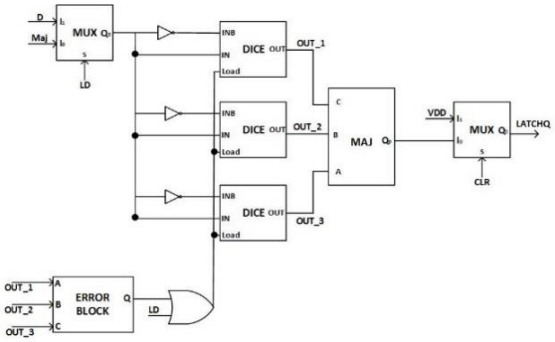


Version 4 (LFoundry)
DICE structure
W_{PMOS}/L_{PMOS}=450nm/150nm
W_{NMOS}/L_{NMOS}=320nm/150nm
D_{2N} = 5.5 µm

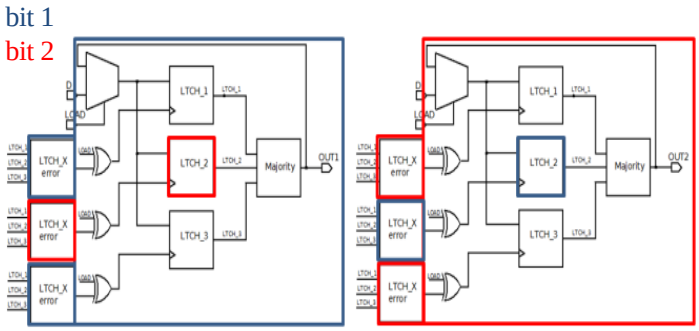
SEU-robustness: TRL Versions



TRL with standard latch

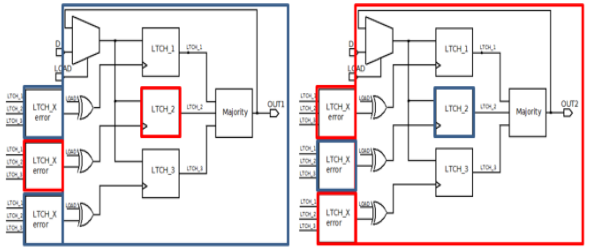


TRL with DICE latch

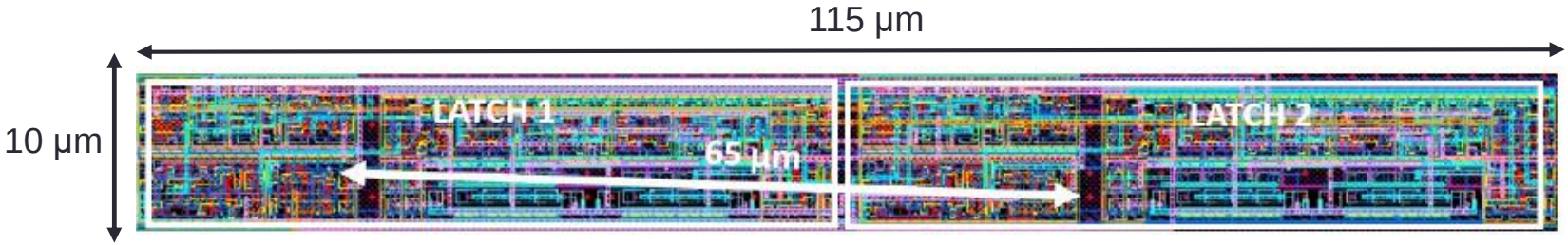


SPLIT TRL with standard latch

- 4 TRL versions have been designed:
  - 1st version: TRL with standard latch.
  - 2nd version: TRL with DICE latch.
  - 3rd version: triplication of the standard latch and increasing the distance between a minimum distance between 2 bits (~65 µm).
  - 4th version: triplication of the DICE latch.

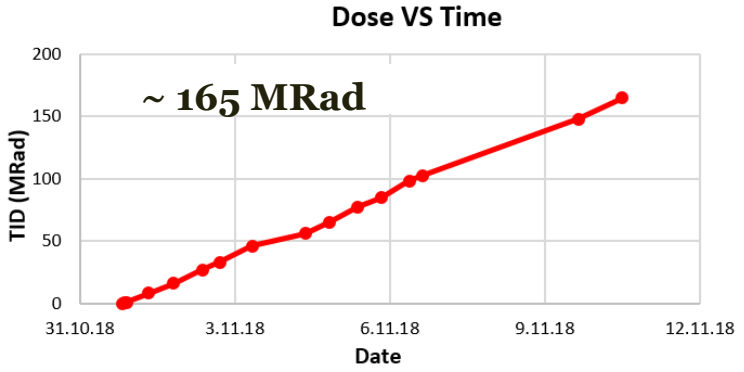


SPLIT TRL with DICE latch



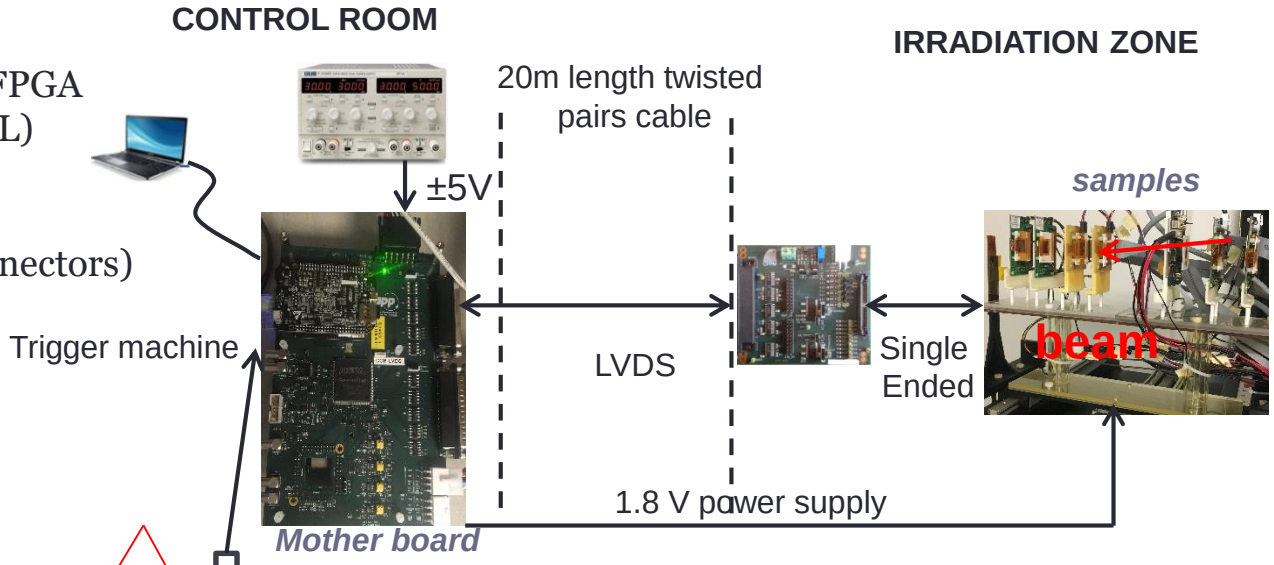
Experimental Setup for AMS SEU test IC

- **24 GeV protons beam line at CERN (east zone PS)**
  - Beam size 1 cm^2
  - Mean dose rate 1.1 MRad/hr
  - TID: 165 MRad
  - Exposure time 10 days
  - 2 AMS chips were installed



Dose does not affect the behavior of the AMS SEU chip

- **Mother board V2**
  - Collaboration with LAPP
  - NanoPC BeagleBone card + FPGA
  - Flexible programming (VHDL)
  - Digital signals
    - 40 TTL signals
    - 32 LVDS signals (DB-37 connectors)
  - Analog channels
    - 4 SAR ADC (16 bits)
    - 10 DAC (16 bits)
  - Lab tests + irradiation tests



- **Test sequence:**

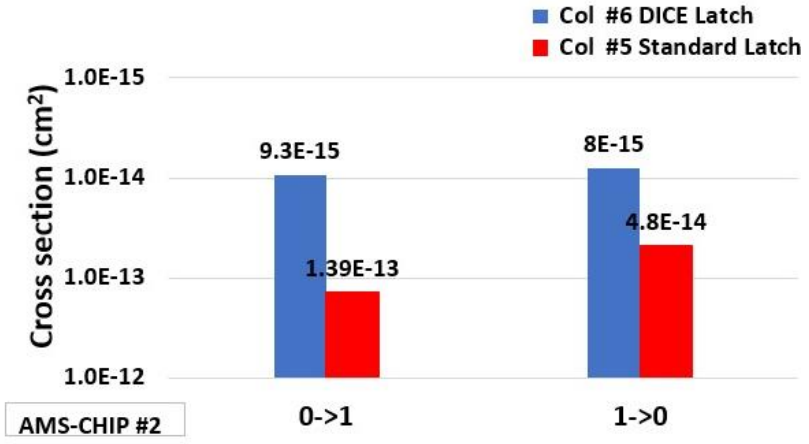
Test results for AMS chip

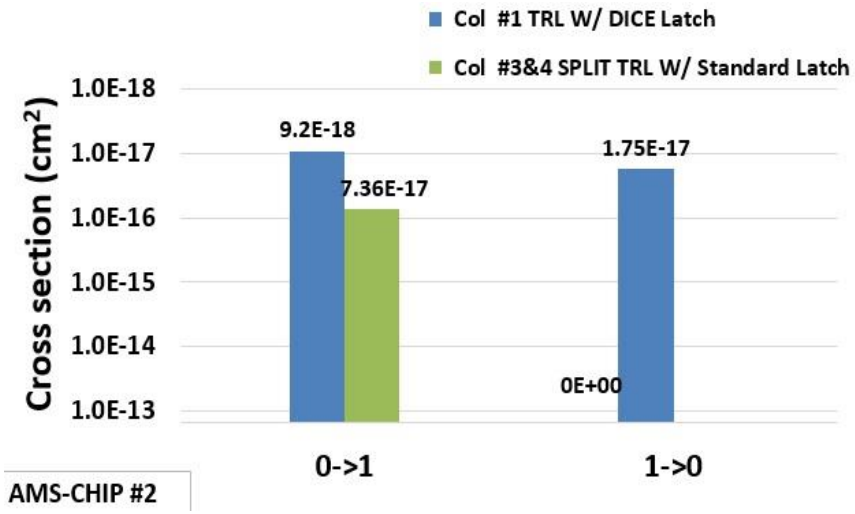
$$\sigma\ (cm^2) = \frac{N_{errors}}{\Phi * N_{latches}}$$

- We stored enough data to extract an acceptable statistic for SEU.

  - 80 cells per type of latch and we reached a spill number > 10000.

- Cross section of the standard latch ~ **138.6 E-15 cm²**
- Cross section of DICE latch ~ **9.3 E-15 cm²**
- SPLIT TRL W/ standard latch shows very good performance with the cross section ~ **7.3 E-17 cm²**
- TRL W/ DICE latch shows very good performance as well with the cross section ~ **9.2E-18 cm²**





DICE is ×15 more robust than the Standard Latch!

TRL w/ DICE Latch is ×15000 more robust than the Standard Latch!

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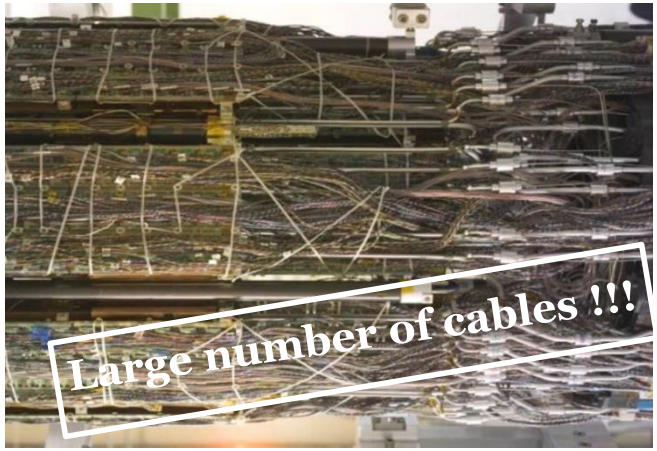
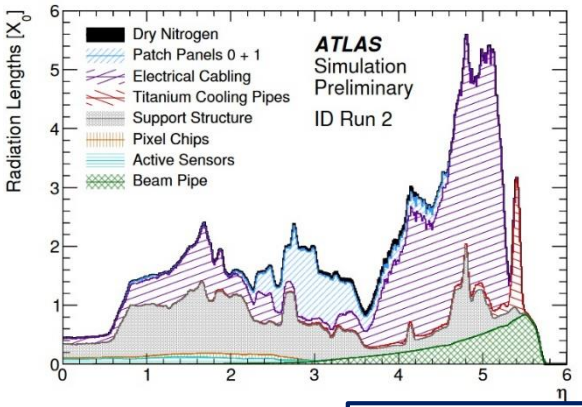
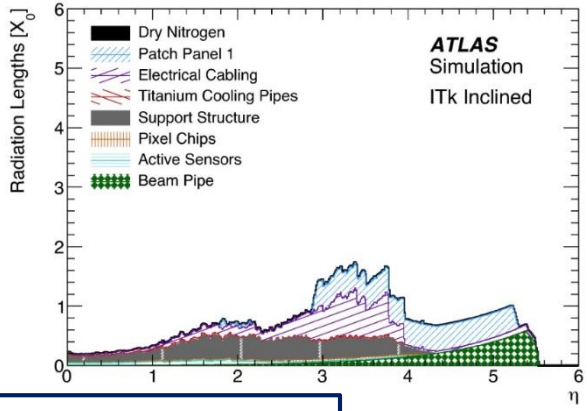
Why choosing Serial Powering?



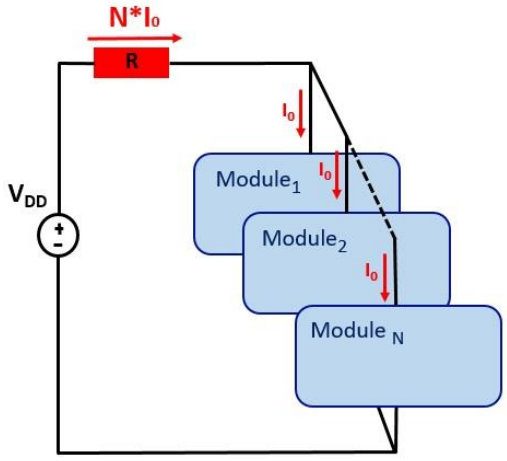




Improved design of services!

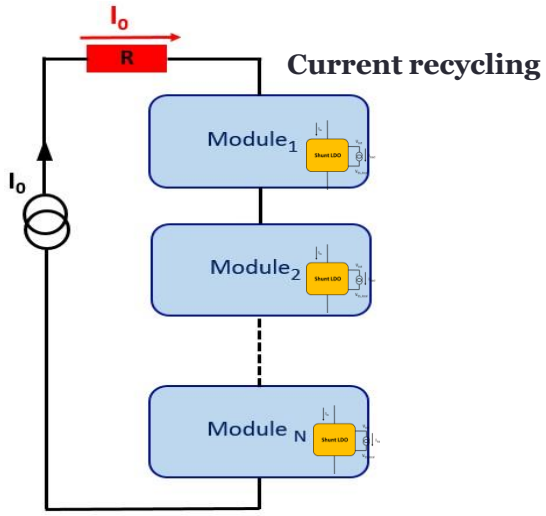
Traditional: Parallel Powering

Big power loss in cables!!!



In ITk: Serial Powering

Small power loss in cables!!!



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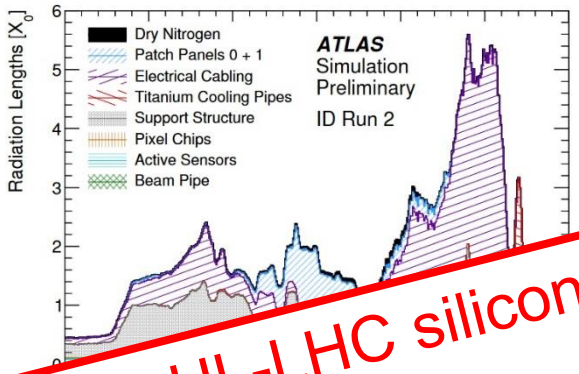
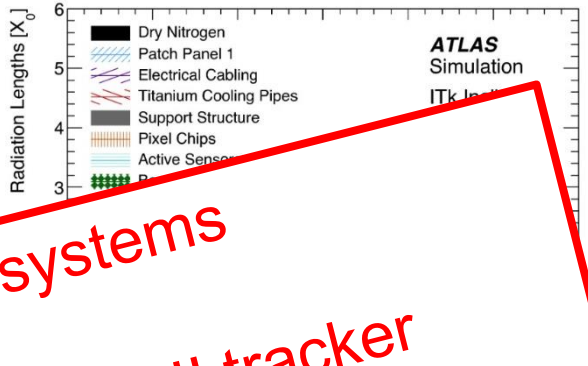
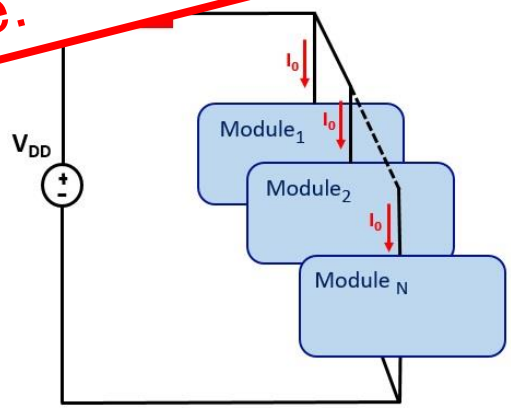


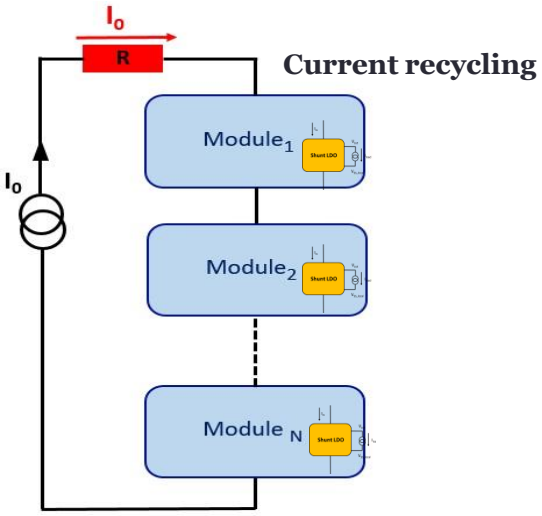


Need for Serial Powering for HL-LHC silicon systems considered self evident.
Parallel Powering no longer used after the Phase II tracker upgrade.

Serial Powering

Small power loss in cables!!!

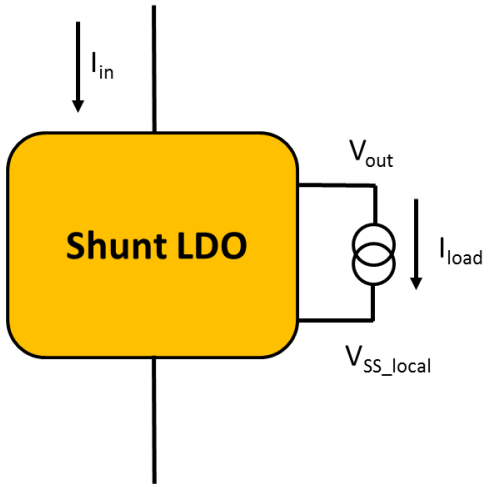


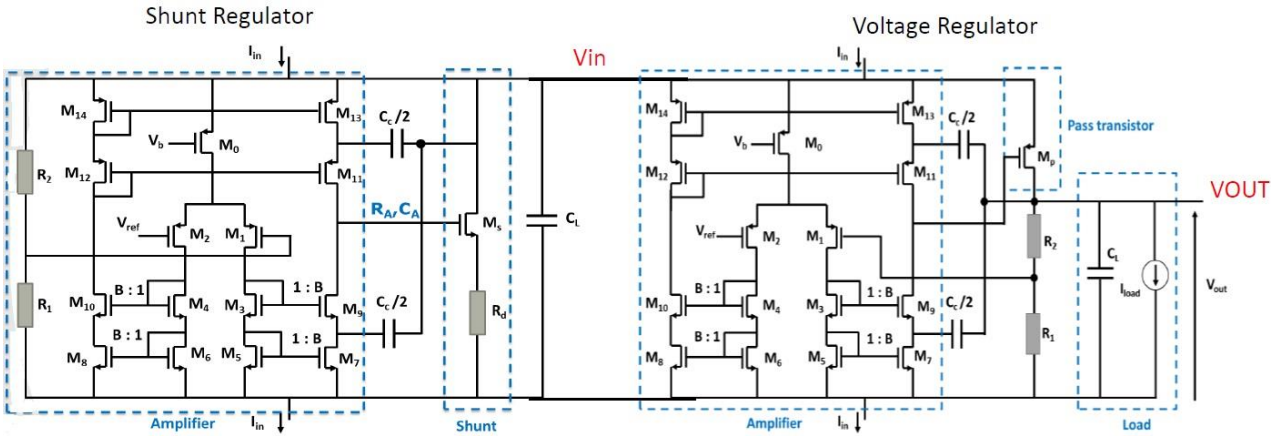


Shunt-LDO: to power electronics

A. Habib, CPPM

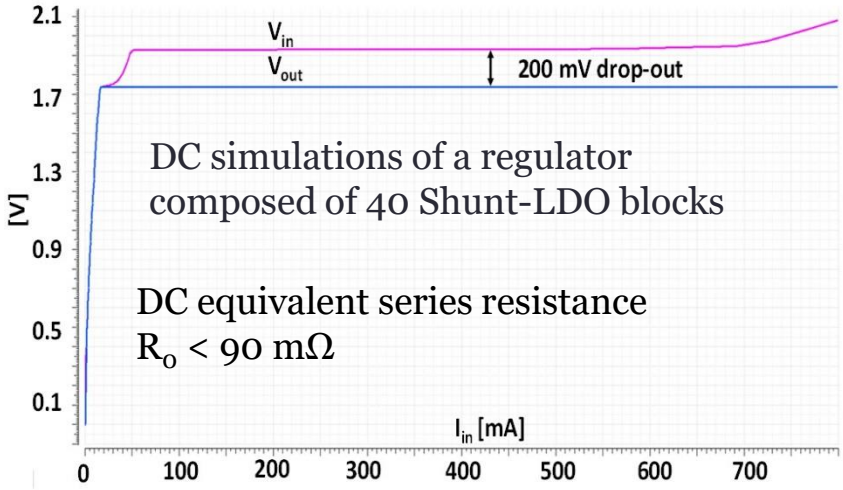
Main idea

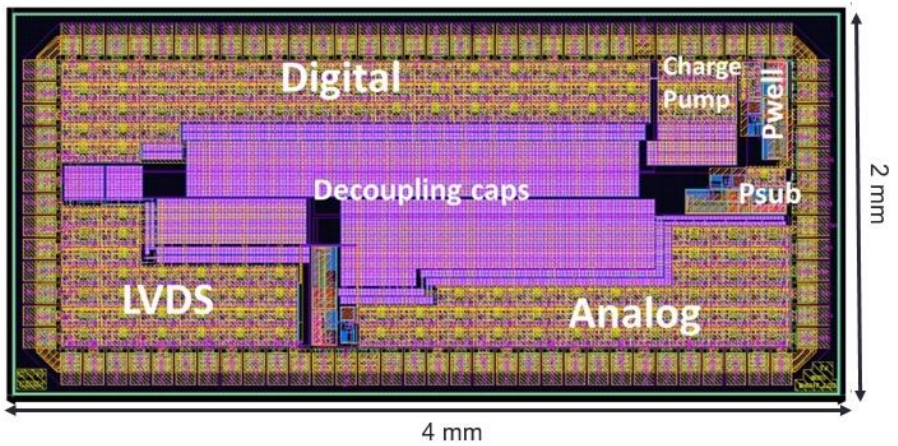




1 Shunt-LDO block delivers an output current of 10 mA

S. Bhat, CPPM

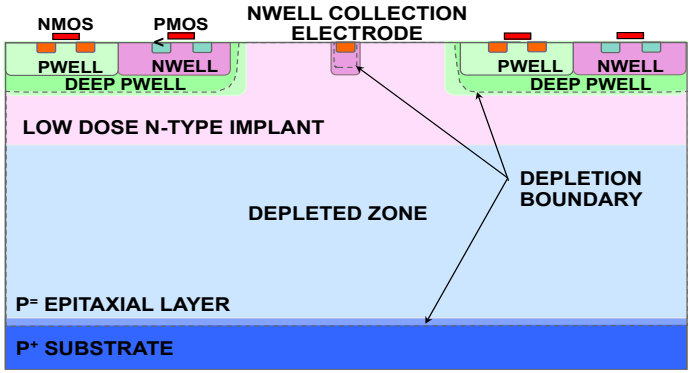




Submitted in Aug. 2018!

Sensor bias: TowerJazz

- Novel modified process developed in collaboration with the foundry.
- Adding a planar **n-type layer** significantly improves depletion under deep pwell.
- Pixel dimensions:
- 36 x 36 μm^2 pixel size
- 3 µm diameter electrodes
- Measured capacitance < 5fF

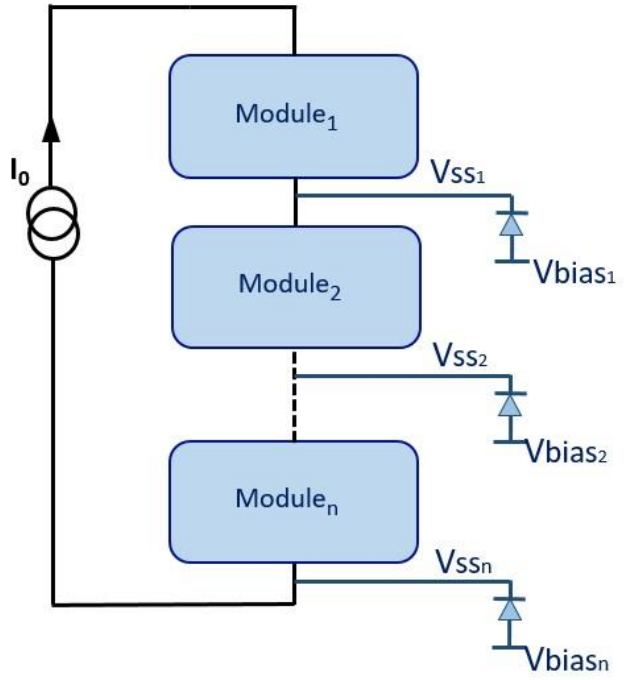


W. Snoeys et al., NIM A871 (2017) 90 – 96.

In order to polarize the sensor in same way

- (Vss_N – $Vbias_N$) must be constant in all modules.
- Since Vss_N is shifted every module

we cannot use the same bias for all modules.

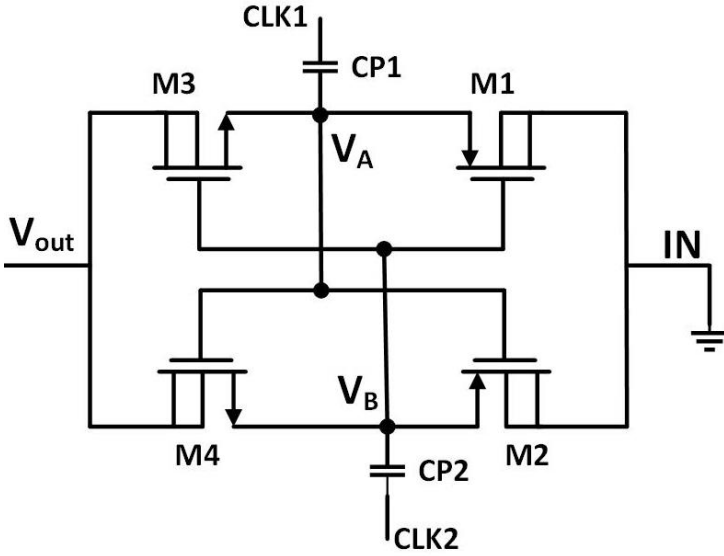


Requirements for Sensor

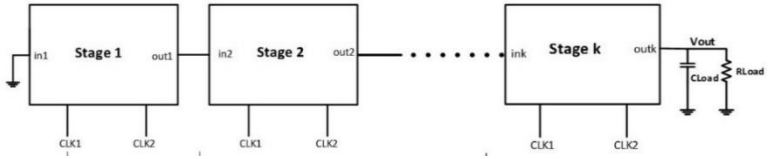
- **HV to pwell = – 6 V**
- **HV to substrate = – 20 V**

Charge Pump: to power sensor

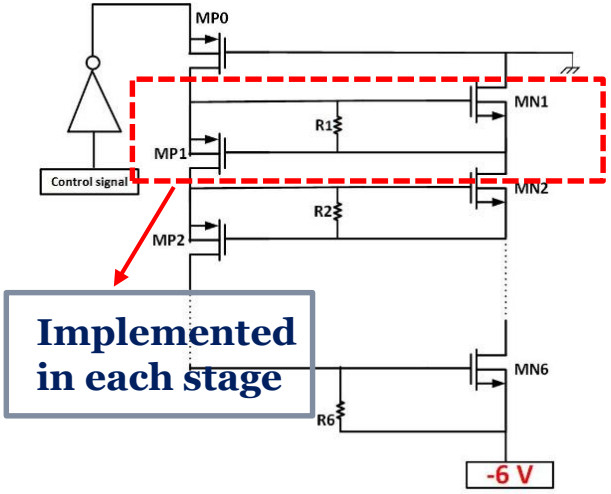
- Cross-coupled architecture of charge pump.
- Two parallel, complementary cross-coupled parts operate in opposite phases.
- The charge pump has several stages.
- The operating frequency is 640 MHz, should deliver 500 µA.



Generating higher voltages



Start-up switch

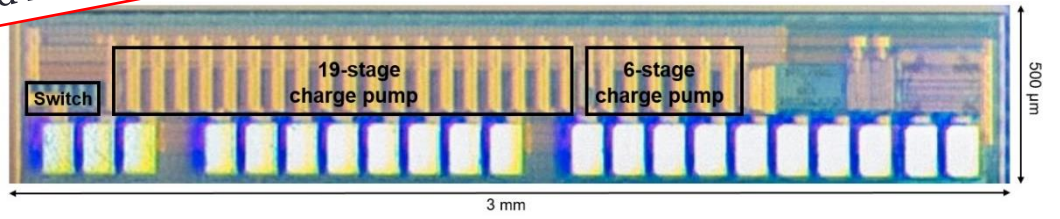


$$Vout = -N * Vdd + N\frac{I_L}{f * Cp}$$

# of stages

Pumping frequency

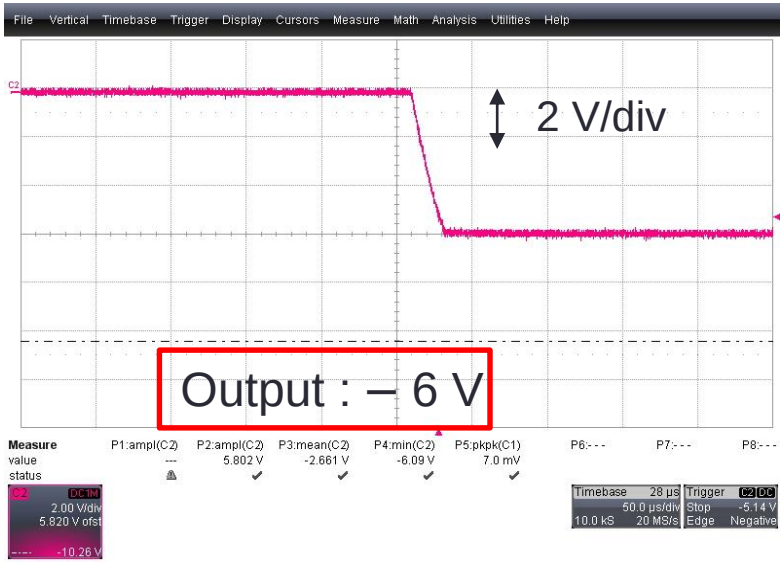
Received in Feb. 2019!

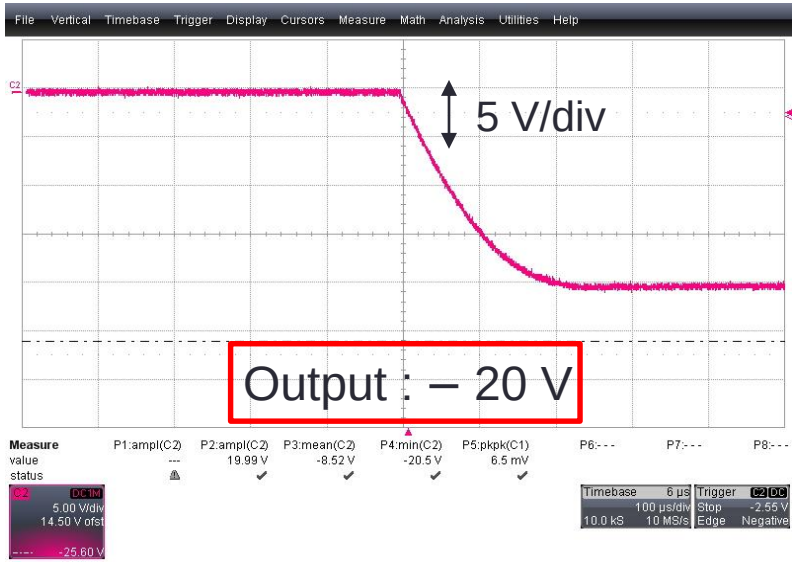


Measurements

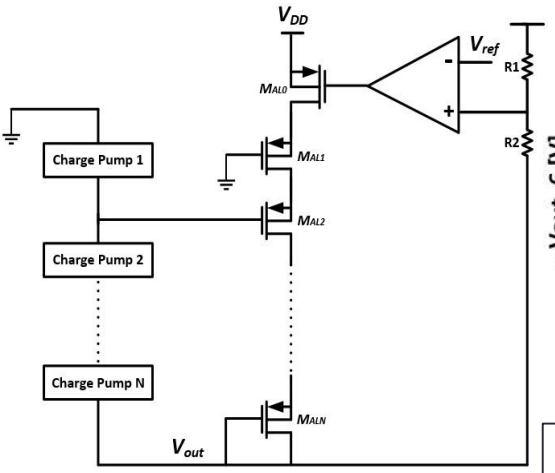
CLK : 640 MHz

Transient response

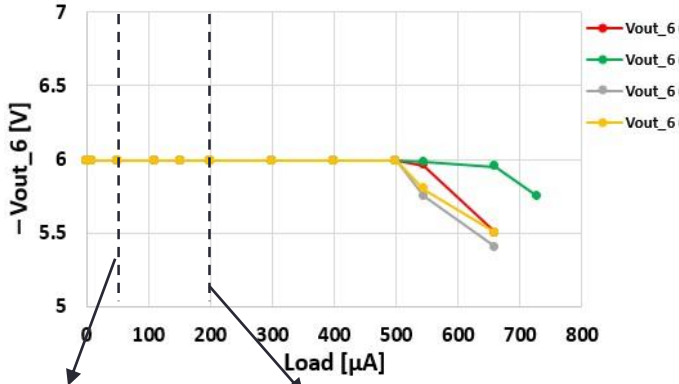




Regulated charge pump



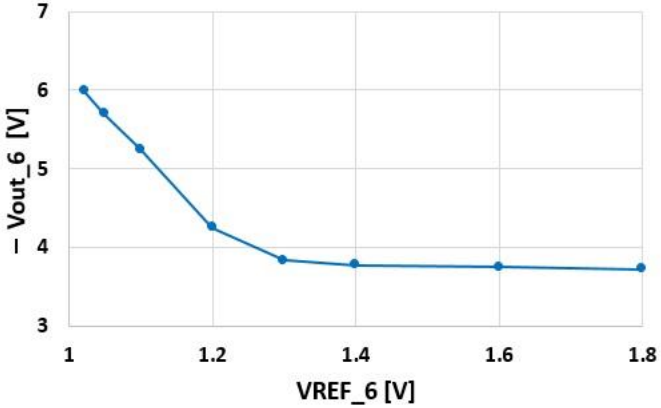
V_{out} vs I_{Load}



TJ MALTA after radiation @ low temp

TJ MALTA after radiation @ room temp

V_{out} vs V_{REF}



Outline

- ATLAS inner detector upgrade for the HL-LHC
- Depleted CMOS Sensor developments
  - Design and measurements of Single Event Upset (SEU) tolerant memories
  - Developments towards Serial Powering
- Conclusions

Conclusions

- **New generation silicon pixel detectors will be an essential part of ATLAS future tracker upgrades where they will be used for tracking and vertexing.**

- **SEU - Radiation Hard Cells**:

→ Designed Single Event Upset tolerant test chips in AMS/TJ/LF technologies in order to study the different architectures for various technologies.

→ Keeping the area almost same as standard latch, DICE is ~15× immune to SEU.

→ TRL have big area penalty (typ: ~20×) but are ~15000× more immune to SEU.

- **Serial Powering is necessary for ATLAS ITk detector**:

→ **Shunt-LDO Regulator for Electronics**:

– The block is able to generate constant voltage of 1.8 V up to 1.4 A of input current for Serially Powering CMOS modules in ATLAS ITk.

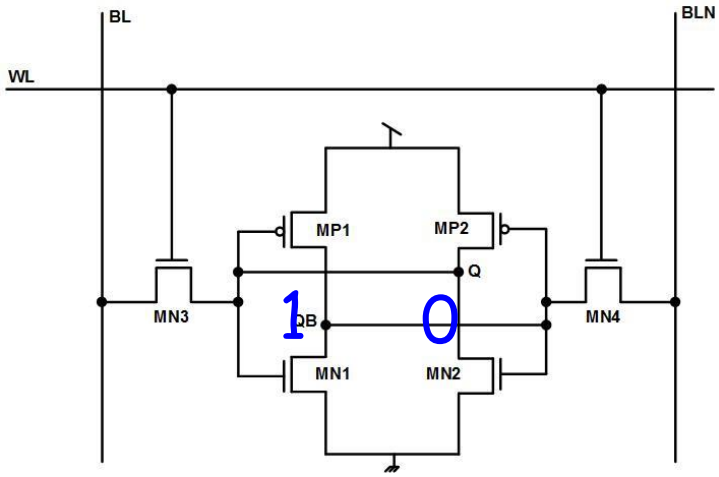
→ **Charge Pump for Sensor Bias**:

– From the measurements → 2 versions of the charge pump circuit show good and stable response and could be used to bias the CMOS sensor.

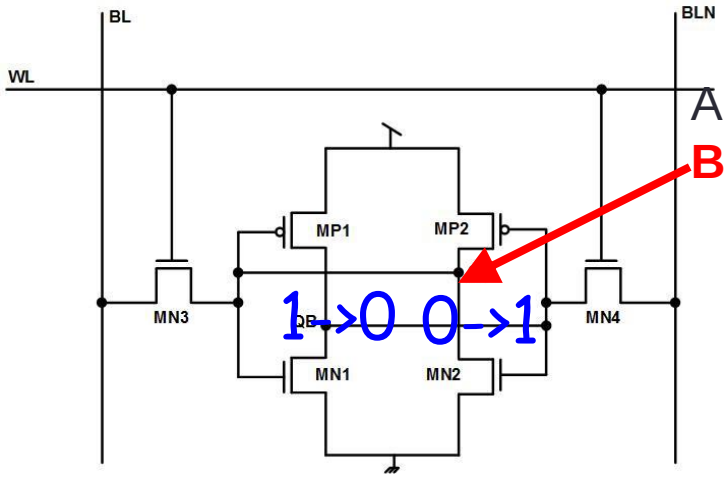
Thank you!

Backup

Critical charge simulations



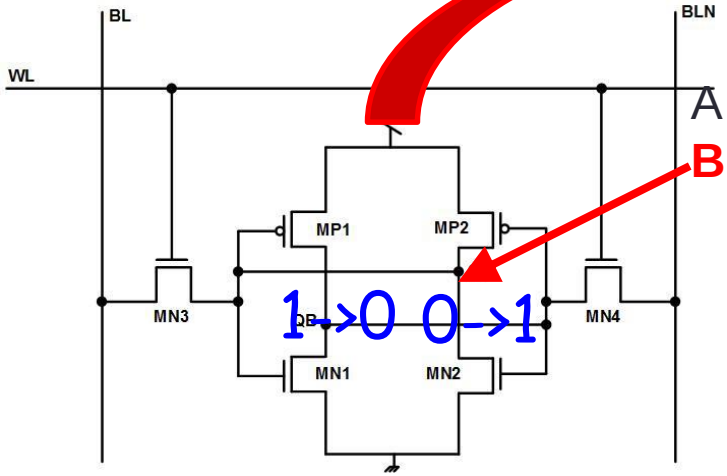
Critical charge simulations



A particle strike

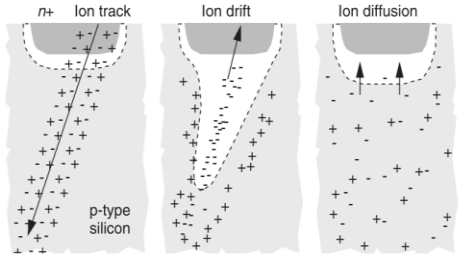
Bit Flip !!!

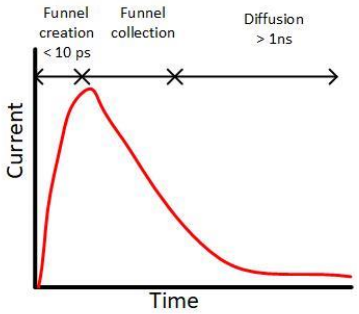
Critical charge simulations



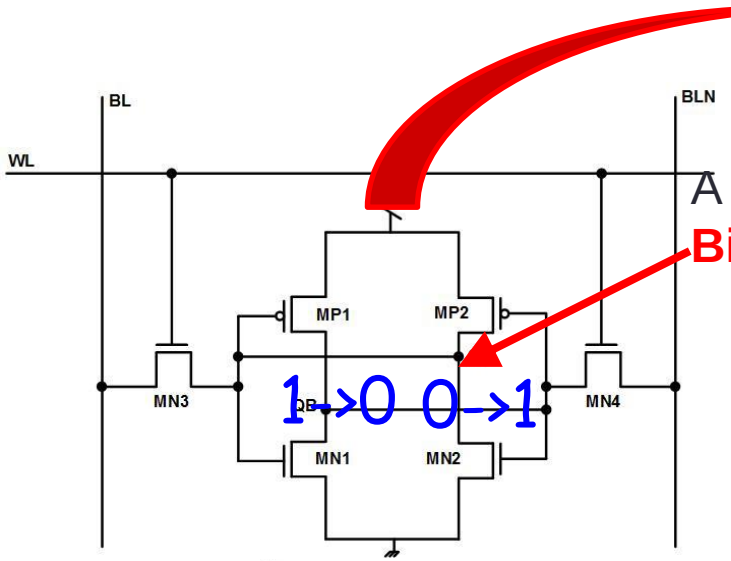
A particle strike

Bit Flip !!!



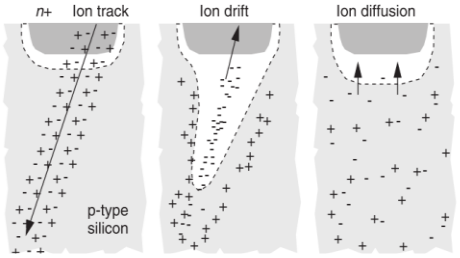


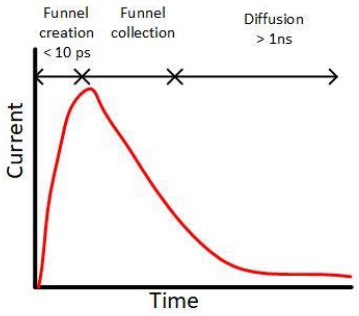
Critical charge simulations

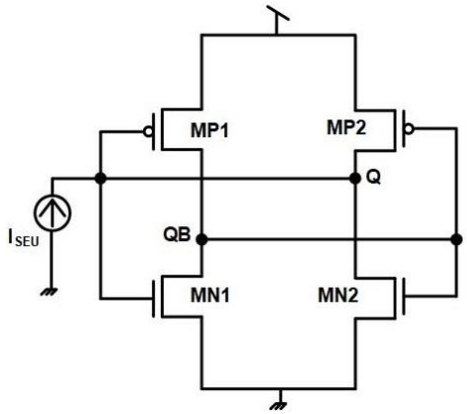


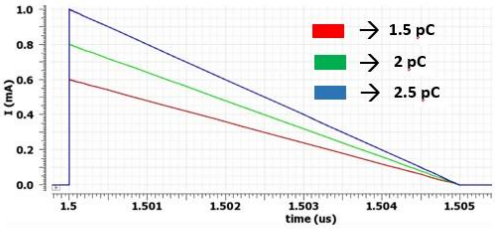
A particle strike

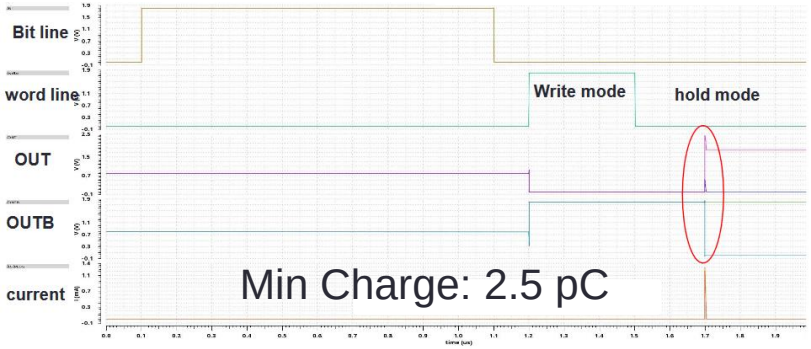
Bit Flip !!!





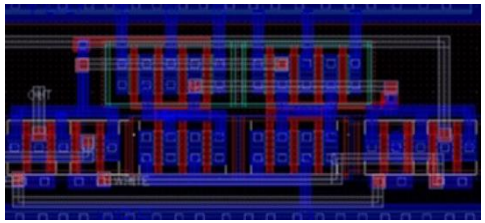






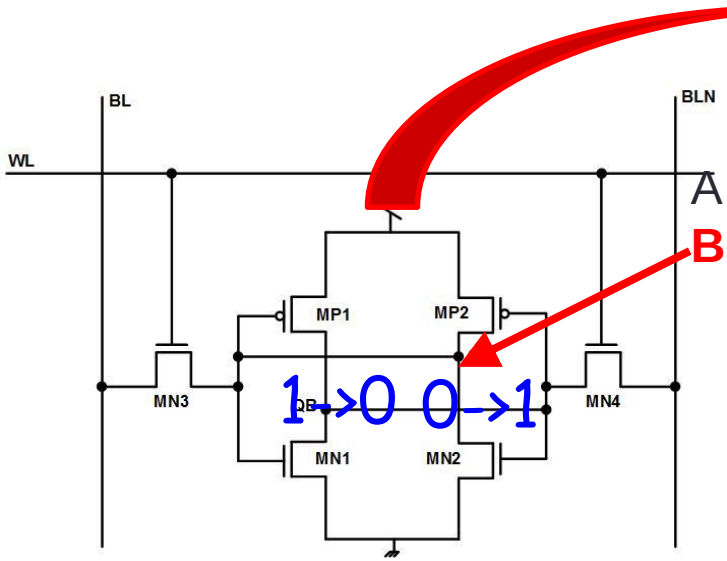
8.5 µm

4 µm



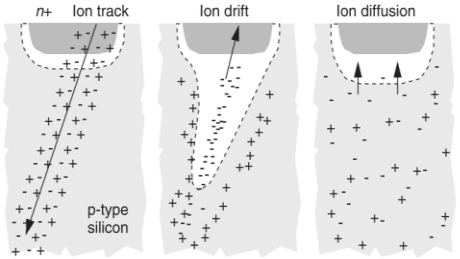
1 bit- dual port SRAM cell in 0.15 µm CMOS.

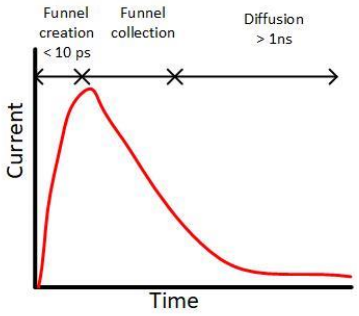
Critical charge simulations

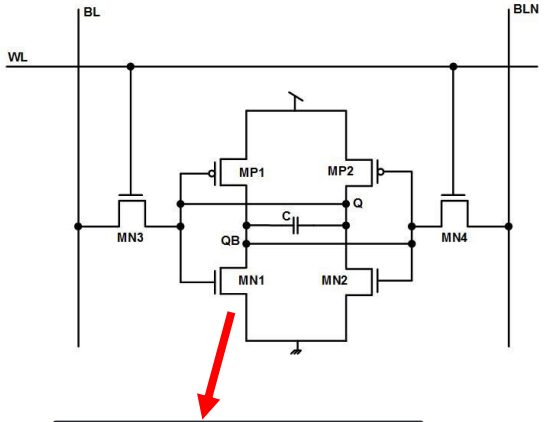


A particle strike

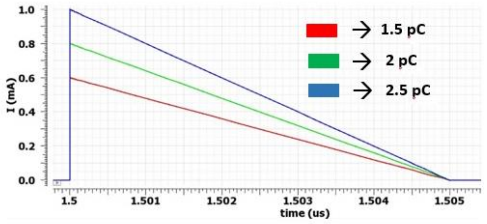
Bit Flip !!!

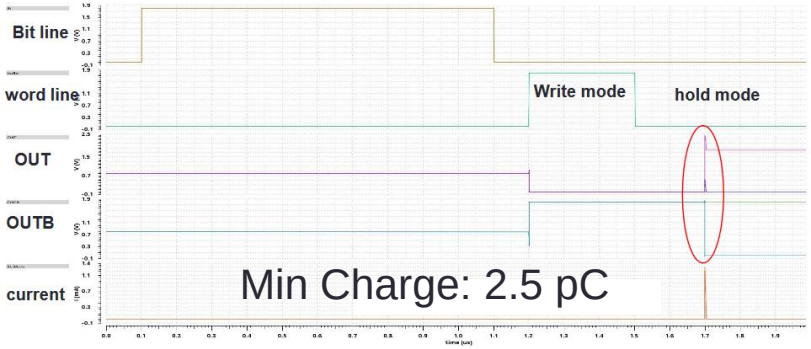






Capacitor: 700 fF





8.5 µm

4 µm

1 bit- dual port SRAM cell in 0.15 µm CMOS.

Area of SEU memories

AMS

Column # (Design)	Area (μm^2)	Distance b/w 2 sensitive nodes (D_2N- µm)
1. TRL W/ DICE latch	400	14
2. TRL W/ standard latch	330	7
3. SPLIT TRL W/ standard latch	450	50
4. SPLIT TRL W/ standard latch	450	50
5. Standard latch	24	-
6. DICE latch	32	3.5

TJ

Column # (Design)	Area (μm^2)	Distance b/w 2 sensitive nodes (D_2N- µm)
1. TRL W/ DICE latch	360	15
2. TRL W/ standard latch	300	8.2
3. SPLIT TRL W/ standard latch	350	65
4. SPLIT TRL W/ DICE latch	370	65
5. Standard latch	27	-
6. DICE latch	47	5.5

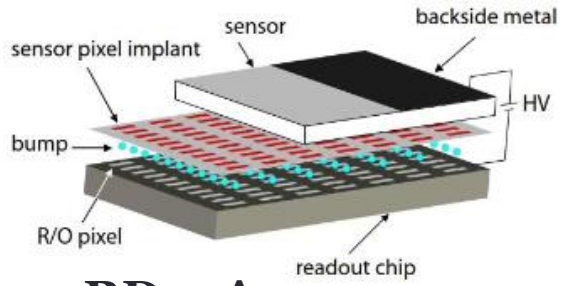
LF

Column # (Design)	Area (μm^2)	Distance b/w 2 sensitive nodes (D_2N- µm)
1. TRL W/ DICE latch	400	11
2. TRL W/ standard latch	400	9
3. SPLIT TRL W/ standard latch	350	65
4. SPLIT TRL W/ DICE latch	370	65
5. Standard latch	27	-
6. DICE latch	32	2.5
7. Enhanced DICE	44	5.5
8. SRAM	40	

Hybrid detectors

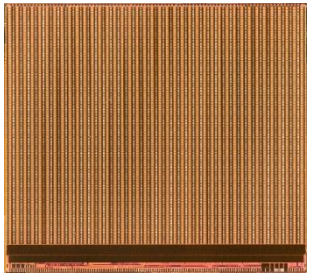
- Hybrid pixels are used as tracking devices in the innermost layers of LHC experiments.
- Sensor and ASIC are independent units.

Availability of smaller CMOS technology nodes!

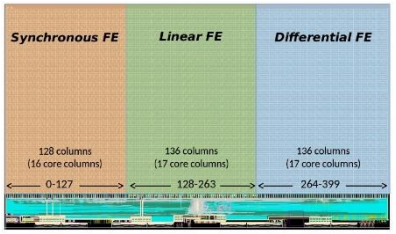


FE-I3

FE-I4

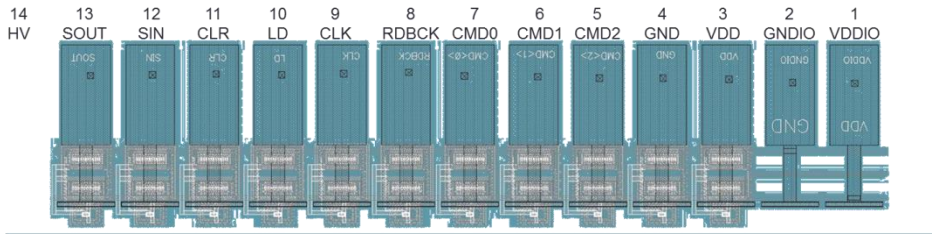


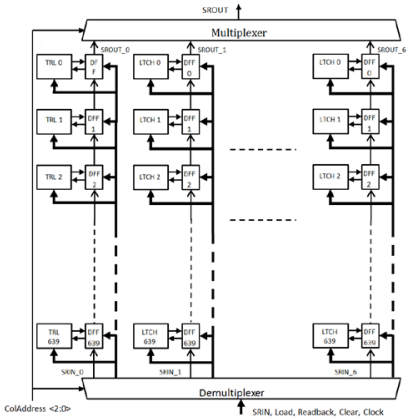
RD53A



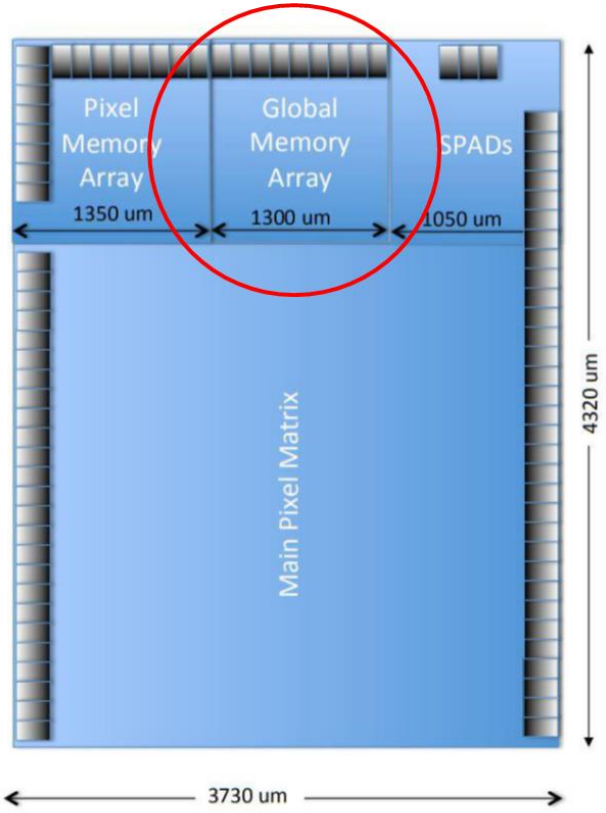
	FE-I3 LHC Run 1	FE-I4 LHC Run 2-3	FE-65 LHC Run 4-5
Tech node	250 nm	130 nm	65 nm
Chip size [mm²]	7.4 × 11	18.8 × 20.2	~20 × 20
# transistors	3.5 M	87 M	1G
Hit rate [Hz/cm²]	100 M	400 M	3 G
Pixel size [µm]	400 x 50	250 x 50	50 x 50
TID [Rad]	100 M	250 M	~0.5-1 G

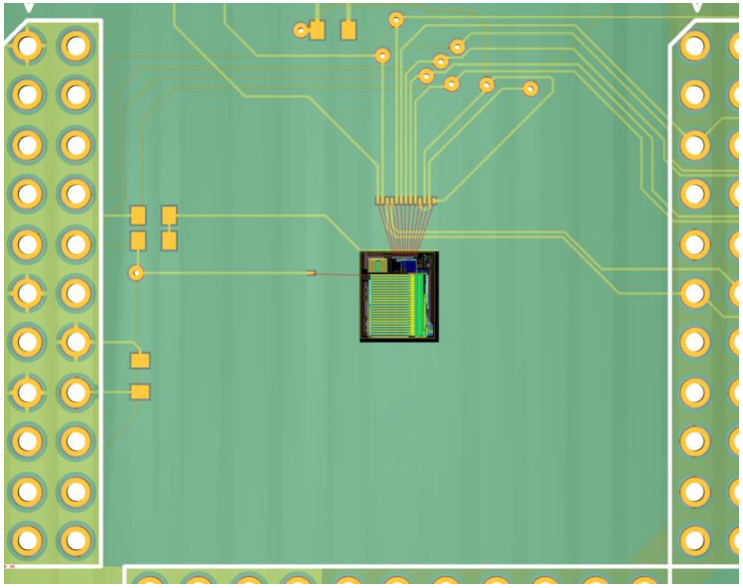
ATLASpix2 and Test Board





LD	IN	Load	Data loading
CK	IN	Clock	
RDBCK	IN	ReadBack	Latches data loading in SR
CLR	IN	Clear	Reset

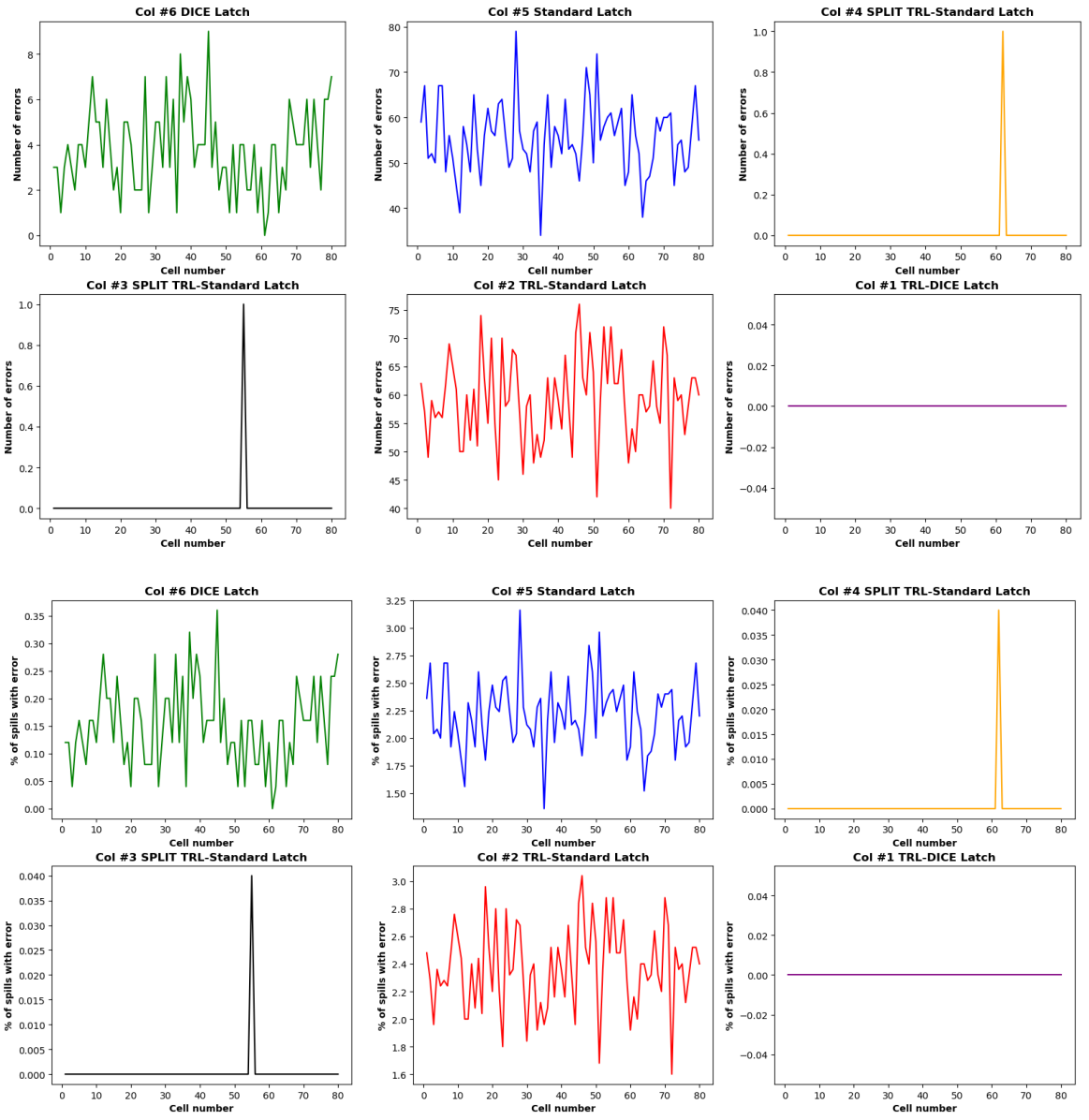




Errors with pattern all “0” for Chip #2

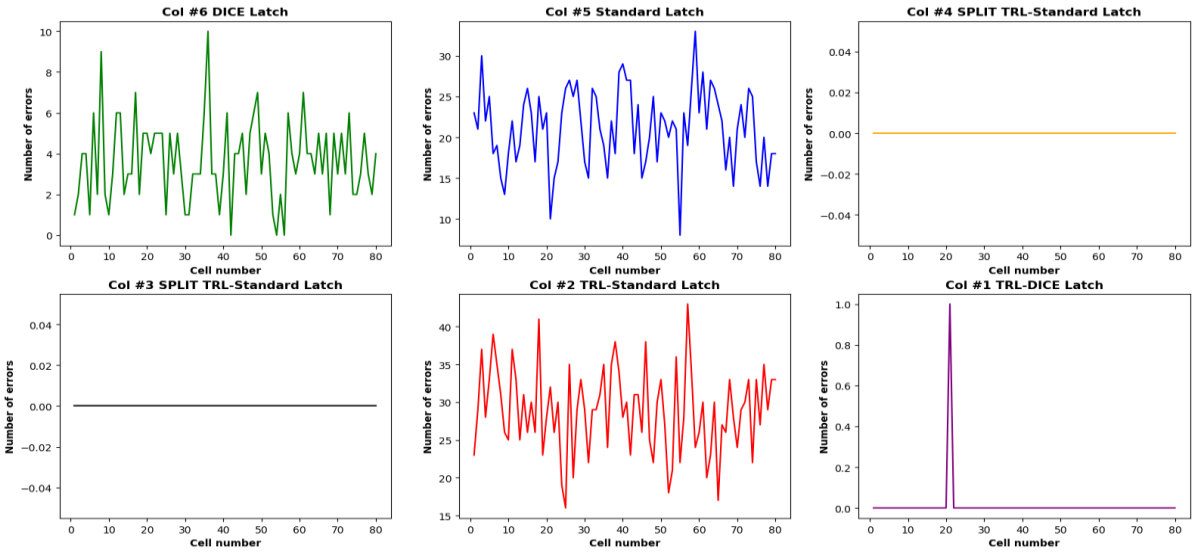
- # errors VS the cell # is shown.
- Col#5 and col# 2 shows similar behaviour.
- # acquisitions : 2500
- # spills : 2500
- Col #1,#3, #4 **are very robust.**

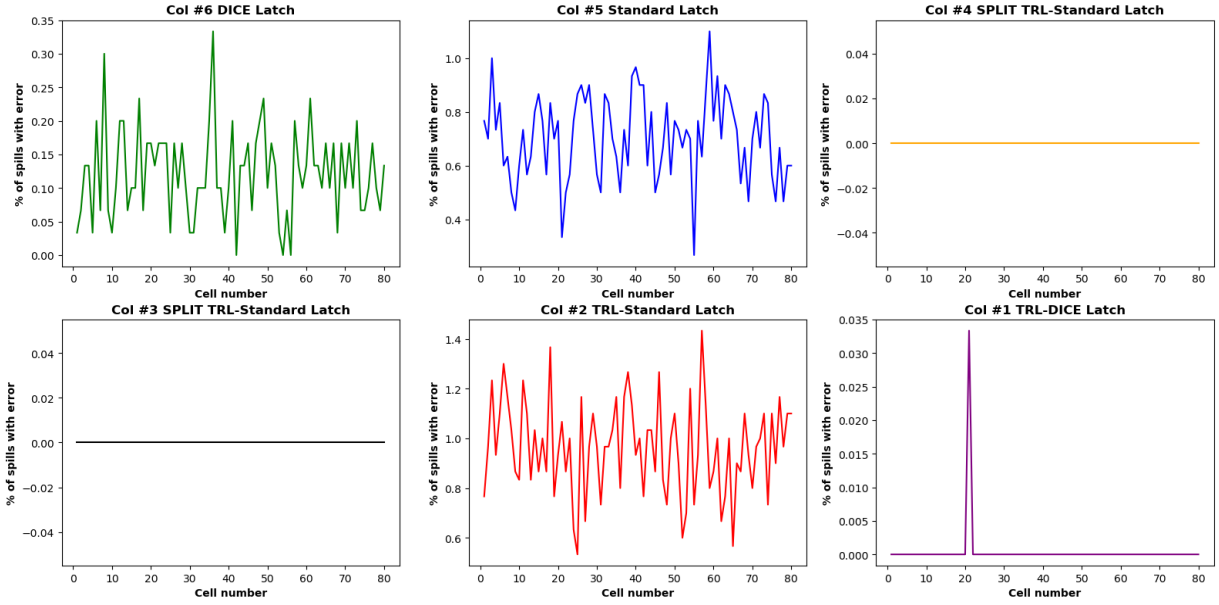
- % spills W/ errors VS cell # is shown.



Errors with pattern all “1” for Chip #2

- # errors VS the cell # is shown.
- Col#5 and col# 2 shows simil behaviour.
- # acquisitions : 3000
- # spills : 3000
- Col #1,#3, #4 **are very robust.**

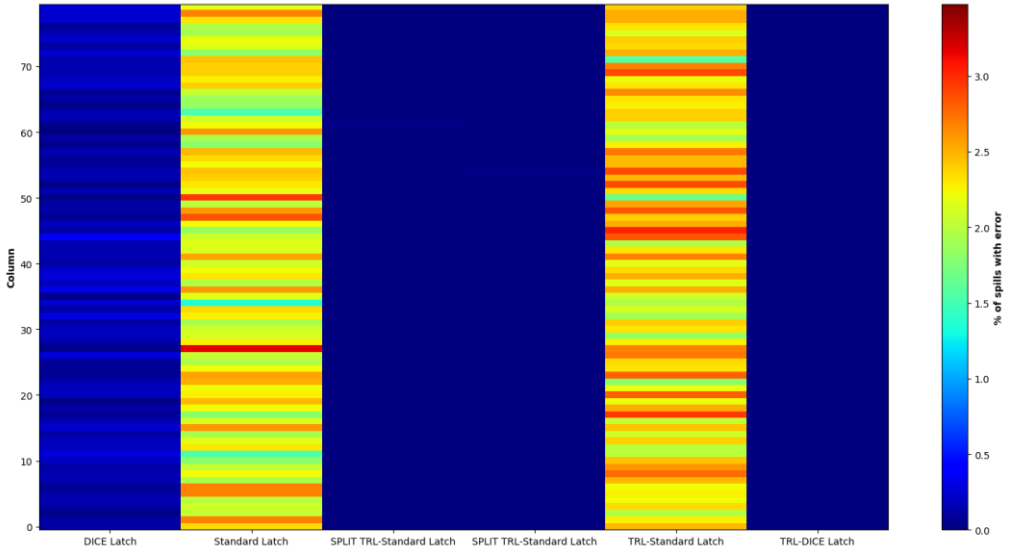




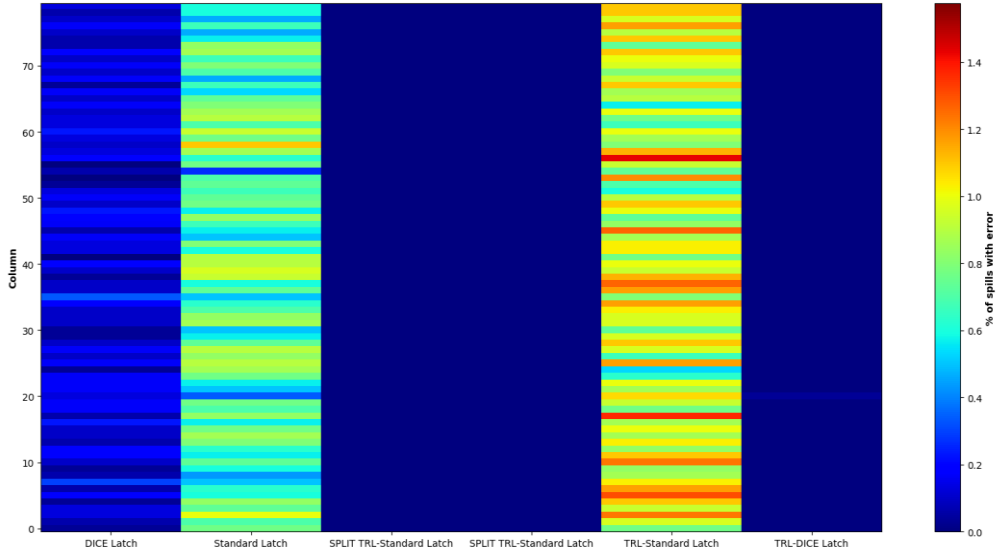
Error mapping for all “0” and all “1” for chip#2

- # errors VS the cell # is shown.
- Col #5 and col # 2 shows similar behaviour.
- # acquisitions > 3000.
- # spills ~ 3000
- Error variation between DICE and standard latch can be seen.
- Col #1, #3, #4 **are very robust.**

All “0” pattern

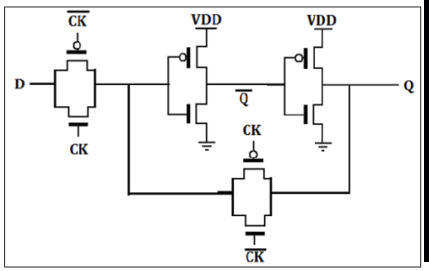


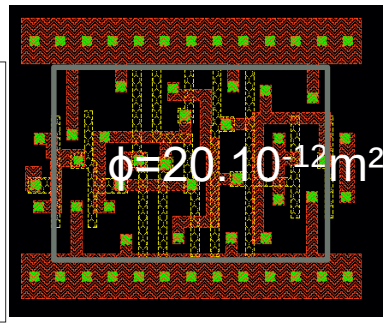
All “1” pattern



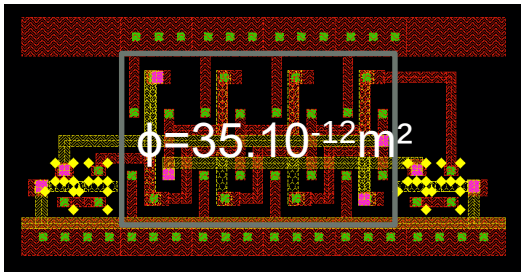
Latch(s) description

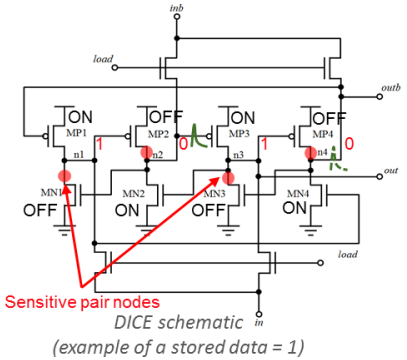
- Standard cell "LHX1_HV" from the CORELIB_HV Lib
- Active area $\phi=20.10^{-12}$ m²





- DICE "Dual Interlocked Storage Cell" cell
- DICE latch structure is based on the conventional cross coupled inverters: Active area
  - The charges deposited by a ionising particle strike one node can't be propagated due to the stability of this architecture.
  - If 2 sensitive nodes (corresponding to the OFF transistors drain area) are affected simultaneously, the immunity is lost and the DICE latch is upset





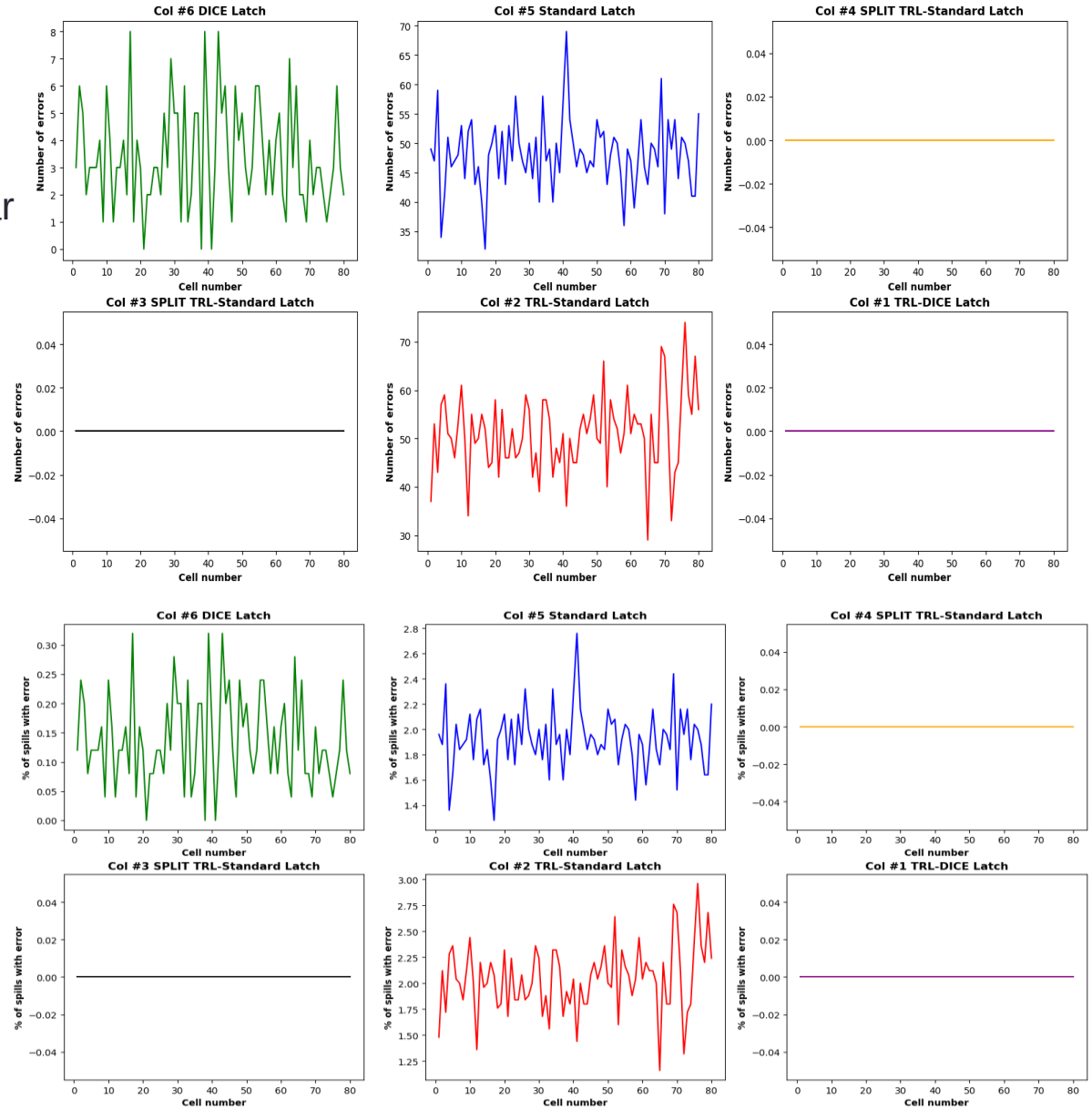
DICE schematic (example of a stored data = 1)

- We expect to gain by 5 the BER robustness (Standard cell "LHX1_HV" is the reference)

Errors with pattern all “0” for Chip #1

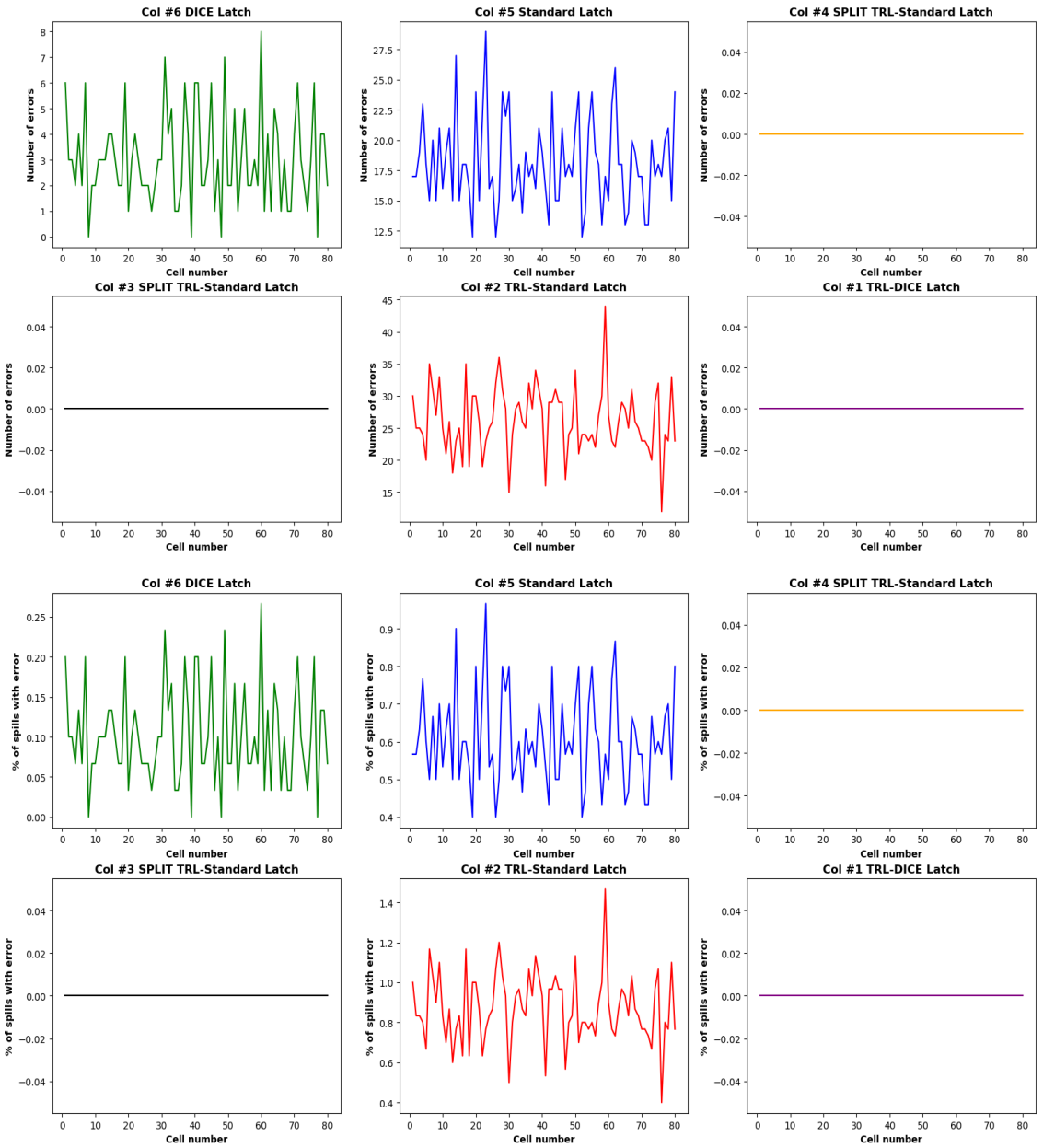
- # errors VS the cell # is shown.
- Col#5 and col# 2 shows similar behaviour.
- # acquisitions : 2500
- # spills : 2500
- Col #1,#3, #4 **are very robust.**

- % spills W/ errors VS cell # is shown.



Errors with pattern all “1” for Chip #1

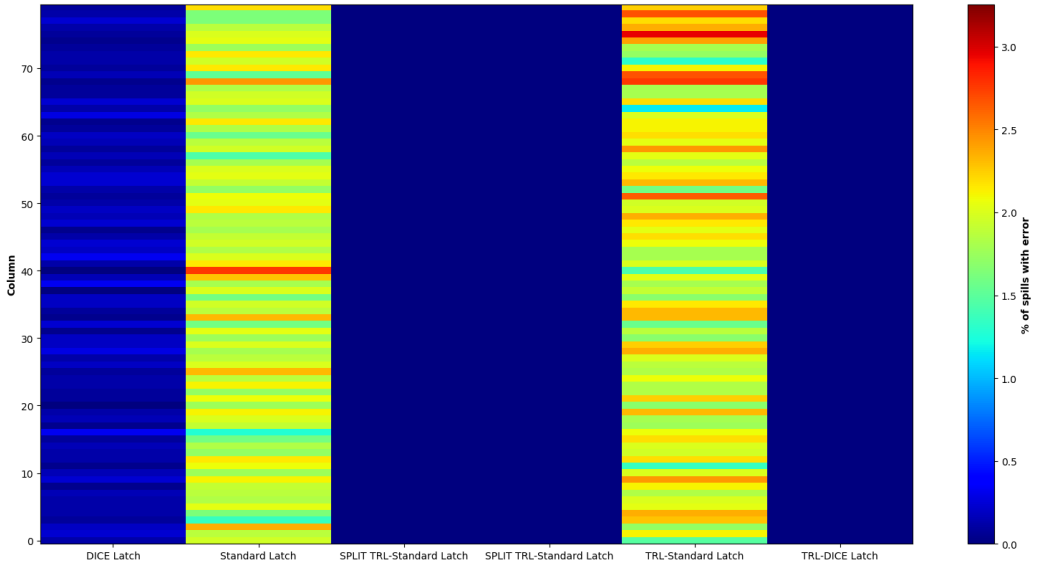
- # errors VS the cell # is shown.
- Col#5 and col# 2 shows similar behaviour.
- # acquisitions : 3000
- # spills : 3000
- Col #1,#3, #4 **are very robust.**



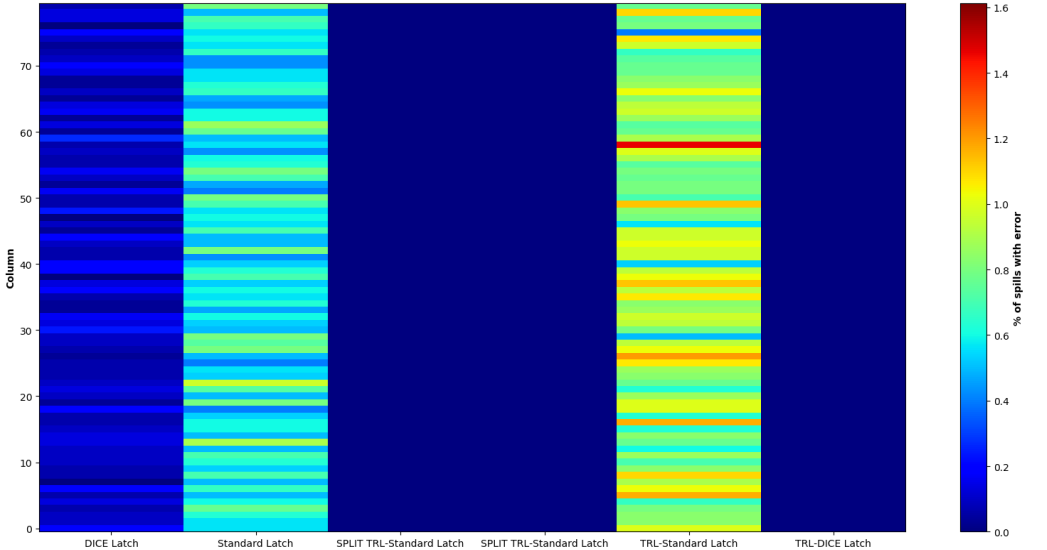
Error mapping for all “0” and all “1”

- # errors VS the cell # is shown.
- Col #5 and col # 2 shows similar behaviour.
- # acquisitions > 3000.
- # spills ~ 3000
- Error variation between DICE and standard latch can be seen.
- Col #1, #3, #4 **are very robust.**

All “0” pattern



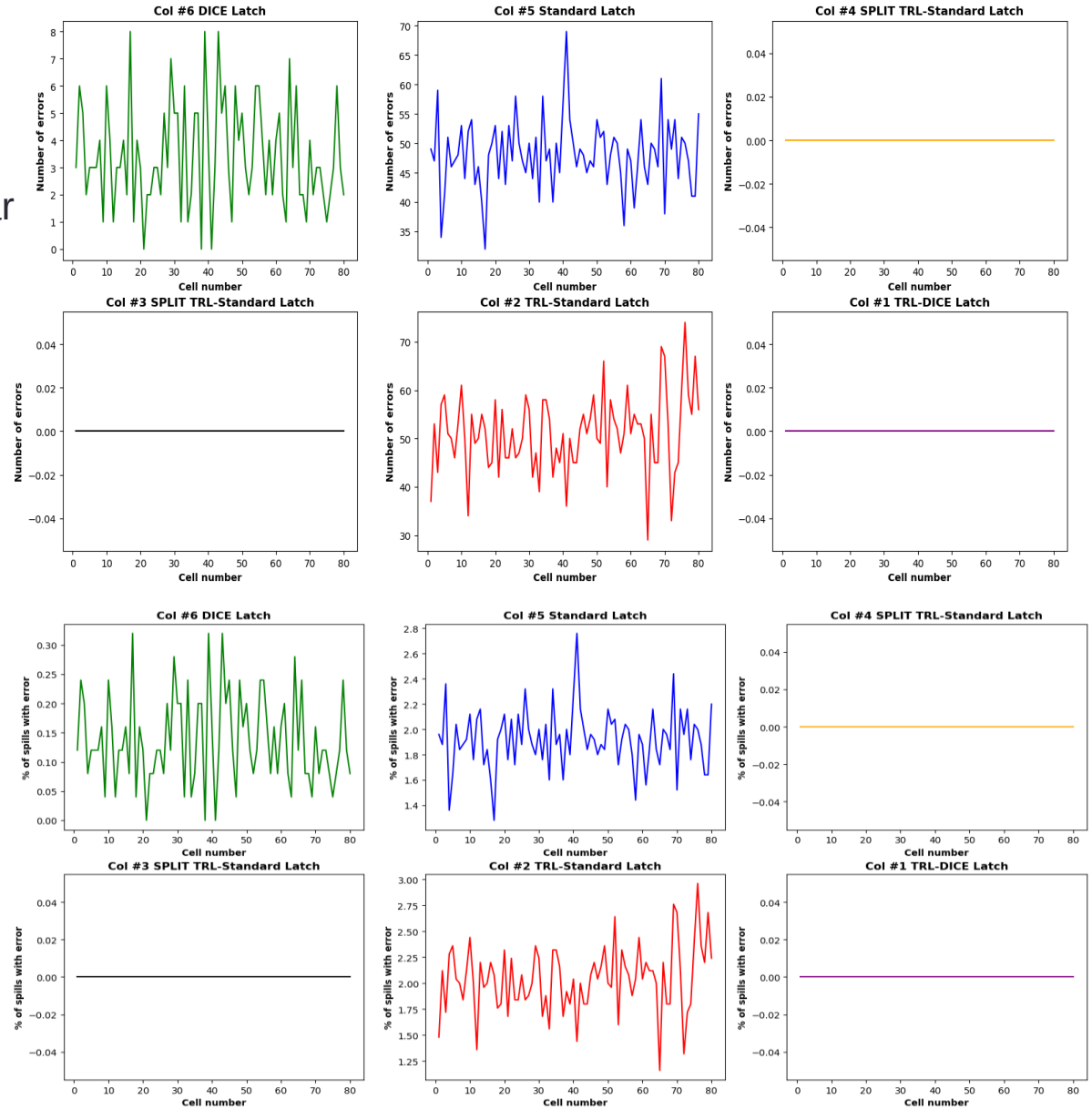
All “1” pattern



Errors with pattern all “0” for Chip #1

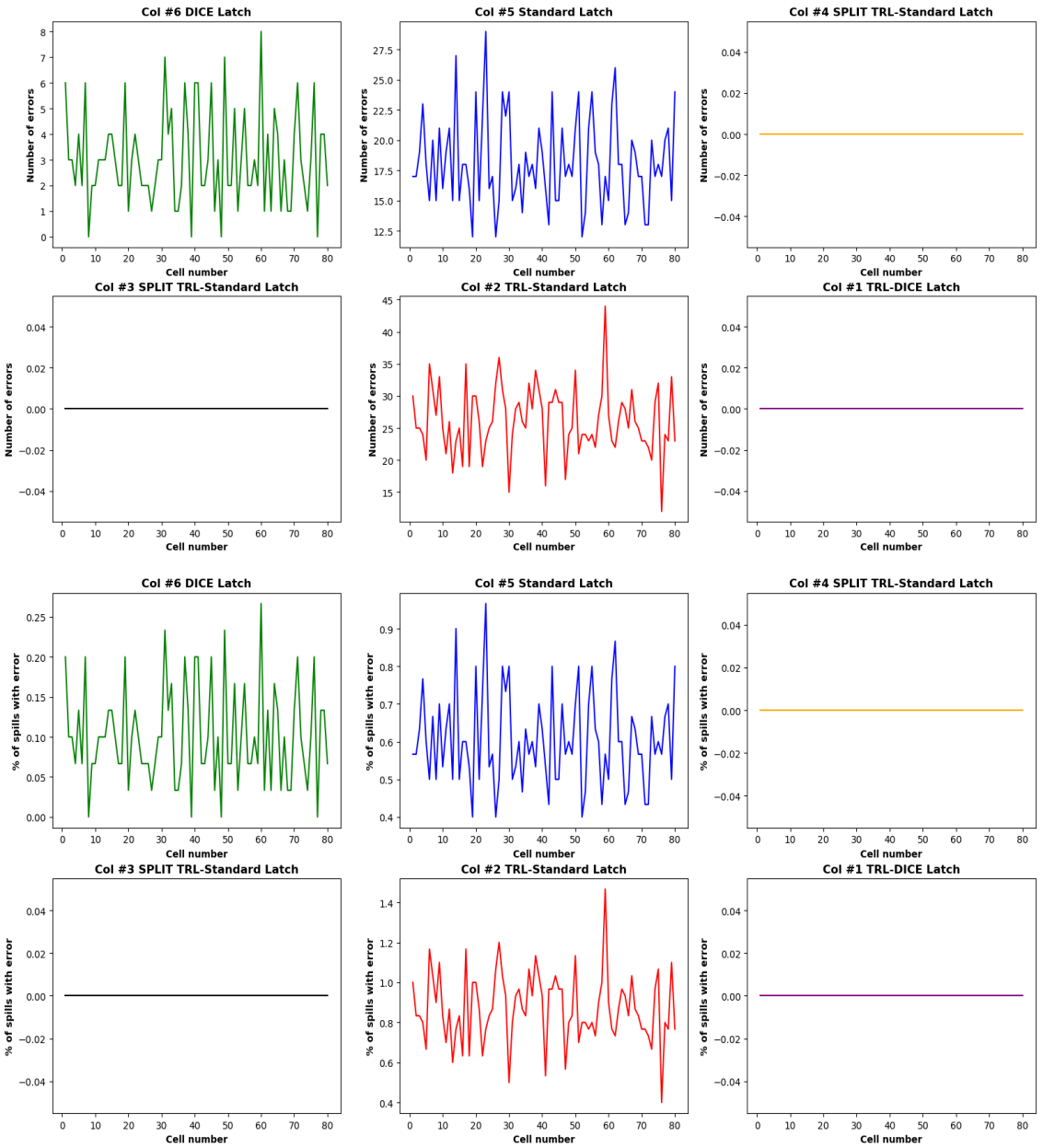
- # errors VS the cell # is shown.
- Col#5 and col# 2 shows similar behaviour.
- # acquisitions : 2500
- # spills : 2500
- Col #1,#3, #4 **are very robust.**

- % spills W/ errors VS cell # is shown.



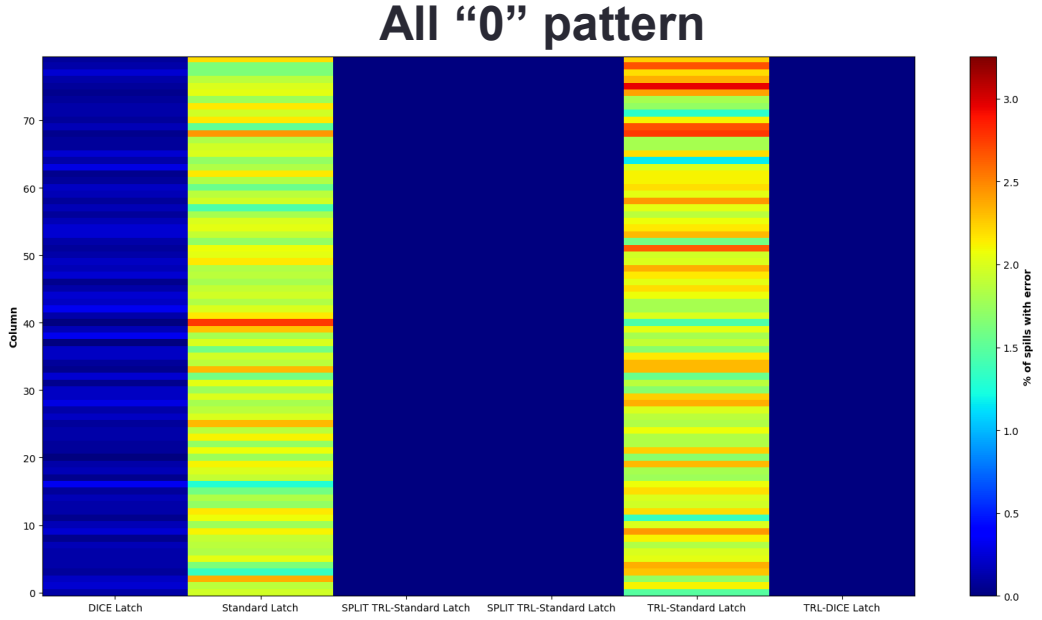
Errors with pattern all “1” for Chip #1

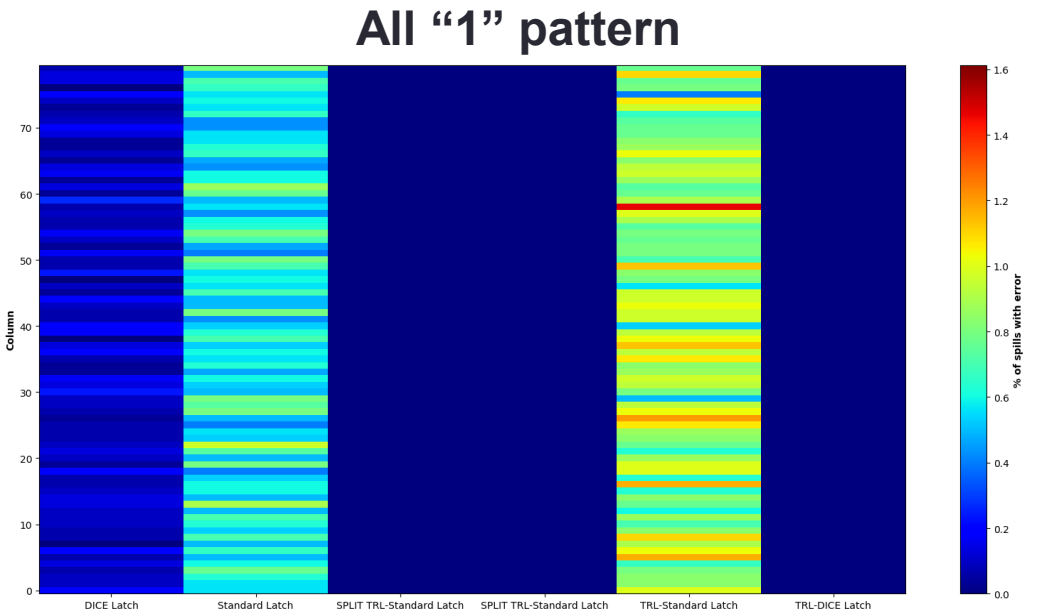
- # errors VS the cell # is shown.
- Col#5 and col# 2 shows similar behaviour.
- # acquisitions : 3000
- # spills : 3000
- Col #1,#3, #4 **are very robust.**



Error mapping for all “0” and all “1”

- # errors VS the cell # is shown.
- Col #5 and col # 2 shows similar behaviour.
- # acquisitions > 3000.
- # spills ~ 3000
- Error variation between DICE and standard latch can be seen.
- Col #1, #3, #4 **are very robust.**

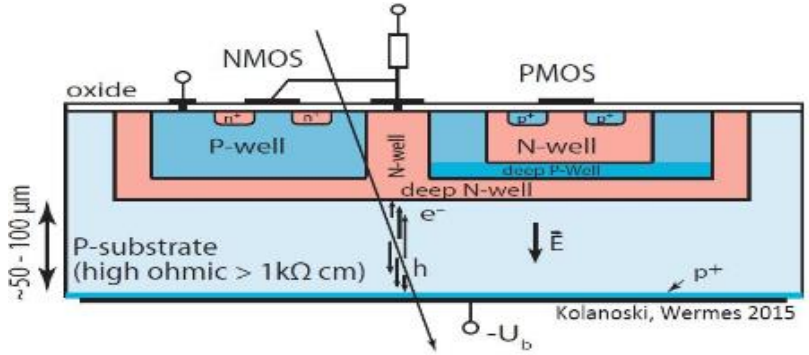




Depleted Monolithic Active Pixel Sensors (DMAPS)

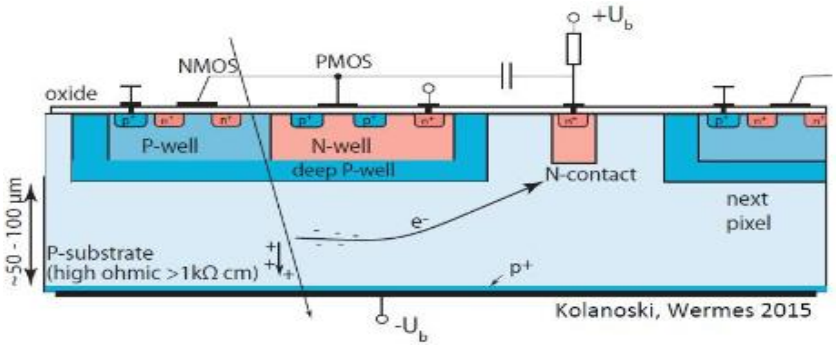
Monolithic sensors with electronics all in one!

2 lines of development followed : (a) large electrode design / (b) small electrode design



- matured over several years
- radiation hardness (TID & NIEL) proven
- rate capability for L4 (and even L3/L2) shown
- timing close to specs

(→ LF / AMS)



- very promising wrt. timing and power
- Vendor already established at CERN
- rate capability for L4 (and even L3/L2) shown
- fast timing due to small C
- radiation hardness -> Sept. 2018

(→ TJ)