904 Integration Operations

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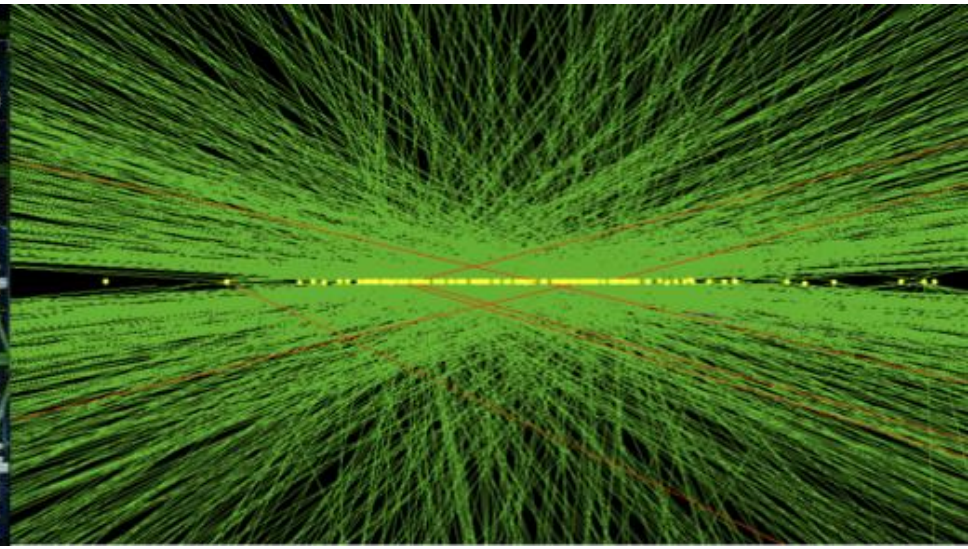
Commissioning and Operations @XXIV GEM Workshop

October 1, 2019



Overview

- GE1/1
  - SW Development
  - GEM-CSC Integration
- GE2/1
  - Electronics Integration
  - Noise Studies
  - Efficiency Studies
- ME0
  - First Prototypes Integration

GE1/1 @904 Integration

- Available Hardware
  - 1 chamber above CSC ME1/1
- Available Electronics
  - The chamber is partially equipped with VFATs (roughly half of slots populates)
  - Separate uTCA backend with the CTP7 dedicated only to GE1/1 developments and tests
- Available Services
  - Gas (pre-mixture bottle, shared with GE2/1)
  - HV
- Software
  - RCMS installed and fully functional, few different configs provided to fulfill the needs
  - 1 fully configured dev PC is reserved for the GE1/1 software development and tests

GE1/1 @904 Integration

- GEM-CSC Trigger Integration
  - OTMB FW provided by Tao Huang
  - Successful communication established
    - Synchronization achieved
    - Resync and BC0 markers added to the GEM trigger stream (A. Peck)
  - Cluster unpacking achieved
  - Rolling S-bit partition scan provided
  - GEM-specific counters implemented in OTMB software
    - Cluster rates per VFAT
    - Synchronization errors
    - Etc
  - GEM hot channel masking implemented in OTMB firmware similarly to internal GEM functionality

GE1/1 @904 Integration

- GEM-CSC Trigger Integration

TMB Info

```
TMB Firmware version (month/day/year - compile type) : (09/05/2019 - c)--->> BAD <<--- should be (8/28/2019 - c)
Firmware Type             : c
Firmware Version Code     : e
Geographic Address        : 06
Firmware Revision Code    : 0006
Power Comparator          : 1f
Time since Hard-Reset     : 00:01:11
```

On-board temperatures and voltages (in decimal) :

```
TMB (FPGA)        =   43 deg C
TMB (PCB)         =   22 deg C
RAT (Heat sink)   =   21 deg C
RAT (PCB)         =   20 deg C
```

Power line	Voltage (V)	Current (A)
TMB 5.0 V	4.93	1.63
TMB 3.3 V	3.29	
MEZ 3.3 V	3.27	2.36
TMB 1.5 V Core	1.498	2.39
TMB 1.5 V TT	1.50	
TMB 1.0 V TT	1.00	
RAT 1.8 V	1.81	0.04

```
Total 3.3V Supply current = 4.76A
```

Andrew etc

Optical input status

```
->CFEB GTX optical input control and monitoring:
   Input enable [DCFEB# 1-7]:          [ 1 1 1 1 1 1 1 ]
   Input reset [DCFEB# 1-7]:           [ 0 0 0 0 0 0 0 ]
   PRBS test enable [DCFEB# 1-7]:      [ 0 0 0 0 0 0 0 ]
   Input ready [DCFEB# 1-7]:           [ 1 1 1 1 1 1 1 ]
   Link good [DCFEB# 1-7]:             [ 1 1 1 1 1 1 1 ]
   Link had errors [DCFEB# 1-7]:       [ 0 0 0 0 0 0 0 ]
   Link unstable [DCFEB# 1-7]:         [ 0 0 0 0 0 0 0 ]
   Link error count [DCFEB# 1-7]:      [ 0 0 0 0 0 0 0 ]

->GEM GTX optical input control and monitoring:
   Input enable [GEMs 0-3]:      [ 1 1 1 1 ]
   Input reset [GEMs 0-3]:       [ 0 0 0 0 ]
   PRBS test enable [GEMs 0-3]:  [ 0 0 0 0 ]
   Input ready [GEMs 0-3]:       [ 1 1 1 1 ]
   Link good [GEMs 0-3]:         [ 1 1 0 0 ]
   Link had errors [GEMs 0-3]:   [ 0 0 1 1 ]
   Link unstable [GEMs 0-3]:     [ 0 0 0 0 ]
   Link error count [GEMs 0-3]:  [ 0 0 0 0 ]
```

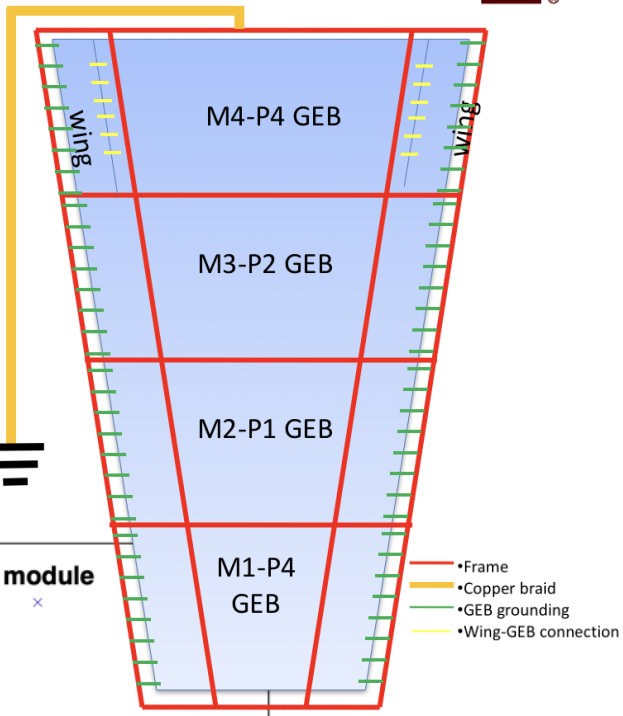
GEM fiber status using only two trigger fibers from GE1/1 test stand

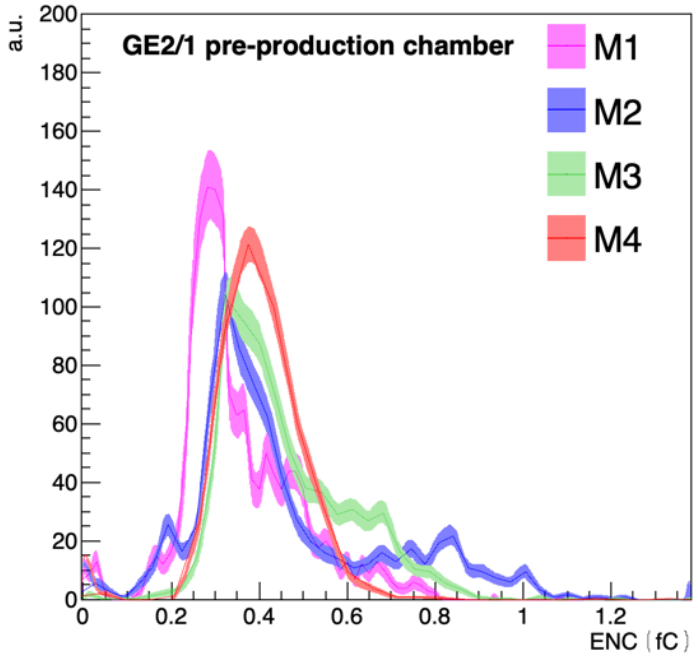
GE2/1 Electronics Integration

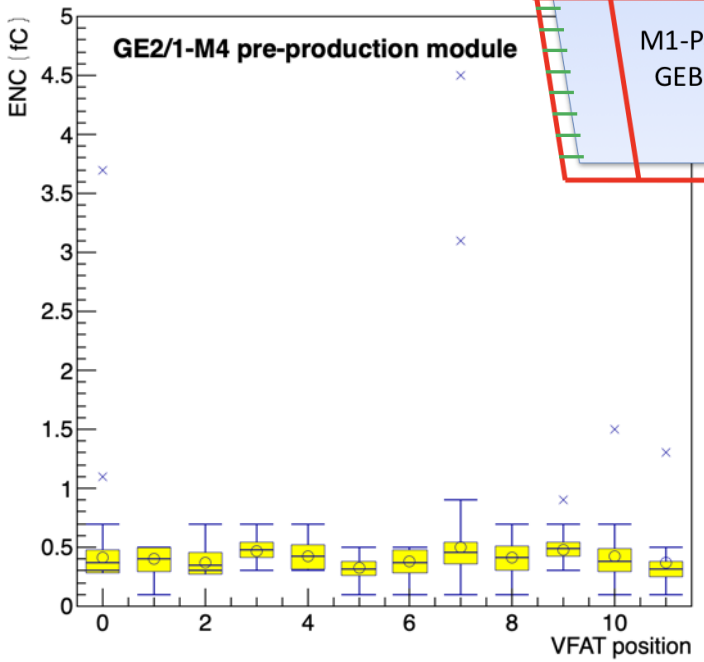
- GE2/1 M1-M5 prototype modules with all mezzanine components except the PlugIn cards are produced and integrated
  - Small modification required from the OptoHybrid and GEB design
  - M6-M8 modules are under review and almost ready to be submitted for a pre-production batch
- VFAT3 packaging pinout is confirmed
  - PlugIn card design should be finished this or next week
- Still need to decide on copper/no-copper ROB
  - Noise studies shows preference towards no-copper ROB

GE2/1 Noise Studies

- Ultimate grounding configuration is identified
  - Requires the use of all pads
  - Not very convenient for production
  - Optimization studies are ongoing





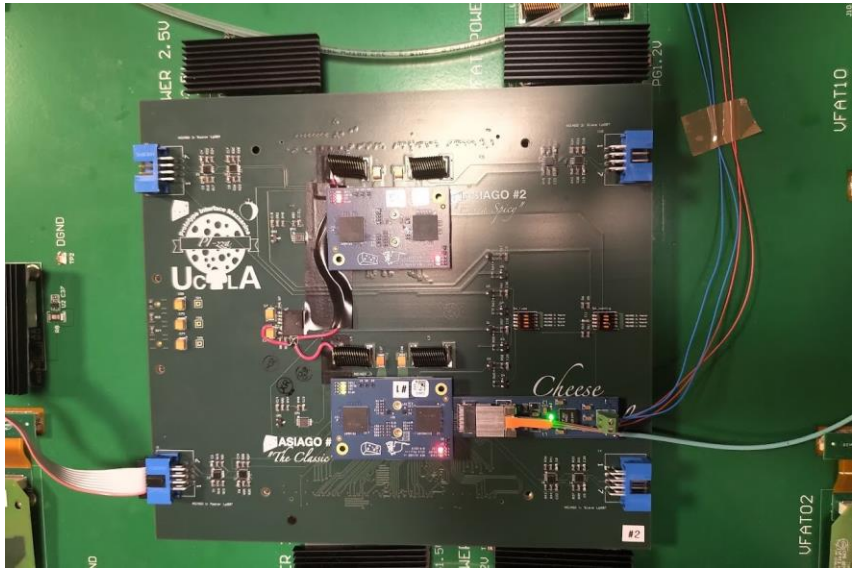


GE2/1 RnD Plans

- HV/Gas integration, efficiency studies
  - October 2019
- Electronics
  - Converge on GND scheme and VFAT input protection
    - Special camp is scheduled on 18-22 Nov. 2019
  - Complete GEB boards M6-M8
    - Timeline: by the end of 2019
  - Minor adjustments and optimization of OptoHybrid and select GEB boards to correct small mechanical issues
  - Validate packaged VFAT3 chips
  - Integrate and test, including proof of principle with ATCA backend
    - ATCA backend ordered, estimated delivery: Nov. 2019
- Cooling
  - Test scheduled on 4-8 Nov. 2019

ME0 Electronics Integration

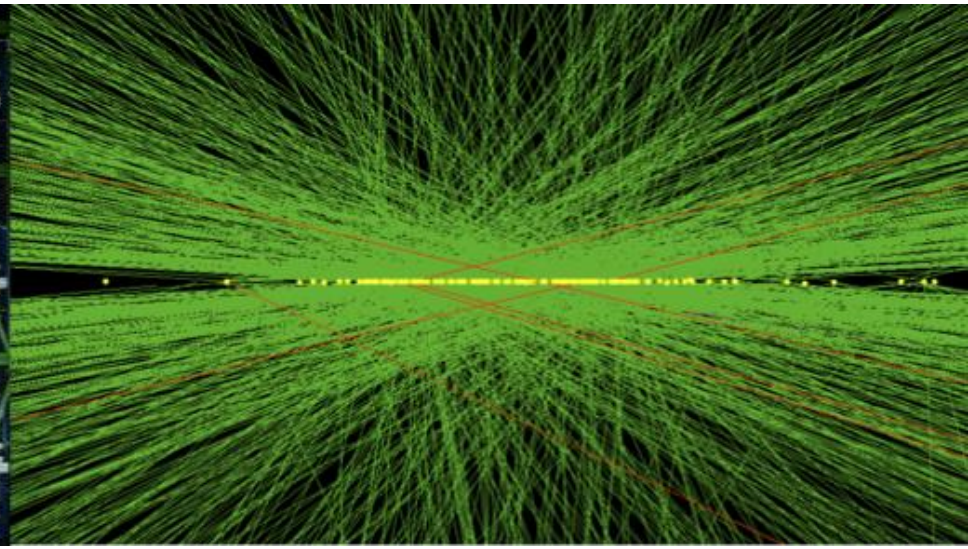
- Electronics Design
  - FPGA-less on-chamber electronics design is ready
    - Prototypes produced
      - ASIAGO (ME0 OptoHybrid board)
      - PIZZA (Special board to place ASIAGO over GE2/1 GEB)
      - Adapter for FireFly transceivers until Vlplus aren't available
    - Integration started using GE2/1 detector
    - Communication between LpGBT and VFAT chips is established!



Summary

- GE2/1 and ME0 RnD and prototyping progressing very fast
- GE2/1 prototype is fully integrated and efficiency studies are ongoing
- ME0 electronics prototypes are delivered to CERN
  - Successful communication between LpGBT and VFAT chips is observed

Backup



Electronics R&D Schedule

- The “waterfall” plot for the updated R&D schedule

#	Title	Expected Start	Expected End
626	**Milestones**	**July 11, 2018**	**Aug 21, 2020**
627	GE2/1 R&D T4: Special ROB-0A prototype manufactured and ready for installation on chamber	July 11, 2018	July 11, 2018
628	GE21 R&D T4: Gen-1 Prototypes Electronics Designs Complete, Ready for Project Level Review	Sep 13, 2018	Sep 13, 2018
629	GE2/1 R&D T4: Make a decision on the copper layer on ROB	Sep 20, 2018	Sep 20, 2018
630	**GE2/1 R&D T5: On-chamber electronics prototypes engineering design complete**	Sep 28, 2018	Sep 28, 2018
631	GE2/1 R&D T4: Special ROB-0B prototype manufactured and ready for installation on chamber	Oct 4, 2018	Oct 4, 2018
632	GE2/1 R&D T4: ROB-1B prototype ready for installation on the demonstrator chamber	Nov 29, 2018	Nov 29, 2018
633	GE2/1 R&D T4: Initial Testing of GEB-1 and Mechanical Integration Validation Complete	Dec 5, 2018	Dec 5, 2018
634	GE2/1 R&D T4: ROB-1A prototype ready for installation on the demonstrator chamber	Dec 7, 2018	Dec 7, 2018
635	GE2/1 R&D T4: Make a decision on the ROB strip layout configuration	Dec 13, 2018	Dec 13, 2018
636	GE21 R&D T4: uTCA-based Backend System for Gen-1/2 GE21 electronics is Ready for Trial Integration with Gen-1 on-Chamber Electronics and Preliminary Measurements of Noise with Stage-1 Demonstrator	Dec 21, 2018	Dec 21, 2018
637	GE21 R&D T4: uTCA-based Backend System for Gen-1/2 GE21 electronics is Ready for Full Integration Testing with Gen-1 on-Chamber Electronics	Jan 4, 2019	Jan 4, 2019
638	GE2/1 R&D T4: All Gen-1 Electronics Boards for one module are ready for mechanical integration assessment with the Stage-1 Demonstrator @ CERN	Feb 19, 2019	Feb 19, 2019
639	**GE2/1 R&D T5: On-Chamber Prototype Electronics Manufacturing and Testing is Complete [At least One Full Module]**	Feb 19, 2019	Feb 19, 2019
640	GE2/1 R&D T4: Pre-Integration and GEB production Test-stand @ PKU Complete	Feb 20, 2019	Feb 20, 2019
641	GE21 R&D T4: ROB-2 Boards Testing @ CERN Completed	Mar 12, 2019	Mar 12, 2019
642	GE2/1 R&D T4: Testing and Assessment of the modules for Stage-2A Demonstrator w/ APV electronics Complete	Mar 27, 2019	Mar 27, 2019
643	GE2/1 R&D T4: Ready for Foil PRR (Modified due to GE21-002 Change Control)	May 3, 2019	May 3, 2019
644	**GE2/1 T5: PRR for Foil Production**	May 22, 2019	May 22, 2019
645	GE2/1 R&D T4: Testing and Assessment of Stage-2A Demonstrator (partial: GEB M1-2) w/ Gen-1 electronics Complete	May 17, 2019	May 17, 2019
646	GE2/1 R&D T4: Ready for EDR	May 17, 2019	May 17, 2019
647	**GE2/1 R&D T5: Performance of the Demonstrator chamber with Prototype Electronics is Validated**	May 22, 2019	May 22, 2019
648	**GE2/1 E5: EDR (CMS TC - External Constraint)**	May 22, 2019	May 22, 2019
649	GE2/1 R&D T4: All Gen-1 On-Chamber Prototype Electronics Manufacturing and Testing is Complete. Ready for full integration with the Stage-2A Demonstrator @ CERN.	May 29, 2019	May 29, 2019
650	GE2/1 R&D T4: Testing and Assessment of Stage-2A Demonstrator w/ Gen-1 electronics Complete	Jun 18, 2019	Jun 18, 2019
651	GE21 R&D T4: uTCA-based Backend System for Gen-2 GE21 electronics is Ready for Full Integration Testing with Gen-2 on-Chamber Electronics	Aug 9, 2019	Aug 9, 2019
652	**GE2/1 R&D E5: RISK MANAGEMENT DECISION POINT: LpGBT or GBTX-based readout selected for ESR**	Aug 30, 2019	Aug 30, 2019
653	GE21 R&D T4: Hardware/firmware ready for integrated testing of the packaged chips	Oct 1, 2019	Oct 1, 2019
654	GE21 R&D T4: Components of the ATCA-based Backend Readout System Hardware Test-Stand are Ready for Integration	Nov 4, 2019	Nov 4, 2019
655	GE21 R&D T4: Gen-2 Electronics Design Complete; Ready for Manufacturing	Oct 31, 2019	Oct 31, 2019
656	GE2/1 R&D T4: Packaged Chips Bonding to PlugInCards-2 starts at a European vendor	Nov 28, 2019	Nov 28, 2019
657	GE21 R&D T4: Packaged VFAT3 performance testing and packaging validation at INFN/Bari completed	Dec 27, 2019	Dec 27, 2019
658	GE2/1 R&D T4: All Gen-2 Electronics Boards are Ready for Installation on Stage-2B Demonstrator and mechanical integration studies @ CERN	Jan 31, 2020	Jan 31, 2020
659	GE2/1 R&D T4: Testing and Assessment of Phase-2B Demonstrator w/ Gen-2 electronics Complete	April 3, 2020	April 3, 2020
660	**GE2/1 R&D T5 (OPTION): Ready for ESR in GBTX-based scenario**	April 3, 2020	April 3, 2020
661	GE21 R&D T4: ATCA-based Backend System for Gen-2/3 GE21 electronics is Ready for Full Integration Testing with Gen-3 on-Chamber Electronics	Mar 23, 2020	Mar 23, 2020
662	GE21 R&D T4: All Gen-3 Electronics Components Designs Complete	Mar 27, 2020	Mar 27, 2020
663	GE21 R&D T4: GEB-3 Boards Arrive to CERN	Jun 19, 2020	Jun 19, 2020
664	GE21 R&D T4: Development of the Software and Firmware infrastructure with fully integrated backend Complete	Jun 26, 2020	Jun 26, 2020
665	GE2/1 R&D T4: All Gen-3 Electronics Boards are Ready for Installation and mechanical integration studies @ CERN	July 17, 2020	July 17, 2020
666	GE2/1 R&D T4: Testing and Assessment of Stage-3 Demonstrator w/ Gen-3 electronics Complete. Ready for ESR	Aug 21, 2020	Aug 21, 2020
667	**GE2/1 R&D T5: On- and Off-Chamber Readout Prototype Electronics Integration and Performance Studies Completed**	Aug 21, 2020	Aug 21, 2020
668	**GE2/1 E5: ESR (CMS TC - External Constraint)**	Aug 21, 2020	Aug 21, 2020