GEM Trigger

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Introduction

- The GEM trigger group is tasked with studying the performance of the L1 muon trigger system with additional GEM hits from GE1/1, GE2/1 and ME0

✓ GEM-CSC integrated local trigger

✓ GEM hits in the standalone L1 muon trigger

✓ ME0 trigger stubs in the standalone L1 muon trigger

✓ Designing algorithms

✓ Developing trigger objects

✓ Integrating the GEM trigger in the L1 muon trigger

GEM Trigger System

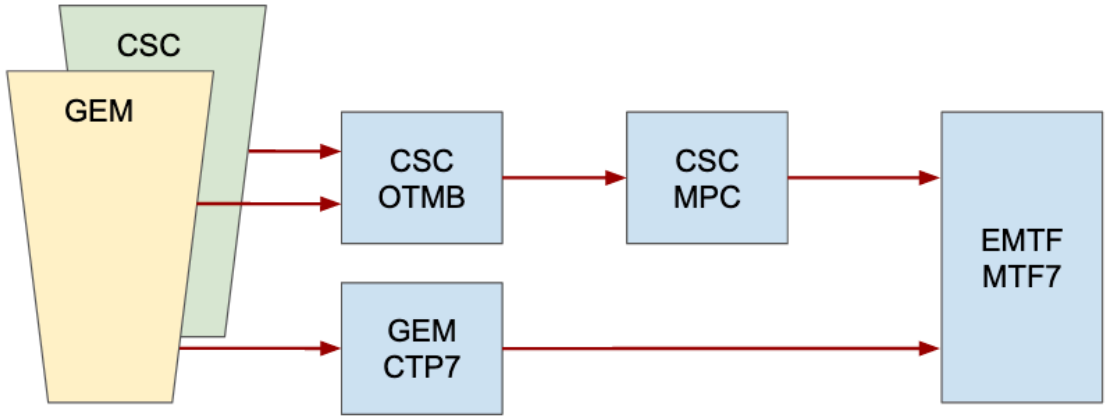
- Motivation for installing GEMs in the forward region and using hits in the L1 muon trigger is clear

- Need to maintain excellent trigger performance in the forward region in high luminosity LHC era (and Run-3)
  - ✓ Soft muons multiple scatter in the endcap system causing a mismeasurement and flattening of the rate curve
    - ◉ Though with improved MVA based techniques (BDT, DNN), there has been great improvement in EMTF for Run-2 and Phase-2
  - ✓ GEMs provide redundancy against large system failures

- Installation of GEM detectors allows for efficient triggering on displaced muons in the endcap
  - ✓ Much of this work has been done for the muon TDR (2017)
  - ✓ Many new physics models suggest LLP with nonnegligible lifetime decaying to pairs of muons
    - ◉ Resulting in displaced muons
  - ✓ L1 Track trigger alone is not efficient to trigger on displaced muons
    - ◉ But combined with muon system is very effective

GEM Trigger System

- GE1/1 and GE2/1 hits are combined with CSC trigger stubs in the CSC trigger system
  - ✓ This can include full CSC trigger information or partial trigger information
- Integrated GEM-CSC stubs are sent from CSC trigger motherboards via muon port card (MPC) to the endcap muon track finder (EMTF)
- At the same time, GE1/1 and GE2/1 hits are sent directly to the EMTF as well via the standalone trigger path
- ME0 hits are not combined with CSC information, nor are sent directly to the EMTF
  - ✓ ME0 hits are preprocessed into ME0 trigger stubs
    - ◉ These ME0 stubs are then sent to the EMTF



GEM Trigger in CMSSW

- Trigger primitive objects:
  - ✓ Key objects in the GEM trigger simulation are defined in DataFormats/GEMDigi
    - ◉ GEM pad (GEMPadDigi)
    - ◉ GEM coincidence pad (GEMCoPadDigi)
    - ◉ GEM pad cluster (GEMPadDigiCluster)
    - ◉ ME0 pad (ME0PadDigi)
    - ◉ ME0 trigger stub (ME0TriggerDigi)
  - ✓ All objects are defined and most have been used in simulation for a few years now
    - ◉ ME0 trigger stub is relatively recent
    - ◉ GEM pad cluster has yet to be used in the trigger simulation

- Trigger primitive producers:
  - ✓ Are maintained by this group
  - ✓ Can be found in CMSSW under
    - ◉ SimMuon/GEMDigitizer
    - ◉ L1Trigger/ME0Trigger
    - ◉ L1Trigger/CSCTriggerPrimitives

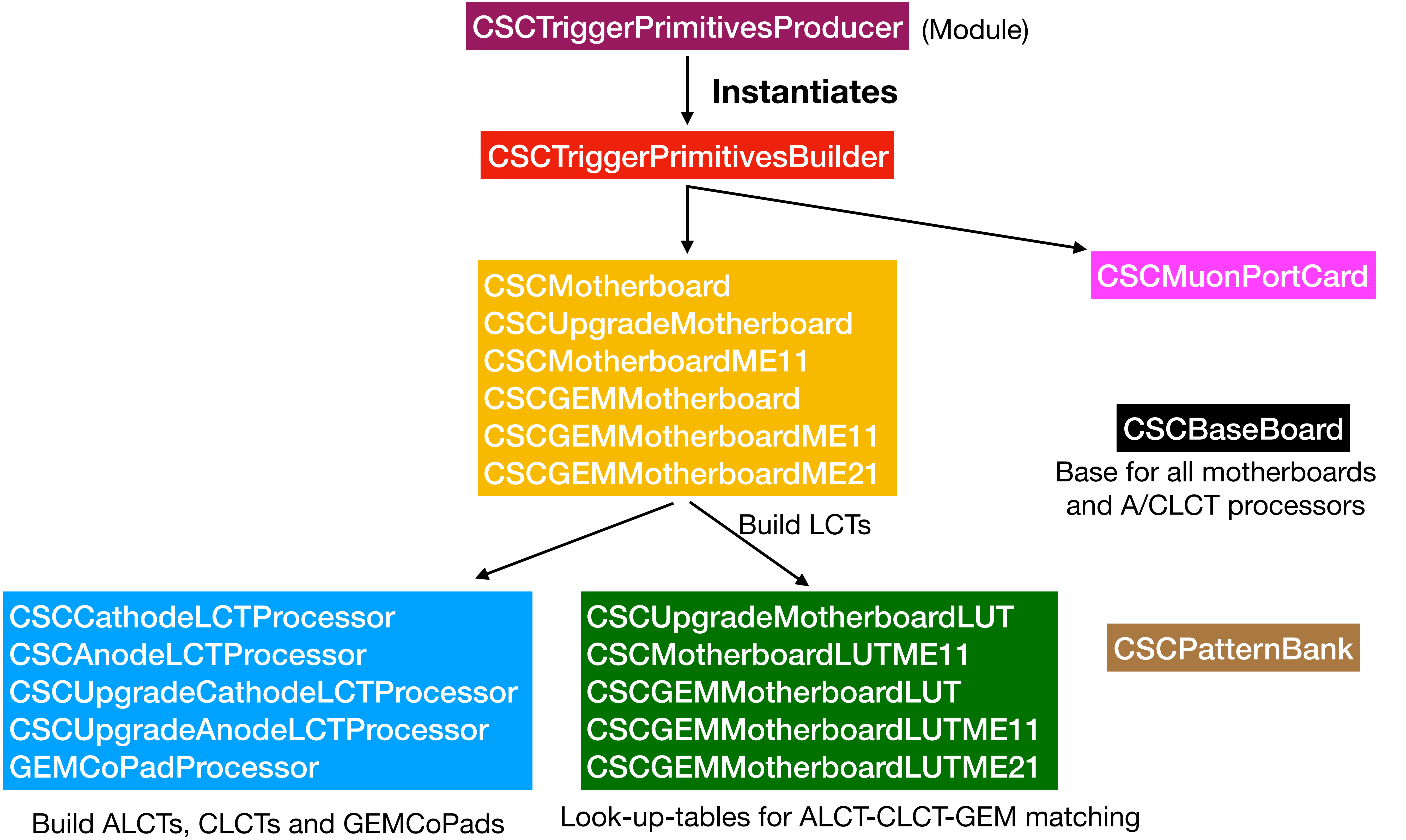
GEM-CSC integrated trigger

- Arguably most of the work is invested in improving the CSC local trigger and GEM-CSC integrated trigger

- GEM-CSC trigger combines GEM trigger pads and coincidence pads with CSC ALCTs and CLCTs by matching in time (BX) and space (by CSC half-strip or wire group)
  - ✓ Matching is done in the CSC ME1/1 and ME2/1 motherboards
  - ✓ Many look-up-tables are used to perform this matching

- With GEM and CSC information, different types of LCTs are produced - depending on what was available:
  - ✓ Original
    - ◉ ALCT-CLCT (default in firmware), CLCT-ALCT, ALCT-only, CLCT-only
  - ✓ With GEMs
    - ◉ ALCT-CLCT-GEM, ALCT-CLCT-2GEM, ALCT-2GEM, CLCT-2GEM

GEM-CSC Trigger in Simulation



CSCTriggerPrimitivesProducer (Module)

Instantiates

CSCTriggerPrimitivesBuilder

CSCMuonPortCard

CSCMotherboard
CSCUpgradeMotherboard
CSCMotherboardME11
CSCGEMMotherboard
CSCGEMMotherboardME11
CSCGEMMotherboardME21

CSCBaseBoard

Base for all motherboards and A/CLCT processors

Build LCTs

CSCCathodeLCTProcessor
CSCAnodeLCTProcessor
CSCUpgradeCathodeLCTProcessor
CSCUpgradeAnodeLCTProcessor
GEMCoPadProcessor

Build ALCTs, CLCTs and GEMCoPads

CSCUpgradeMotherboardLUT
CSCMotherboardLUTME11
CSCGEMMotherboardLUT
CSCGEMMotherboardLUTME11
CSCGEMMotherboardLUTME21

Look-up-tables for ALCT-CLCT-GEM matching

CSCPatternBank

CSCUpgradeMotherboardLUTGenerator

Recent work done

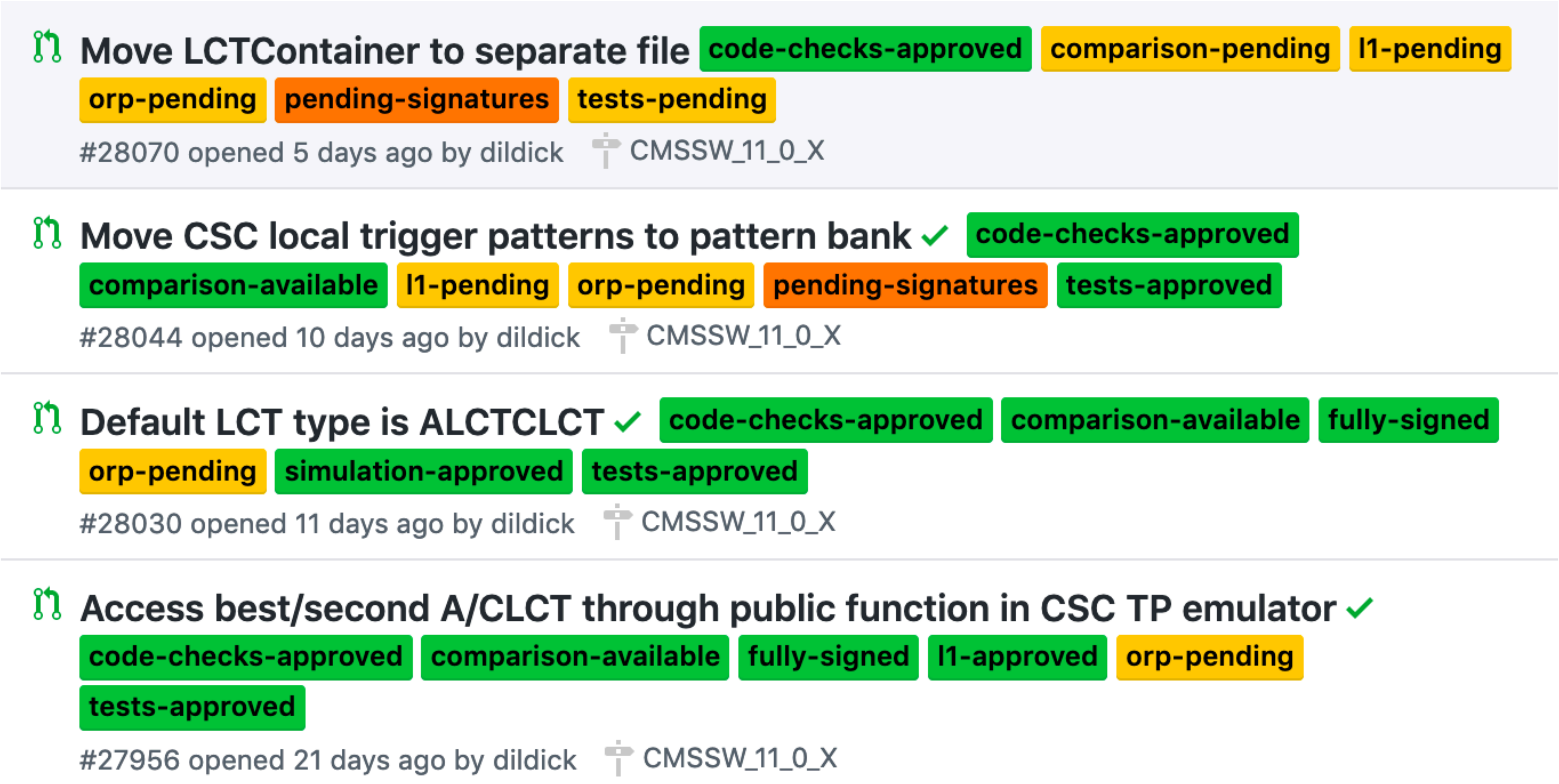
- In view of the L1T Trigger TDR, work has been done to improve the GEM-CSC integrated local trigger
  - ✓ Fix mix-up between the physical and the trigger chamber number in upgrade CSC motherboard.
    - ◉ Without the fix the upgrade motherboards do not produce coincidence pads.
    - ◉ https://github.com/cms-sw/cmssw/pull/27958
  - ✓ Update GE2/1 LUTs for GE2/1-ME2/1
    - ◉ GE2/1 geometry changed some time ago from 12 to 8 eta partitions. The out-of-date LUTs caused significant drops in efficiency for the GE2/1-ME2/1 integrated trigger stubs.
    - ◉ https://github.com/cms-sw/cmssw/pull/27957
  - ✓ Update GEMPadDigi clustering procedure (with Andrew Peck)
    - ◉ Update of the clustering procedure so it matches the implementation in the GEM optohybrid firmware
    - ◉ https://github.com/cms-sw/cmssw/pull/27832

Recent work done

- More work on GE1/1-ME1/1 was recently done (last week)
  - ✓ Fix CLCT-GEM valid flag
  - ✓ Update ME11 LUTs
  - ✓ Add LUT to convert gem roll to CSC wire group
  - ✓ Bugfixes in functions to provide LUTs for ME1/1 and ME2/1
  - ✓ This work has yet to be integrated in official CMSSW
    - ◉ But needs to be provided ASAP to analysis goups studying the performance of the L1 muon endcap trigger system (1.6 < |eta| < 2.4)

- Other recent work that is in the pipeline is shown on next slides

Recent pull requests



Move LCTContainer to separate file code-checks-approved comparison-pending l1-pending orp-pending pending-signatures tests-pending

#28070 opened 5 days ago by dildick CMSSW_11_0_X

Move CSC local trigger patterns to pattern bank ✓ code-checks-approved comparison-available l1-pending orp-pending pending-signatures tests-approved

#28044 opened 10 days ago by dildick CMSSW_11_0_X

Default LCT type is ALCTCLCT ✓ code-checks-approved comparison-available fully-signed orp-pending simulation-approved tests-approved

#28030 opened 11 days ago by dildick CMSSW_11_0_X

Access best/second A/CLCT through public function in CSC TP emulator ✓ code-checks-approved comparison-available fully-signed l1-approved orp-pending tests-approved

#27956 opened 21 days ago by dildick CMSSW_11_0_X

L1T TDR Contribution

- As mentioned by Teruki in his DPG overview slides, I am tasked to deliver text and plots for the endcap muon trigger primitives
    - ✓ https://indico.cern.ch/event/847049/contributions/3565342/attachments/1917344/3172366/190930_GEM_DPG_v3.pdf
    - ✓ GEM-CSC, ME0 part of my work
        - ◉ GEM-CSC trigger performance, ME0 trigger performance
        - ◉ Also cover CSC trigger performance plots
            - Is part of the GEM-CSC trigger studies
    - ✓ Jay Hauser writes description of CSC trigger algorithm

- Text without plots was delivered to L1T TDR ~2 weeks ago
    - ✓ Currently reviewing the text with Texas A&M University collaborators
    - ✓ Plots now need to be made VERY URGENTLY
        - ◉ Need to be finalized by October 15, to be approved in GMM and L1T meeting
        - ◉ Include in TDR by end of October

L1T TDR Contribution: Plots

- CSC stub efficiency in ME1/1 and ME2/1
  - ✓ CSC stub efficiency at PU0
  - ✓ CSC-only efficiency @ PU = 200
  - ✓ GEM-CSC efficiency @ PU = 200
  - ✓ GEM-CSC efficiency @ PU = 200 + ageing
    - ◉ Is definition of ageing scenario available?
- ME0 stub efficiency
  - ✓ PU0
  - ✓ PU200
- Directional resolution (can reuse plot from muon TDR)
  - ✓ CSC-only resolution
  - ✓ CSC-only resolution with SLHC upgrades
  - ✓ CSC-GEM combined resolution
  - ✓ ME0-ME1/1 combined resolution
- Positional resolution (can reuse plot from muon TDR)
  - ✓ GEM
  - ✓ CSC
  - ✓ ME0

L1T TDR Contribution: Plots

- Plots are coming…
  - ✓ …and hopefully in time

- For the positional and directional resolution plots we can largely rely on the muon TDR plots
  - ✓ Those are driven by the resolution of the GEM and CSC readout
    - ◉ Have not changed since 2017

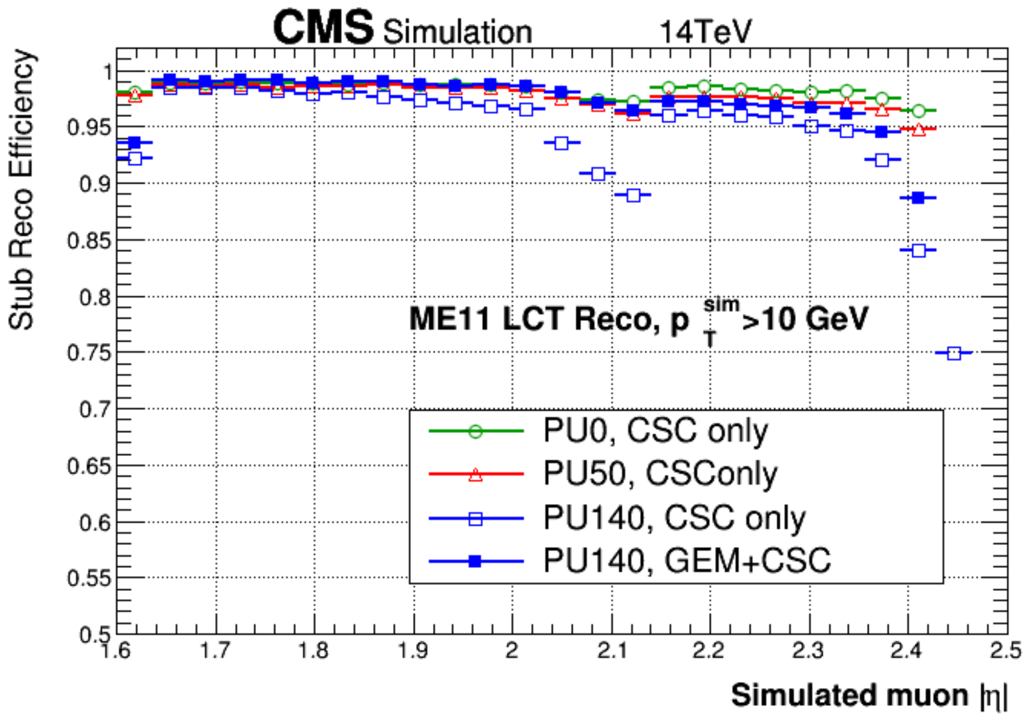
- Efficiency plots are more pressing
  - ✓ Those need to be redone, since the algorithms have been improved during 2018 and 2019
    - ◉ ALCT and CLCT processors were updated. To be understood how capable to handle high pileup
  - ✓ I am processing official L1T Phase-2 samples at PU0 and PU200 with recent bugfixes in the code to assess the trigger efficiency
    - ◉ /Mu_FlatPt2to100-pythia8-gun/PhaseIITDRSpring19DR-PU200_106X_upgrade2023_realistic_v3-v2/GEN-SIM-DIGI-RAW
    - ◉ /Mu_FlatPt2to100-pythia8-gun/PhaseIITDRSpring19DR-NoPU_106X_upgrade2023_realistic_v3-v1/GEN-SIM-DIGI-RAW

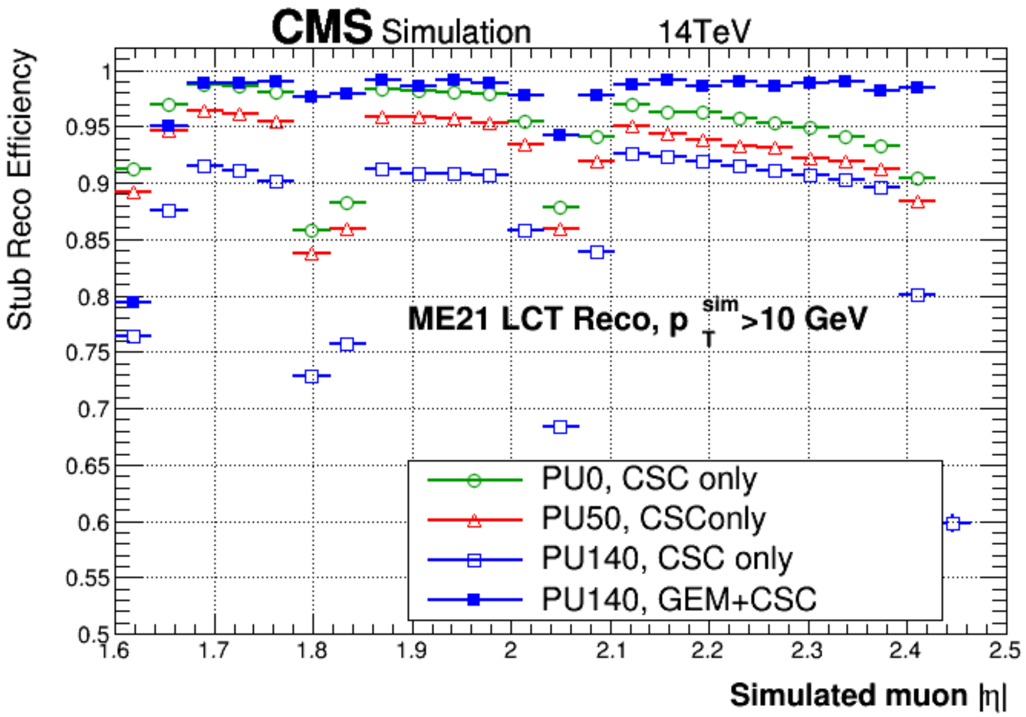
L1T TDR Contribution: Plots

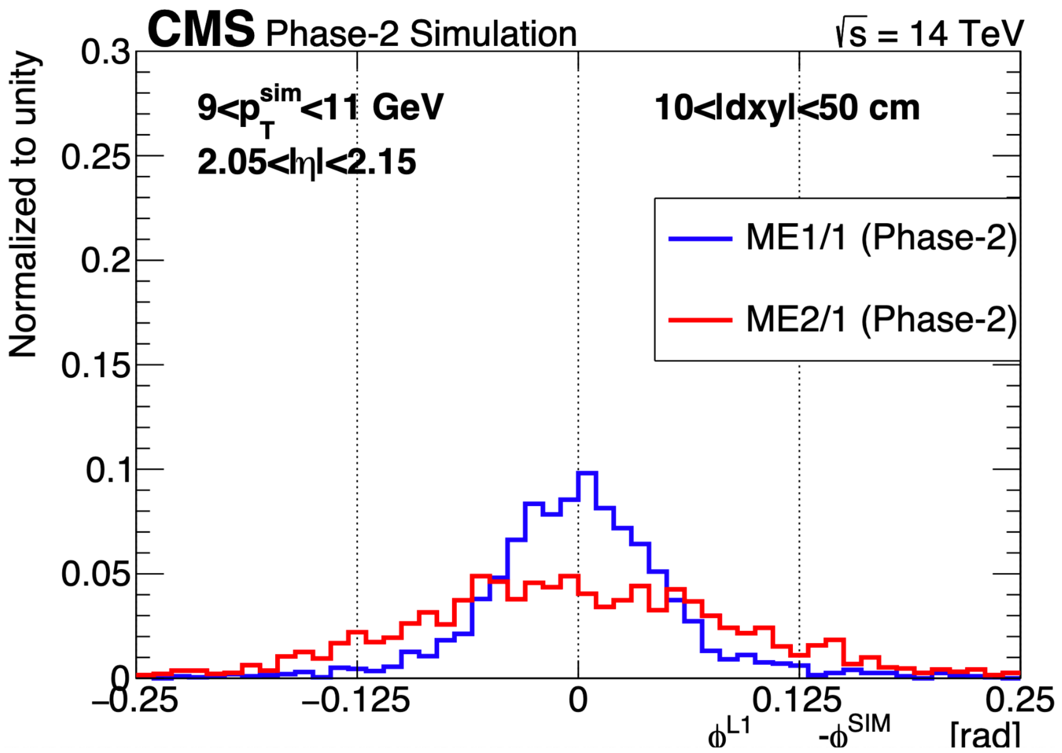
- Preliminary efficiency plots not included in these slides
  - ✓ First look at GEM-CSC combined efficiency in ME1/1 and ME2/1: looks very good
    - ◉ Nearly 100% efficiency, except for near spacers in CSC where the high-voltage drops
    - ◉ Efficiency is substantially higher than what we saw for muon TDR studies
      - Even without GEM hits enabled it is >95%, while it should be less
    - ◉ I'm trying to understand with help from Tao Huang why the efficiency is so high
      - Due to actual improvement in ALCT/CLCT processors or TMBs?
      - Too generous matching of simulated track to trigger stubs?
  - ✓ First batch of plots should be ready by end of this week
    - ◉ Need to be approved by October 15!
- Urgently need help in producing plots!
  - ✓ For muon TDR: Sven & Tao Huang
    - ◉ Tao occupied with firmware studies
  - ✓ For trigger TDR: currently only me

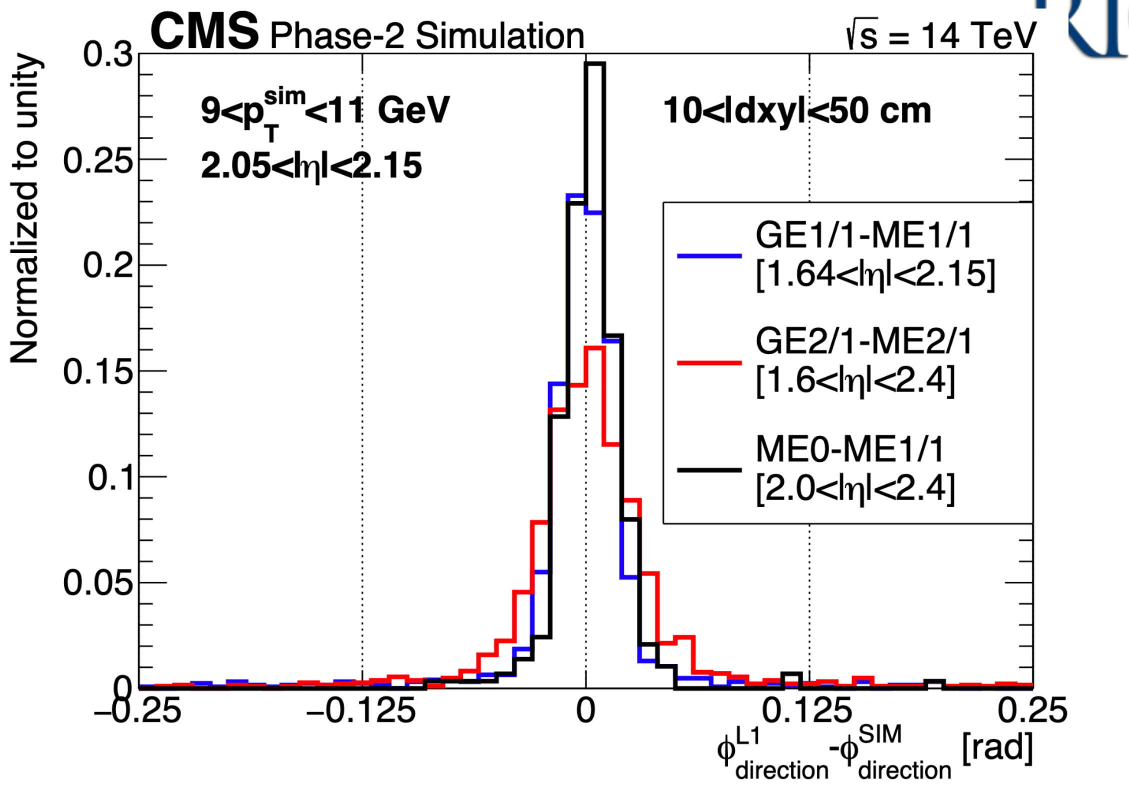
Old Muon TDR plots

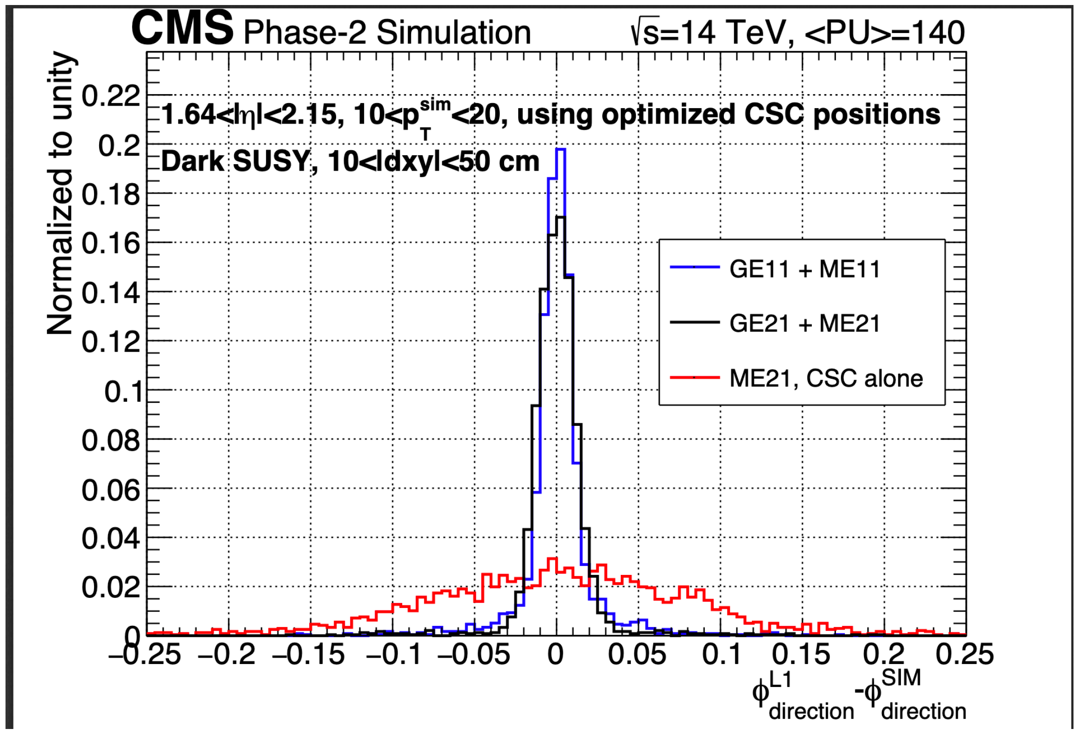
- As a reference, here are two key plots that we prepared for ME1/1 and ME2/1
- Without GEM enabled at high pileup (here PU140)
  - ✓ Efficiency in ME1/1 shows strong drop near ~2.1 (known gap in the CSC readout)
  - ✓ Efficiency in ME2/1 without GEMs around 90% efficient

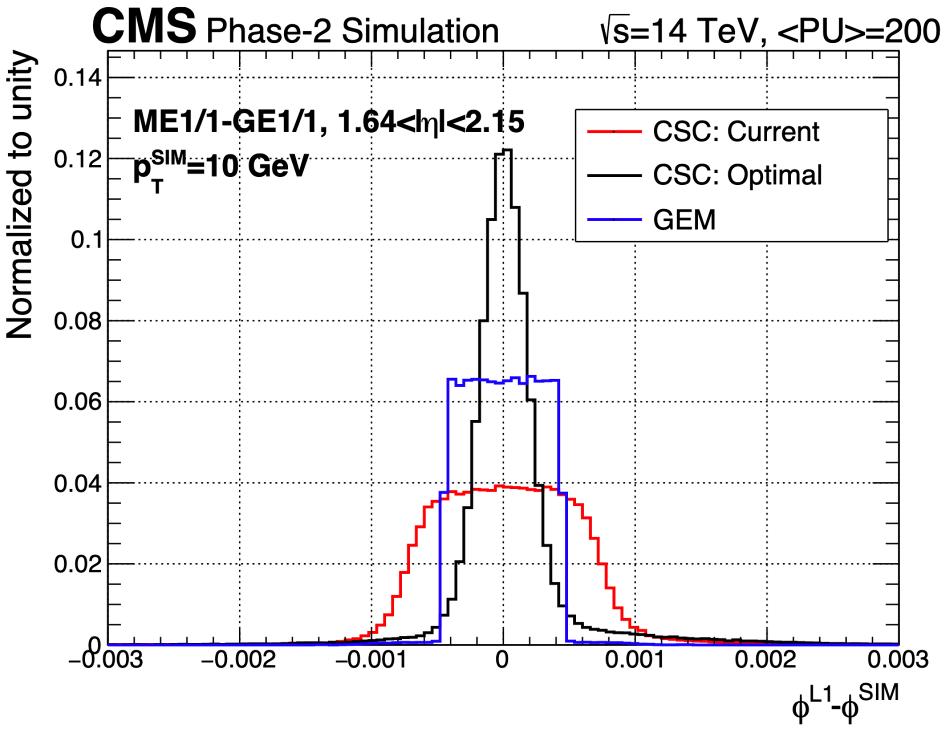





CMS Phase-2 Simulation
√s = 14 TeV
9<p_T^sim<11 GeV
2.05<|η|<2.15
10<|dxy|<50 cm
ME1/1 (Phase-2)
ME2/1 (Phase-2)
Normalized to unity
0.3
0.25
0.2
0.15
0.1
0.05
0
−0.25
−0.125
0
0.125
0.25
φ^L1 -φ^SIM [rad]

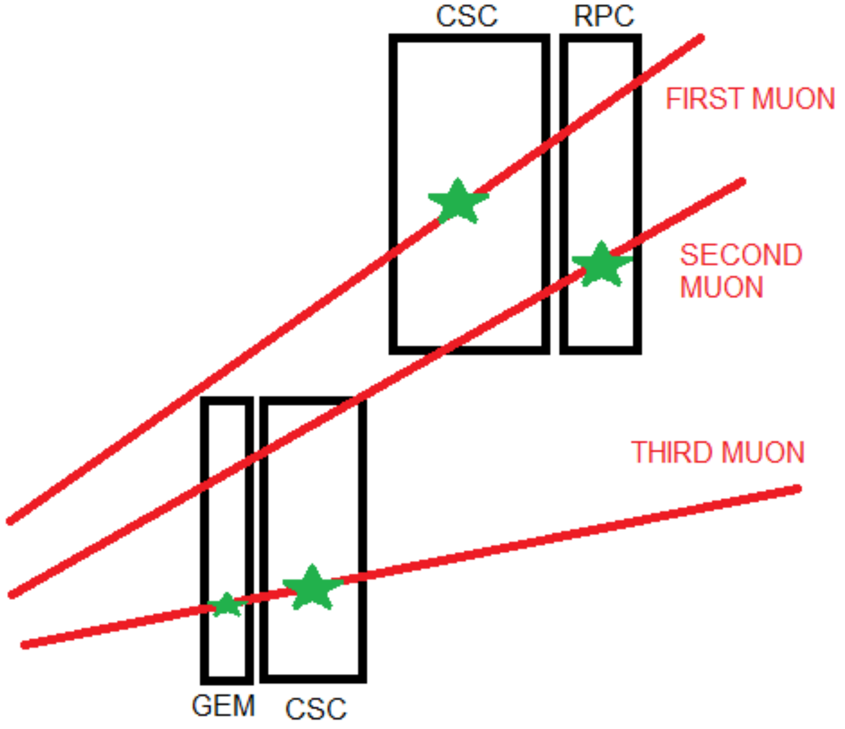

CMS Phase-2 Simulation
√s = 14 TeV
9<p_T^sim<11 GeV
2.05<|η|<2.15
10<|dxy|<50 cm
GE1/1-ME1/1 [1.64<|η|<2.15]
GE2/1-ME2/1 [1.6<|η|<2.4]
ME0-ME1/1 [2.0<|η|<2.4]
Normalized to unity
0.3
0.25
0.2
0.15
0.1
0.05
0
−0.25
−0.125
0
0.125
0.25
φ^L1_direction -φ^SIM_direction [rad]


CMS Phase-2 Simulation
√s=14 TeV, <PU>=140
1.64<|η|<2.15, 10<p_T^sim<20, using optimized CSC positions
Dark SUSY, 10<|dxy|<50 cm
GE11 + ME11
GE21 + ME21
ME21, CSC alone
Normalized to unity
0.22
0.2
0.18
0.16
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
−0.25
−0.2
−0.15
−0.1
−0.05
0
0.05
0.1
0.15
0.2
0.25
φ^L1_direction -φ^SIM_direction


CMS Phase-2 Simulation
√s=14 TeV, <PU>=200
ME1/1-GE1/1, 1.64<|η|<2.15
p_T^SIM=10 GeV
CSC: Current
CSC: Optimal
GEM
Normalized to unity
0.14
0.12
0.1
0.08
0.06
0.04
0.02
0
−0.003
−0.002
−0.001
0
0.001
0.002
0.003
φ^L1-φ^SIM

Tau to 3 Mu trigger

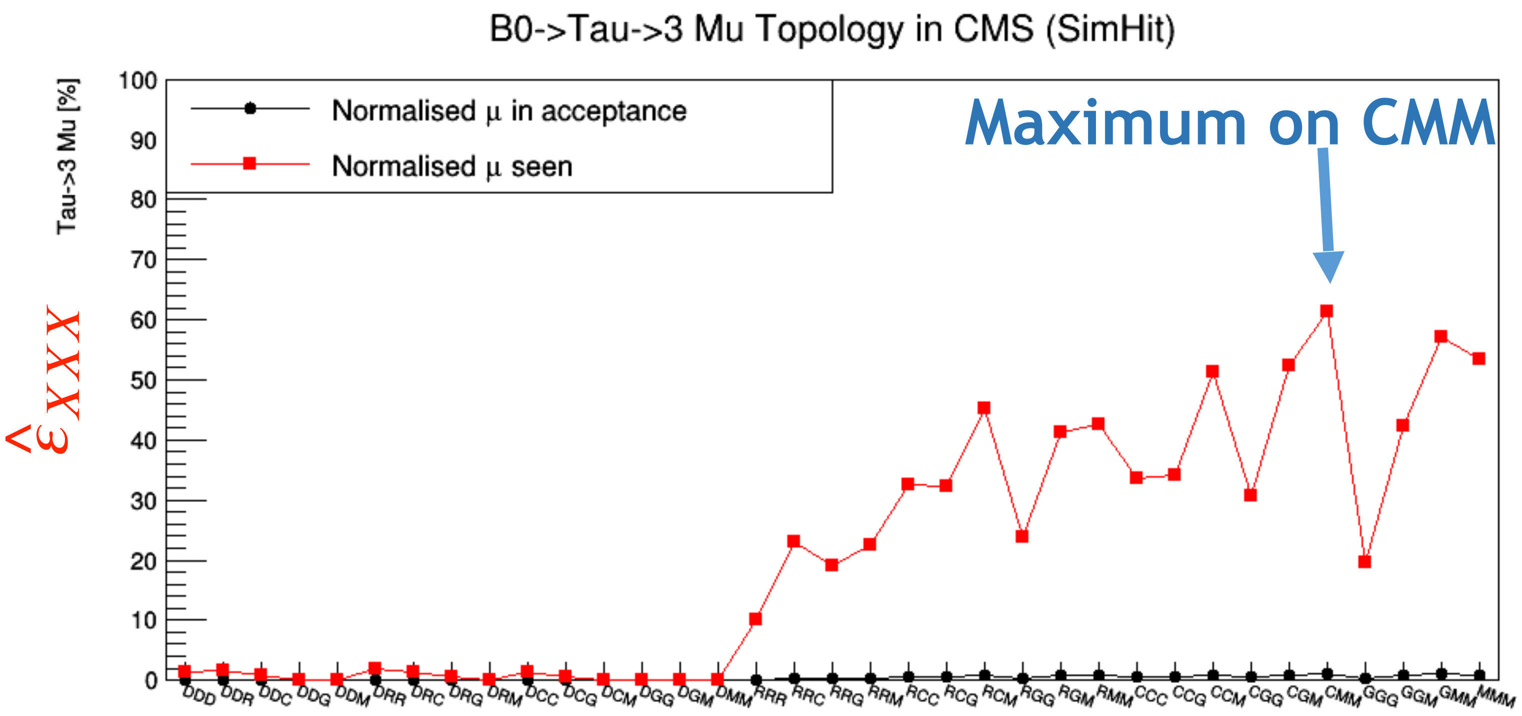
- Trigger with ME0 station
- Design of a multi-stub trigger algorithm for the detection of decays, extending Martina Ressegotti’s study using only the ME0 station
  - Efficiency: evaluated from dataset only without PU with a "forced" decay per event
  - Trigger rate: evaluated from MinimumBias dataset (/DoubleNuE1Eta14_31/PhaseIITDRSpring17DR-PU200_NoSmear_91X_upgrade2023_realistic_v3-v2/GEN-SIM-RECO)
- A dataset containing decays is prepared from the decay of B0 and Ds particles - 83% of events with tau leptons observed in CMS are from B0 and Ds meson decays
- Particles are generated in <3.0
  - Only one B0 or Ds meson per event is forced to decay in tau lepton.
  - Of multiple tau leptons in each event, only one tau lepton is forced to decay into 3 muons.
  - Then: at least 2 muons in |eta| < 3 are required.



Tau to 3 Mu trigger

- ❑ SimHit in the muon detectors have been matched to the GenParticle of each of 3 muons coming from the tau lepton decay.
  - ▪ Definition of XXX Boolean variables where each X can be:
    N = NONE, D = DT, R = RPC, C = CSC, G = GEM, M = ME0
  - ▪ = Number of events where each of 3 muons is in CMS fiducial volume and produce SimHits

- ❑ **Example with a muon seen by more than one detector**: Muon1 produces SimHits only in CSC, Muon 2 only in RPC, Muon 3 in CSC and GEM. This event will count 1 for variable RCC and 1 for variable RCG.
- ❑ Preliminary finding: Large contributions from XXX = CMM along with from CSC, GEM and ME0
- ❑ Plan to study the trigger with GE1/1 and ME1/1 (GEM and CSC station closest to Interaction Point)



Summary

- Lot of work has recently been done on the GEM-CSC trigger simulation to improve the performance

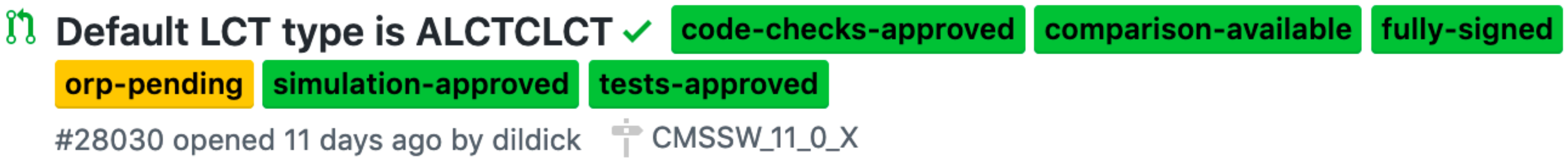
- Many improvements included in CMSSW
  - ✓ Many more in the pipeline

- Performance plots (efficiency, resolution) now need to be made ASAP for the Trigger TDR
  - ✓ Urgently need help to work on set of plots!

- Preliminary studies on multi-stub ME0 trigger are interesting, but need to be fleshed out more before any conclusions can be made

Backup Slides

PR28030



Default LCT type is ALCTCLCT ✓ code-checks-approved comparison-available fully-signed orp-pending simulation-approved tests-approved

#28030 opened 11 days ago by dildick CMSSW_11_0_X

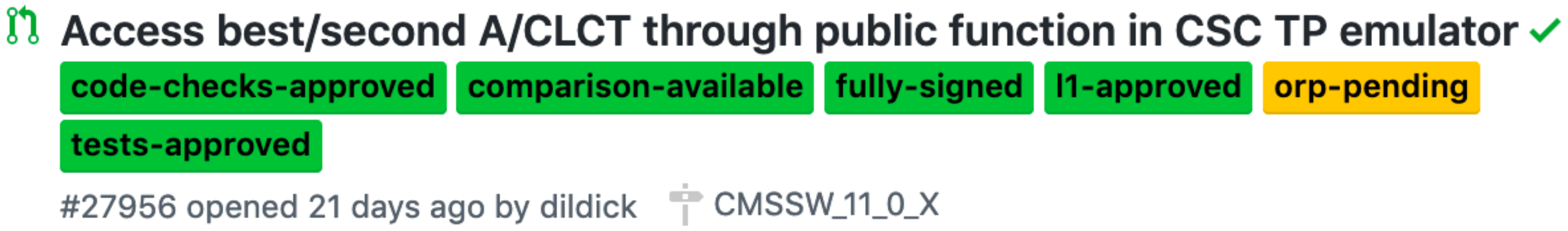
- In PR 19786 I expanded the LCT data format in simulation by adding a member "type_" which is only defined for LCTs when running the CSC local trigger emulator on MC or data digit
  - ✓ Is not defined for unpacked LCTs in RAW data

- The member type_ may only be used to debug the CSC local trigger.
  - ✓ It must **NOT** be used in OMTF/EMTF or DQM

- Type_ can be ALCTCLCT (ALCT-centric), CLCTALCT (CLCT-centric), ALCTCLCTGEM, ALCTCLCT2GEM, ALCT2GEM, CLCT2GEM, CLCTONLY, ALCTONLY

- This PR changes the default type from CLCTALCT to ALCTCLCT
  - ✓ CSC local trigger in simulation and firmware is always ALCT-centric, i.e. the ALCT BX is taken as reference around which potential CLCTs with matching BX's are considered

PR27956



Access best/second A/CLCT through public function in CSC TP emulator ✓

code-checks-approved comparison-available fully-signed l1-approved orp-pending tests-approved

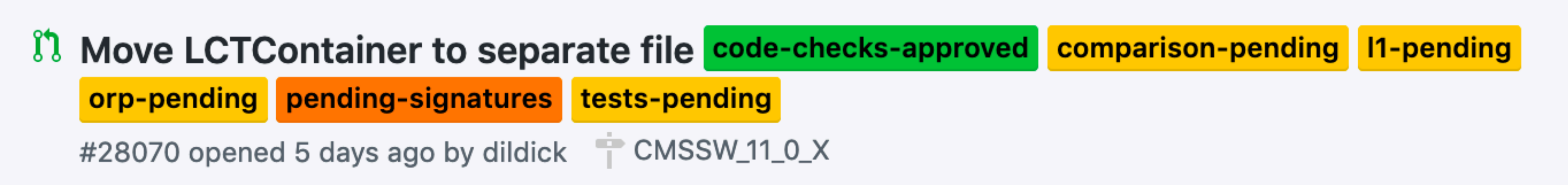
#27956 opened 21 days ago by dildick CMSSW_11_0_X

- This PR replaces the usage of public member variables (e.g. `bestALCT`) to public member functions (e.g. `getBestALCT()`) in CSC motherboard classes
  - ✓ an artifact of the legacy CSC TP emulator code

- In addition, it appears that the CLCT BX shift in PR #24402 was incomplete.
  - ✓ The public variables `bestCLCT` and `secondCLCT` would return CLCTs at central BX7.
    - ◉ The new public functions `getBestCLCT()` and `getSecondCLCT()` return CLCTs with central BX8.

- However, the CLCT readout remains unchanged.
  - ✓ It will produce produce the CLCT digi collection with a central BX of 7.
  - ✓ Also, this change won't have an effect on the LCT reconstruction efficiency, since the ALCT-CLCT BX matching window is at least 3 to 7 BX wide.

PR28070



Move LCTContainer to separate file code-checks-approved comparison-pending l1-pending orp-pending pending-signatures tests-pending

#28070 opened 5 days ago by dildick CMSSW_11_0_X

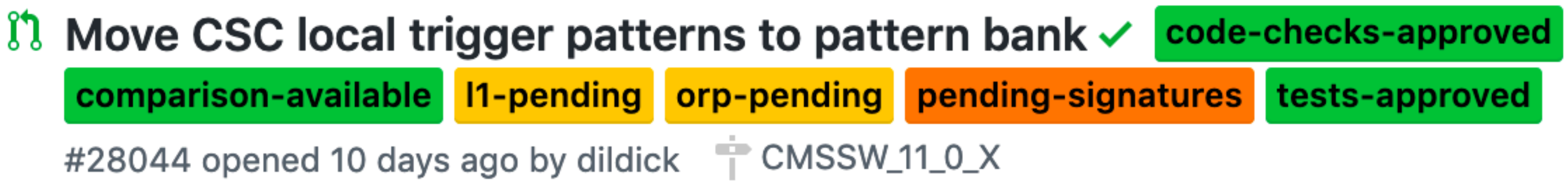
- The class LCTContainer was introduced in PR18560 to store candidate LCTs for any MEX/1 upgrade motherboard.

  ✓ Both for Run-3 & Phase-2 scenarios

- This PR moves `LCTContainer` from inside `CSCUpgradeMotherboard` to a separate class definition `LCTContainer.h`.

- It is part of the ongoing work to make the CSC local trigger as simple as possible to understand.

PR28044



Move CSC local trigger patterns to pattern bank ✓ code-checks-approved

comparison-available l1-pending orp-pending pending-signatures tests-approved

#28044 opened 10 days ago by dildick CMSSW_11_0_X

- The ALCT and CLCT trigger patterns have historically been defined in the ALCT and CLCT processors.

  ✓ Ideally, the patterns are stored in a dedicated class

- This PR moves the ALCT/CLCT trigger patterns defined in `CSCAnodeLCTProcessor` and `CSCCathodeLCTProcessor` to a new class `CSCPatternBank`.

- The CSCPatternBank can be extended with new LCT patterns (designed by UCLA a few years ago) which would improve the directional and positional resolution