GE2/1 & ME0 backend electronics

Evaldas Juska (TAMU)

1. Overview

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- **Common backend**
  - Aiming to have common ATCA-based hardware for GE2/1, ME0, CSC
  - Have identified the APT board as a baseline choice that meet the requirements of all three systems
  - ATCA test stand at CERN is already underway (all components ordered)
    - Additional test stands are being planned
- **Firmware reusability between all GEM systems**
  - GE1/1 backend firmware was designed from ground up to be flexible
    - Reusable across different hardware architectures
    - Reusable across the different GEM systems: GE1/1, GE2/1, ME0
    - Software interface is also kept compatible
  - This has contributed a lot in the fact that we were able to get GE2/1 and ME0 tests working so quickly
  - Even CSC FED system has reused a lot of the GEM firmware backend components
- **Hardware support**
  - CTP7 is the main hardware platform right now
  - GLIB support is being finalized (more details in Laurent's talk)
  - Will start on adding APT support soon as the ATCA stand is setup
  - Another low cost alternative is being investigated for test stands

2. GE2/1 System Overview

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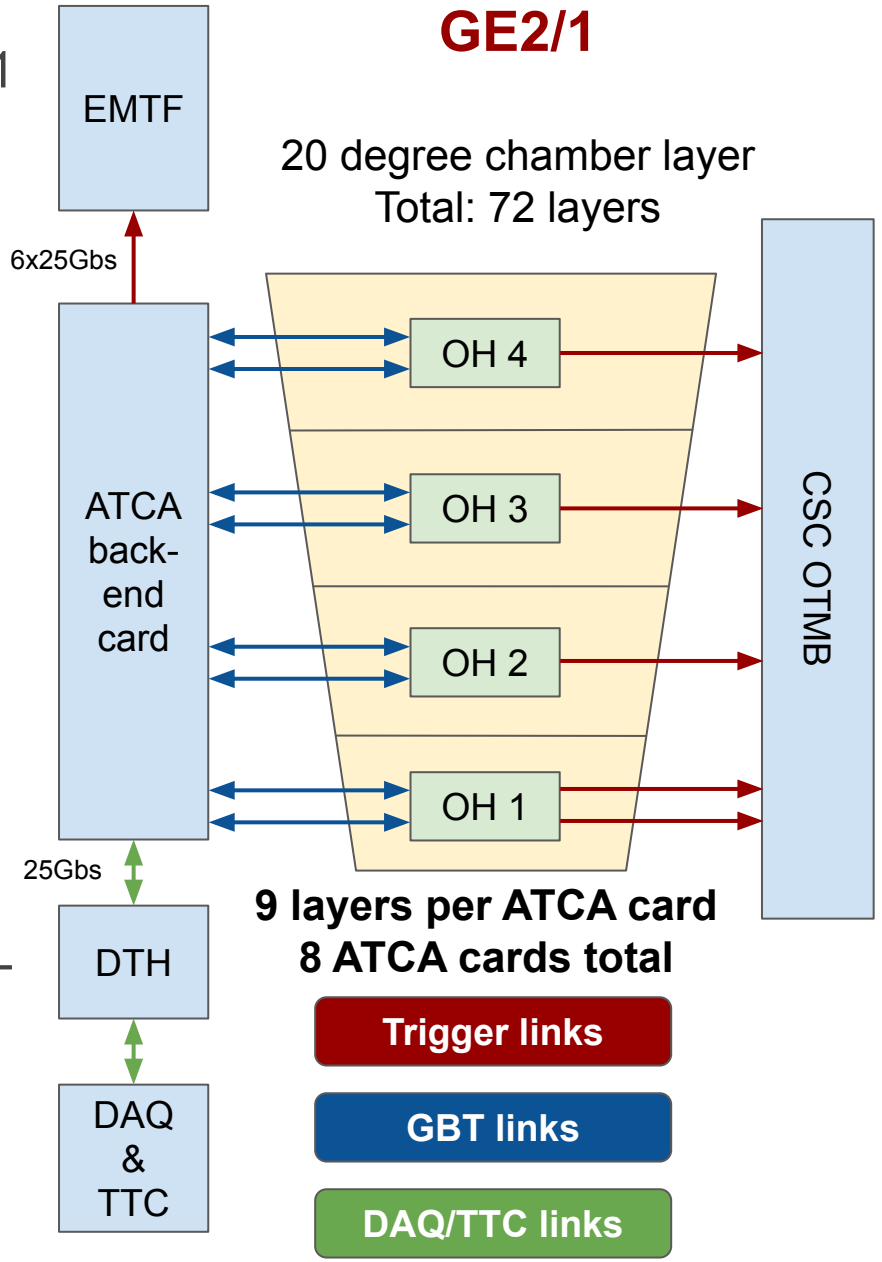
- **Overview**
  - Functionality is the same as GE1/1
  - Hardware is ATCA
- **Firmware**
  - Already have a fully functional firmware working on CTP7, which is being used by the integration team at CERN regularly
  - Final system-level firmware will be adapted to new ATCA hardware
    - Fiber links, clocking, etc..
  - All the GEM logic can be directly reused adjustments
- **Links**
  - 576 bidirectional GBTX links
  - Trigger data also received via GBT
  - 48x 25Gb/s links to EMTF
  - 8 ATCA cards total
- **Estimated data rate: 4.6 Gb/s**



3. GE2/1 differences w.r.t. GE1/1

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- **2 GBTX & 12 VFATs per OH instead of 3 GBTX & 24 VFATs**
  - Elink maps are different
  - Minor change
- **PROMless programming, and SCA interfacing**
  - Different OH FPGA
  - Elink maps are different
  - SCA I/O is different
  - All are minor changes
- **Trigger data embedded into GBT links**
  - Notice that were no red lines from OH to backend in previous slide
  - More on this in the next slide
- **ATCA interfaces**
  - New generation of FPGA (Virtex Ultrascale+)
  - The backend FPGA I/O will be different
  - Interfacing with DTH instead of AMC13
- **Interface documentation can be found here**

4. GE2/1 trigger data to backend

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- **GBT bandwidth in GE2/1**
  - 2.24Gb/s of unused bandwidth from OH to backend in current prototype
  - Next prototype will use GBTX wide-bus mode to extend this to 3.52Gb/s
  - This is more than enough to fit the sbit cluster (trigger) data
    - Need to be able to transfer up to 5 clusters per BX = 2.6Gb/s
    - Extra bandwidth will be used for error detection codes (CRC) and provide extra margin for possible future needs
  - Transmitting trigger data on GBT links is very similar to ME0
  - Can remove the extra links to backend, and also one VTTX on OH
  - Allows to fit the backend into 8 cards
- **GBTX wide-bus mode**
  - Standard feature of GBTX where asymmetric bandwidth is needed
  - Converts 4 output elinks to input elinks (each running at 320Mb/s)
  - In our case the 4 output elinks were unused
  - In the direction of OH to backend the Forward Error Correction code is removed and replaced by user data
    - Note that DAQ data already includes CRC for error detection
    - We will also add CRC to the trigger data
  - CSCs are operating with CRCs (no FEC) for many years
    - They also have a new board using GBTX in wide-bus mode

5. ME0 System Overview

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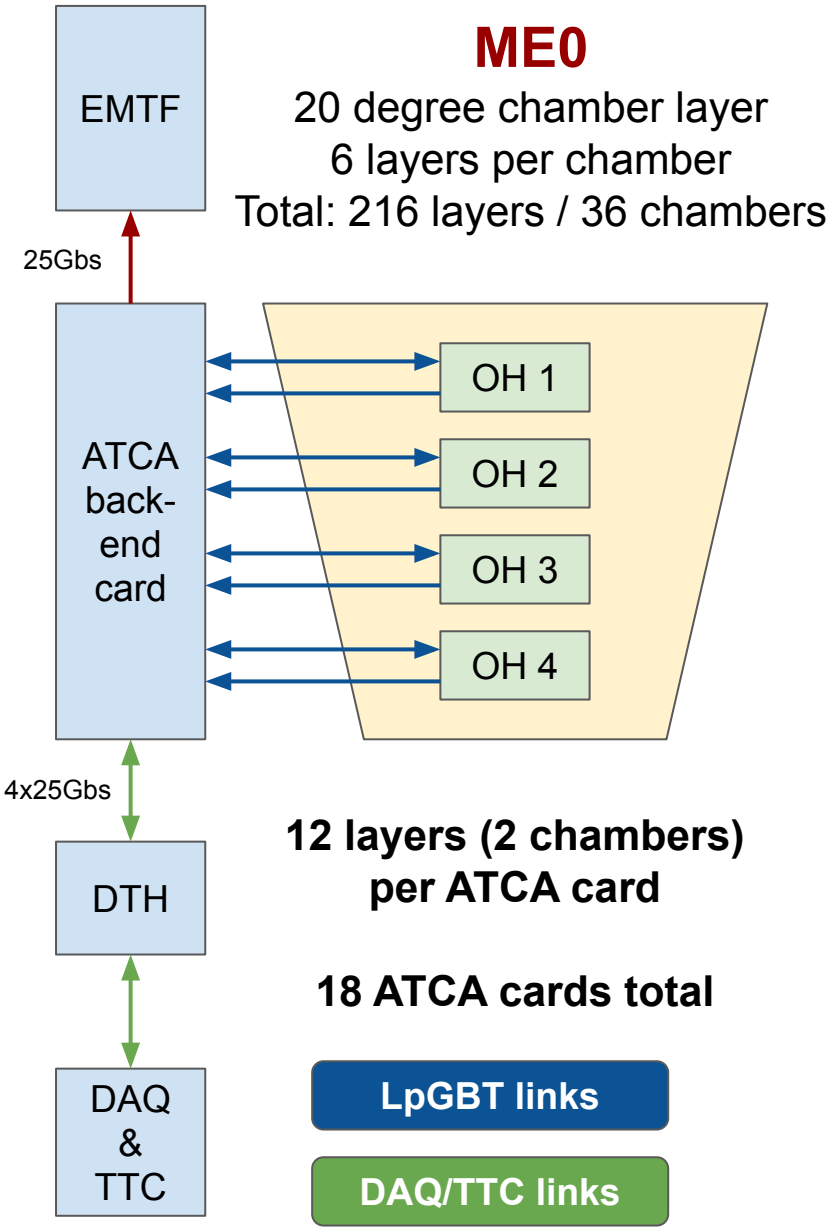
- **No FPGA on OH**
  - All components are rad-hard
  - Lossless DAQ and trigger data transmission to the backend
- **Backend requirements**
  - 2 stacks per card
    - 18 cards total
  - 6 layer stub building
    - Up to 16 stubs per BX
    - Very resource intensive
  - High number of LpGBT cores (96)
  - High DAQ bandwidth
    - 706Gb/s for full system
  - Number of links
    - 864 bidirectional (LpGBT)
    - 864 unidirectional (LpGBT)



6. ME0 backend firmware status

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- **Functional firmware for CTP7 already implemented, being tested**
  - 10.24Gb/s transceivers implemented and verified
  - LpGBT cores have been integrated and tested
  - Internal Control of the master LpGBT is working, slave is being tested
  - Communication to VFATs is already working!
    - Both fast control and slow control
    - Need addressing functionality to test full capabilities of slow control
  - Basic trigger data processing is in the works
  - See Andrew's report for more details on the testing progress

- **Differences w.r.t. GE1/1 are much greater**
  - LpGBT is quite different compared to GBTX both on frontend and backend sides
  - No OH FPGA to worry about (no PROMless, no FPGA slow control)
  - Only 6 VFATs per OH
    - So far DAQ events have been structured around OH
    - 1 block per OH containing all VFAT data
    - For ME0 will change this to be 1 block per layer or even stack
  - Biggest change by far: 6 layer stub building for trigger
    - Work on this should start soon
    - Simulation studies are also needed

7. ME0 Stub Building

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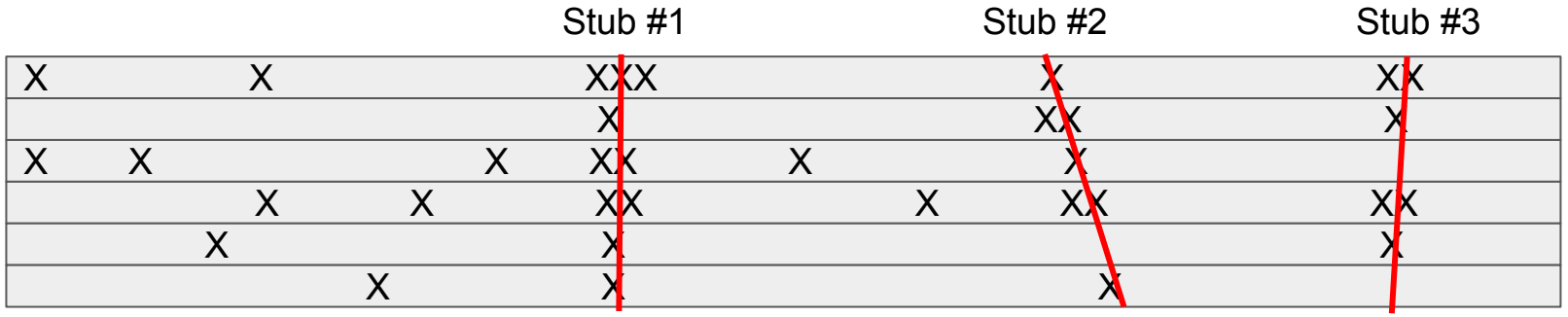
- **Local 6 layer stub finding logic resources**
  - FPGA resource intensive task
  - CSC has a dedicated board (OTMB) for this function (for each chamber)
    - Current firmware for ME1/1 OTMB uses about 80k virtex 6 “logic cells”
  - ME0 has 1536 di-strips vs. 224 half-strips in ME1/1
    - Simply extrapolating linearly results in 549k “logic cells” per ME0 chamber
  - We will have 2 ME0 chambers per ATCA card, and build up to 16 stubs
    - Extrapolated CSC algorithm would take about half of VU9P resources
  - Although ME0 stub-finding firmware most likely will be very different from CSCs, and possibly use less resources than this simple extrapolation

- **Saves a lot of bandwidth in trigger and DAQ**
  - Only one 25Gb/s link to EMTF per 2 chambers is needed to transmit 16 stubs per BX per chamber
  - DAQ data can be selectively readout based on stub presence (optional)



8. ATCA APT card

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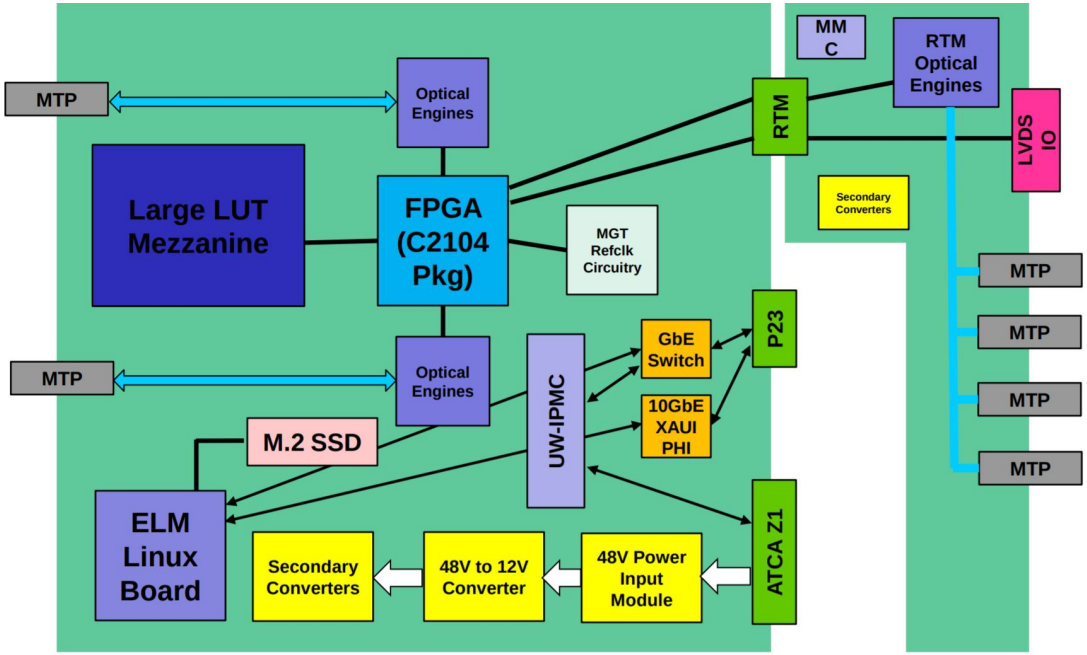
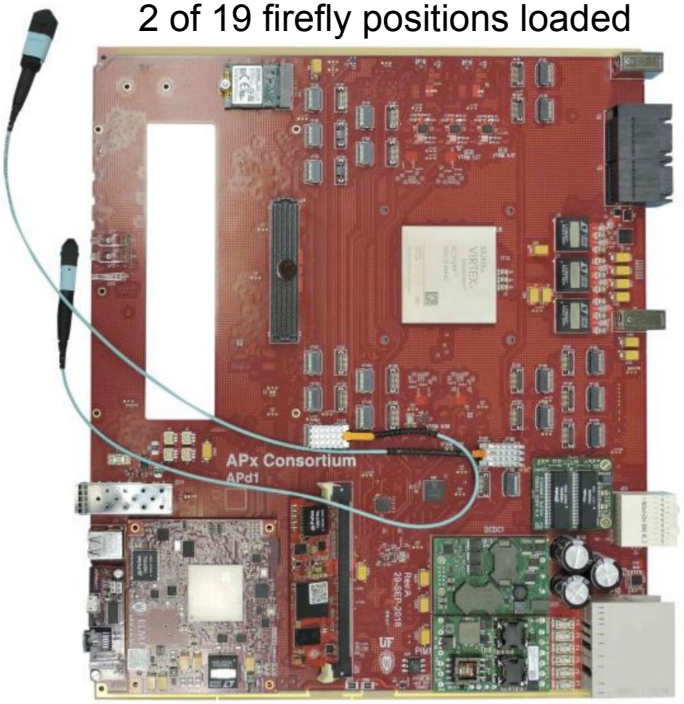
- **Advanced Processor by APx consortium (baseline option)**
  - Large VU9P FPGA
  - Up to 100 x 28Gb/s optical TX and RX
  - Onboard linux, similar to CTP7 (but faster CPU and faster link to FPGA)
  - Satisfies all GE2/1, ME0, and CSC needs
  - We will have a prototype at CERN by the end of 2019





9. DTH

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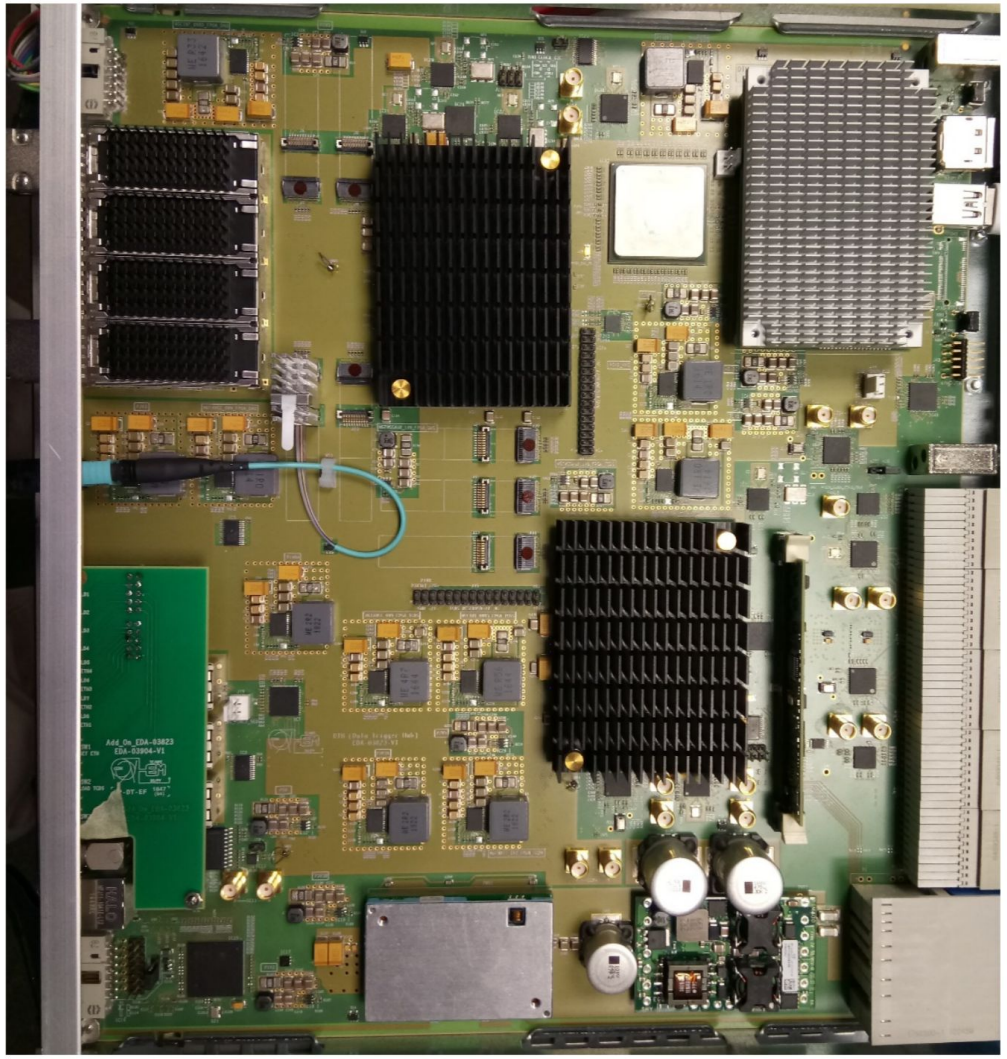
- **Status**
  - First prototype produced
  - Used by DAQ and TCDS groups to develop firmware
  - Second prototype will be available to subsystems in January 2020
  - Current version supports 400Gb/s bandwidth
  - Final card expected to support 800Gb/s
  - We need one card per crate
    - 1 for GE2/1
    - 2 for ME0
      - Must support at least 800Gb/s per card



10. CTP7 boards

- **Currently using 15 CTP7s for GE1/1, GE2/1, ME0, CSC**
  - 6 boards at QC7/8 (one endcap worth of boards)
  - 2 at 904 integration stands (one for GE1/1, and one for GE2/1 / ME0)
  - 1 at P5
  - 5 boards at university test stands (TAMU, UCLA, Rice, ULB)
  - 1 board used by CSC
  - We will acquire 2 more boards in Q2 next year
- **Minus endcap commissioning at P5 (4 CTP7s as of October 2019)**
  - Covers ⅔ of the endcap, will have to rotate until June 2020
  - 1 board is already at P5
  - 1 board comes from TAMU
  - 2 or possibly 3 boards come from QC7
    - These are the two additional QC7 stations
    - We are planning to replace them with GLIBs
- **Both endcaps commissioning at P5 (12 CTP7s as of June 2020)**
  - All boards from QC7/8 will move to P5
  - 2 new boards will be acquired
  - 2 boards will come from test stands (one ops spare will be at 904 stand)
  - Note: ATCA test stands will be already available

11. CTP7 and ATCA alternatives

- **High density**
  - Due to high density of CTP7, the number of boards is tight
  - Test stands usually only require to connect to one chamber
    - 8% of the board's capability
  - Density and cost of ATCA cards is even higher

- **Alternatives**
  - Low cost alternative cards are useful for test stand use
  - Currently GLIB serves that purpose
    - Firmware is being updated by Laurent
  - GLIB has several limitations:
    - Optical links limited to 6Gb/s by FPGA
    - Only 4 optical links in standard configuration
      - Can be extended to 8 links with a mezzanine card
    - Ok for GE1/1 and GE2/1, but larger test sites require a lot of cards (FIT)

12. CTP7 and ATCA alternatives

- **FPGA based PCIe "accelerator" cards for PC**
  - Available from multiple vendors (e.g. Bittware, Xilinx)
    - Other projects at CERN are also using these cards (Bittware also mentioned CMS)
  - Typically offer 16 optical links @ up to 25Gb/s
    - Some can be extended to 32 links, but 16 is enough for most test sites
    - Compatible with GE1/1, GE2/1, ME0, CSC needs
  - FPGA choice is wide, but cards with 16 links normally have VU9P or VU13P
  - We don't yet have quotes, but expecting the cost to be around $6k
  - Copper I/O is available on some cards
    - E.g. for external trigger signals, or synchronization across several cards
  - Optional DDR4 modules can be installed
    - E.g. useful for simulated FE data for ME0 algorithm development
  - PCIe interface provides a fast & high bandwidth communication w/ CPU
    - Fast execution of calibration scans
    - DAQ can write directly to the host PC's system memory
  - Possible use cases
    - Test stand at FIT
    - QC7 for GE2/1
    - Other test stands

13. Summary

- **Firmware status is in good shape**
  - Fully functional CTP7-based firmware for GE2/1, used regularly
  - CTP7-based firmware for ME0 being tested now with good results
  - Proven flexibility and portability across different systems

- **ATCA status**
  - Test stand at CERN expected before the end of the year
  - Do not expect any showstoppers
  - Some time will have to be invested to make the current firmware compatible

- **Cards for test stands**
  - As GE1/1 is moving towards commissioning, the CTP7s are becoming more scarce
  - Being compensated by the GLIB developments
  - Another low cost alternative is being pursued
    - Fast optical links (same as ATCA)
    - Higher link count than GLIB
    - Large FPGA