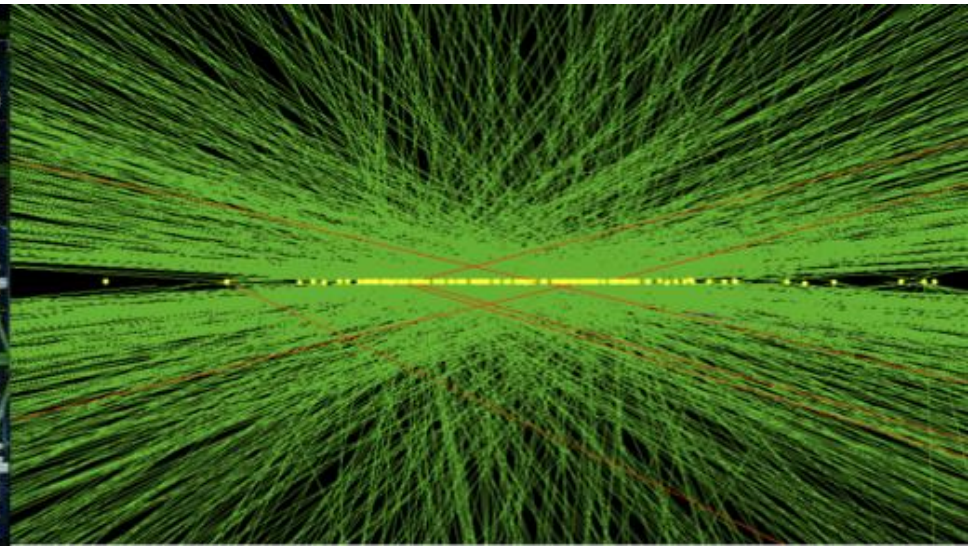
# Cost, Schedule and Risks

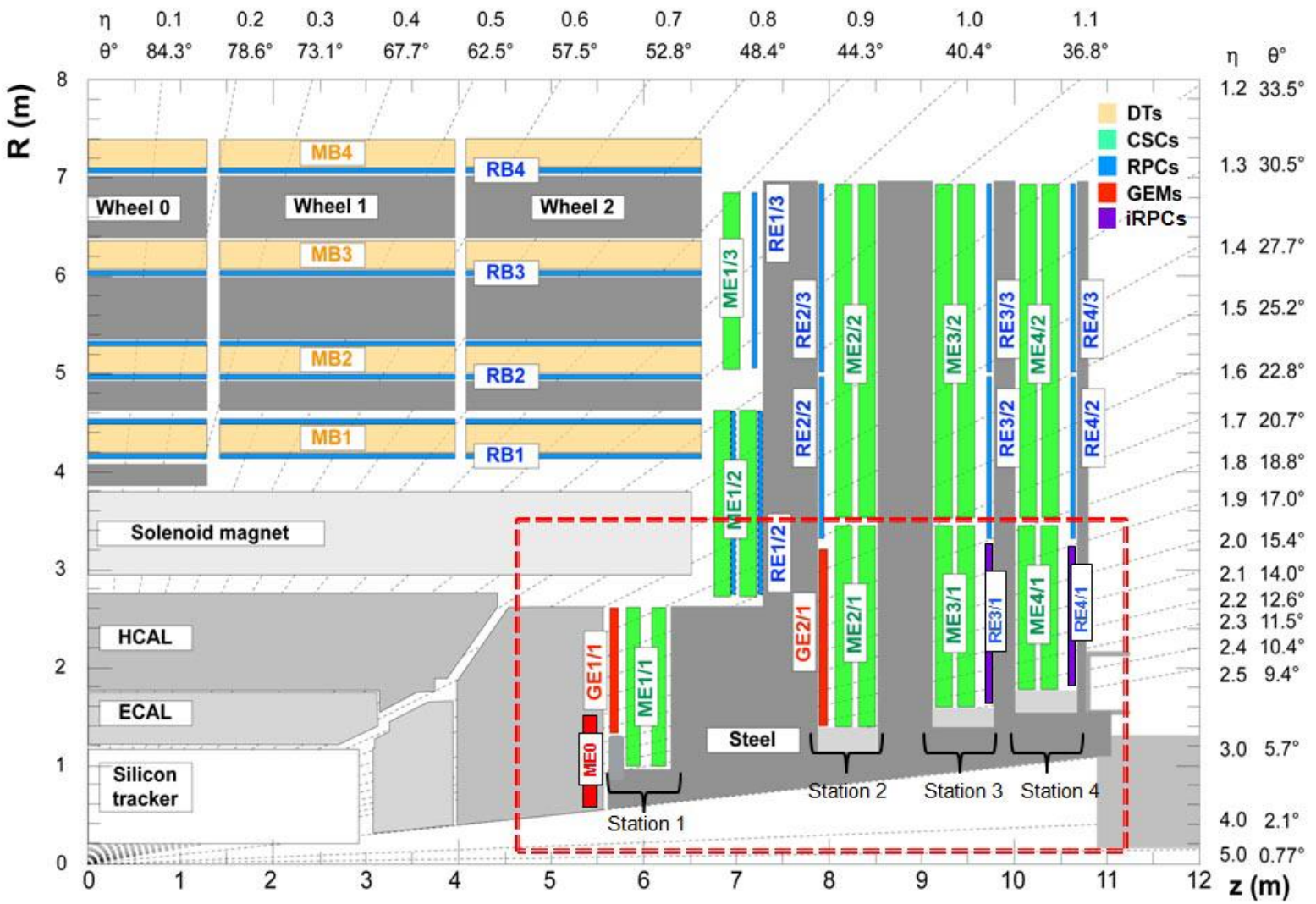
Alexei N. Safonov, CMS Muon GEM Upgrade Coordinator

GE2/1 TCR Review

August 30, 2019

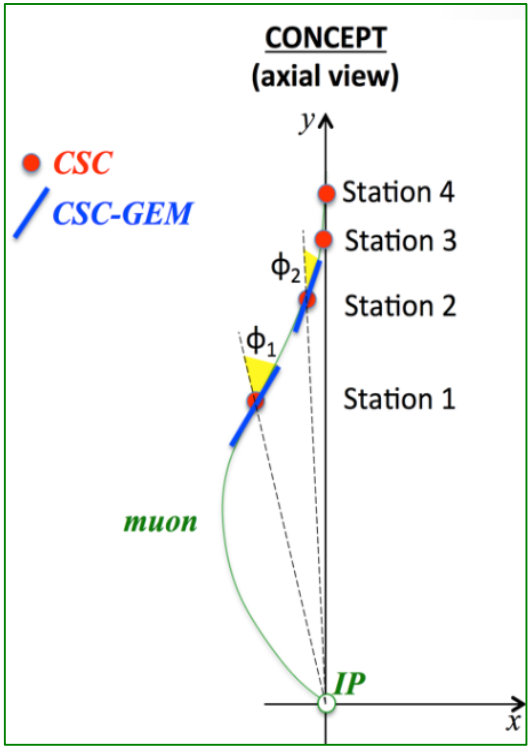


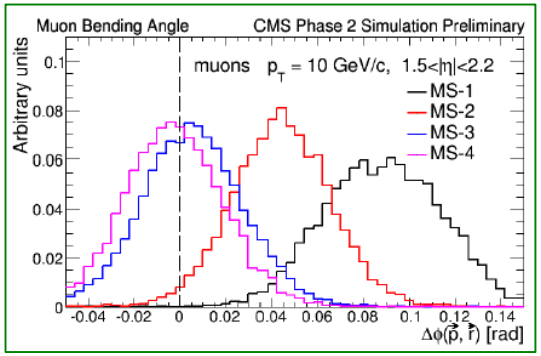
# CMS Muon Upgrade Scope



# Science Requirements

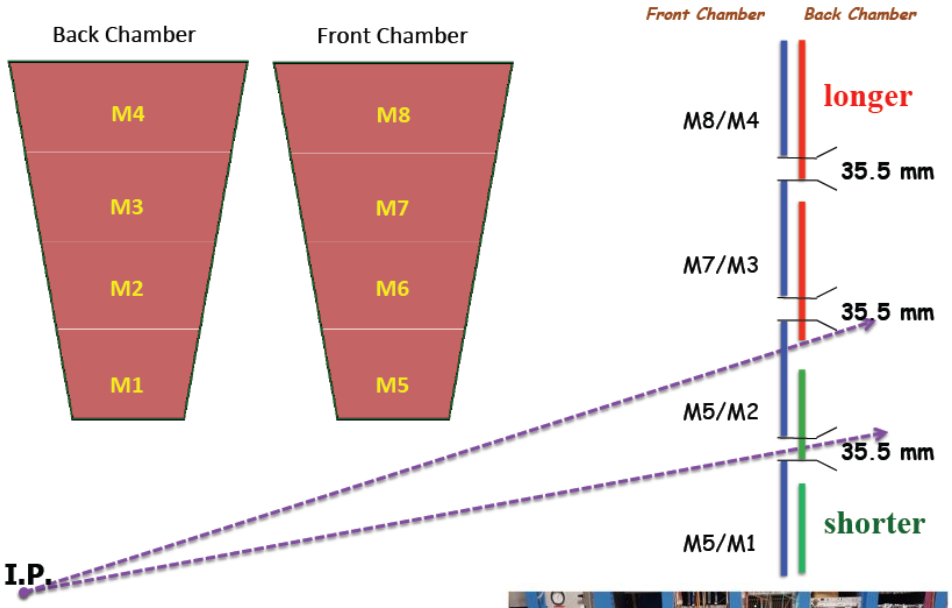
- Motivated by improving capabilities of the Level-1 muon trigger
  - Impact on a broad range of physics: Higgs, EW measurements and new physics searches, e.g. searches for long-lived particles decaying to muons
- Principles similar to GE1/1:
  - Works with the CSC
  - Boost segment-finding efficiency
  - Disentangle combinatorial "ghosts" in CSCs (short strips in GEMs)
  - Muon direction within a station
- Trigger performance sets key design requirements:
  - Position and timing resolution
- Additional requirements set by "environmental" factors:
  - Operational capabilities provided high incident hit rate, radiation environment, longevity, compact design due to limited spaces, cost optimization etc.



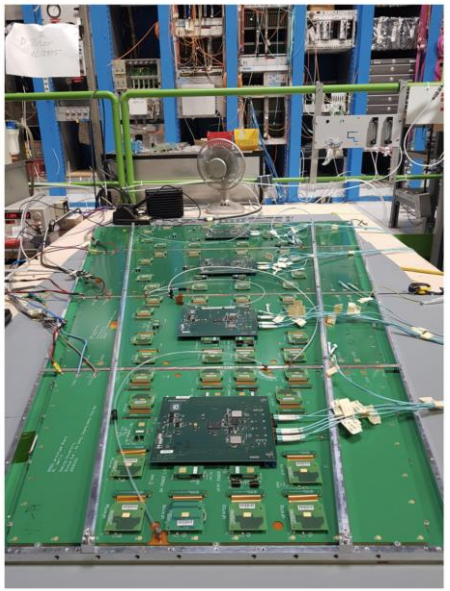



# Key Performance Parameters

- GE21 Detector System
  - 72 chambers arranged in 2 layers installed
    - 4 triple GEM modules per chamber
    - Mechanical structures, including chimneys and support elements
    - On-chamber elements providing connectivity (mechanical, electrical, services)
    - On-chamber cooling circuits




- On-chamber and off-chamber electronics complete with firmware & software
- Power system
- Infrastructure and Services
  - Services and power
  - Optical fiber plant



# GE2/1 Milestones from TDR

- Up to the start of the construction project

| | ID | Milestone title | Date | |
|---|---|---|---|---|
| Design | GE21.RD.DET.1 GE21.RD.FE.1 GE21.RD.BE.1 | GE2/1 R&D: Key detector system design parameters are defined based on performance requirements | 21.Mar.17 | Achieved |
| | GE21.RD.FE.2 | GE2/1 R&D: On-chamber electronics preliminary design completed and interfaces defined | 19.Jun.17 | Achieved |
| | GE21.RD.BE.2 | GE2/1 R&D: Off-chamber electronics preliminary design completed and interfaces defined | 12.Mar.18 | Achieved |
| | GE21.RD.DET.2 | GE2/1 R&D: A full size chamber prototype with partially instrumented readout built, tested and performance validated | 1.May.18 | Achieved |
| | GE21.RD.DET.3 | GE2/1 R&D: Detector design parameters optimization completed, final chamber design is selected for the demonstrator | 8.May.18 | Achieved |
| | GE21.RD.FE.3 | GE2/1 R&D: On-chamber electronics prototypes engineering design complete | 1.Jun.18 | Achieved 28.Sep.18 |
| Prototyping | GE21.RD.FE.4 | GE2/1 R&D: On-chamber electronics prototype electronics manufacturing and testing is complete | 9.Oct.18 | Achieved 19.Feb.19 |
| | GE21.RD.DET.4 | GE2/1 R&D: Performance of the demonstrator chamber with prototype electronics is validated | 12.Mar.19 | Achieved 17.May.19 |
| | GE21.RD.FE.5 GE21.RD.BE.3 | GE2/1 R&D: On-chamber and off-chamber prototype electronics integration and performance studies completed | 12.Dec.19 | Expect in May.20 |
| | | GE2/1 PRR for the On-Detector Services | 3.Aug.2018 | Achieved (Jul.18) |
| | | GE2/1 PRR for the Foil Production | 13.Nov.2018 | Achieved 22.May 19 |
| | | GE2/1 Detector EDR | 12.Mar.2019 | Achieved 22.May.19 |
| | | GE2/1 ESR | 12.Dec.2019 | Expect in May.20 |

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| | GE21.RD.FE.2 | GE2/1 R&D: On-chamber electronics preliminary design completed and interfaces defined | 19.Jun.17 | Achieved |
| | GE21.RD.BE.2 | GE2/1 R&D: Off-chamber electronics preliminary design completed and interfaces defined | 12.Mar.18 | Achieved |
| | | | | ed |
| | | | | ed |
| | | | | ed 28.Sep.18 |
| Prototyping | | is complete | | ed 19.Feb.19 |
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**Project high level status as of today:**

- Services: well in the construction phase
- Chambers: early construction phase (hampered by funding related delays)
- Electronics: last stretch of the R&D phase

# Key Performance Parameters

- GE21 Detector System
  - 72 chambers arranged in 2 layers installed
    - 4 triple GEM modules per chamber
    - Mechanical structures, including chimneys and support elements
    - On-chamber elements providing connectivity (mechanical, electrical, services)
  - On-chamber cooling elements (circuits)
- On-chamber and off-chamber electronics complete with firmware & software
- Power system
- Infrastructure and Services
  - Services and power
  - Optical fiber plant

EDR May. 2019

Combine with ESR (May. 2020)

ESR (May. 2020)

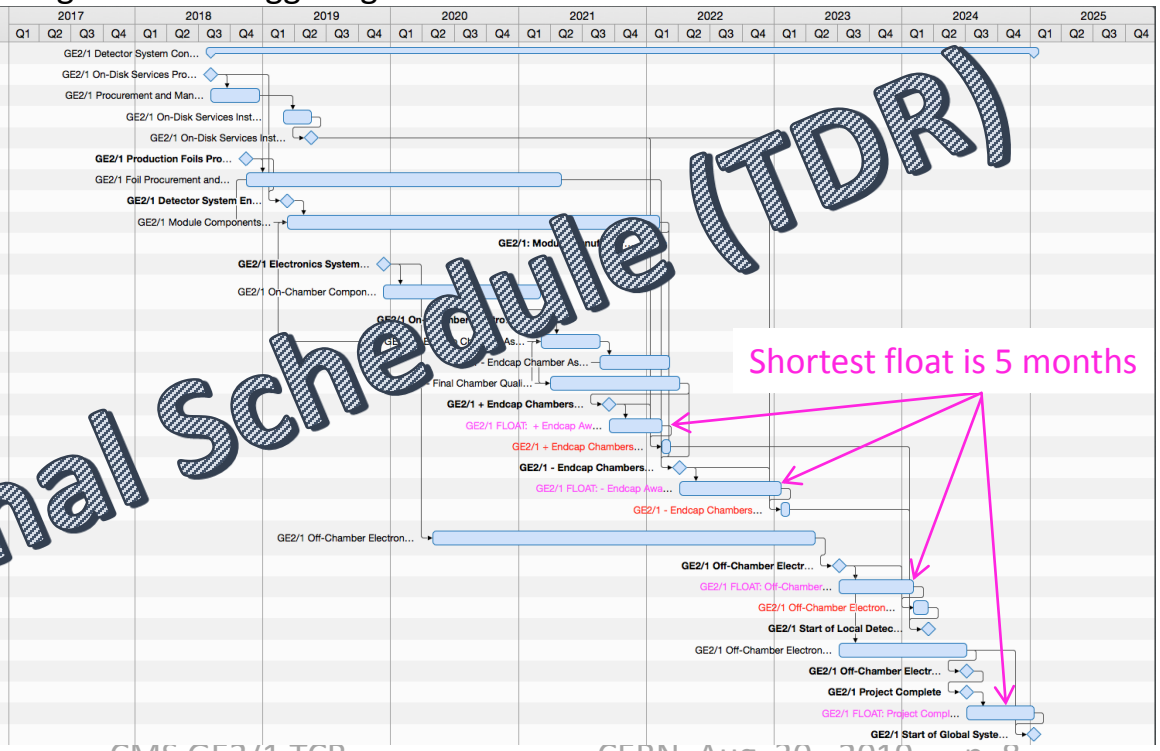
PRR (Jun. 2018) for LS-2 installation

Combine w/ ESR or an earlier PRR

# GE2/1 Construction Schedule Overview

- EDR, ESR, PRR kick-start the project, subject to various constraints
  - R&D program completion, availability of the facilities for module/chamber assembly, funding availability, resource leveling among three GEM projects (GE1/1, GE2/1, ME0)
- Critical path for the GE2/1 project:
  - Chamber assembly has to finish in time for installation
  - Assembly is preceded by GEM module and on-chamber electronics production
  - Shortest float is 5 months for "+" Endcap
    - Actual floats somewhat larger due to staggering of batches

| Title | Expected Start | Expected End |
|---|---|---|
| **GE2/1 Detector System Construction** | **Aug 3, 2018** | **Jan 13, 2025** |
| GE2/1 On-Disk Services Procurement Readiness Review (PRR) | Aug 3, 2018 | Aug 3, 2018 |
| GE2/1 Procurement and Manufacturing of Components for On-Disk Services | Aug 6, 2018 | Dec 21, 2018 |
| GE2/1 On-Disk Services Installation (as part of the LS-2 activities) | Mar 1, 2019 | May 17, 2019 |
| GE2/1 On-Disk Services Installation Complete | May 20, 2019 | May 20, 2019 |
| **GE2/1 Production Foils Procurement Readiness Review (PRR)** | Nov 13, 2018 | Nov 13, 2018 |
| GE2/1 Foil Procurement and Manufacturing at Vendor Sites | Nov 14, 2018 | May 3, 2021 |
| **GE2/1 Detector System Engineering Design Review (EDR)** | Mar 12, 2019 | Mar 12, 2019 |
| GE2/1 Module Components Procurement, Assembly & Testing | Mar 12, 2019 | Feb 7, 2022 |
| **GE2/1: Module Manufacturing and Testing is Complete** | Feb 7, 2022 | Feb 7, 2022 |
| **GE2/1 Electronics System Review (ESR)** | Dec 12, 2019 | Dec 12, 2019 |
| GE2/1 On-Chamber Components of the DAQ Electronics System Production and Testing | Dec 12, 2019 | Mar 3, 2021 |
| **GE2/1 On-Chamber Electronics Ready for Chamber Assembly** | Mar 3, 2021 | Mar 3, 2021 |
| GE2/1 + Endcap Chamber Assembly & Testing | Mar 5, 2021 | Aug 19, 2021 |
| GE2/1 - Endcap Chamber Assembly & Testing | Aug 20, 2021 | Mar 8, 2022 |
| GE2/1 - Final Chamber Quality Certification at the Cosmic Stand Facility | April 2, 2021 | April 5, 2022 |
| **GE2/1 + Endcap Chambers Ready for Installation** | Sep 16, 2021 | Sep 16, 2021 |
| GE2/1 FLOAT: + Endcap Awaiting Installation | Sep 16, 2021 | Feb 14, 2022 |
| GE2/1 + Endcap Chambers Planned Installation in YETS-2021 | Feb 15, 2022 | Mar 9, 2022 |
| **GE2/1 - Endcap Chambers Ready for Installation** | April 5, 2022 | April 5, 2022 |
| GE2/1 FLOAT: - Endcap Awaiting Installation | April 6, 2022 | [illegible] |
| GE2/1 - Endcap Chambers Planned Installation in YETS-2022 | Jan 20, 2023 | [illegible] |
| GE2/1 Off-Chamber Electronics Procurement, Production, Testing and Integration | [illegible] | [illegible] |
| **GE2/1 Off-Chamber Electronics Ready for Installation** | [illegible] | [illegible] |
| GE2/1 FLOAT: Off-Chamber Electronics Awaiting Installation | [illegible] | [illegible] |
| GE2/1 Off-Chamber Electronics Planned Installation at P[illegible] | [illegible] | [illegible] |
| **GE2/1 Start of Local Detector Commissionning** | Mar 15, 2024 | Mar 15, 2024 |
| GE2/1 Off-Chamber Electronics Global CMS Integration | July 6, 2023 | July 3, 2024 |
| **GE2/1 Off-Chamber Electronics Integration into Global CMS Complete** | July 3, 2024 | July 3, 2024 |
| **GE2/1 Project Complete** | July 3, 2024 | July 3, 2024 |
| GE2/1 FLOAT: Project Completion to the Global System Commmissionning Start | July 4, 2024 | Jan 10, 2025 |
| **GE2/1 Start of Global System Commissionning** | Jan 13, 2025 | Jan 13, 2025 |



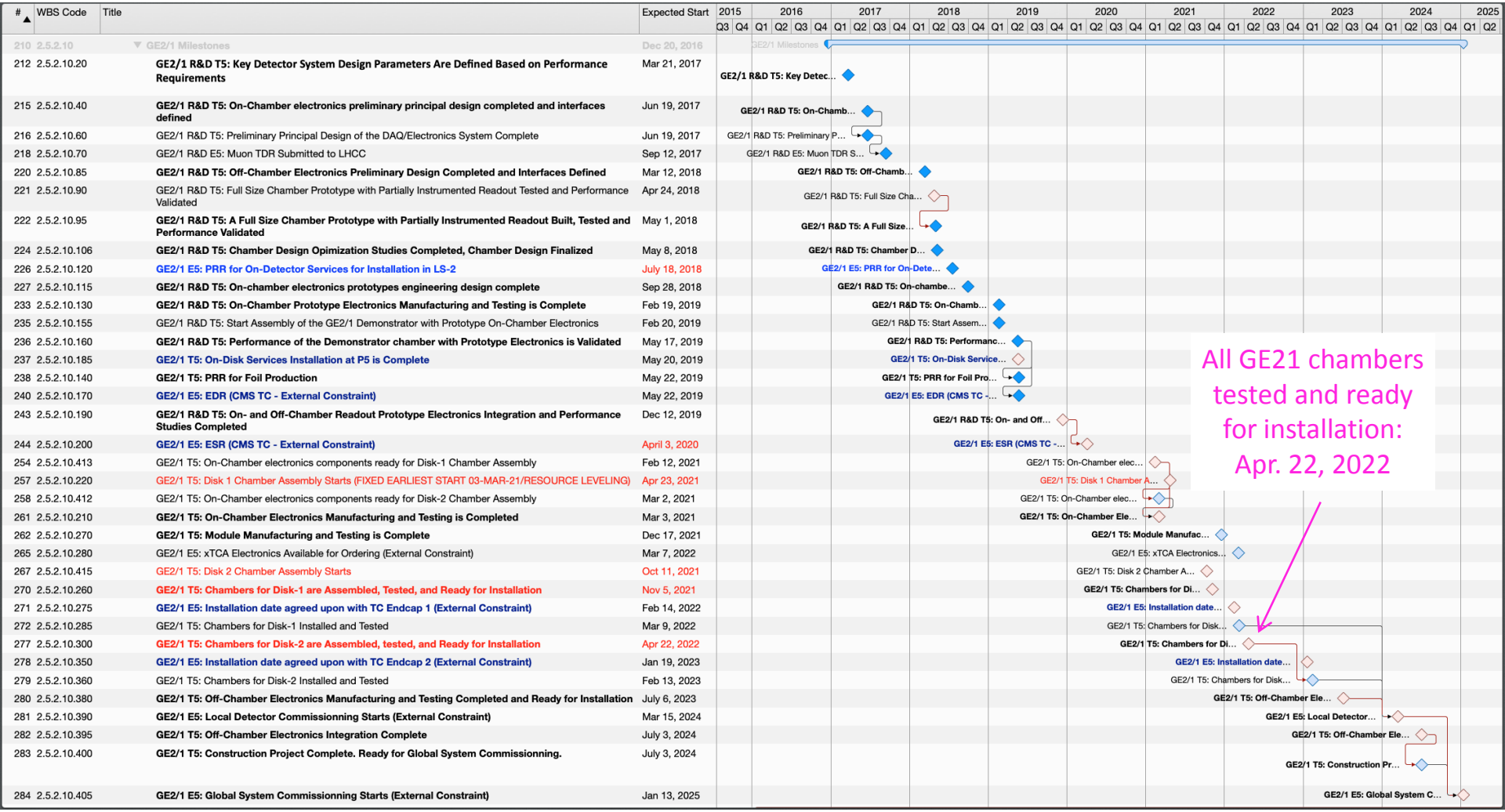
# Schedule Updates

- Update to the CMS official need-by-date for the full GE2/1 system to be ready for installation:
  - Ready for installation: August 2023
    - Readiness in the baseline schedule should be at least 6-12 months earlier to provide adequate float for delays as a number of risks will realize
- Significant change compared to the original need-by dates set in the TDR:
  - Ready for installation Endcap-1: Feb. 2022
  - Ready for installation Endcap-2: Jan. 2023
- Additional (welcome) cushion to offset expected schedule delays, not a reason to slower down
  - We have seen significant risks that have already realized related to funding availability delays, e.g. in India

# New (Draft) Baseline Schedule

- Chamber assembly completed well ahead of either the installation in YEST22-23 (9 months float) or the need-by-date of Aug.'23

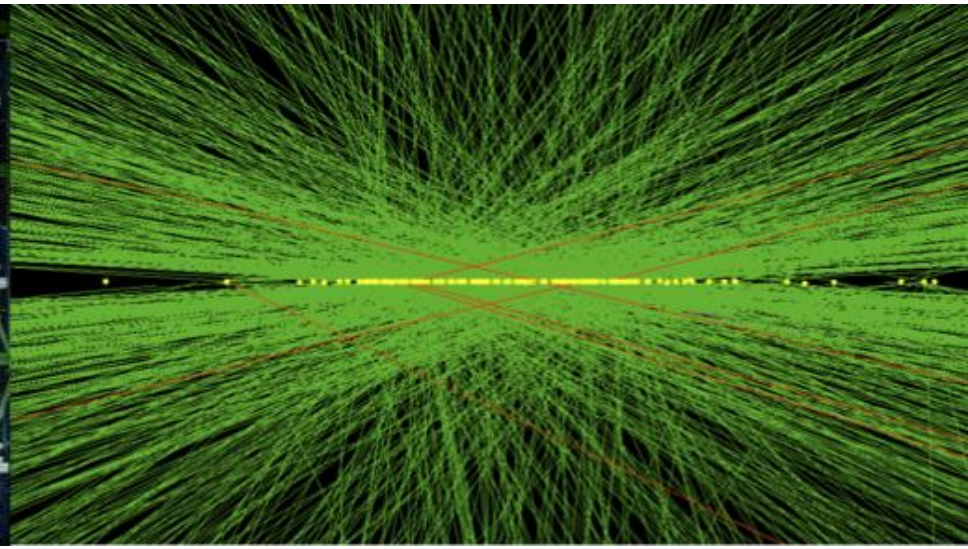
| # | WBS Code | Title | Expected Start |
|---|---|---|---|
| 210 | 2.5.2.10 | GE2/1 Milestones | Dec 20, 2016 |
| 212 | 2.5.2.10.20 | **GE2/1 R&D T5: Key Detector System Design Parameters Are Defined Based on Performance Requirements** | Mar 21, 2017 |
| 215 | 2.5.2.10.40 | **GE2/1 R&D T5: On-Chamber electronics preliminary principal design completed and interfaces defined** | Jun 19, 2017 |
| 216 | 2.5.2.10.60 | GE2/1 R&D T5: Preliminary Principal Design of the DAQ/Electronics System Complete | Jun 19, 2017 |
| 218 | 2.5.2.10.70 | GE2/1 R&D E5: Muon TDR Submitted to LHCC | Sep 12, 2017 |
| 220 | 2.5.2.10.85 | **GE2/1 R&D T5: Off-Chamber Electronics Preliminary Design Completed and Interfaces Defined** | Mar 12, 2018 |
| 221 | 2.5.2.10.90 | GE2/1 R&D T5: Full Size Chamber Prototype with Partially Instrumented Readout Tested and Performance Validated | Apr 24, 2018 |
| 222 | 2.5.2.10.95 | **GE2/1 R&D T5: A Full Size Chamber Prototype with Partially Instrumented Readout Built, Tested and Performance Validated** | May 1, 2018 |
| 224 | 2.5.2.10.106 | **GE2/1 R&D T5: Chamber Design Opimization Studies Completed, Chamber Design Finalized** | May 8, 2018 |
| 226 | 2.5.2.10.120 | **GE2/1 E5: PRR for On-Detector Services for Installation in LS-2** | July 18, 2018 |
| 227 | 2.5.2.10.115 | **GE2/1 R&D T5: On-chamber electronics prototypes engineering design complete** | Sep 28, 2018 |
| 233 | 2.5.2.10.130 | **GE2/1 R&D T5: On-Chamber Prototype Electronics Manufacturing and Testing is Complete** | Feb 19, 2019 |
| 235 | 2.5.2.10.155 | GE2/1 R&D T5: Start Assembly of the GE2/1 Demonstrator with Prototype On-Chamber Electronics | Feb 20, 2019 |
| 236 | 2.5.2.10.160 | **GE2/1 R&D T5: Performance of the Demonstrator chamber with Prototype Electronics is Validated** | May 17, 2019 |
| 237 | 2.5.2.10.185 | **GE2/1 T5: On-Disk Services Installation at P5 is Complete** | May 20, 2019 |
| 238 | 2.5.2.10.140 | **GE2/1 T5: PRR for Foil Production** | May 22, 2019 |
| 240 | 2.5.2.10.170 | **GE2/1 E5: EDR (CMS TC - External Constraint)** | May 22, 2019 |
| 243 | 2.5.2.10.190 | **GE2/1 R&D T5: On- and Off-Chamber Readout Prototype Electronics Integration and Performance Studies Completed** | Dec 12, 2019 |
| 244 | 2.5.2.10.200 | **GE2/1 E5: ESR (CMS TC - External Constraint)** | April 3, 2020 |
| 254 | 2.5.2.10.413 | GE2/1 T5: On-Chamber electronics components ready for Disk-1 Chamber Assembly | Feb 12, 2021 |
| 257 | 2.5.2.10.220 | GE2/1 T5: Disk 1 Chamber Assembly Starts (FIXED EARLIEST START 03-MAR-21/RESOURCE LEVELING) | Apr 23, 2021 |
| 258 | 2.5.2.10.412 | GE2/1 T5: On-Chamber electronics components ready for Disk-2 Chamber Assembly | Mar 2, 2021 |
| 261 | 2.5.2.10.210 | **GE2/1 T5: On-Chamber Electronics Manufacturing and Testing is Completed** | Mar 3, 2021 |
| 262 | 2.5.2.10.270 | **GE2/1 T5: Module Manufacturing and Testing is Complete** | Dec 17, 2021 |
| 265 | 2.5.2.10.280 | GE2/1 E5: xTCA Electronics Available for Ordering (External Constraint) | Mar 7, 2022 |
| 267 | 2.5.2.10.415 | GE2/1 T5: Disk 2 Chamber Assembly Starts | Oct 11, 2021 |
| 270 | 2.5.2.10.260 | **GE2/1 T5: Chambers for Disk-1 are Assembled, Tested, and Ready for Installation** | Nov 5, 2021 |
| 271 | 2.5.2.10.275 | **GE2/1 E5: Installation date agreed upon with TC Endcap 1 (External Constraint)** | Feb 14, 2022 |
| 272 | 2.5.2.10.285 | GE2/1 T5: Chambers for Disk-1 Installed and Tested | Mar 9, 2022 |
| 277 | 2.5.2.10.300 | **GE2/1 T5: Chambers for Disk-2 are Assembled, tested, and Ready for Installation** | Apr 22, 2022 |
| 278 | 2.5.2.10.350 | **GE2/1 E5: Installation date agreed upon with TC Endcap 2 (External Constraint)** | Jan 19, 2023 |
| 279 | 2.5.2.10.360 | GE2/1 T5: Chambers for Disk-2 Installed and Tested | Feb 13, 2023 |
| 280 | 2.5.2.10.380 | **GE2/1 T5: Off-Chamber Electronics Manufacturing and Testing Completed and Ready for Installation** | July 6, 2023 |
| 281 | 2.5.2.10.390 | **GE2/1 E5: Local Detector Commissionning Starts (External Constraint)** | Mar 15, 2024 |
| 282 | 2.5.2.10.395 | **GE2/1 T5: Off-Chamber Electronics Integration Complete** | July 3, 2024 |
| 283 | 2.5.2.10.400 | **GE2/1 T5: Construction Project Complete. Ready for Global System Commissionning.** | July 3, 2024 |
| 284 | 2.5.2.10.405 | **GE2/1 E5: Global System Commissionning Starts (External Constraint)** | Jan 13, 2025 |



# Production Schedule Scenarios

- Assumptions:
  - Implement “faster” GEM module production based on a larger number of sites
    - Credible based on GE11 experience, validated and presented at the GE21 EDR in May 2019
    - Major impact on schedule dynamics: in previous versions, completion of the second endcap chamber assembly at CERN was dependent on too slow arrival of GEM modules
  - Implement an adjustable external delay with the arrival of Indian funding for the corresponding risk
    - Assume the start date of procurement of readout boards and other module components in Indian scope: Jan. 10, 2020
  - Electronics R&D completion and approval for construction:
    - ESR on Apr. 3, 2020; procurement of Versatile Link ASICs (GBTX, VTT/RX) procurement starts on Apr. 4, 2020

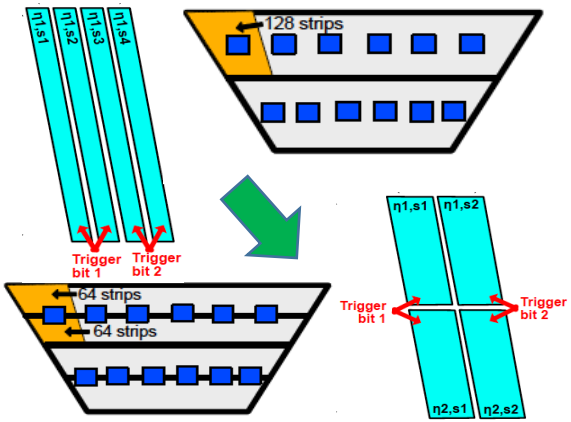
# Design Evolution

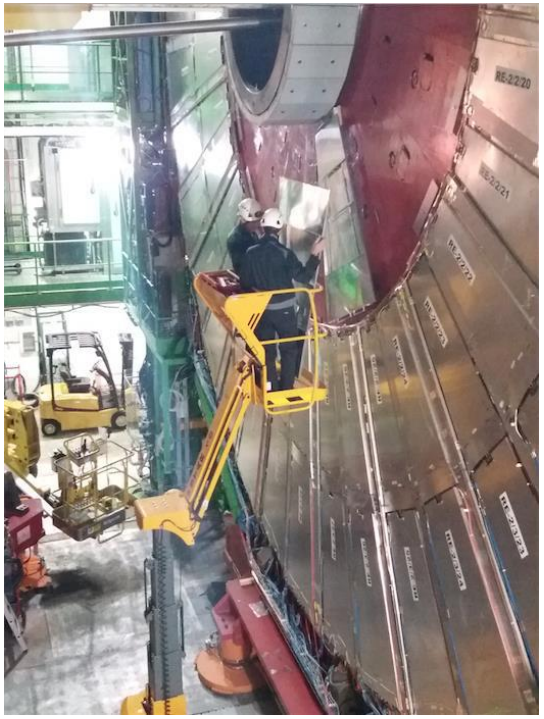


# R&D and Design Evolution

*See Marcus's talk*

- An intense technical R&D program focusing on completing two main goals prior to the EDR:
  - Thorough validation of the detector design
    - Follow the experience and pay close attention to the lessons of the GE1/1 development and slice test
    - Build validation program around verification of formal requirements, focus on identifying potential issues/concerns and developing solutions early
    - Several non-negligible design improvements since TDR (change control)
  - Validate and freeze interfaces
    - Multi-faceted effort including validation of external mechanical interfaces, interfaces with services, internal interfaces, interfaces with the DAQ electronics
      - Working our electronics interfaces has been a particularly high priority focus due to inherit complexities
  - Closely integrated with the risk management program



# GE2/1 Design Evolution

**CMS GEM Phase2 Upgrade**

**System Design Modification GE21-001** June 21, 2018

This document describes the details of a set of related modifications introduced in the design of the CMS GE2/1 detector system compared to the previous version of the system design.

Update description document

**GE2/1 Power: LV System Updated Design Cost Basis of Estimate**

GE2/1 Low Voltage power system serves GE2/1 chambers electronics providing four power channels per chamber. The overall number of channels in the system is therefore 288

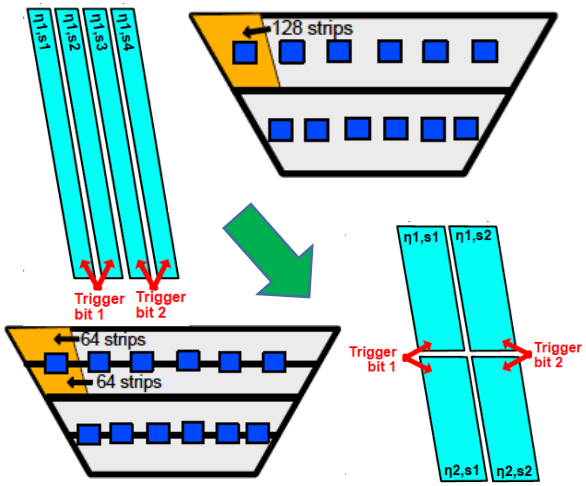
Update Base of Estimate

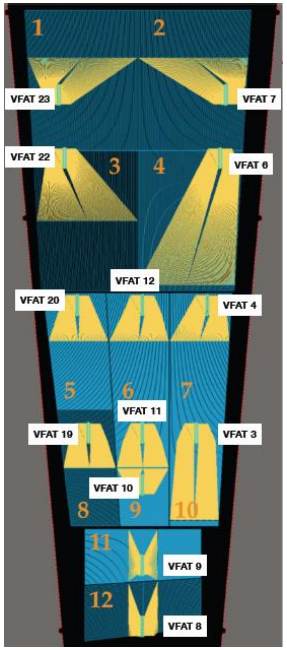
| Expand CORE / Merlin Assoc. | | | | Cost Item Name | KCHF (2017) | Standard Component ID | Expand CORE Calculation |
|---|---|---|---|---|---|---|---|
| CORE CBS Number | Merlin Unique ID | Associated Merlin # | Merlin WBS Number | | | | Unit Description |
| | | | 2.5.2 | GE2/1 Detector System: TOTAL | 4166.907 | | |
| 2.5.2 | 6wbur7d9Soi4Ux488CxkpA | 1.019 | 2.5.2.1 | GE2/1 Detectors | 1606.01 | | |
| 2.5.2.1 | 3B2yp_zQT3CxAnCaDlNYyQ | 1.218 | 2.5.2.1.1 | GE2/1 Detector Components & Assembly | 1547.68 | | |
| 2.5.2.1.1 | eVJ1Rl4NR5ygKofvk42A1A | 1.219 | 2.5.2.1.1.1 | Readout PCB Boards | 168.46 | | Set of Readout PCBs per chamber |
| 2.5.2.1.1.1 | Sp6iJY52R6Wlo6lLBmHqrg | 1.22 | 2.5.2.1.1.2 | Drift PCB Boards | 124.03 | | Set of Drift PCBs per chamber |
| 2.5.2.1.1.2 | 0SW7zggpThOzsGcEokvwaA | 1.225 | 2.5.2.1.1.3 | GEM Foil Kits | 799.20 | | Set of GEM foils per chamber |
| 2.5.2.1.1.3 | gUGv8mobQSKaz8t3X4MUcA | 1.229 | | | | | |

Update costbook

# Change-GE21-001-A: Strip Layout

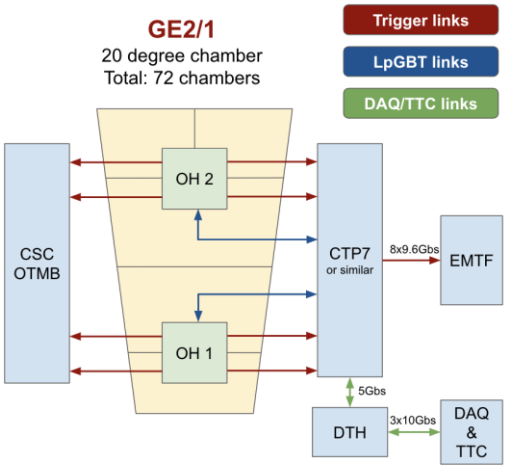
- Measurements in the Spring of 2018 have shown higher than desired S/N
  - GE21 strips are substantially longer than GE11
  - Has been a tracked risk for a while
- Design modifications to the Readout Board:
  - Split strips and change pairing for Level-1 trigger to reduce capacitance thus lowering noise
  - Preserves Level-1 trigger granularity (trigger strips are pairs of strips)
- Actual measurements of S/N with the new layout are in progress
  - A special ROB-0B GE11-size board manufactured and is being tested
  - ROB-1A prototypes using new schema sent for production in July, will be arriving soon
  - ROB-2 (final boards for EDR) to be launched shortly following testing of ROB-1A and ROB-0B
- Cost: no impact
- Schedule: has been fit into prototyping stages of the existing schedule

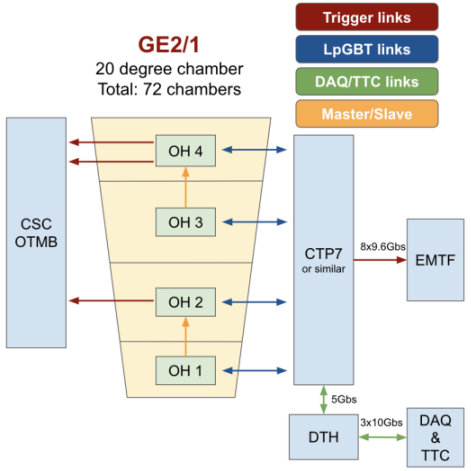


# Change-GE21-001-B: 2->4 OHs

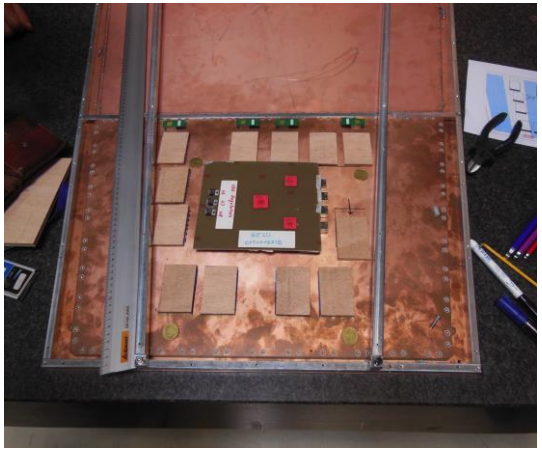
- Motivation:
  - Avoid potential mechanical stress issues (learnt from recent GE11 experience)
  - Grounding/noise concerns to avoid introducing ground loops
  - Reduce schedule risks (less dependences, e.g. don't need to have two modules to test optohybrids)
  - Reduce impact of losing one OH (twice smaller area affected)
- Design modifications:
  - Switch from using one OH per 2 adjacent modules to one OH per module
  - Can use inexpensive FPGAs as each OH handles less VFAT3 FE ASICs (12 instead of 24)
  - Consolidate trigger and data fiber paths, trigger will now use rad hard links
- Current developments – full design cycle complete:
  - New OHs: just arrived from the vendor, testing started
  - ROBs: all 4 types in manufacturing
  - GEBs: smallest module (highest density and complexity) in manufacturing, others will follow shortly
- Cost Impact: reduction by CHF 12k
- Schedule impact:
  - Direct: 4 months delay (electronics design completion milestone slipped from June 1 to the end of September)
  - Ultimate: mitigation to recover by EDR (March 12, 2019)

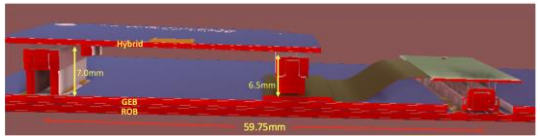


# Change-GE21-001-C: Plug-In Cards

- VFAT3 ASIC chips will be placed on special plug-in cards that connect to GEBs instead of direct soldering
  - Not critical for GE21 as geometrical constraints are not a limiting factor
- Motivation:
  - Schedule risks mitigation: allows parallel development of electronics and FE chip package as new electronics designs can be tested with existing GE11 hybrids, more time to allow full testing of the electronics until the arrival of packaged VFAT3 chips, less dependence on delays with packaged chips arrival, shorten schedule by removing R&D on soldering many chips on a thin large GEB board and vendor qualification
  - Reduce technical risks associated with potentially low yield for GEBs with many soldered ASICs, simplifies long term maintenance (easy to remove and replace)
  - Addresses export control issues (allows separating steps involving export controlled elements in manufacturing)

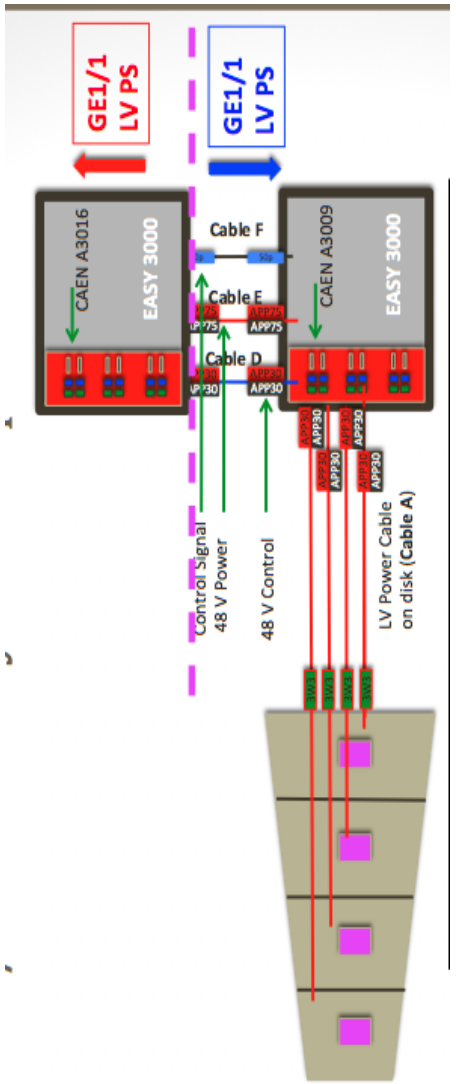





- Design modifications:
  - New small PCBs holding VFAT3s, plug into the GEB boards and connect to the ROB via a flexPCB
- Current developments:
  - Awaiting arrival of Gen-1 electronics prototypes (plug-in cards are not used in Gen-1 prototypes, instead we use GE11 hybrids), will launch production of flexPCBs and plugInCards with Gen-2 prototypes
- Cost Impact: increase by CHF 102k
- Schedule impact:
  - Direct: 4 month delay to complete the design, which shifted the corresponding milestone from June 1 to the end of September (in reality, opportunistic in the shadow of the 2->4 OH changes)

# Change-GE21-001-D: Power System

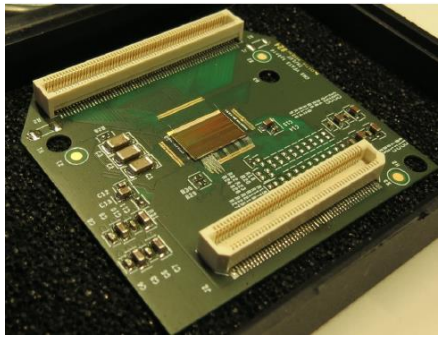
- Motivation:
  - Matching changes for Change-GE21-001-B to allow independent powering of Ohs
  - Technical risks mitigation reducing potential for elevated noise due to ground loops by disconnecting GEBs in different modules
- Design modifications:
  - Change layout to add an extra mainframe, switch to a different type of LV power supply boards (less power, more channels), updated cable layout
- Current developments:
  - All required new components identified, changes are straightforward
  - On-disk elements design reviewed in CMS PRR over the summer
- Cost Impact: reduction by CHF 6.8k
- Schedule impact:
  - No impact



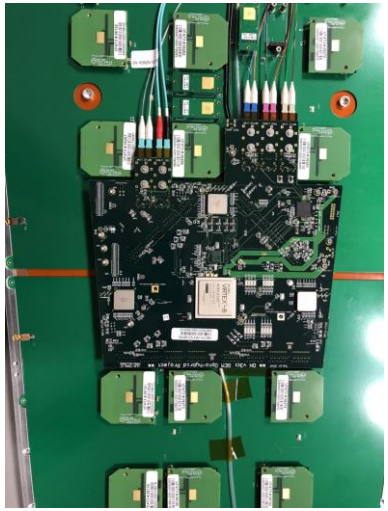
# Lessons learned from GE1/1

- Substantial design modifications relative to the conceptual (TDR) design
  - A number of them driven by the GE1/1 experiences

➢ In GE1/1, VFAT3 die bonded on hybrid:

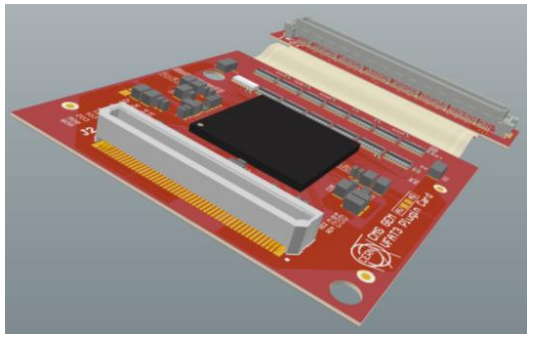


GE1/1 hybrid:
- VFAT3 dies assembled on a small (~4.5 x 4.5 cm$^2$ rigid PCB)
- PCB difficult to manufacture and to bond, because of the small bond pitch (60 um)

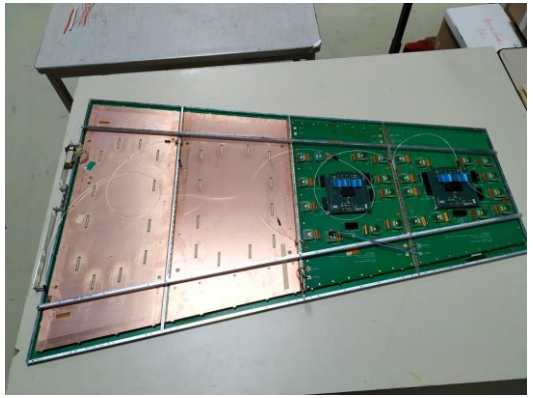


GE1/1:
- Optohybrid connected to two independent GEB half-boards
- Increased potential for mechanical stress
- Evolved powering schema and grounding

➢ In GE2/1, a packaged VFAT3 on a Rigid+Flex PCB (PlugIn card):



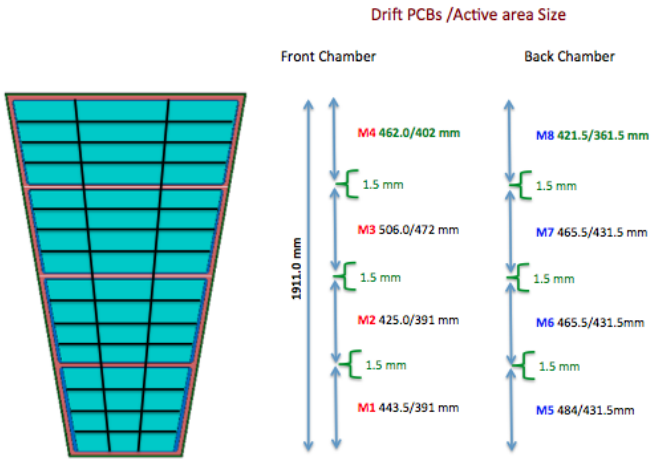
The flex part absorbs residual misalignment of GEB vs ROB
- Rigid part is also hosting VFAT3 input protection circuit

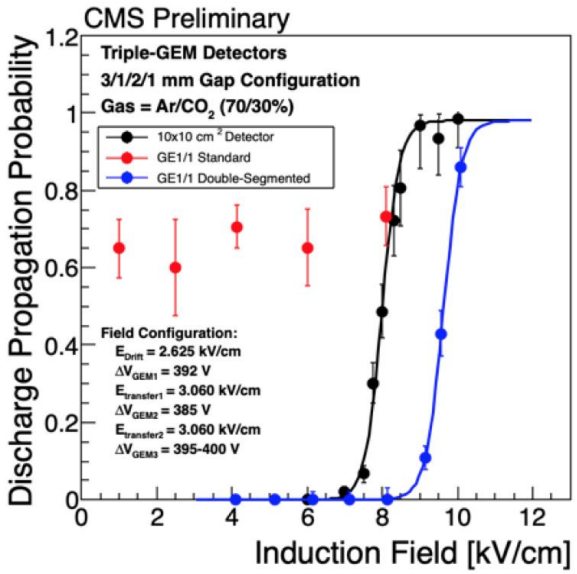


GE2/1:
- Each module has its own OH
- No potential for mechanical stresses from misalignments
- Independent powering, separate grounds
- Small lower power FPGA (Artix-7)

# Change GE21-002

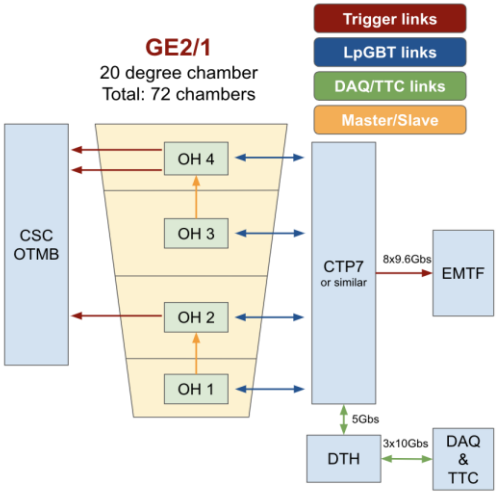
- Rationale: a mechanical conflict discovered of the GE21 chamber in the TDR design with the elements of the RPC system
  - Triggered expedited re-design of modules M4 and M8 mechanics and building new prototypes
- A second key change:
  - Enhanced segmentation of GEM foils to reduce the energy released in discharges
    - Further increases safety margin in addition to other system modifications to increase resistance to effects of discharges
- Cost impact insignificant

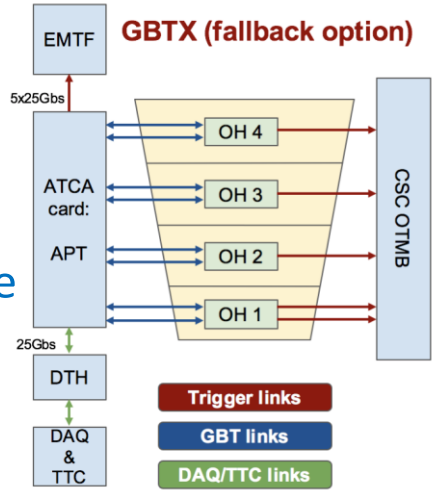


# Change GE21-003

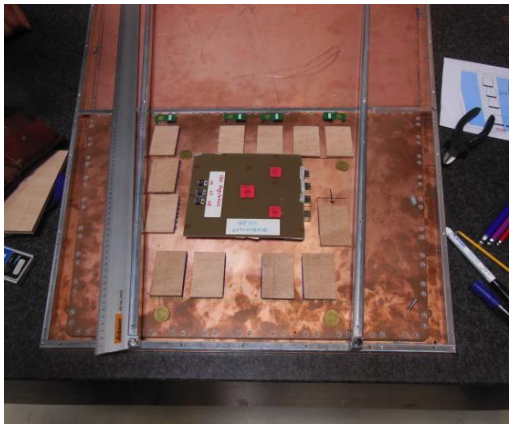
- Rationale: further delays of the LpGBT chip development
  - Triggered re-design of the final system to use existing Versatile Link (VL) chipset instead of VL+
    - No impact on physics performance, just more links to compensate slower link speed
    - Links optimization (trigger links on rad hard path now)
    - Increased backend system size without changes to architecture of baseline processor board
- Core cost increase around 200k CHF
  - Additional backend boards and optical fibers
  - The reality is that GBTX is more cost efficient once labor costs included (these elements are in the US scope where labor is part of the project cost)
- Avoids delays as current electronics prototypes are very similar to the new baseline
  - Intentional as we were planning that this risk may realize
- Avoids pushing GE21 schedule to overlap with the ME0 schedule
  - This has been a major concern for the GEM upgrade coordination team

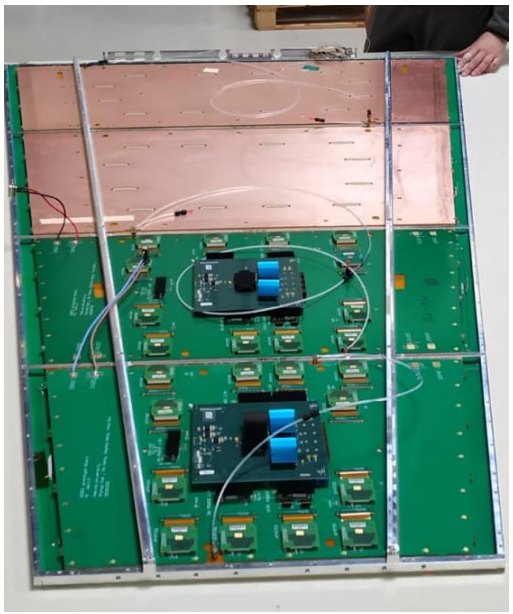


# GE2/1 DAQ/Electronics R&D

- One of the goals of electronics R&D has been to reliably freeze all chamber-electronics interfaces early
  - Accelerate electronics development, heavy focus on early design integration to minimize mistakes
  - Allow ample time for electronics integration and studies of the performance (noise levels!)
- Current status:
  - Fully functional system on first trial with only a few trivial to fix issues related to optimization of component placement
  - Mature near-final prototypes for the OH and GEBs, a bridging prototype of FlexPCB in order to use existing GE1/1 VFAT3 hybrid being replaced with an actual plugin-card
    - Packaged prototype chips to arrive in the Fall, lots of logistics work to put a very well thought out contract for chip production
  - Extensive testing at 904, the test stand bow includes chamber and the electronics
    - Noise measured well below 1 fC – excellent and well within specs
- Conclusions:
  - Achieved mature level of understanding of the electronics design
  - Interfaces frozen: remaining electronics developments are self-contained and do not affect chamber design
    - The only exception is the cooling circle that we want to separate from this review

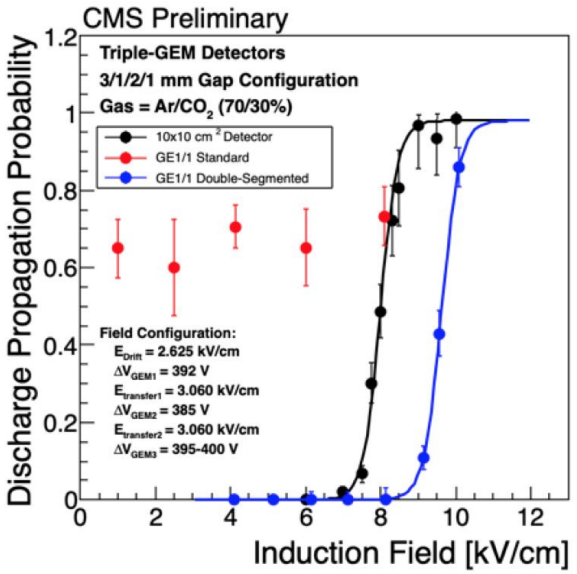


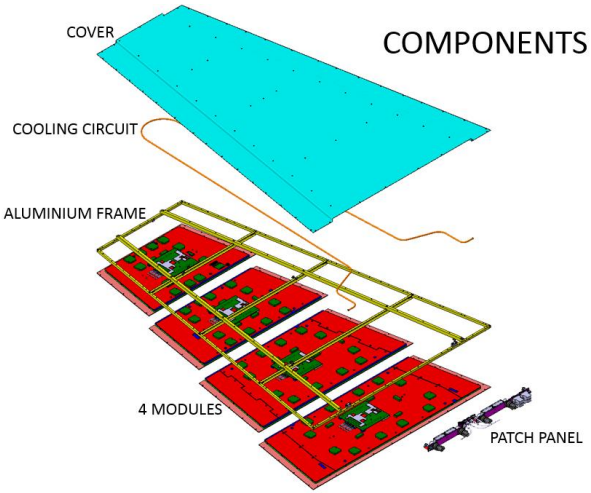


# GE2/1 Chamber Design Maturity

*See Marcus's talk*

- Chamber design development work flow:
  - Establish a clear set of performance and operational requirements, track internal and external interfaces and external constraints
  - Systematically validate each requirement through a dedicated test or tests yielding either a confirmation of the technical solutions or a design revision, systematically validate each interface via a dedicated test or other appropriate verification methods
    - Including the GE1/1 experience, and the slice test studies
- Facilitate transparent development of interface areas
  - The Triad Task Force working on the ROB-flexPCB-GEB interface bringing people from the detector and electronics communities
  - Formal internal reviews of all designs, which required sign-offs by the designers of the elements that have a common interface with the the design under review
  - Integrate with the risk management program



# R&D Steps to Completion

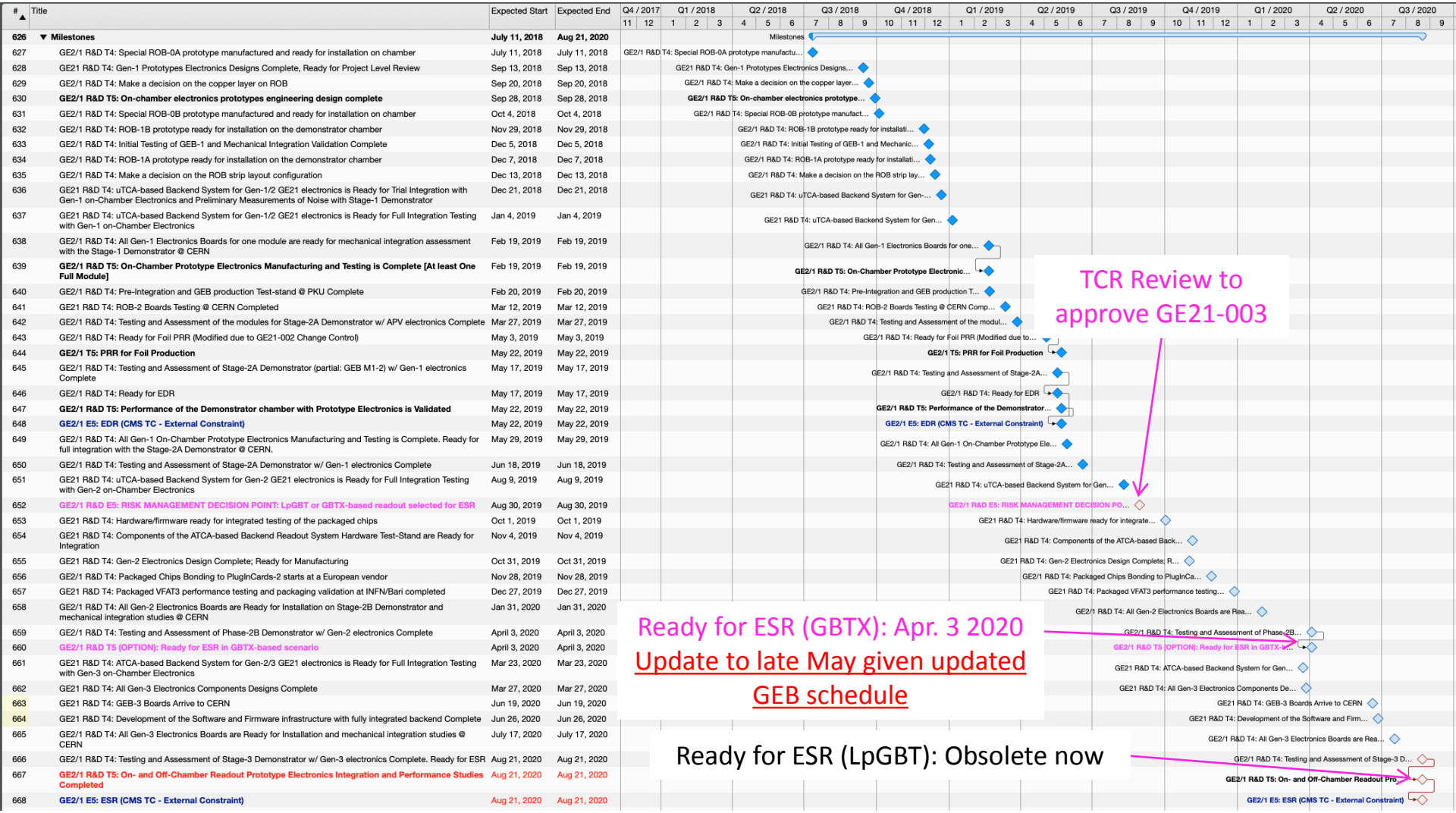
- Electronics (ESR in late May 2020):
  - Complete GEB boards M6-M8
    - Drives critical path for the ESR readiness, risks moderate, it just takes time
  - Minor adjustments and optimization of Optohybrid and select GEB boards to correct small mechanical issues
  - Validate packaged VFAT3 chips
    - Very close to critical path, may well get onto critical path if further delays
  - Optimize chip protection and manufacture PlugIn-Cards
    - Related to the above
  - Integrate and test, including proof of principle with ATCA backend
    - Lower risk, but potential for delays as the likelihood that at least one of over a dozen components would need another iteration is significant

# Reviews

- Many reviews as the system gets finalized:
  - GEM Foils review to release design files and start production at Mecaro - Friday afternoon session
  - GEB M6-M7-M8: need to finalize several rounds of reviewing the prototypes boards design to send them into production – this Friday afternoon session
    - Been missing critical information and input from GEM mechanics/engineering team
  - VFAT3 packaged chip design review – next week
    - Awaiting simulation results from the vendor
  - Readout Board design review – next week
    - Finalize the decision on the copper layer based on all available information, essential to allow start of pre-series production in India
  - PlugIn-Cards review – upcoming, has dependencies:
    - Requires final VFAT3 package design
    - Requires a decision on the optimal spark protection – electronics experts "camp" planned in around middle of November
  - ATCA backend – a full test-stand deployment planned for late Fall'19
    - Surprises very unlikely as it is a generic plug-n-play optical backend; we are not relying on any "high tech" functionality of those boards
- Coordinated by Kevin Black, the GEM upgrades reviews coordinator
  - Became a full time job, we are lucky we have Kevin's help
  - Critical element in risk mitigation towards the success of the project

# Electronics R&D Schedule

- The “waterfall” plot for the updated R&D schedule




| # | Title | Expected Start | Expected End |
|---|---|---|---|
| 626 | **Milestones** | **July 11, 2018** | **Aug 21, 2020** |
| 627 | GE2/1 R&D T4: Special ROB-0A prototype manufactured and ready for installation on chamber | July 11, 2018 | July 11, 2018 |
| 628 | GE21 R&D T4: Gen-1 Prototypes Electronics Designs Complete, Ready for Project Level Review | Sep 13, 2018 | Sep 13, 2018 |
| 629 | GE2/1 R&D T4: Make a decision on the copper layer on ROB | Sep 20, 2018 | Sep 20, 2018 |
| 630 | **GE2/1 R&D T5: On-chamber electronics prototypes engineering design complete** | Sep 28, 2018 | Sep 28, 2018 |
| 631 | GE2/1 R&D T4: Special ROB-0B prototype manufactured and ready for installation on chamber | Oct 4, 2018 | Oct 4, 2018 |
| 632 | GE2/1 R&D T4: ROB-1B prototype ready for installation on the demonstrator chamber | Nov 29, 2018 | Nov 29, 2018 |
| 633 | GE2/1 R&D T4: Initial Testing of GEB-1 and Mechanical Integration Validation Complete | Dec 5, 2018 | Dec 5, 2018 |
| 634 | GE2/1 R&D T4: ROB-1A prototype ready for installation on the demonstrator chamber | Dec 7, 2018 | Dec 7, 2018 |
| 635 | GE2/1 R&D T4: Make a decision on the ROB strip layout configuration | Dec 13, 2018 | Dec 13, 2018 |
| 636 | GE21 R&D T4: uTCA-based Backend System for Gen-1/2 GE21 electronics is Ready for Trial Integration with Gen-1 on-Chamber Electronics and Preliminary Measurements of Noise with Stage-1 Demonstrator | Dec 21, 2018 | Dec 21, 2018 |
| 637 | GE21 R&D T4: uTCA-based Backend System for Gen-1/2 GE21 electronics is Ready for Full Integration Testing with Gen-1 on-Chamber Electronics | Jan 4, 2019 | Jan 4, 2019 |
| 638 | GE2/1 R&D T4: All Gen-1 Electronics Boards for one module are ready for mechanical integration assessment with the Stage-1 Demonstrator @ CERN | Feb 19, 2019 | Feb 19, 2019 |
| 639 | **GE2/1 R&D T5: On-Chamber Prototype Electronics Manufacturing and Testing is Complete [At least One Full Module]** | Feb 19, 2019 | Feb 19, 2019 |
| 640 | GE2/1 R&D T4: Pre-Integration and GEB production Test-stand @ PKU Complete | Feb 20, 2019 | Feb 20, 2019 |
| 641 | GE21 R&D T4: ROB-2 Boards Testing @ CERN Completed | Mar 12, 2019 | Mar 12, 2019 |
| 642 | GE2/1 R&D T4: Testing and Assessment of the modules for Stage-2A Demonstrator w/ APV electronics Complete | Mar 27, 2019 | Mar 27, 2019 |
| 643 | GE2/1 R&D T4: Ready for Foil PRR (Modified due to GE21-002 Change Control) | May 3, 2019 | May 3, 2019 |
| 644 | **GE2/1 T5: PRR for Foil Production** | May 22, 2019 | May 22, 2019 |
| 645 | GE2/1 R&D T4: Testing and Assessment of Stage-2A Demonstrator (partial: GEB M1-2) w/ Gen-1 electronics Complete | May 17, 2019 | May 17, 2019 |
| 646 | GE2/1 R&D T4: Ready for EDR | May 17, 2019 | May 17, 2019 |
| 647 | **GE2/1 R&D T5: Performance of the Demonstrator chamber with Prototype Electronics is Validated** | May 22, 2019 | May 22, 2019 |
| 648 | **GE2/1 E5: EDR (CMS TC - External Constraint)** | May 22, 2019 | May 22, 2019 |
| 649 | GE2/1 R&D T4: All Gen-1 On-Chamber Prototype Electronics Manufacturing and Testing is Complete. Ready for full integration with the Stage-2A Demonstrator @ CERN. | May 29, 2019 | May 29, 2019 |
| 650 | GE2/1 R&D T4: Testing and Assessment of Stage-2A Demonstrator w/ Gen-1 electronics Complete | Jun 18, 2019 | Jun 18, 2019 |
| 651 | GE21 R&D T4: uTCA-based Backend System for Gen-2 GE21 electronics is Ready for Full Integration Testing with Gen-2 on-Chamber Electronics | Aug 9, 2019 | Aug 9, 2019 |
| 652 | **GE2/1 R&D E5: RISK MANAGEMENT DECISION POINT: LpGBT or GBTX-based readout selected for ESR** | Aug 30, 2019 | Aug 30, 2019 |
| 653 | GE21 R&D T4: Hardware/firmware ready for integrated testing of the packaged chips | Oct 1, 2019 | Oct 1, 2019 |
| 654 | GE21 R&D T4: Components of the ATCA-based Backend Readout System Hardware Test-Stand are Ready for Integration | Nov 4, 2019 | Nov 4, 2019 |
| 655 | GE21 R&D T4: Gen-2 Electronics Design Complete; Ready for Manufacturing | Oct 31, 2019 | Oct 31, 2019 |
| 656 | GE2/1 R&D T4: Packaged Chips Bonding to PlugInCards-2 starts at a European vendor | Nov 28, 2019 | Nov 28, 2019 |
| 657 | GE21 R&D T4: Packaged VFAT3 performance testing and packaging validation at INFN/Bari completed | Dec 27, 2019 | Dec 27, 2019 |
| 658 | GE2/1 R&D T4: All Gen-2 Electronics Boards are Ready for Installation on Stage-2B Demonstrator and mechanical integration studies @ CERN | Jan 31, 2020 | Jan 31, 2020 |
| 659 | GE2/1 R&D T4: Testing and Assessment of Phase-2B Demonstrator w/ Gen-2 electronics Complete | April 3, 2020 | April 3, 2020 |
| 660 | **GE2/1 R&D T5 (OPTION): Ready for ESR in GBTX-based scenario** | April 3, 2020 | April 3, 2020 |
| 661 | GE21 R&D T4: ATCA-based Backend System for Gen-2/3 GE21 electronics is Ready for Full Integration Testing with Gen-3 on-Chamber Electronics | Mar 23, 2020 | Mar 23, 2020 |
| 662 | GE21 R&D T4: All Gen-3 Electronics Components Designs Complete | Mar 27, 2020 | Mar 27, 2020 |
| 663 | GE21 R&D T4: GEB-3 Boards Arrive to CERN | Jun 19, 2020 | Jun 19, 2020 |
| 664 | GE21 R&D T4: Development of the Software and Firmware infrastructure with fully integrated backend Complete | Jun 26, 2020 | Jun 26, 2020 |
| 665 | GE2/1 R&D T4: All Gen-3 Electronics Boards are Ready for Installation and mechanical integration studies @ CERN | July 17, 2020 | July 17, 2020 |
| 666 | GE2/1 R&D T4: Testing and Assessment of Stage-3 Demonstrator w/ Gen-3 electronics Complete. Ready for ESR | Aug 21, 2020 | Aug 21, 2020 |
| 667 | **GE2/1 R&D T5: On- and Off-Chamber Readout Prototype Electronics Integration and Performance Studies Completed** | Aug 21, 2020 | Aug 21, 2020 |
| 668 | **GE2/1 E5: ESR (CMS TC - External Constraint)** | Aug 21, 2020 | Aug 21, 2020 |

# Risk Management Program

- Pro-active risk management program carried throughout the R&D stage will continue into the construction phase
  - Continuously updating risk register, reviewing and analyzing potential new threats, developing mitigation and response strategies
- Detectors: risks significantly reduced relative to the original version of the risk register

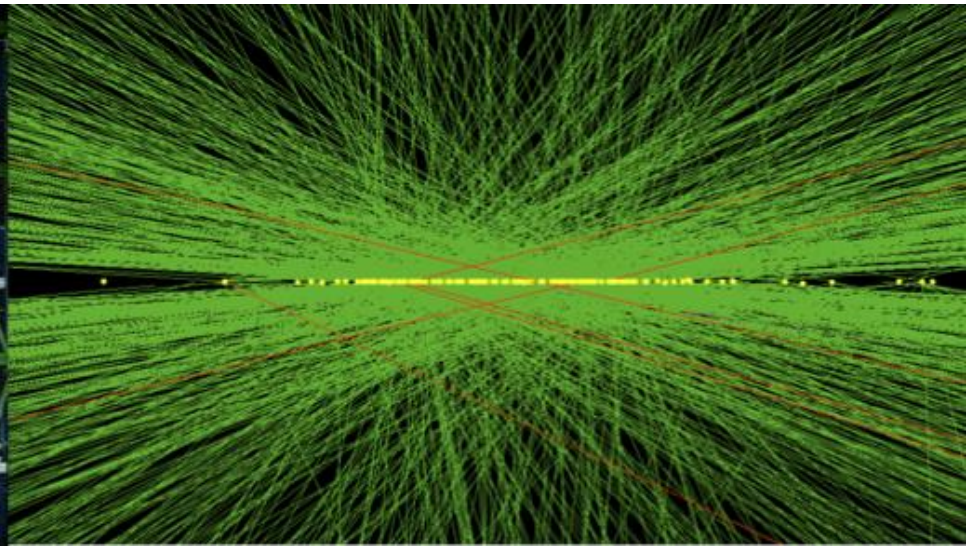
| CORE CBS Number | Merlin WBS Number | Activity | Risk ID | Risk Description | Impact Description | Likelihood (L/M/H) | CORE cost impact (L/M/H) | Schedule Impact (L/M/H) | Mitigation | Action |
|---|---|---|---|---|---|---|---|---|---|---|
| 2.5.2.1 | 2.5.2.1 | GE2/1 Detectors | 4.1 | Sub-standard quality of the GEM foils delivered by external vendors or delays in manufacturing | If quality of GEM foils is inadequate, foils will need to be re-made leading to delays in the schedule and potentially lead to cost increases. If the impact on schedule is severe enough, it can impact readiness of the detector for installation | M | L | M | Mitigation includes (i) putting contracts in place with two vendors to allow adequate floats in the schedule to be able to accommodate potential delays in manifacturing, (i) rigorous quality monitoring process of all ariving foils so any problems are discovered immediately to reduce schedule impact, (iii) schedule monitoring, (iv) adequate floats in the schedule to allow absorbing potential delays, (v) ensuring that contracts with vendors explicitly account for mechanisms to deal with quality problems to minimize impact on the cost incurred by the project. | Work with the vendors to correct the problem and speed up the foil manufacturing schedule, identify additional manpower to increase the number of shifts at module production sites and the chamber assembly facility at CERN to increase the throughput so that delays compared to original schedule are minimized. |
| | | | 4.2 | Delay in detailed designs of 8 different module types | Delay in completion of the detailed engineering drawings/designs can delay the start of production of GEM modules and impact the schedule. | L | L | M | Mitigate via regular monitoring of the progress (biweekly meetings and periodic reviews) to ensure that falling behind schedule is detected early and additional engineering resources can be directed to ensure any delays are remedied or minimized | identify additional resources (expert engineers) to speed up the completion of the designs. Work with the module production sites so that whatever delay remains can be absorbed by increasing the module produciton throughput to minimize impact on the overall schedule. |
| | | | 4.3 | Delay in production of other module and chamber components | If components required for module or chamber construction arrive late, that can potentially delay production of GEM modules. | M | L | M | Place orders early to esnure the schedule impact is minimal should manufcaturing schedule be delayed. Improve accuracy of estimating production yield while working with vendors on R&D and prototyping, work with vendors on streamlining the process to minimize mistakes in production which can lead to delays in shipping final components, monitor production progress with industrial partners very closely. | Work with the vendor to speed up the process. If the delay is signficant, allocate additional resources to use faster shipping options to reduce schedule delay, work on increasing the througput of module production sites, use faster shipping options for shipment of ready modules to CERN. |
| | | | 4.4 | Insufficient module assembly rate at certain production sites | Lower than expected rate of module produciton at one or more pmodule production sites has the potential of delaying completion of GEM modules and the overall schedule of production and manufacturing. | L | L | M | Mitigate by (i) ensuring that the number of production sites and their throughput are sufficient so the schedule can accommodate reasonable delays or lower produciton rate from some of the production sites, (ii) ensuring sufficient floats in the schedule so the impact on chamber assembly and detector installation is minimal should this risk realize, (iii) plan so that should there be a necessity the production rate at other assembly sites can be increaased by redirecting manpower and going to a larger number of shifts per day to compensate for reduced throughput at other sites, (iv) rigorous monitoring of production sites preparation and certification and later regular monitoing of the production schedule so that any delays are detected early and risks can be responded to minimizing the impact. | Allocate additional resources to increase the number of shifts at one or more module production sites and the chamber assembly facility at CERN to increase the throughput so that delays compared to original schedule are minimized. Allocate resources to use faster shipping options to reduce schedule delays. |
| | | | 4.5 | GE1/1 production schedule delays impacting GE2/1 schedule | As GE2/1 production relies on the same resources (manpower, module production sites, chamber assembly sites, storage and cosmis stand facilities at CERN) as GE1/1 production, delays in GE1/1 construction project can reduce the available manpower and access to facilities involved in production of GE2/1 detectors. The risk can realize independently of whether GE1/1 is installed on time and the severity is determined by how much of the delay is accumulated. Up to 6 month delay (max schedule impact associated to this risk ) can be absorbed by the available float in the schedule. | L | L | M | Mitigate by (i) ensuring that the number of production sites and their throughut are sufficient so the schedule can accommodate reasonable delays or lower produciton rate from some of the production sites, (ii) ensuring sufficient floats in the schedule so the impact on chamber assembly and detector installation is minimal should this risk realize, (iii) plan so that should there be a necessity the production rate at other assembly sites can be increaased by redirecting manpower and going to a larger number of shifts per day to compensate for reduced throughput at other sites, (iv) rigorous monitoring of production sites preparation and certification and later regular monitoing of the production schedule so that any delays are detected early and risks can be responded to minimizing the impact. | Identify and allocate resources to speed up the completion of the GE1/1 module production and, if necessary, GE2/1 module production by increasing the number of shifts and/or production lines at the module production sites. |

# Risk Management Program

- Pro-active risk management program carried throughout the R&D stage will continue into the construction phase
  - Continuously updating risk register, reviewing and analyzing potential new threats, developing mitigation and response strategies
- Electronics: risks completely retired (e.g. LpGBT) or significantly reduced relative to the original version of the risk register

| CORE CBS Number | Merlin WBS Number | Activity | Risk ID | Risk Description | Impact Description | Likelihood (L/M/H) | CORE cost impact (L/M/H) | Schedule Impact (L/M/H) | Mitigation | Action |
|---|---|---|---|---|---|---|---|---|---|---|
| 2.5.2.2 | 2.5.2.2 | GE2/1 DAQ System | 4.6 | delay of the design completion for one of the boards (except on-chamber boards) due to unforeseen circumstances, e.g. repitative failure of alternate components to pass radiation requirements, or due to external factors | Completion of board design leading to board production affecting the schedule and potentially leading to a late delivery of the board. | L | L | L | Monitor design process, perform intermediate internal reviews in addition to formal reviews, test most of key features with early prototypes. | Identify and allocate additional engineering resources to complete the design of the board, and speed up the follow-up steps in the schedule to absorb or minimize the delay. If appropriate, switch to faster board manufacturing options (in all cases, default options aim to minimize costs by using slower manufacturing options) and use faster shipment options |
| | | | 4.7 | Problem in design or production yield of GE21 on-chamber electronics boards | If a problem occurs in design or production, then the schedule can be significantly delayed, which in the worst case can result in a late delivery to CMS, which in turn will not allow CMS to install GE21 chambers early and require re-scheduling its installation. The severity depends on the lateness of the time a problem is dicovered, so while the schedule impact would increase as afunction of time, the likelihood of such event decreases if appropriate mitigation measures are in place. | L | M | H | Multiple rounds of prototyping and prototype testing before completing the design, internal reviewing to ensure early detection of problems, careful schedule monitoring. These steps help ensure that any problems are discovered early so the impact on the schedule can be minimized with appropriate response. For potential problems in manufacturing, mitigation focuses on vendor qualification in preceeding steps, development of advanced and detailed QC procedures for testing production boards well ahead of time, manufacturing several early pre-series boards ahead of giving green light for full production board, extensive testing of production boards. | Identify and allocate additional resources to complete the design, work with the vendor to switch to faster board manufacturing option (in all cases, default options aim to minimize costs by using slower manufacturing options), switch to faster shipment options, allocate additional resources for follow-up steps in board testing and certification to minimize impact on the schedule |
| | | | 4.8 | lpGBT chip delay impact on GE2/1 construction | The risk addresses the situation, in which the LpGBT chip is not available in time for the GE2/1 Optohybrid board final design validation and start of production. GE2/1 is one of earliest sub-projects of the forward muon sub-projects with the target installation prior to LS3. Because of its early installation, the GE2/1 detector assembly takes place substantially earlier than most Phase-2 CMS Upgrade projects, and with the updates on the LpGBT schedule reported, the expected delivery date for LpGBT is getting closer to the time when these chips would be necessary for the OH board assembly that preceeds the full chamber assembly. | H | M | L | Mitigation strategy inclides (i) closely monitoring the status of the LpGBT chip development by CERN so any delays can be detected early, (ii) designing the Optohybrid board so that the GBT chip and related components (SCA chip and optical transimtters/receivers) are a single block (or a mezzanine card), which can be replaced with the existing GBTX-based components if the LpGBT chip is not delivered on time. | Switch the GE2/1 OH design to the variant relying on an existing GBTX chip, identify and allocate resources to complete the new design, and acquire aditional fibers and backend boards that would be required in this case. |
| | | | 4.9 | VFAT3 ASIC performance significantly substandard due to mismatch in capacitance wth the detector | The risk addresses the situation, in which the VFAT3 chip's operational characteristics (noise) are found to be substantially substandard given mismatch in strip capacitance. The VFAT3 chip being produced and qualified for GE11 has been optimized for the GE11 detector's capacitances, which are not the same as those of GE21 detector. If the difference in capacitane turns out to be sufficient to impact chip performance in a substantive way, that would require a partial design update to the chip, submission for an engineering run yielding increased cost and additional testing that would impact the schedule | L | L | H | Mitigation strategy inclides early testing the VFAT3 chips with the early prototype detectors to measure noise levels and evaluate operational characteristics of the chip for GE2/1 as early as possible so that this risk can be either retired or addressed early to reduce or eliminate impact on the schedule. | Perform design adjustments for the chip, identify and allocate resources for an additional engineering run to produce the variant of the ASIC with modified capacitance (baseline plan assumes production of additional chips in the default design of the chip without an enginering run) and follow up testing of the modified ASIC. |
| | | | 4.10 | Loss of key engineer on the Project | Completion of the electronics design, testing of the electronics, completion of the design of firmware or software components, completion of electronics integration activities | L | L | M | Ensure that all key roles have several knowledgable people so should the departure of one of the engineers be unexpected, other engineers can continue development of the affected project or provide assistance to the replacement engineer to minimize the time to take over the affected part of the project. | Depending on how late in the project the risk realizes, either re-assign duties of the existing engineers to ensure the tasks led by the departing engineer are continues or identify and allocate additional engineering resources, including potentually hiring a new engineer. GEM PM will bring any critical lack of personnel to the attention of the Muon System manager. |

# Production Planning



# GE2/1 Foil Production Planning

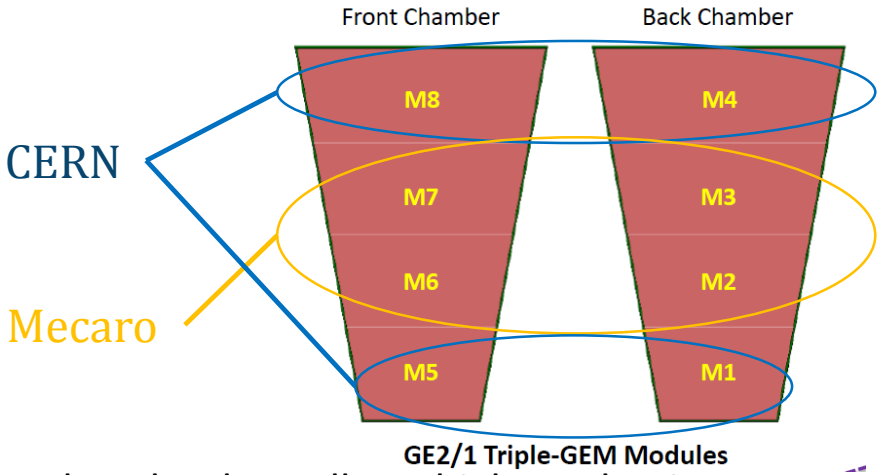
*See Inseok's talk*

- GE2/1 project GEM foils:
  - 114 (108=18*2*3+6 spares) foils per module type M1-M8
- Two vendors:
  - CERN: M1, M4, M5 and M8
    - Well calibrated process flow, single mask technology

Ongoing

  - Mecaro (Korea): M2, M3, M6 and M7
    - Partnership with industry, double mask technology allows high production yields, extensive R&D

Soon




- Schedule parameters: 2 vendors w/ production rate of 18 foils/month each, start date of September 12, 2019 (procurement and setup starts after EDR)
  - Updated projections: 32 foils/month at CERN, Mecaro projection is that it can achieve as many as 40 foils/month
  - With 18 foils/month per site, foils arrival slightly outpaces module production
- Risk management:
  - Schedule risk analysis: no impact on the "short float" for up to a 5 months delay in production, the "longer float" gets reduced to 14 weeks by a 4 months delay
  - Integrated risk (in risk register) covers a range of possible scenarios from small hickups that are fairly likely to extremely unlikely catastrophic scenarios
  - Risk responses range proportionally to the impact: from "do nothing" to revert full production to CERN

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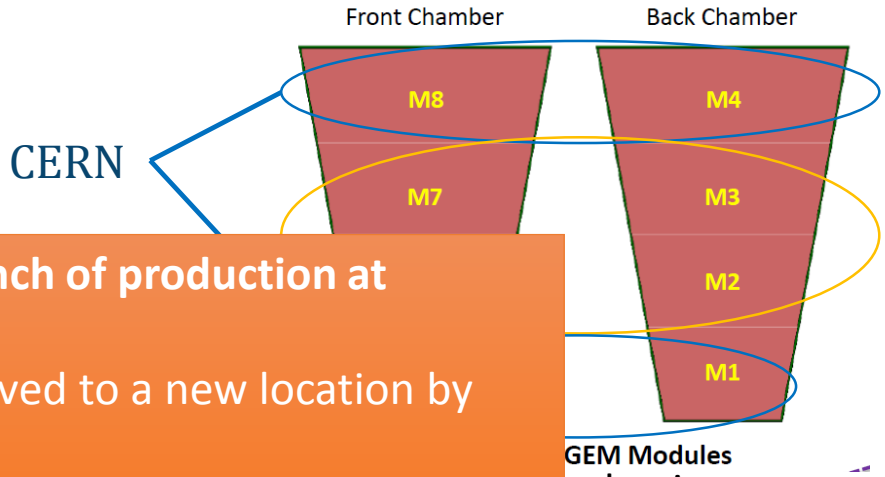



**A first hiccup – delay of the launch of production at Mecaro:**

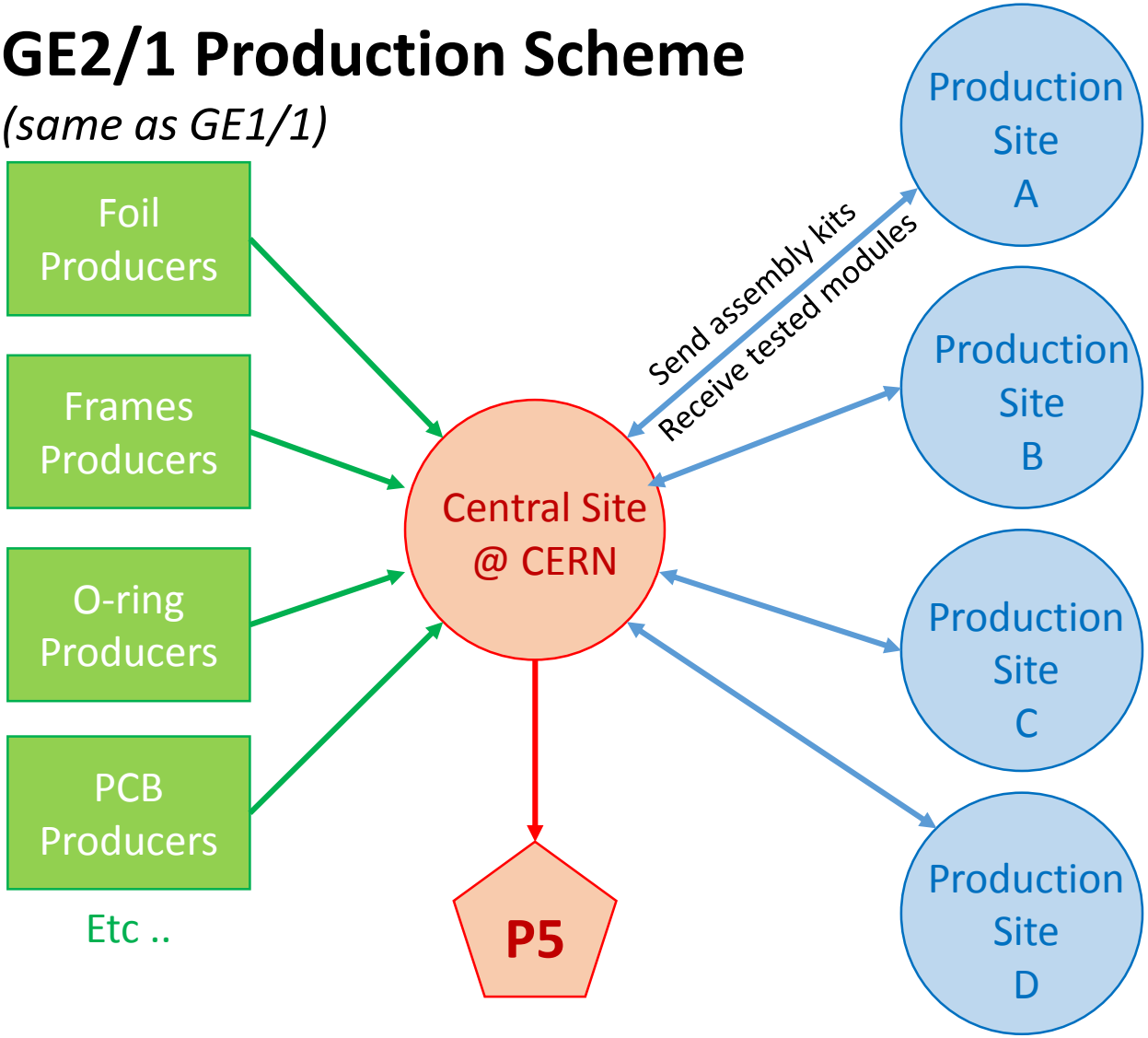
- GEM production facilities moved to a new location by the vendor
- Some adjustments to vendor's planning due to another order of GEM foils from a non-CMS project
- Not on critical path yet, we expect to recover
  - We also expect that faster foil production will allow mitigating this delay

# GE2/1 Module/Chamber Production

*See Jeremie's talk*

## GE2/1 Production Scheme

*(same as GE1/1)*

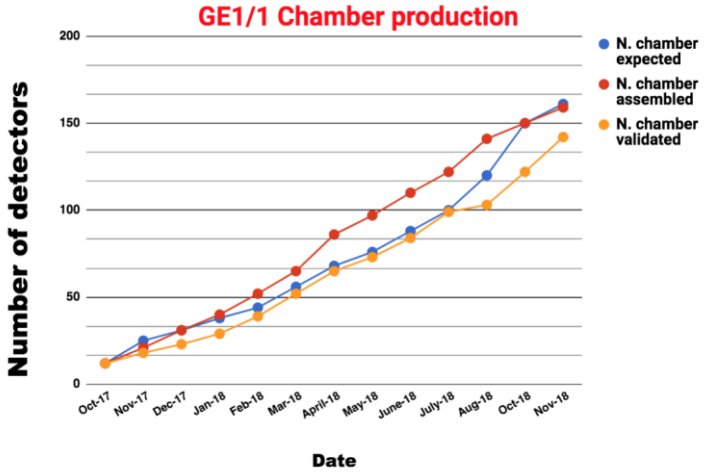



- **Central Site (at CERN)**
  - Material inspection
  - Pre-assembly work
  - Assembly kit preparation
  - Shipment

  + also a production site
- **External Production Sites**
  - Module assembly
  - QC2-QC5 tests
  - Data Base updates
- **Production community (all)**
  - Review of the QC data
  - Validation of modules
  - Participate to central site activities

# GE2/1 Production Readiness

- Primary focus as module production sets the overall schedule pace
  - Dominates critical path in the second half od the project
  - Major handle for schedule risk mitigation: delays elsewhere can be compensated if we increase the pace of module production
- An experienced management team in place with a strong record of delivering on schedule
  - Excellent technical expertise stemming from GE1/1, detailed QA/QC protocols
  - Well established responsibilities and reporting lines
- GE2/1 master schedule built assuming 4 production lines
  - We know now that we will have at least 7
  - Schedule optimization potential and a major extra resilience against unexpected delays




| Site | Number of Production lines | Certification (participation in GE1/1) | Infrastructure ready and tested | Production rate Max. (day/module) | Comments |
|---|---|---|---|---|---|
| Belgium | 1 | YES | YES | 3 | Produced 30 GE1/1 detectors |
| Germany | 1* | YES | YES | 2 | *QC only (no clean room) Tested 21 GE1/1 det. |
| Italy | 2 | YES | YES | 3.5 per line | Produced 26 GE1/1 detectors |
| India | 2 (+2 under approval) | YES (+2 on-going) | YES (+2 on-going) | 4 per line | Produced 17 GE1/1 detectors |
| Pakistan | 1 | YES | YES | 5 | Produced 13 GE1/1 detectors |
| Sri-Lanka | 1 | YES | YES | 3 | Using CERN infrastructure and tooling |
| China | 1 | On-going | On-going | N-C | New site, QC Jamboree in progress |

# GE2/1 Production Readiness

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  - Dominates critical path in the second half od the project
  - Maj… dela… incr…
- An exper… strong re…
  - Exce… expe… GE1… prot…
  - Well… resp… repo…
- GE2/1 ma… assuming…
  - We … have at least 7
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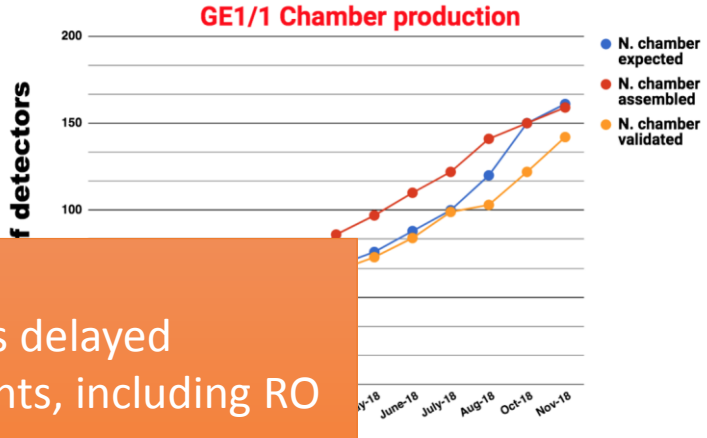


**Incurred a substantial delay already:**

- Funding availability problem in India has delayed manufacturing of key module components, including RO and Drift PCBs
- Indian colleagues working on securing funds to allow pre-series production of these components
  - Will allow to get production sites going
- We expect to mitigate these delays with faster module production
  - Capabilities have been demonstrated with GE11, also additional sites provide an additional boost to the production pace

| | | | | | |
|---|---|---|---|---|---|
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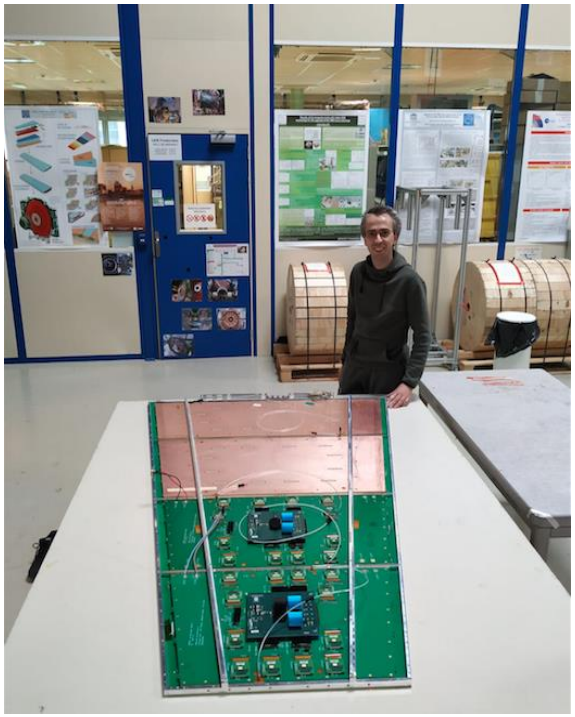
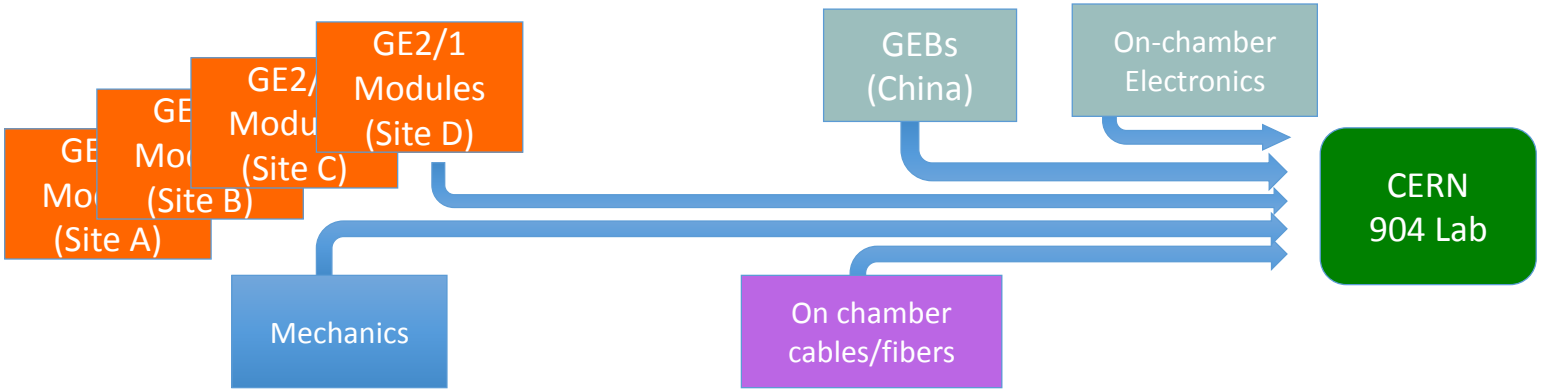
# GE2/1 Chamber Assembly

*See Michele's talk*

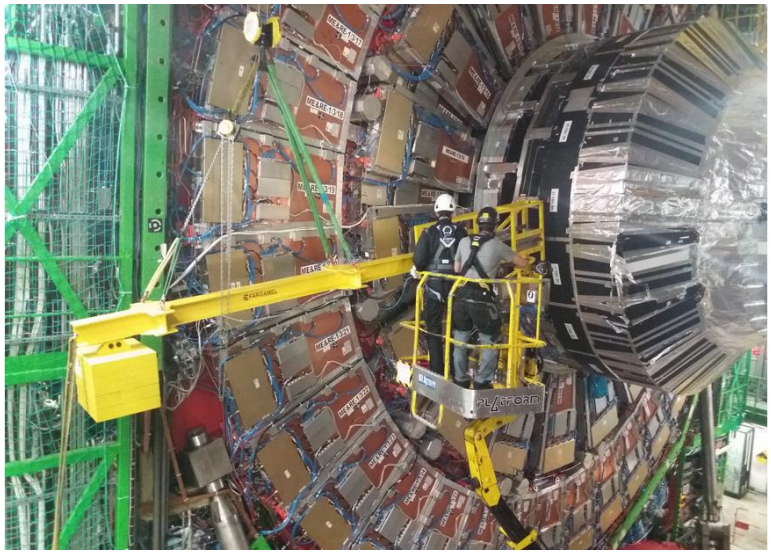
- GE2/1 chamber assembly components:
  - Four triple GEM modules (M1-4 or M5-8)
  - Custom designed mechanics structure
  - On-chamber electronics (GEBs, plug-in cards carrying VFAT3 ASIC, Optohybrid board)
- Technical aspects worked out as part of developing the GE2/1 demonstrator system
  - Two complete and fully validated GE2/1 chambers (w/ analogue electronics used in production testing)
  - Two modules with electronics closely resembling final system
- Logistics follows GE1/1 experience and re-uses the same facilities
  - CERN continues to provide logistical support and assistance, but a much increased role of the GEM participating institutions and increased presence at CERN

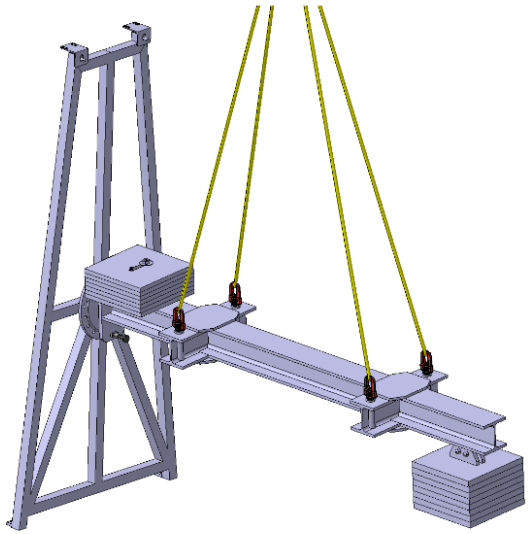




# Installation Planning

- Good understanding of the logistics and the scale of the work stemming from the ongoing GE1/1 efforts
- Special installation tools developed, including a special jig
  - GE1/1 insertion (May.16.2019) gives strong confidence as the GE1/1 jig is a similar (although a more complex) system
- Trial installation of two GE2/1 chambers in May of 2019
  - Primary goal was to validate mechanical interfaces, but also valuable experience





# Summary

- The GE21 project has so far been progressing well
  - Money-wise, 2/3 of the construction funds released by CMS (services and chambers)
- We have been able to anticipate risks and react to them early to prevent significant problems from occurring in the first place
  - A number of design changes improving robustness of the system and avoiding schedule dependences exposing project to schedule risks
- We have done well in the reviews:
  - All major reviews (PRRs, EDR, ECR/TCRs) passed with strong endorsements from the CMS review panels
- Very intense time with several key near term challenges
  - Resolving problems with launching module production
  - Sending foil production at Mecaro into cruising mode
  - Completion of electronics R&D to start electronics construction
  - Some elements of the production plan need better understanding, e.g. mass production logistics for the plug-in cards