ELECTRONICS

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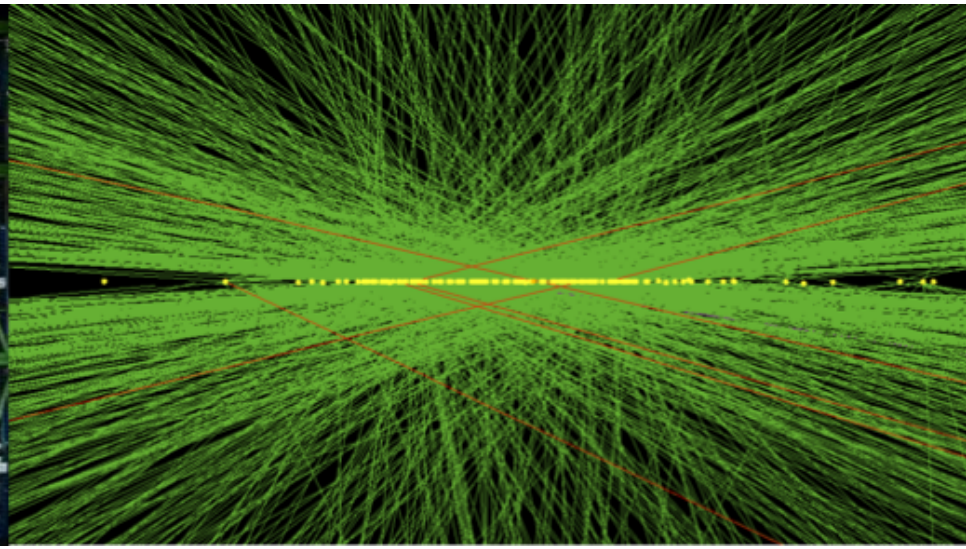
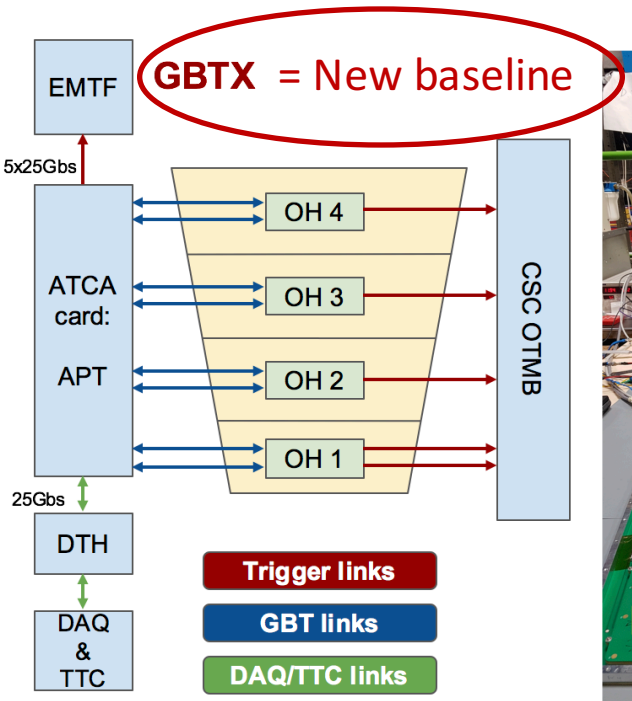
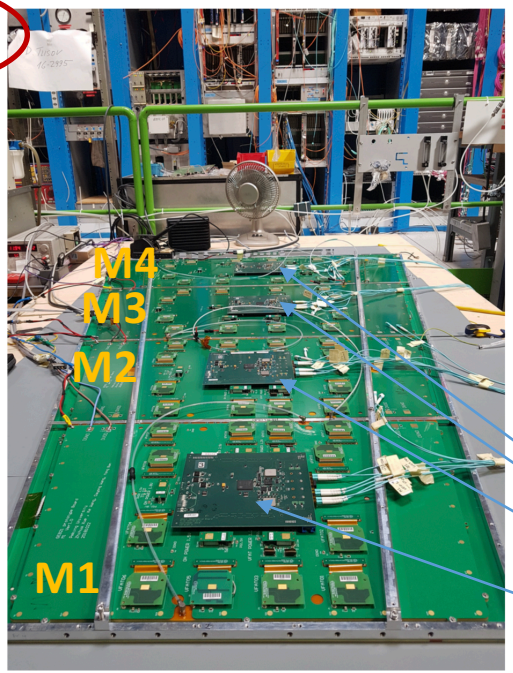
GE2/1 Electronics

October 2nd, 2019

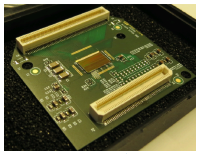


GE2/1 Electronics Overview





Plug-In card:



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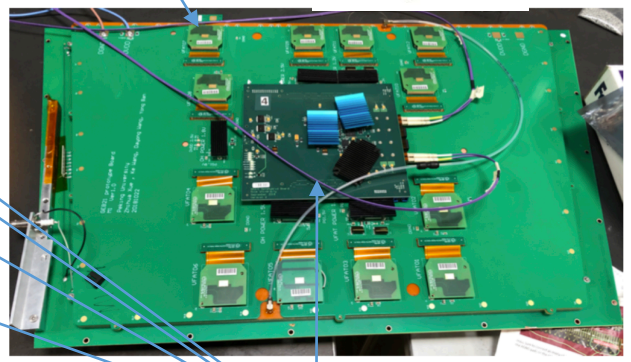
Packaged VFAT3



GBT-based OH

This talk will cover the FE part
See Evaldas' talk on Thursday morning for BE part
See Misha's talk on Friday integration and tests

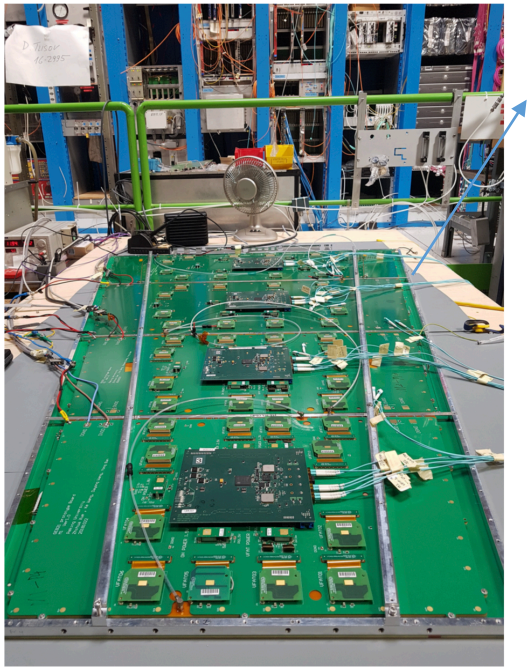
Report from the referees:

- **The change request has been accepted conditionally that all components are available!**
  - Order GBTx AND VTRx ASAP in order to ensure availability.
- For schedule considerations, exploit the new need-by-date August 2023
- Make GEB lpGBT compatible to ensure future upgradability
- Fully exploit any lessons learnt from GE1/1 operation during Run-3 where possible
  - Add a risk in the risk registry that issues during Run-3 with GE1/1 (now similar to GE2/1 also using GBTx), could lead to a re-design of the OH and then potentially with lpGBT.

Reminder: GE2/1 ESR date: May 2020

Current status

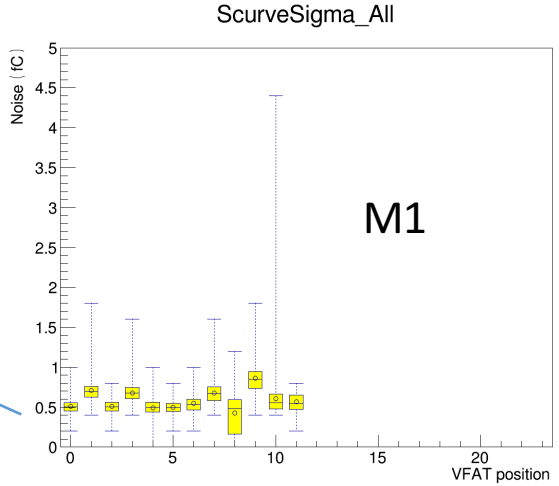
- 6 GEB boards (M1-M5) & OH (GBT-based) designed
  - 1 OH board design fitting 8 different GEB boards
  - M6-M8 GEB designs still under review
  - Shown here, one GE2/1 detector fully equipped with electronics ; still using GE1/1 VFAT3 hybrids



Tests on-going now on M1-M5 modules

Since June, one full GE2/1 detector equipped

- Worked from the 1st attempt
- Powering scheme validated
- Communication w/. all VFATs on all modules
- GBT phase scans
- Routinely performing DAC scans & S-curves
- Preliminary noise measurements
- Now optimizing GNDing



Comparable with GE1/1 noise

Current status

- M1-M5 GEBs produced
- M6-M8 GEB designs in review
- GE2/1-GBT-OH Gen-1 produced
  - OH FPGA irradiated in proton beam well beyond GE2/1 TID
  - All other components selected for their radiation hardness
- Flex PCB adaptor for GE1/1 VFAT3 hybrids validated (precursor of Plug-In)
- VFAT3 package designed, just got back from vendor the substrate design files -> a review is being organized
  - More in Francesco L. talk
- VFAT3 Plug-In card design almost completed
  - Was waiting for freezing of VFAT3 package pinout
  - More in Ali's talk

R&D steps to completion

- M6-M8 GEBs production
- Minor adjustments and optimization to M1-M4 GEBs
  - Powering scheme
  - Addressing scheme (to be compatible with LpGBT)
- OH v2
  - Some modifications needed to embed trigger data into the GBT path
    - A VTTx could be dropped then
    - 1 GBT would run in wide-bus mode (no FEC)
    - Master-Slave interface is reduced from 12 to 6 bits
- VFAT3 package production & validation
- Finalize VFAT3 Plug-In card design & production
  - Selection of chip protection optimization
  - Was wait for confirmation that VFAT3 package pinout won't change
- Integrate and test
  - Including proof of principle with ATCA backend
  - Using one GBT in wide bus mode for trigger data

Near term schedule

- May 2020: ESR
- Jan 31 2020: Start testing and assessment of Gen-2 electronics for ESR
- Still to be done:
  - GEBs:
    - M6-M8 start of production: mid October
    - M6-M8 delivery: end of 2019
    - M1-M4 rework: end of 2019
    - Note: delays here will now impact ME0 GEB design schedule, fortunately ME0 electronics can already be tested with GE2/1 electronics
  - OH v2:
    - Review in the coming days
    - Routing, procurement & manufacturing done by end of 2019
  - VFAT3 package:
    - Review of substrate design in the coming days
    - Production by end of 2019
  - Plugin-card
    - Finalize the layout now that VFAT3 package pinout is fixed
    - Selection of optimal chip protection: end of November
      - Could the design be ready such that production starts as soon as the protection scheme is known ?
    - Assembly with VFAT3 package: beginning of 2020

Towards the ESR

- The electronics should not be final
  - Some design modifications can still happen after ESR
    - In GE1/1 we passed the ESR with VFAT slot 5 not working
- However we need to plan enough time for integration and testing of the new components (VFAT3 package, Plugin card)
  - Will typically start in Jan 2020
  - We have to demonstrate trigger data over GBT link with OH v2
    - *Quid* of the Master-Slave -> oTMB modification ?
  - Noise seems under control (although we do not really understand why the proposed scheme works better)
    - Would like to re-evaluate the copper – nocopper ROB
  - We need to perform efficiency measurements
    - Need a set-up with scintillators, …
    - Scan efficiency VS. HV & Threshold
    - Monitor sbit rates
  - Cooling
    - There should not be a problem of cooling in terms of power dissipated however we should come with a cooling design, mechanically more flexible than GE1/1.

Conclusion

- GE1/1 experience really helped to smooth the design & development phase.
  - GE2/1 Electronics worked from 1st trial
- Still important steps in the GE2/1 Electronics development
  - Packaged VFAT3 on Plugin-card
  - OH version-2 with 1 GBT running in wide-bus mode
  - Move from uTCA to ATCA
- Despite the approval to keep GBT on GE2/1 OH the schedule remains tight before we enter into production
  - Will have basically 4 months to integrate and test all the new parts before ESR
  - All the designs & production flows have to stay on schedule