24th GEM Workshop

VFAT3b package

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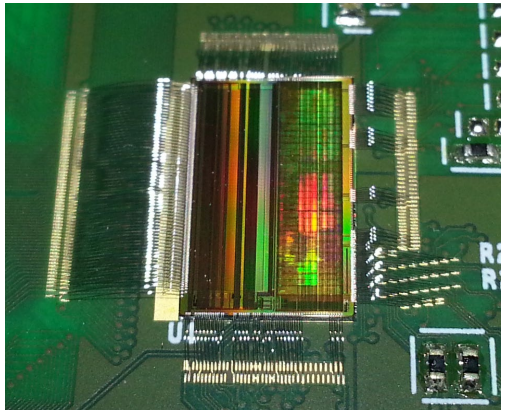
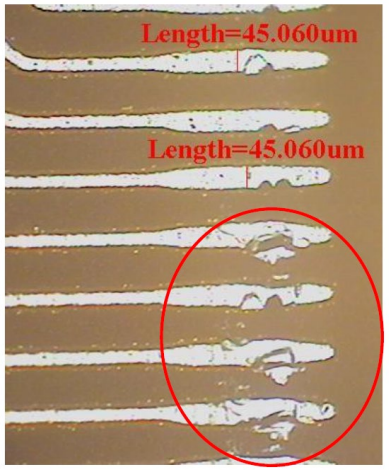
VFAT3 packaging

Why packing? The package will improve the plugin card production yield thanks to an easier design, less constrains for the board production and the replacement of the VFAT3 bonding phase with a much more reliable soldering procedure.

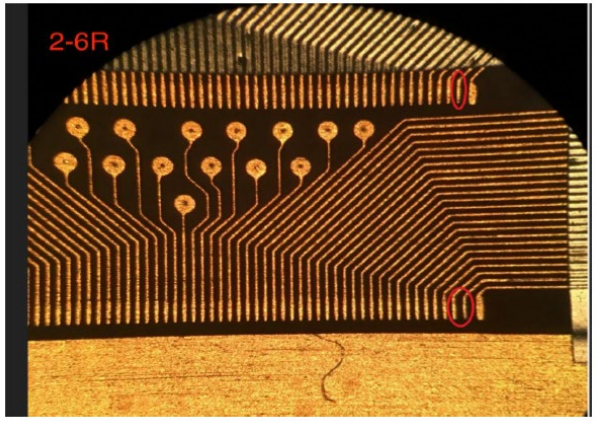
Some problems encountered during hybrid production*:



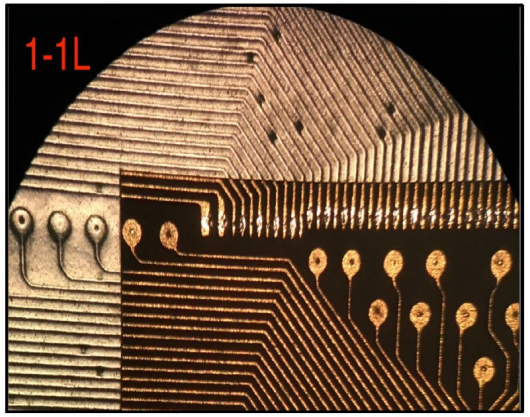
VFAT3 bondend on the hybrid



Pad catering



Over-etching on the channel pads: pads width about 37 μm < IPC standard for wire bonding 48 μm.

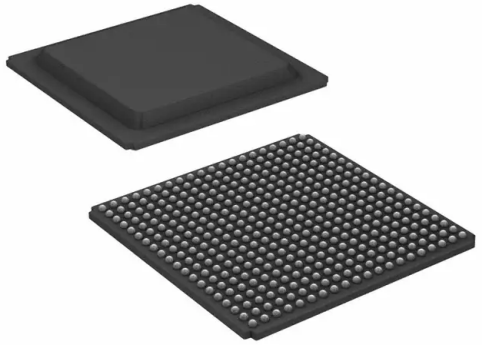


Breakage on the PCB surface/tracks and scratches ofnthe landing pads/vias.

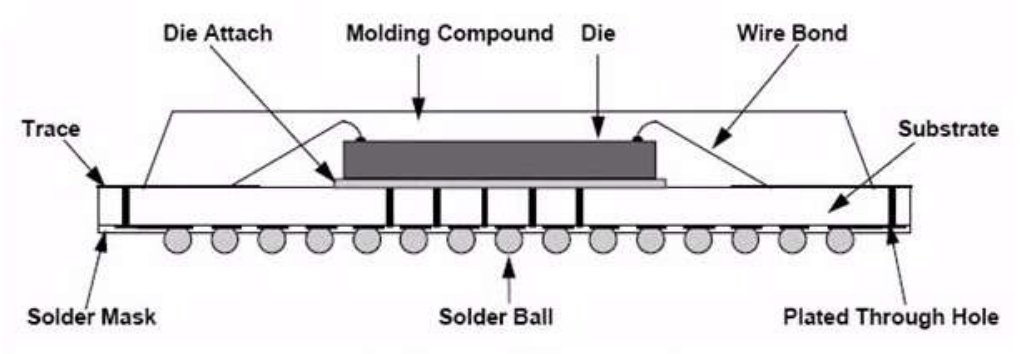
*Hybrid (HV3b_V4) Production & Packaged Hybrid Status, Mohsin Hayat, 6/12/2018.

BGA Package

VFAT3 will be packaged in a full Ball Grid Array (BGA) package.



BGA package example



BGA package cross-section

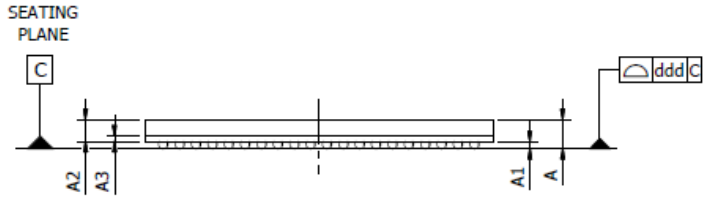
- The substrate is a small PCB, realized by means of advanced techniques, that hosts the die and provides the connections between the bonding wires and the solder balls.
- Solder balls are used for the electrical connection with an external PCB, mechanical support and heat transfer.
- Molding compound, plastic in this case or a metal coverage in others, protect the die and the wire bonding.

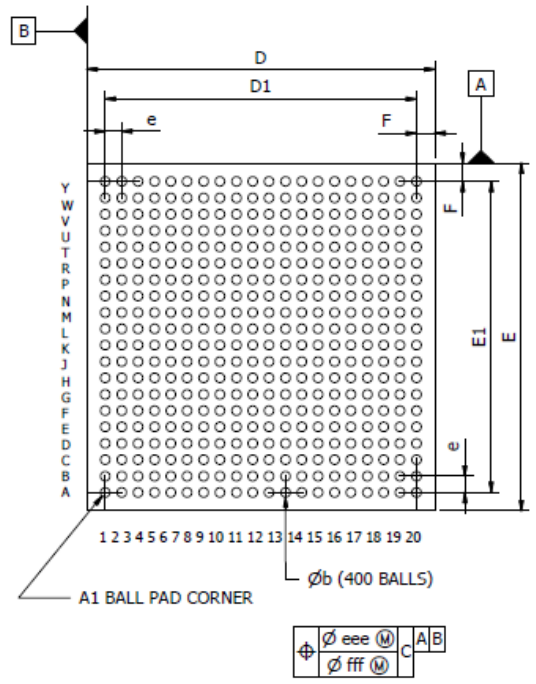
Package specifications

Package specifications:

- Ball grid array: 20 x 20
- Size: 17 x 17 mm^2
- Ball pitch: 0.8 mm
- Plastic encapsulation
- Ball bonding
- Ball solder composition: SAC 305 (96.5% Sn, 3% Ag, 0.5% Cu)
- 7 SMD passive components inside the package:
  - **4 capacitors** for power supply decoupling,
  - **2 capacitors** for reference decoupling (ADCs),
  - **1 resistor** for current monitoring.

PACKAGE OUTLINE
LFBGA 17x17 400 R20x20 PITCH 0,8 BALL 0,45





DIMENSIONS [mm]			
SYMBOL	MIN.	NOM.	MAX.
A			1,60
A1	0,32	0,36	0,4
A2		1,08	
A3		0,28	
b	0,4	0,45	0,5
D	16,85	17,00	17,15
D1		15,20	
e		0,80	
E	16,85	17,00	17,15
E1		15,20	
F		0,90	
ddd			0,15
eee			0,15
fff			0,08

Package ballout

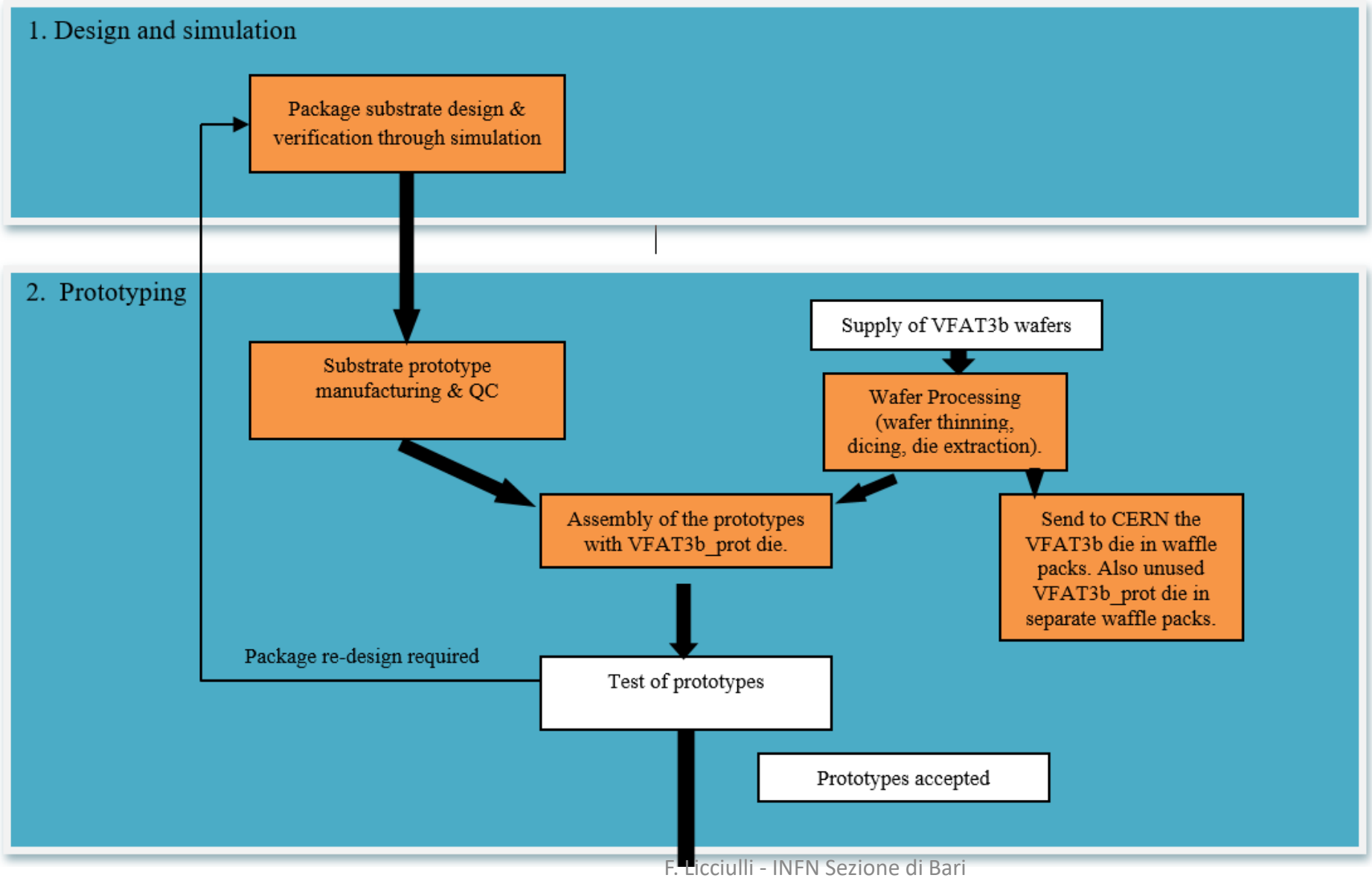
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	IN_128	IN_127	GND_FE	IN_126	IN_125	GND_FE	IN_124	IN_123	GND_FE	DiffBuffOutp	DiffBuffOutn	CFDIan	CFDIap	SCAN_IN0_C	SCAN_EN0_C	SCAN_OUT0_C	SCAN_IN1_A	SCAN_OUT1_C	HDLC_ADDRESS_0	HDLC_ADDRESS_3	A
B	IN_122	GND_FE	IN_121	IN_120	GND_FE	IN_119	IN_118	GND_FE	IN_117	thuff_ibias	Shaperin	DiffBuffIn	CFD_OUT	SCAN_EN0_A	SCAN_OUT0_A	SCAN_IN1_C	SCAN_EN1_C	SCAN_OUT1_B	HDLC_ADDRESS_1	HDLC_ADDRESS_4	B
C	GND_FE	IN_116	IN_115	GND_FE	IN_114	IN_113	GND_FE	IN_112	IN_111	PreAmpOut	ShaperOut	SCAN_IN0_A	SCAN_IN0_B	SCAN_EN0_B	SCAN_OUT0_B	SCAN_IN1_B	SCAN_EN1_B	SCAN_OUT1_A	HDLC_ADDRESS_2	HDLC_ADDRESS_5	C
D	IN_110	IN_109	GND_FE	IN_108	IN_107	GND_FE	IN_106	IN_105	GND_FE	VDD_FE	VDD_FE	AVDD_CFD	AVDD_CFD	DVDD_CFD	DVDD_CFD	VDD	SCAN_EN1_A	BIST_OK	HDLC_ADDRESS_7	HDLC_ADDRESS_6	D
E	IN_104	GND_FE	IN_103	IN_102	GND_FE	IN_101	IN_100	GND_FE	IN_99	VDD_FE	GND_FE	GND_CFD	GND_CFD	DVSS_CFD	DVSS_CFD	VDD	BIST_END	TP_IN_SI	TP_IN_SE	BIST_START	E
F	GND_FE	IN_98	IN_97	GND_FE	IN_96	IN_95	GND_FE	IN_94	IN_93	VDD_FE	GND_FE	GND_CFD	GND_CFD	DVSS_CFD	DVSS_CFD	VDD	SPI_EN	SPI_DO	VSS	VSS	F
G	IN_92	IN_91	GND_FE	IN_90	IN_89	GND_FE	IN_88	IN_87	GND_FE	VDD_PROT	GND_FE	GND_FE	GND_FE	VSS	VDD_IO	VDD	SPI_CLK	SPI_DI	VSS	TU_SwT_p	G
H	IN_86	IN_85	GND_FE	IN_84	IN_83	IN_82	GND_FE	IN_81	IN_80	GND_FE	GND_FE	GND_FE	GND_FE	VSS	VDD_IO	VDD	SCAN_CLK0_EN	VSS	VSS	TU_SwT_n	H
J	IN_79	IN_78	GND_FE	IN_77	IN_76	IN_75	GND_FE	IN_74	IN_73	GND_FE	GND_FE	GND_FE	GND_FE	VSS	VDD_IO	VDD	SCAN_CLK	VSS	TU_TXD_p_0	VSS	J
K	IN_72	IN_71	IN_70	IN_69	GND_FE	IN_68	IN_67	IN_66	IN_65	GND_FE	GND_FE	GND_FE	GND_FE	VSS	VDD_IO	VDD	VDD_EFUSE	VSS	TU_TXD_n_0	VSS	K
L	IN_64	IN_63	GND_FE	IN_62	IN_61	IN_60	GND_FE	IN_59	IN_58	GND_FE	GND_FE	GND_FE	GND_FE	VSS	VDD_IO	VDD	VDD_SLVS	VSS	VSS	TU_TXD_p_1	L
M	IN_57	IN_56	GND_FE	IN_55	IN_54	IN_53	GND_FE	IN_52	IN_51	GND_FE	GND_FE	GND_FE	GND_FE	VSS	VDD_IO	VDD	VDD_SLVS	VSS	VSS	TU_TXD_n_1	M
N	IN_50	IN_49	IN_48	IN_47	IN_46	IN_45	IN_44	IN_43	IN_42	VDD_PROT	GND_FE	GND_FE	GND_FE	VSS	VDD_IO	VDD	VSS	VSS	TU_TXD_p_2	VSS	N
P	IN_41	IN_40	GND_FE	IN_39	IN_38	GND_FE	IN_37	IN_36	GND_FE	VDD_FE	GND_FE	GND_CFD	GND_CFD	DVSS_CFD	DVSS_CFD	VDD	VSS	VSS	TU_TXD_n_2	VSS	P
R	GND_FE	IN_35	IN_34	GND_FE	IN_33	IN_32	GND_FE	IN_31	IN_30	VDD_FE	GND_FE	GND_CFD	GND_CFD	DVSS_CFD	DVSS_CFD	VDD	VSS	TU_TXD_p_6	VSS	TU_TXD_p_3	R
T	IN_29	GND_FE	IN_28	IN_27	GND_FE	IN_26	IN_25	GND_FE	IN_24	VDD_FE	VDD_FE	AVDD_CFD	AVDD_CFD	DVDD_CFD	DVDD_CFD	VDD	VSS	TU_TXD_n_6	VSS	TU_TXD_n_3	T
U	IN_23	IN_22	GND_FE	IN_21	IN_20	GND_FE	IN_19	IN_18	GND_FE	extAC_pulse	V_BGR	Int_Vref_ADC0	RST_TEST_MODE	VSS	RXCLK_p	VSS	TXD_p	VSS	TU_TXD_p_5	VSS	U
V	GND_FE	IN_17	IN_16	GND_FE	IN_15	IN_14	GND_FE	IN_13	IN_12	Imon	V_Tsens_ext	Ext_Vref_ADC1	BOR_DISABLE	VSS	RXCLK_n	VSS	TXD_n	VSS	TU_TXD_n_5	VSS	V
W	IN_11	GND_FE	IN_10	IN_9	GND_FE	IN_8	IN_7	GND_FE	IN_6	En_ext_Iref	VDD_TSENS_INT	POR_DISABLE	TP_MON_CLK	VSS	VSS	RXD_p	VSS	TU_TXD_p_7	VSS	TU_TXD_p_4	W
Y	IN_5	IN_4	GND_FE	IN_3	IN_2	GND_FE	IN_1	IN_0	GND_FE	Ext_Iref	Vmon	EXT_RESET	TP_MON_CLK_EN	VSS	VSS	RXD_n	VSS	TU_TXD_n_7	VSS	TU_TXD_n_4	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Analog Inputs

Power Supply & Digital

The proposed signal assignment has been maintained in the substrate design!

Flowchart of VFAT3b package production 1/2

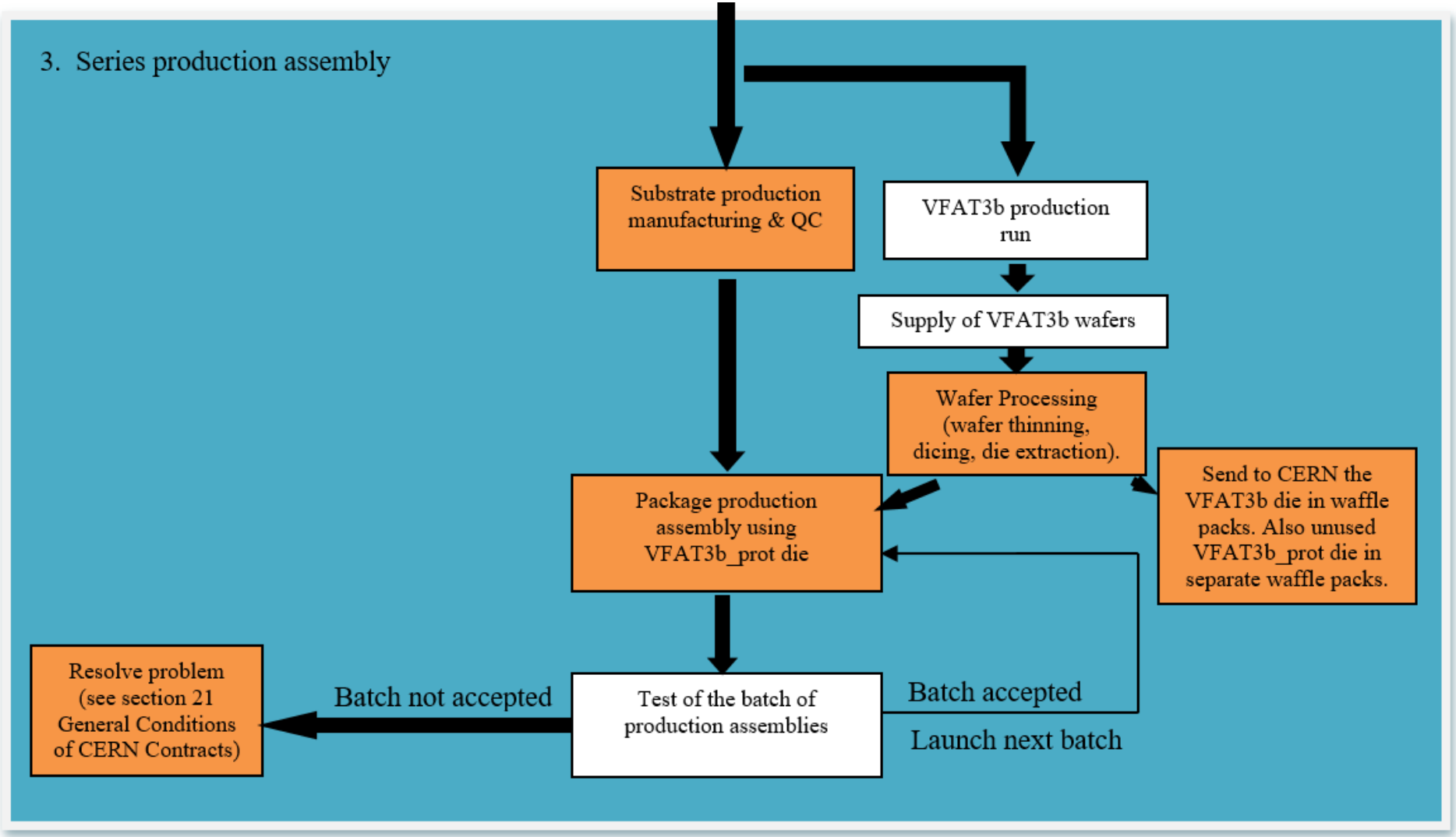


Orange boxes: activities under the responsibility of the contractor

White boxes: responsibility of CERN

Almost completed the first phase.

Flowchart of VFAT3b package production 2/2



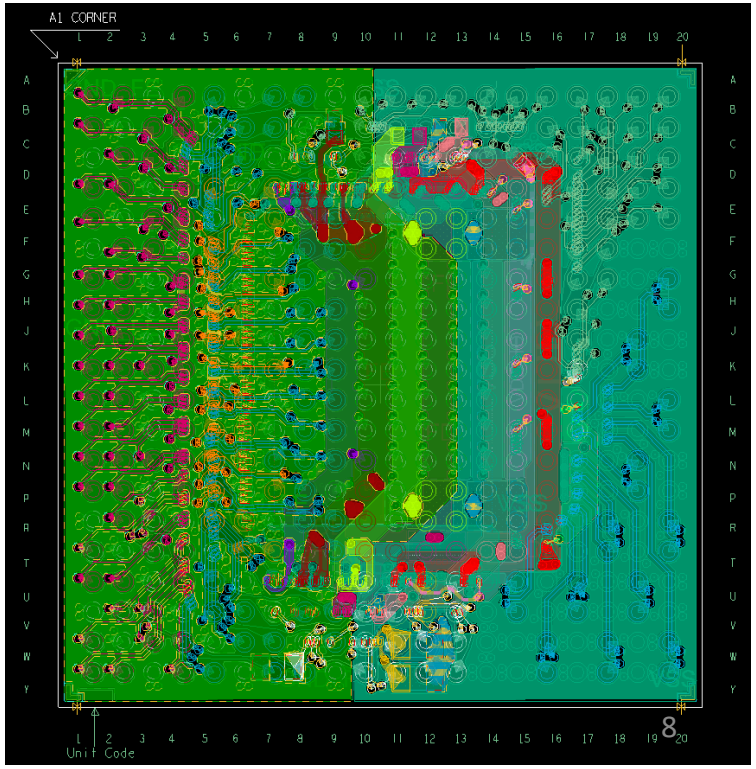
Package Design: 1st phase

First phase: substrate design completed.

Waiting for:

- RLC parasitic package extraction,
- Characteristic impedance simulation for differential lines,
- Crosstalk simulations,
- Package thermal behaviour simulations.

Once all the simulation results will be collected, the substrate design review will be called.

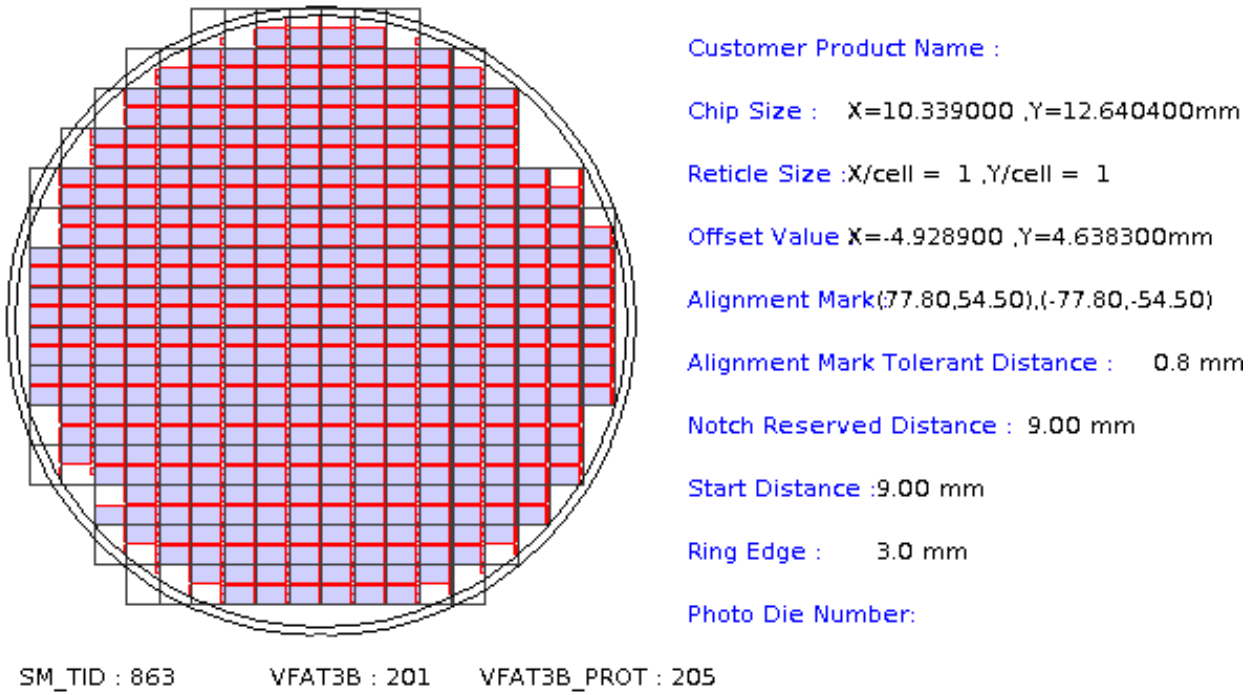


Prototyping: 2nd phase

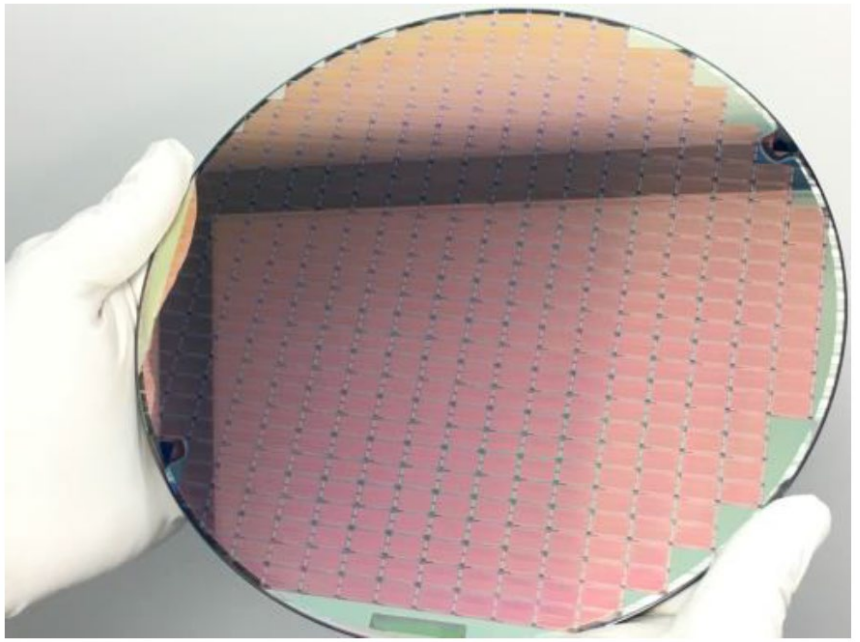
- VFAT3 package prototypes: 200 pieces
- At CERN were available 4 wafers from GE1/1
- Each wafer has 205 VFAT3b_prot dice
- Prototyping: one wafer of GE1/1 can be used

One wafer was sent to IMEC:

received on 19th September 2019



Production: 3rd phase



VFAT3 package series production:

- 5000 VFAT3 for GE2/1
- 7000 VFAT3 for ME0

VFAT3 wafer production:

- Wafers are produced in lots of 25,
- The minimum order quantity for production is one lot,
- Orders are placed in terms of lots,
- The cost of one VFAT3b production lot is approximately 42 kUSD,
- Delivery time is about 3 months.

For the full series production 75 wafers are needed! We will get:

- 15375 VFAT3b_prot
- 15075 VFAT3b.

Package costs

Step	Description	Quantity	Unit Price FCA	Total price
1	Design files and analysis reports (substrate design, electrical simulation, thermal simulation)	1	7,400 (design) 2,500 (Elect Sim) 4,000 (Therm Sim)	13,900
2	Prototype chip assemblies including wafer processing (including substrate tooling, manual ball mount kit, grinding, setup and substrates prototype series)	1 1 1 200	7,800 (tooling) 5,000 (BMK) 2,650 (Setup) 1.72 (unit package incl substr)	15,794
3	Series production chip assemblies including wafer processing – batch 1 (Including substrates for 5K pcs - Copper wiring – see "13" below)	5 000	Including charges to avoid high MoQ (design and tool charges) 1.72 (unit package incl substr)	25,394
4	Series production chip assemblies including wafer processing – batch 2 (including substrates for 7K pcs - Copper wiring – see "13" below)	7 000	Including charges to avoid high MoQ (design and tool charges) 1.72 (unit package incl substr)	28,831
TOTAL PRICE FCA (A)				83,919
COST OF TRANSPORT TO CERN PREVESSIN (FR) AND TRANSPORT INSURANCE (B)				450
TOTAL PRICE DAP CERN PREVESSIN (FR) = (A) + (B)				84,369

- The cost of the two series production is almost equal to the design and prototyping due to the high flexibility required by CERN (stop the production in any moment).
- The manufacturer asks for a series production at least of 20k pieces, only the prototyping can be lower.
- Step 3 and step 4 are like new design and prototyping phases.

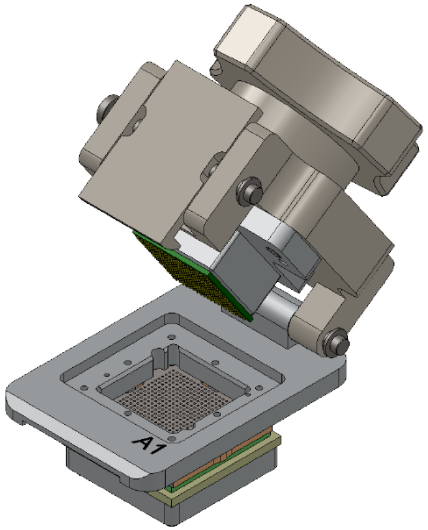
Time schedule

Deliverable/milestone	Relative timescale	Estimated/actual date
Placement of the order by CERN	T_0	Half July 2019
Design files and associated reports	T_1	October 2019
Approval by CERN of the substrate design	T_2	October 2019
Delivery of the prototypes	T_2 + 8 weeks	December 2019
Approval by CERN of the prototypes	T_3	June 2020
Approval by CERN to start work on the series production	T_4	June 2020
Delivery of the series production (first batch)	T_4 + 4 weeks	July 2020

VFAT3 package test

The test will be done in Bari:

- ✓Clam shell sockets ordered and arrived,
- ✓PCB design completed and produced,
- ➢PCBs will be mounted next week,
- ➢Firmware old code from VFAT3 characterization can be used,
- ➢Software to be done (3 weeks, we need the chip for finalization).



5 test systems will be realized in order to speed up the test of the series production.

VFAT3 package test list

Analogue tests:

- Power supply current absorption for shorts
- VFAT3 internal references, DAC scan, ADCs
- Temperature sensors: internal and external (bias current)
- Channel gains, linearity ranges, noise
- Local channel DACs characterization

Digital tests:

- Differential and common mode measurement of the TX SLVS
- Built in self test (BIST)
- Scan path

Bonding of the input channels by means of external injection.