ME0 Electronics Prototypes
Preliminary Testing Results

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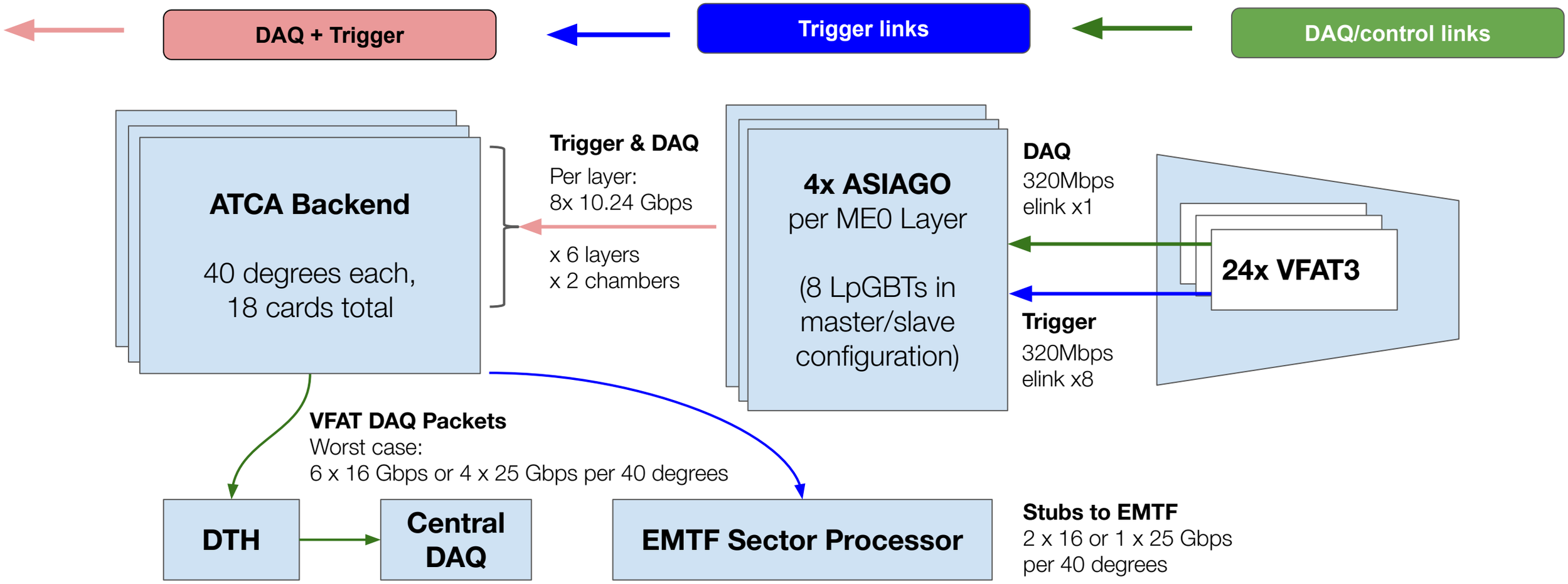
ME0 Electronics Overview



- With APX: each ATCA card handles 40 degrees (2 ME0 super-chambers)
  - Each super-chamber is composed of 6 layers of GEM chambers
- Front-end links (per ATCA card)
  - Uplink: 96x 10.24 Gbps LpGBT for Trigger, DAQ, and Control
  - Downlink: 48x 2.56 Gbps LpGBT for TCDS + Control
- Back-end links (per ATCA card)
  - 1 x 25 Gbps or 2 x 16 Gbps to EMTF
  - 4 x 25 Gbps or 6 x 16 Gbps link to DTH

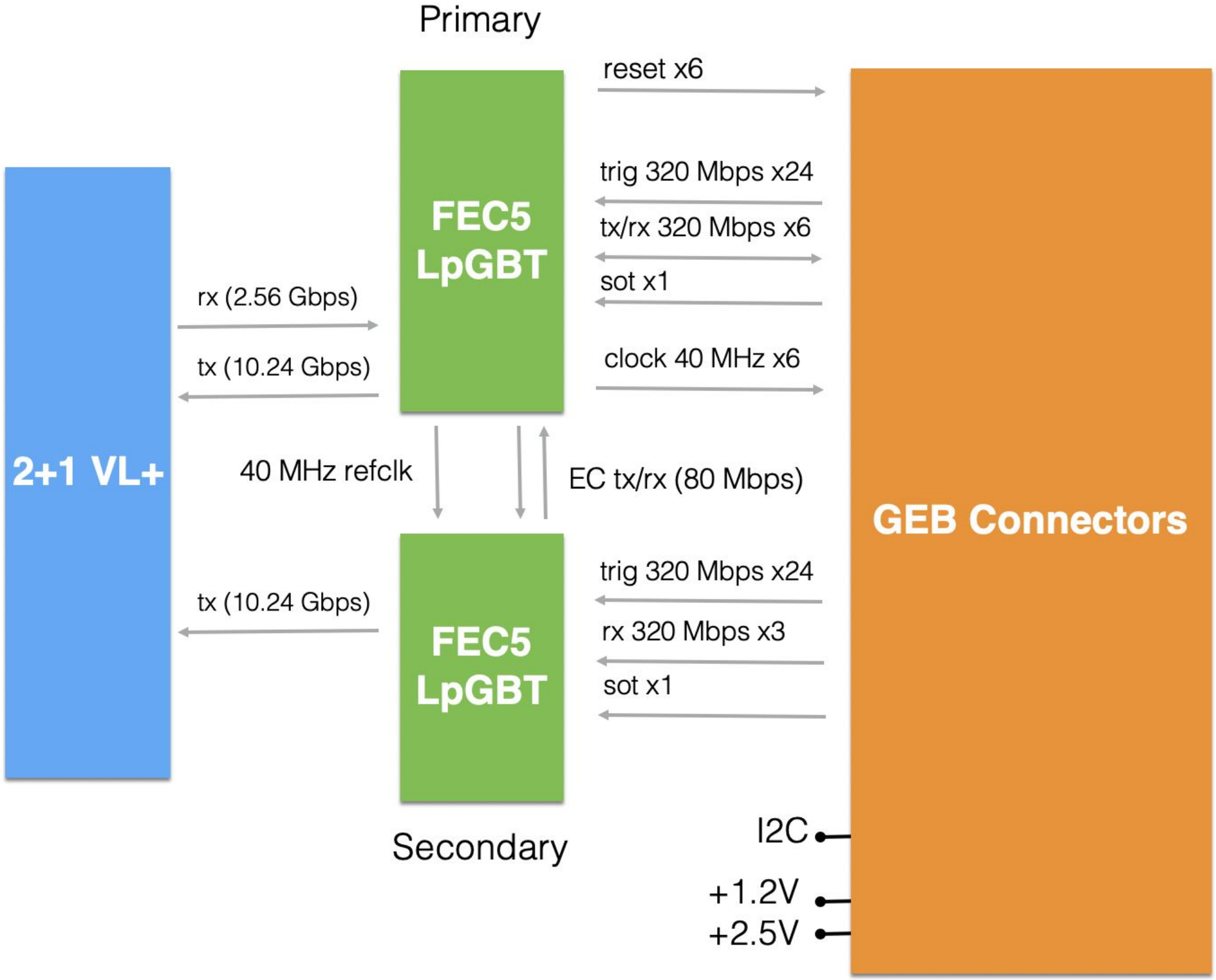
ME0 Electronics Prototypes

- Reminder: docs, schematics, interfaces etc are on the Twiki:
  - https://twiki.cern.ch/twiki/bin/viewauth/CMS/ME0ASIAGO
  - We are trying to be very thorough in documenting everything and providing ALL files... strict adherence to the "hit by the bus" principle of documentation.
    - ✦ Please comment if there is anything else we can add

- Tests are being done using a ME0 Optohybrid Prototype (ASIAGO)
  - An ASIAGO features two LPGBTs in a primary/secondary ("master/slave") configuration with a 2TX + 1RX optical configuration
  - Two ASIAGOs connect to a GE2/1 GEB through a PIZZA (prototype interface mezzanine)
    - ✦ The classic slot handles 6 VFATs and the extra spicy slot handles the other 6
  - Preliminary testing was all done using a Samtec Firefly (commercial optics) connected through a CACIO adapter
    - ✦ CACIO may be useful outside of GEMs.. VLDB+ team is interested; an alternate version of the CACIO with mechanical modifications was designed for CERN

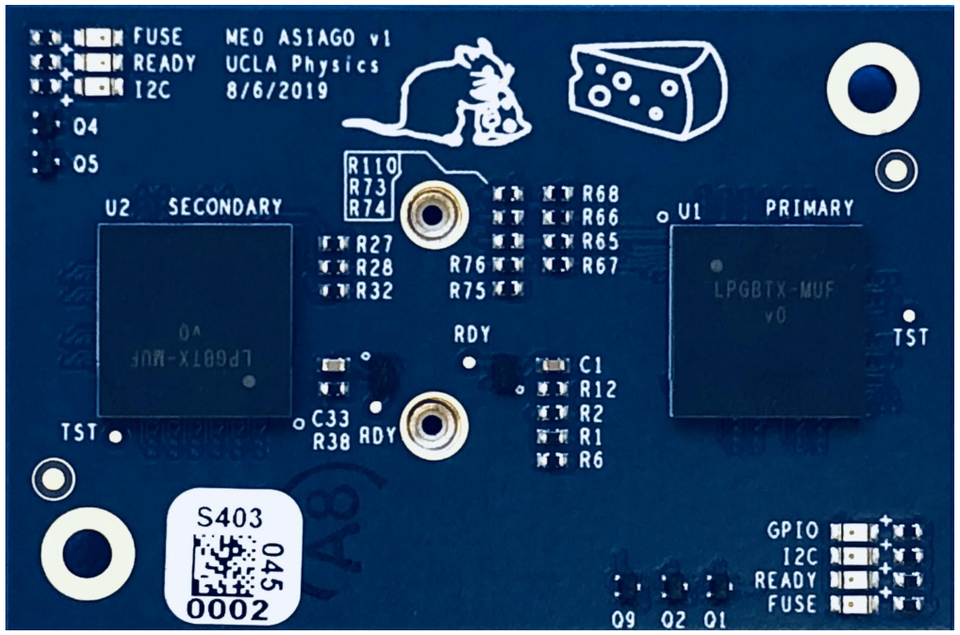
- All boards received 8/29/2019.. just over a month ago. Many thanks to a heroic effort by Evaldas to help get the ME0 electronics project up and running so quickly
  - **Only 6 working days to go from having nothing at all to having boards, firmware, configuration, and VFAT communications!**

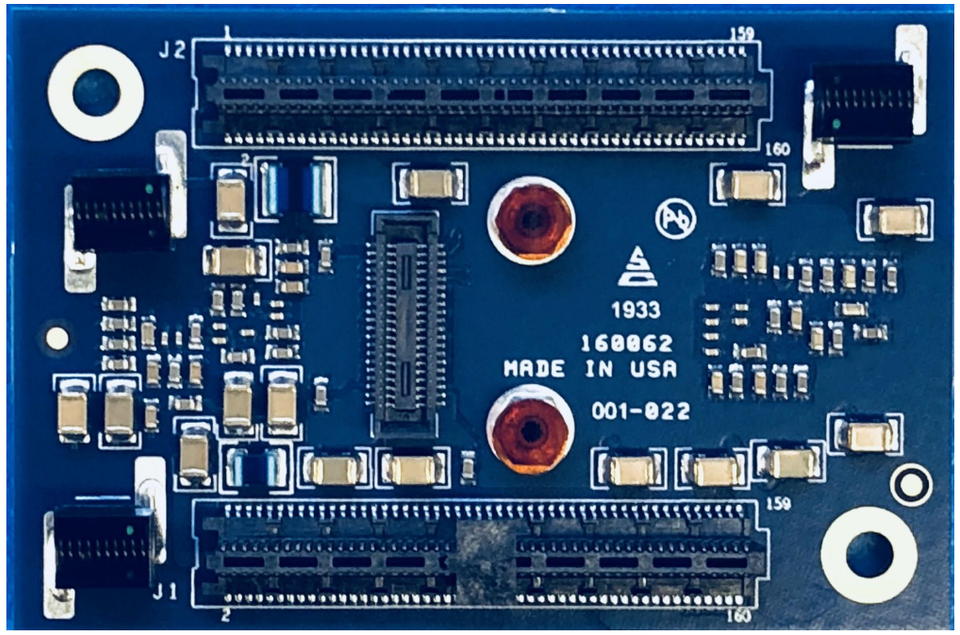
ME0 ASIAGO


Primary
reset x6
trig 320 Mbps x24
tx/rx 320 Mbps x6
sot x1
clock 40 MHz x6
FEC5 LpGBT
rx (2.56 Gbps)
tx (10.24 Gbps)
2+1 VL+
40 MHz refclk
EC tx/rx (80 Mbps)
GEB Connectors
trig 320 Mbps x24
rx 320 Mbps x3
sot x1
tx (10.24 Gbps)
FEC5 LpGBT
Secondary
I2C
+1.2V
+2.5V

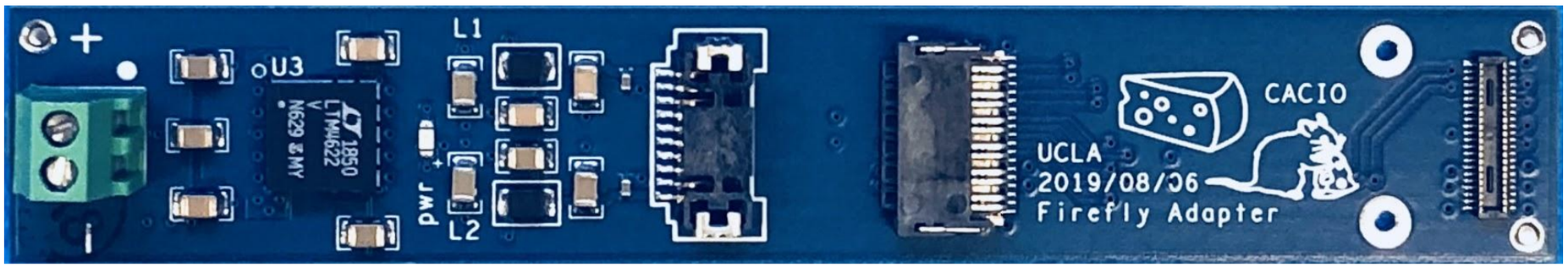
Photos

ASIAGO:: a strong-flavored cow's milk cheese originally made in northern Italy. In our case, ASIAGO is the ASIC and Gigabit Optics.



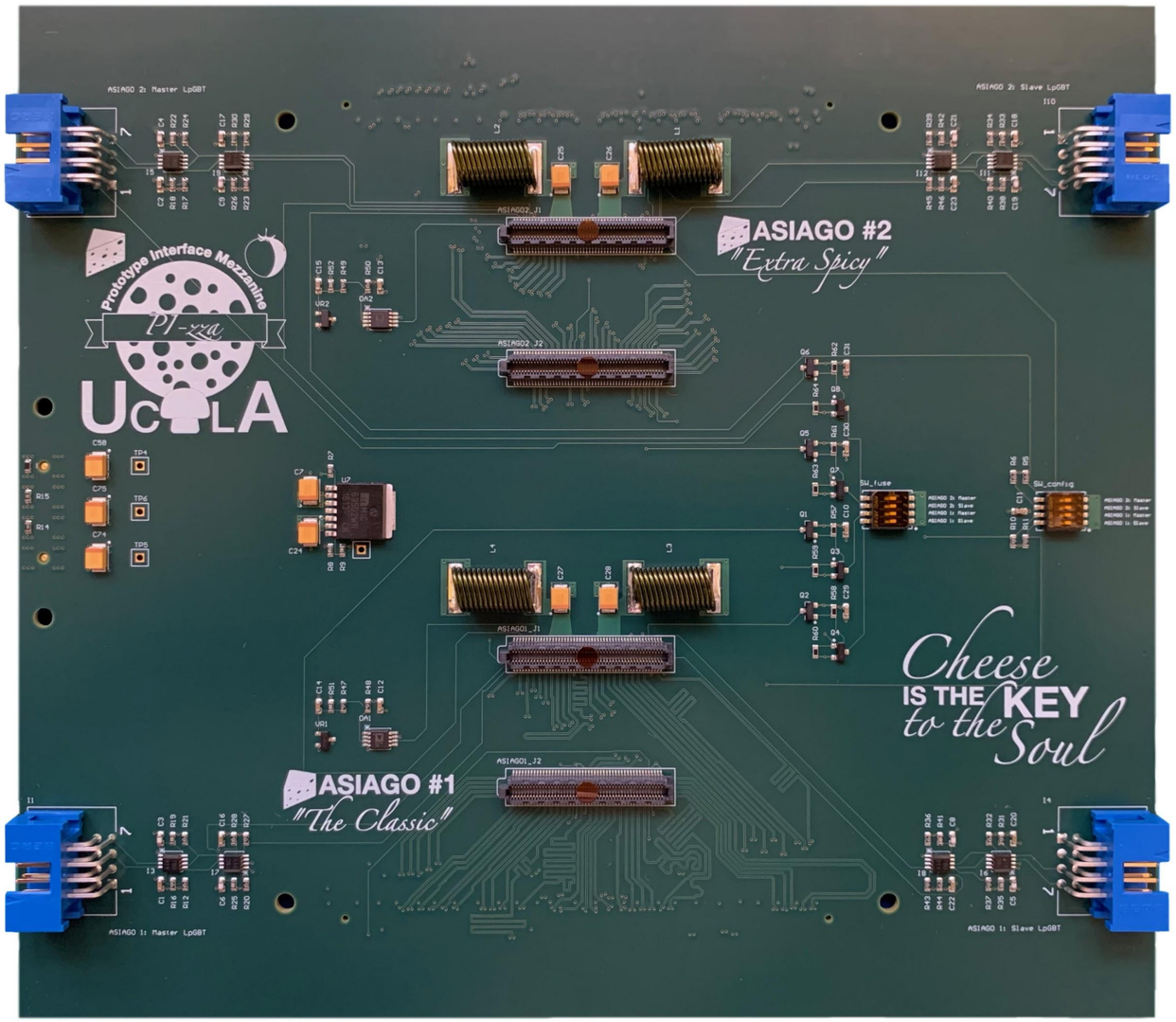


CACIO: The central and southern Italian word "Cacio," as in the pasta sauce Cacio e Pepe (Cheese and Pepper), comes the Latin word, caseus. That is also the origin of the English word “cheese.” In our case, CACIO means the "Custom Alternative to CERN Integrated Optics"



Photos

PIZZA: a savory dish of Italian origin, consisting of a usually round, flattened base of leavened wheat-based dough topped with tomatoes, cheese, and various other ingredients (anchovies, olives, meat, etc.) baked at a high temperature, traditionally in a wood-fired oven. In our case, the PIZZA is the Prototype Interface Mezzanine



pizza design: Nick McColl

LPGBT Software

- LPGBT does not have dedicated software (yet?)
  - Developed our own software based on the GBTX python tools:
    - https://github.com/andrewpeck/me0_scripts
    - Rewrote the USB interface using a cross platform API
    - Now supports Linux, OSX, Windows instead of Windows-only CERN tools
  - Ported *most* of the LPGBT register map into an XML format compatible with our existing CTP7 register access tools and also created a version of the tools compatible with the I2C dongle
  - Developed configuration scripts for base configuration, master / slave configuration
  - Python tools turn out to be much more useful than the GUI interface anyway.. likely will continue using them even if a CERN tool is released eventually
    - Python tools can be used interchangeably either with I2C dongle or through CTP7 IC path!!

- We have a routine for fusing a minimal configuration.. however, still need to validate and test

ASIAGO <—> CTP7 Communications

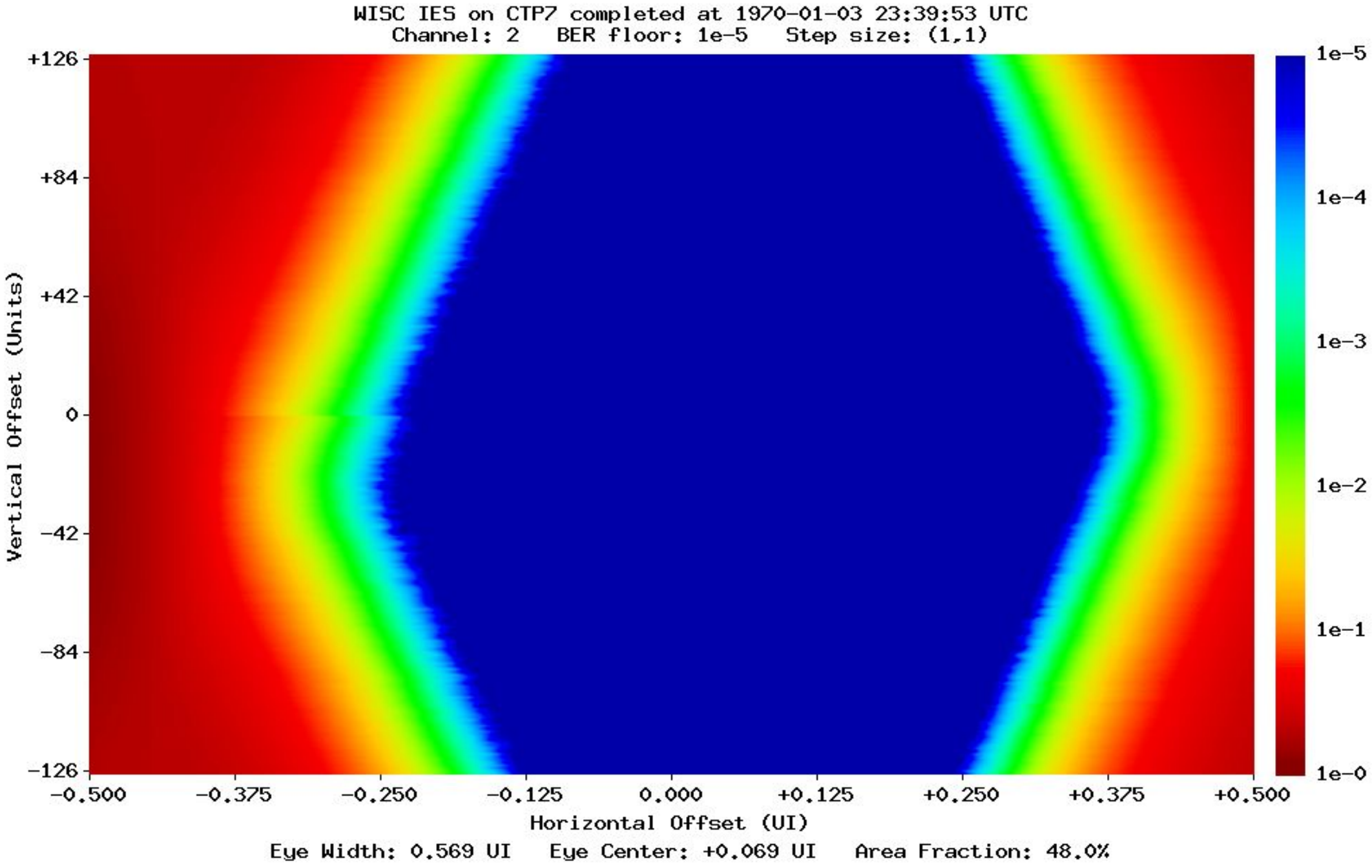
- Communication has been established between LPGBT and CTP7
  - After iteration on firmware and LPGBT configuration we are seeing reliable bi-dreictional communication between the backend and the LPGBT
  - Optical "eyes" are wide open and communication has been reliable so far
    - Example "eyes" on next slides

- Still need to do proper bit-error rate floor measurements over a long period to prove sustained, reliable communications

LPGBT —> CTP7 RX Eye

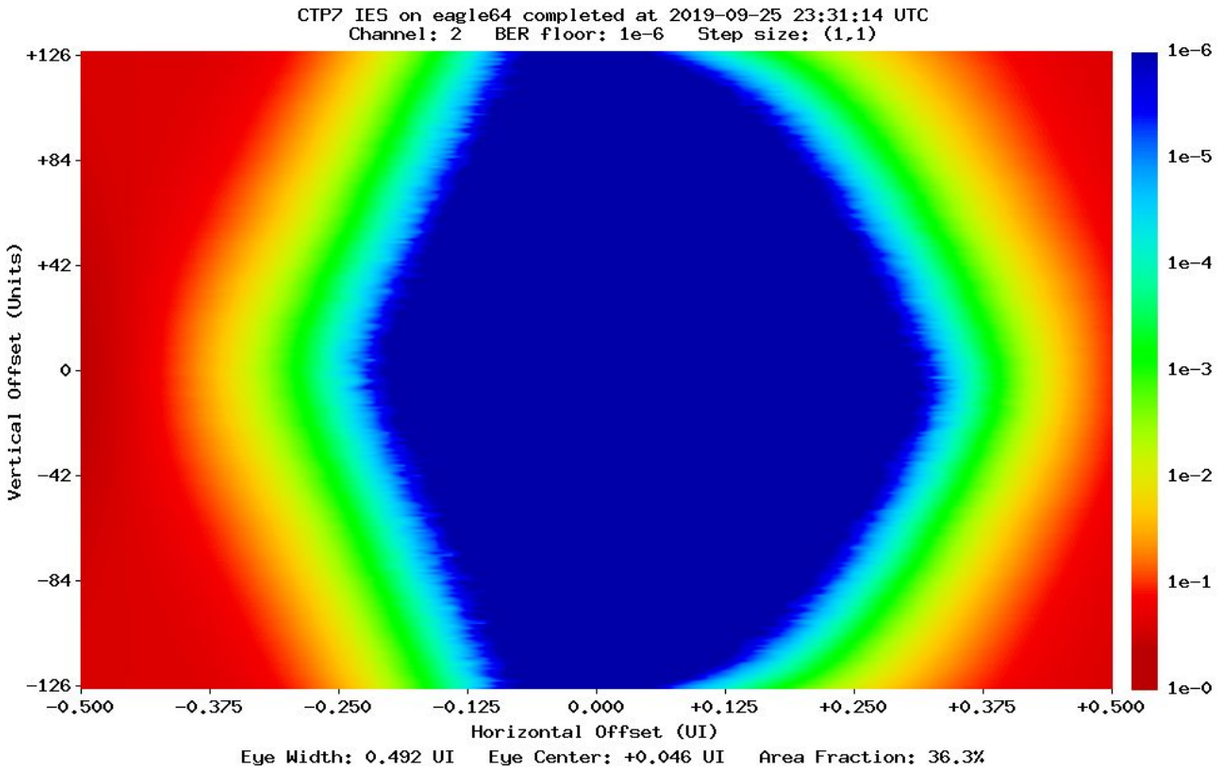
- 10.24 Gbps eye taken with the Virtex-7 IBERT
  - Z-axis specifies a bit error rate floor

Taken with Samtec Firefly

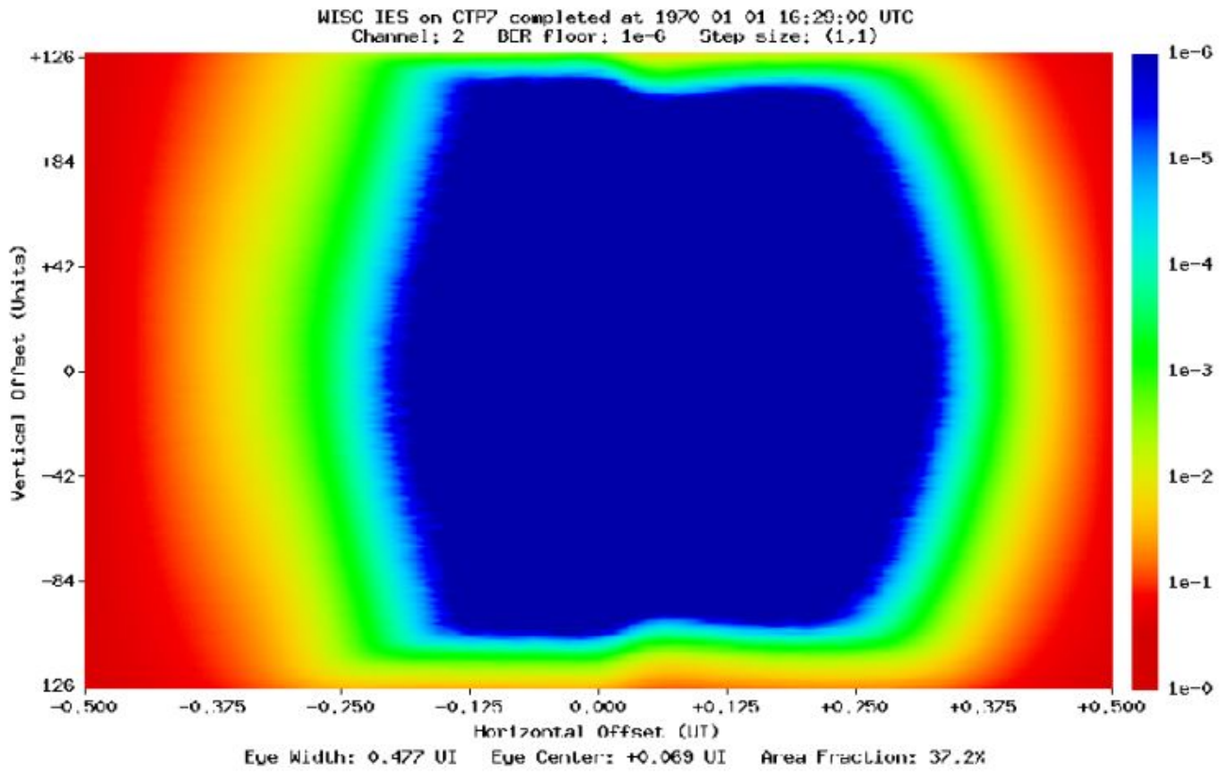


LPGBT —> CTP7 RX Eye

Taken with VL+



Master

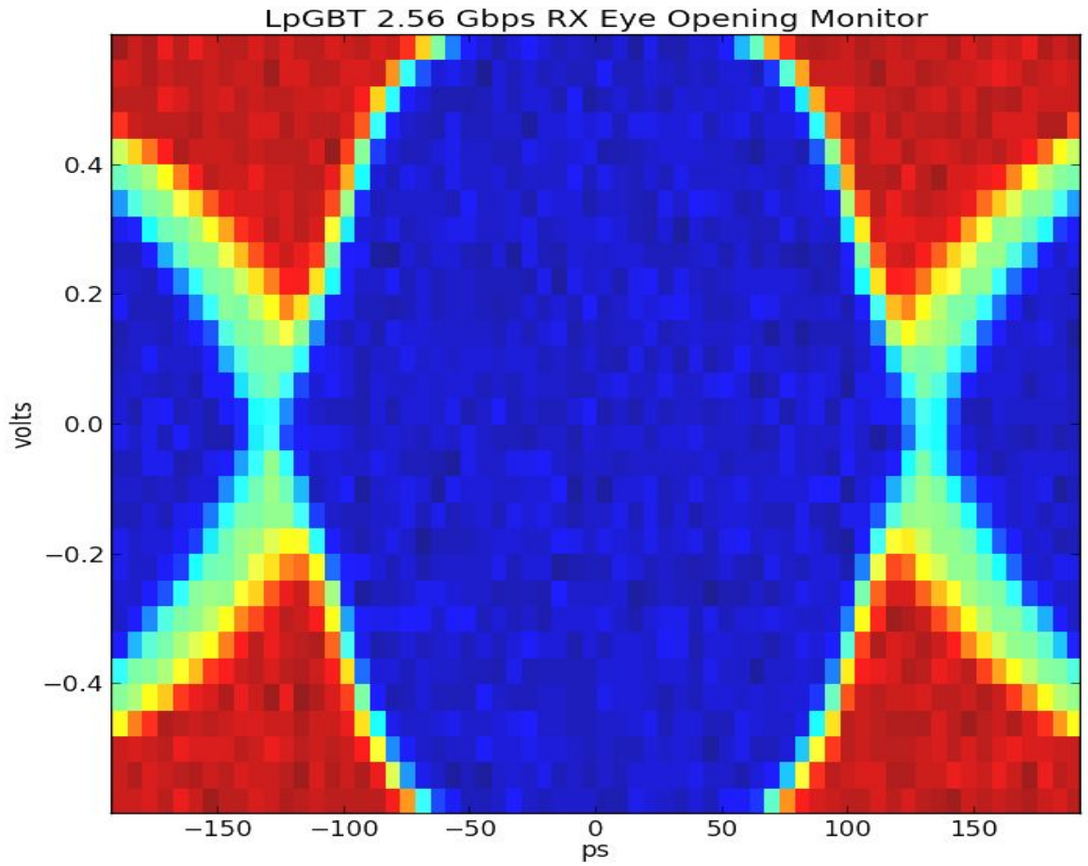


Slave

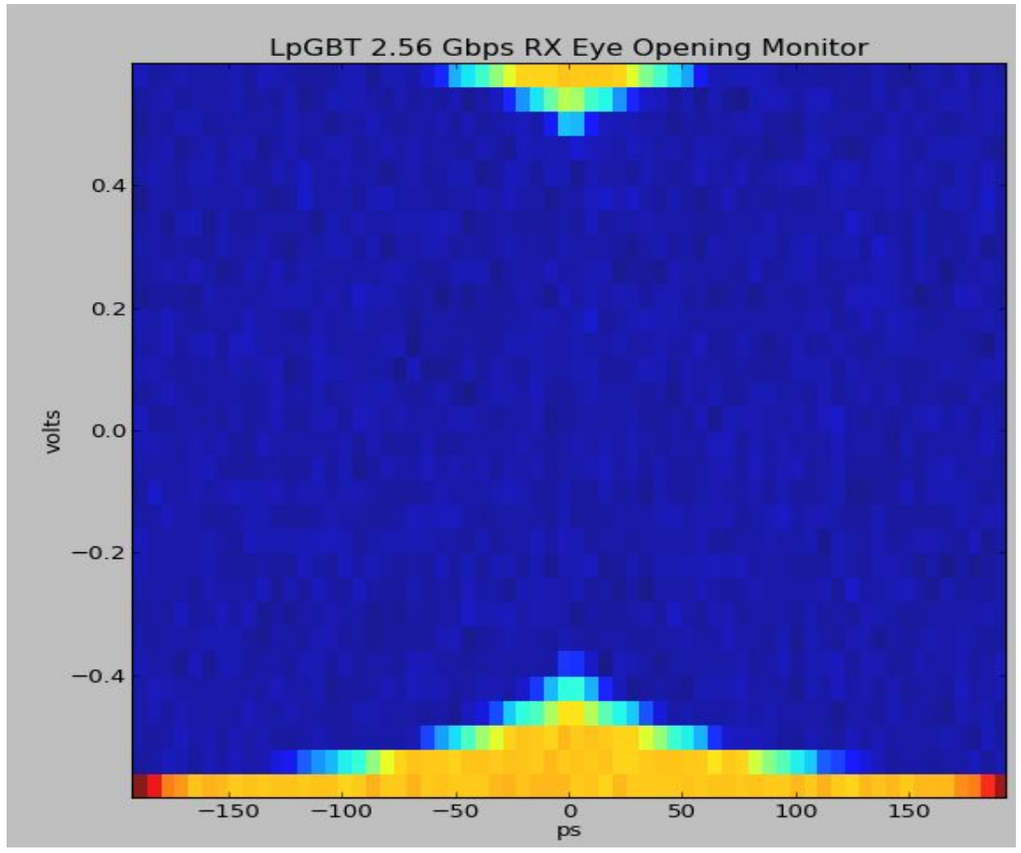
No tuning... expected to improve with adjustment but already good enough as-is

CTP7 —> LPGBT TX Eye

- 2.56 Gbps eye taken with the LPGBT Eye Opening Monitor (https://lpgbt.web.cern.ch/lpgbt/manual/dft.html#eye-opening-monitor)
  - Documentation does not specify any way to interpret the Z-axis.. so Z-axis is arbitrary.. scale normalized such that min/max = 0/100 (It is the area of the blue open shape that matters)
  - n.b. Uplink/downlink eyes are fundamentally different and should not be compared to each other
    - ✦ No axis (x, y, or z) should be compared directly between uplink / downlink eyes
    - ✦ Despite prima facie similarity **these are completely different plots**



Taken with Samtec Firefly



Taken with VL+

- Still trying to understand how to interpret the differences between the two plots..
  - ✦ Documentation on this subject is not thorough so the feature is difficult to interpret

LPGBT Internal Control Path

- Evaldas got the internal control (IC) path of the LPGBT working and tested
  - IC path uses 2 bits of the optical link frame as slow control
  - Initial configuration and fusing will be done through dongle (I2C), while all subsequent configuration will be done through IC path
  - Fun video here: https://twiki.cern.ch/twiki/pub/CMS/ME0ASIAGO/MOV_20190923_1613576.mp4
    - Note the GPIO led slowly turning on and off via python script running on the CTP7

- Still need to work on slave control (use EC output of master LPGBT to drive the EC input of the slave)

LPGBT <—> VFAT3 Communications

- We have been able to establish communication between LPGBT and several VFAT3s, observing working communications in both tx and rx paths as well as with the S-bit SoT signal
  - Need to validate all VFAT slots
    - There are a number of polarity swaps that need to be correctly accounted for
    - Simultaneous validation of all slots depends on packaged VFATs with addressing
  - Right now 2 slots aren't working at CERN... need to debug
    - Spare boards brought to CERN today
    - Could be a bad phase... need to adjust link RX phase to check

- Still need to do proper bit-error rate floor measurements over a long period to prove sustained, reliable communications

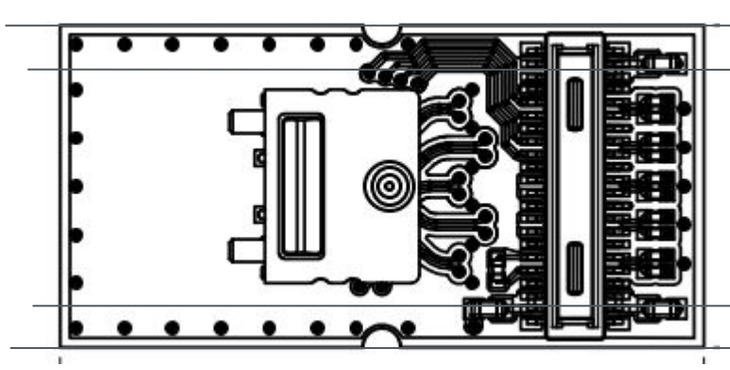
LPGBT Slave

- Testing was also done with the LPGBT slave
  - LPGBT is configured as transmit only (simplex).. no fiber input
  - Control is done through the master LPGBT which can drive the EC (external control) pins of the slave LPGBT
  - No issues seen so far, but still need to test EC path
    - Configuration so far has been done using the I2C dongle

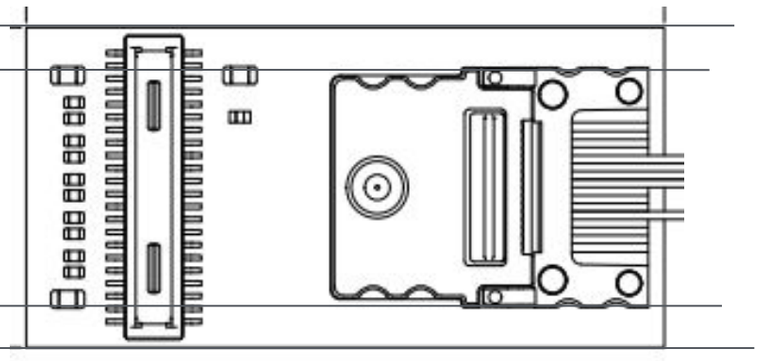
VL+

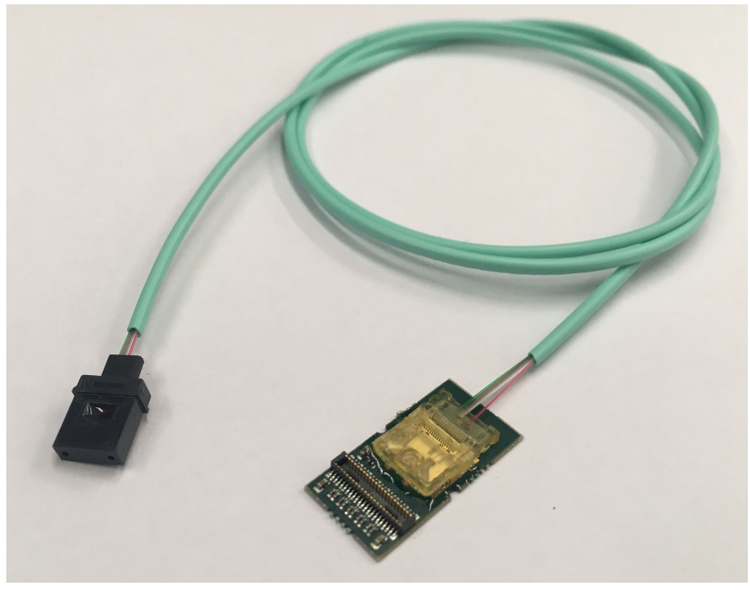
- 4 VL+ modules finally received on 2019/09/25
  - Discovered that the mechanics had changed at the last minute with no warning
    - Size of plastic optical module increased --> mechanical conflict with standoffs
    - Mounting holes removed --> current VL+ has no way to mount reliably :(
      - Awaiting recommendations from designers
    - Better communication with designers would be very helpful!

old design



8/26/2019 new design





  - Evaldas removed the standoffs specified in the original deisgn and installed a VL+
    - Works well! But it can't be screwed down.. not reliable but OK for testing
    - We pray the final version is improved

Fusing

Working on fusing of the LPGBTs through I2C

- **Big issue:** from https://lpgbt.web.cern.ch/lpgbt/manual/known_issues.html#fusing-updateenable-bit
  - Issue: Once updateEnable bit in the [0x0ef] POWERUP2 register is blown no other fuse can be blown.
  - Workaround: Burn the updateEnable bit only after all other registers are burned as required.

- We need to be very careful with fusing!! We only get one shot
  - We are working on scripts for fusing, but need to be very careful with testing and validation before we attempt fusing

Next Steps

Next testing steps in rough order of priority:

1) Fusing LPGBT configuration
2) Test and validate all VFAT3 slots (with polarity inversions etc)
3) Test slave LPGBT EC path
4) Phase scans
5) S-curves with LPGBT on GE2/1 Chamber
6) Need to carefully study operation of the VFAT3 ASIC without access to a SOT signal
7) Test long-term LPGBT <—> CTP7 communications reliability
8) Test long-term LPGBT <—> VFAT3 communications reliability
9) S-bit handling in CTP7 firmware
    - No algorithm yet, just e.g. VFAT hit counters for S-bit threshold scans

Longer term...

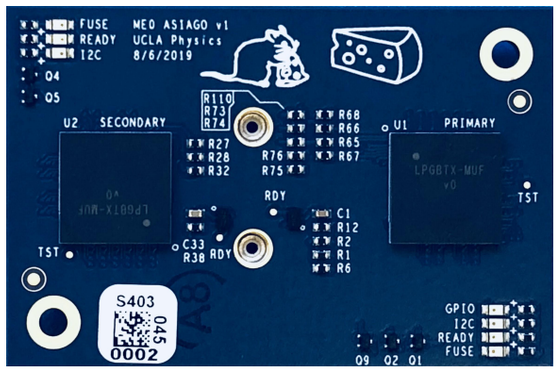
- v2 ASIAGO revision (minor changes, so far just to match future updated VL+ specs)
- Development of production test & qualification software/firmware/hardware

ME0 Electronics Testing Summary

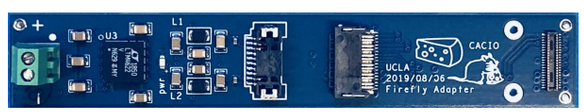
- All ME0 prototype electronics received at UCLA on 08/29/2019
  - "ASIAGO" -- ME0-like LPGBT prototype
  - "CACIO" -- Adapter to use Samtec Firefly in place of VL+
  - "PIZZA" -- Adapter to connect ASIAGO to a GE2/1 GEB

- Testing and development progress: [Evaldas + Andrew]
  - Wrote software for I2C control of LPGBT
  - Wrote LPGBT-based GE2/1 firmware around the ASIAGO + PIZZA
  - Wrote scripts for i2c configuration of master + slave LPGBT
  - Tested optical links:
    - ✦ "Eye diagrams" OK in both directions (tx + rx, master + slave)
  - Communications established with VFAT3 on master + slave
  - Internal control (IC) path established and working
  - Control of GPIO (reset pins) working

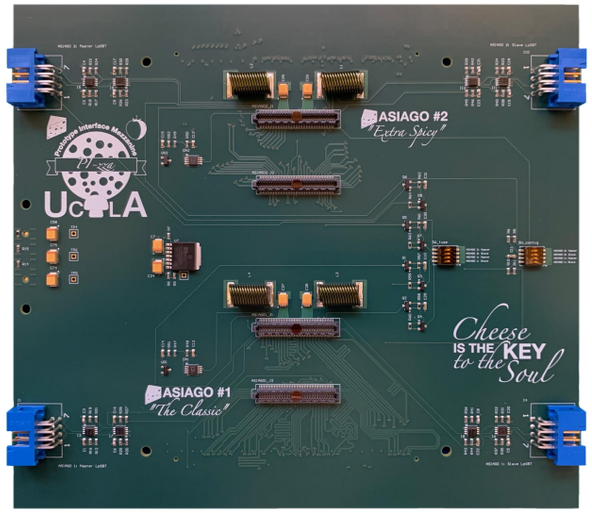
- Major remaining tasks:
  - External control of slave LPGBT (use master to control slave)
  - Fusing of chips
    - ✦ We only get one attempt due to a bug in the LPGBT design!
  - S-bit handling in firmware
  - Careful evaluation of operation without VFAT3 start-of-transmission
  - S-curves, s-bit scans, etc. on GE2/1 chamber



ASIAGO



CACIO



PIZZA