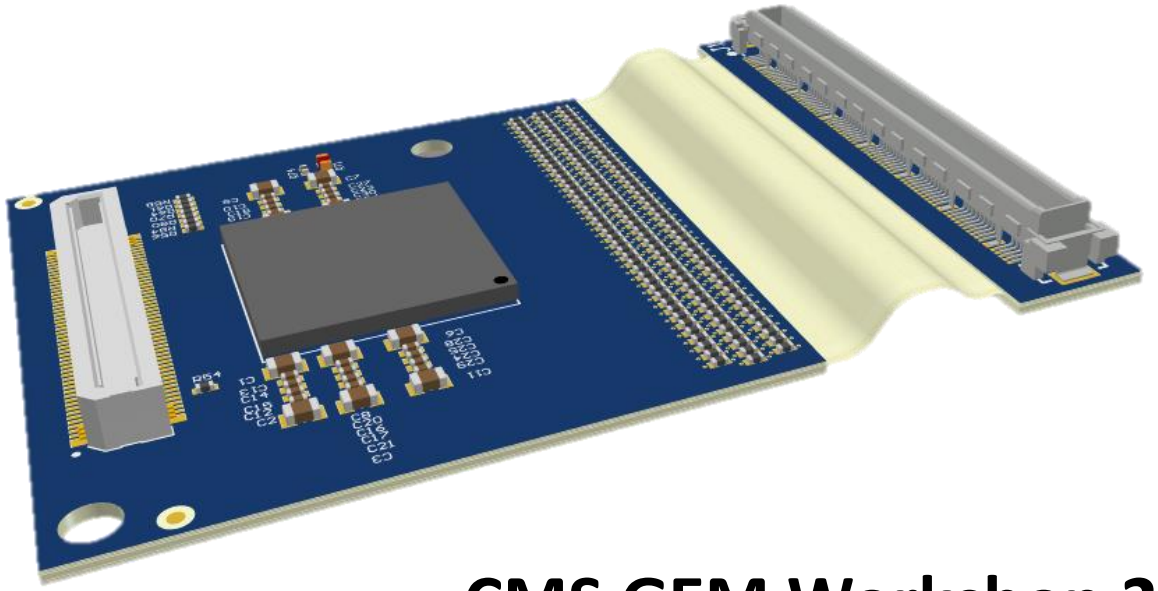
VFAT3b Plugin Card

(PV3b_V1.0)

Design & Status



CMS GEM Workshop 24

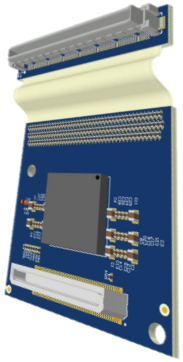
Muhammad Ali, Optics Labs , Pakistan

Outlines

- GE2/1 Plugin Card
- GE1/1 Hybrid VS GE2/1 Plugin Card
- VFAT3 channels protection
- Dimensions/Assembly View
- PCB Layout
- Design Status

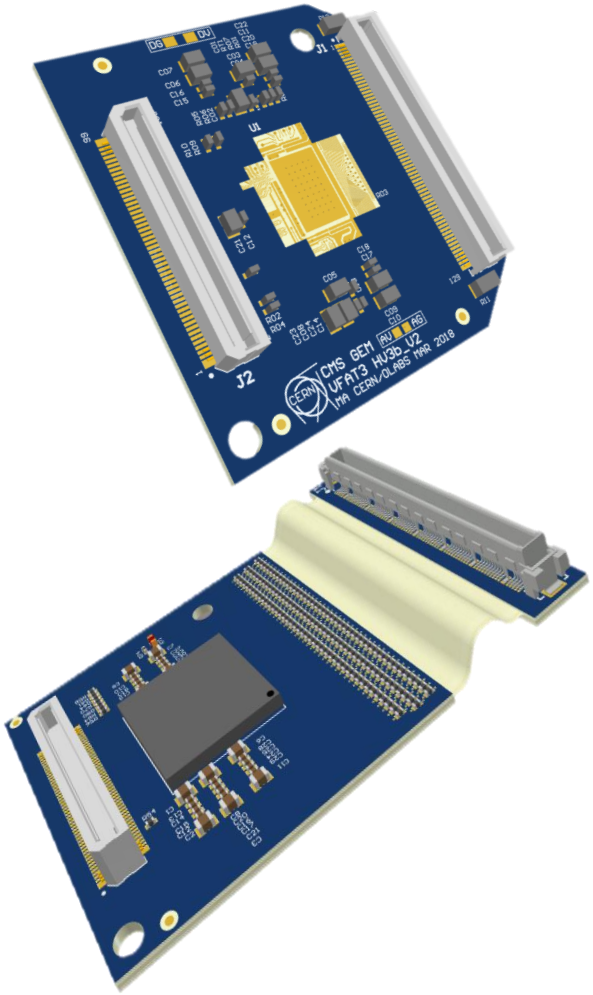
GE2/1 Plugin Card

- A rigid flex single piece HDI PCB based on packaged VFAT3 ASIC
- The rigid part R1 having VAFT3 is plugged on GEB via Panasonic 100 Pin connector (AXK5S00247YG)
- The other rigid part R2 has HRS140 connector (HIROSE_FX10A-140P-14-SV1)is plugged on ROB
- The flex part is capable to accommodate the minor mechanical misalignments between GEB and ROB (observed during GE1/1 detectors assembly)



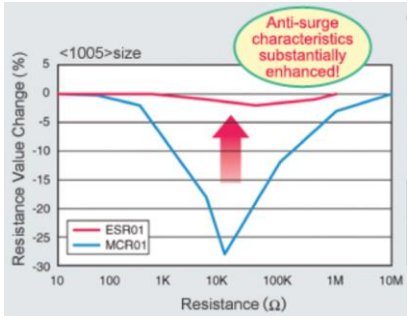
GE1/1 Hybrid VS GE2/1 Plugin Card

- HV3b is 0.8mm HDI PCB while Plugin Card is 0.9mm (rigid) Rigid Flex PCB
- In Plugin Card HDLC Address[3:0] have been added on 100 Pin Connector
- The power resistors connecting ROB AGND to VFAT3 AGND removed (Direct shorted)
- HV3b versions have naked VFAT3 Chip while Plugin Card have packaged VFAT3



VFAT3 channels protection

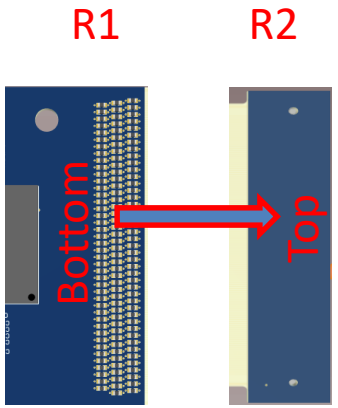
- Discrete anti-surge chip resistors (ESR01MZPJ471) have been added in series and expectedly low cross talk compared to array resistors
- Provide 2kV electrostatic discharge resistance and 3.2 times more rated power in category (0.2W @ 50V)

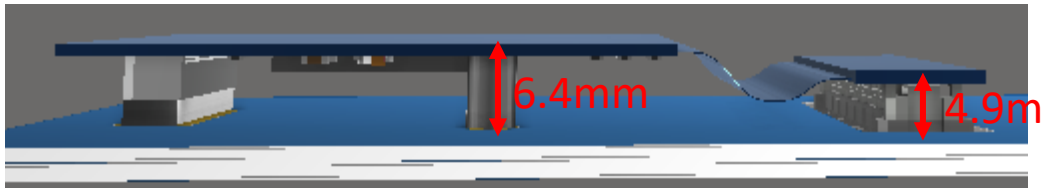


- Searching of ultra low capacitance bidirectional TVS diodes in suitable package for extra protection
- Tried various packages to check the fit in available space on plugin card

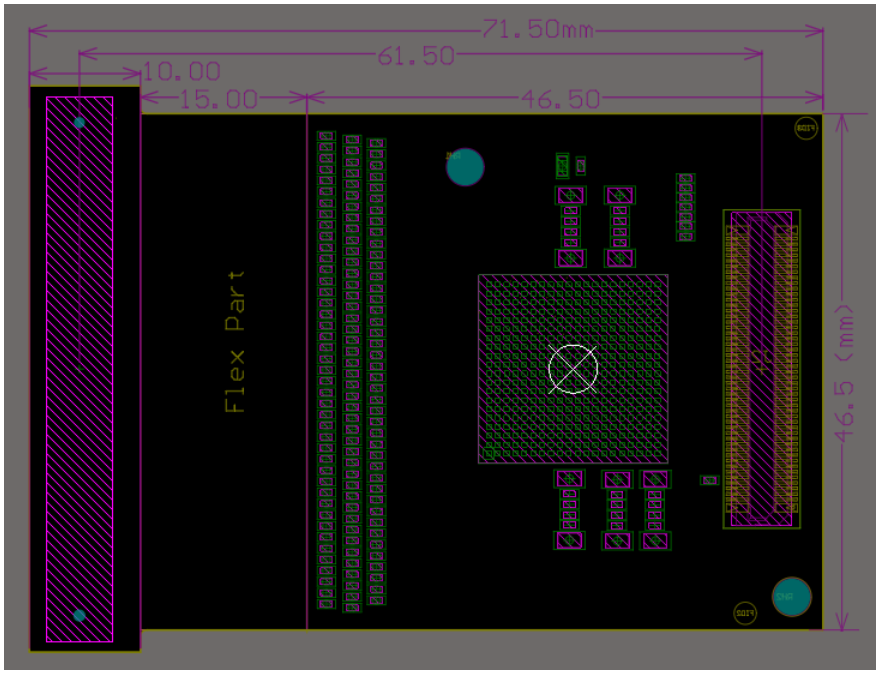
VFAT3 channels protection

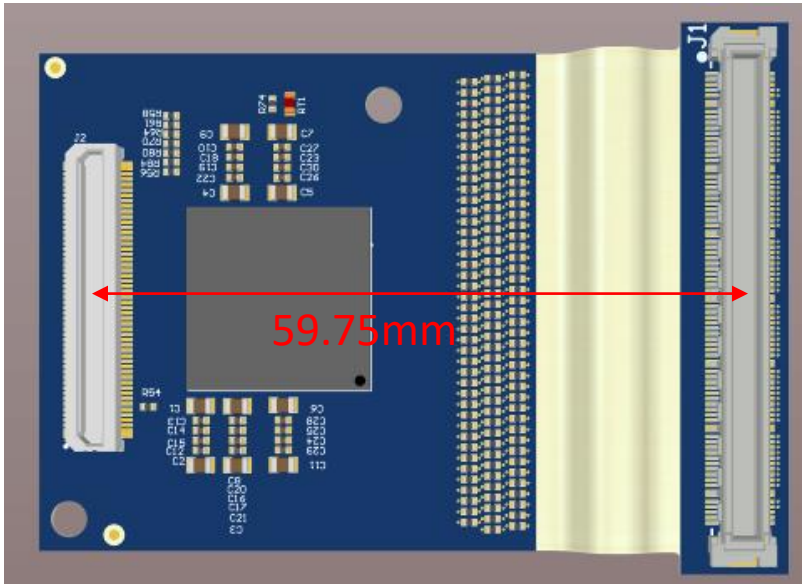
- The available TVS diode arrays with capacitance <0.2pF could not fit in available space
- But still trying to fine suitable package
- The top side of R2 (having HRS140 on bottom) could be used for the placement of resistors.
- There would be enough space to accommodate any package of TVS diode array on R1

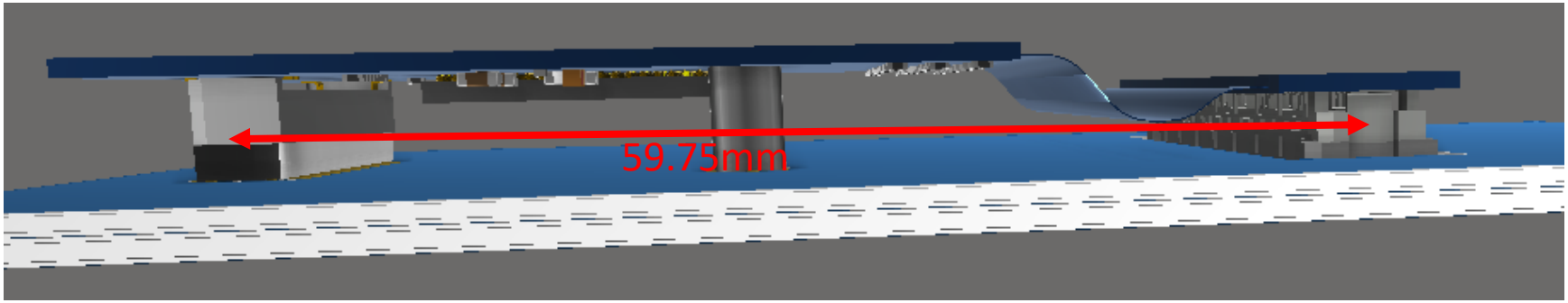




Dimensions/Assembly View







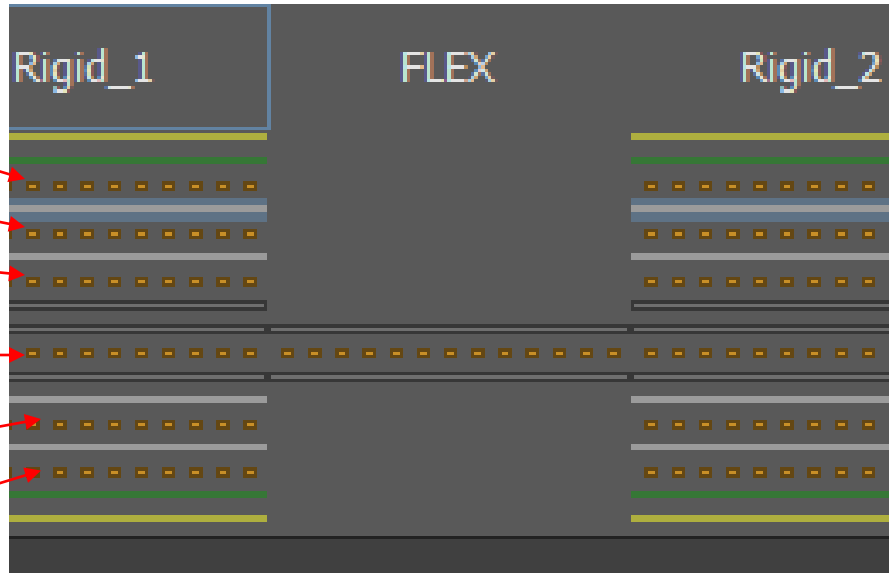
PCB Layout

- Six signal layers have been in rigid regions and single L4 in Flex region
- Blind (100um) Laser Via and Buried (200um) via combinations used (L1-L2, L2-L3 blind -> L3-L4 buried -> L4-L5, L5-L6 blind)
- Input channel routed on layers L4, L5, L6 and no shielding layers added under channels layout to minimize the capacitance
- Digital differential I/Os have 100 Ohm impedance (stackup suggested by PCB fabs)

PCB Layout

		Layer Name	Type	Material	Thickness (mm)
	☑	Top Overlay	Overlay		
	☑	Top Solder	Solder Mask/...	Surface Mat...	0.01199
1	☑	L1-Top	Signal	Copper	0.01801
	☑	Preped	Dielectric	Prepreg	0.1
2	☑	L2	Signal	Copper	0.01801
	☑	Prepeg	Dielectric	Prepreg	0.1
3	☑	L3	Signal	Copper	0.01801
	☑	Core	Dielectric	Core	0.4
	☑	Polymide Core	Dielectric	Core	0.02499
4	☑	L4	Signal	Copper	0.01801
	☑	Polymide Core	Dielectric	Core	0.02499
	☑	Prepeg	Dielectric	Prepreg	0.065
5	☑	L5	Signal	Copper	0.01801
	☑	Prepeg	Dielectric	Prepreg	0.076
6	☑	L6-Solder Side	Signal	Copper	0.01801
	☑	Bottom Solder	Solder Mask/...	Surface Mat...	0.01199

Total Thickness: 0.92301mm



Status

- Schematics are complete reviewed by Francesco and available in Plugin Card's Twiki
- Component placement was done after finalization of VFAT3 package pinout
- The layout is in progress actually was waiting for VFAT3 Package finalization
- Coordinating with rigid flex PCB Fabs for desired impedance adjustments and fabrication point of view
- **The layout will be ready for review by mid October**
- After review the design will be available for fabrication (expectedly PCB Fabs take around 3 Weeks)

Thank You All