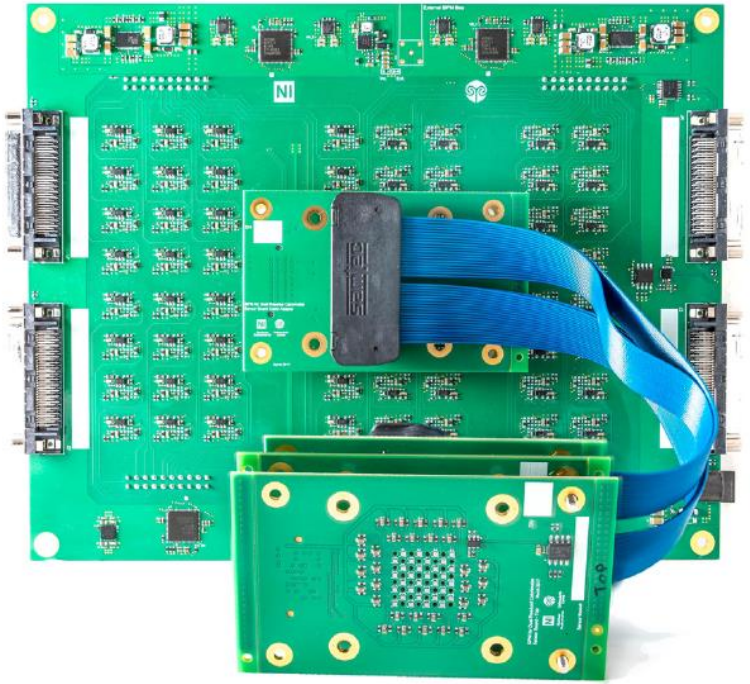
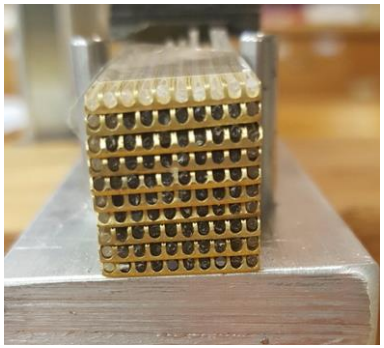
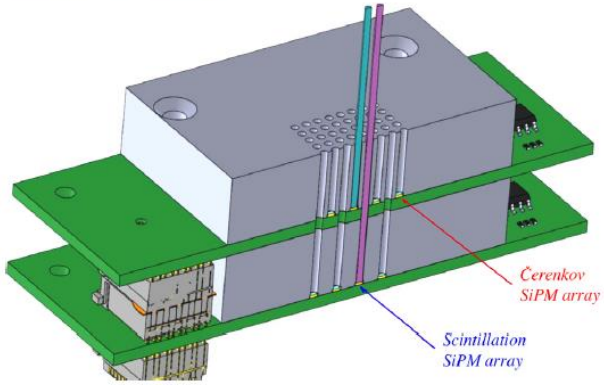
Dual Readout: electronics option

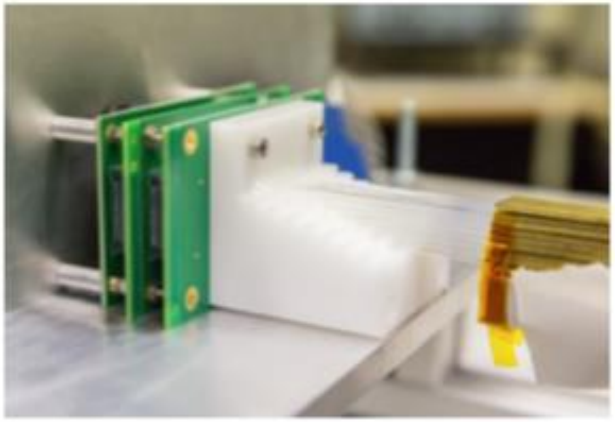
Pictures from the past





10x10 fibers



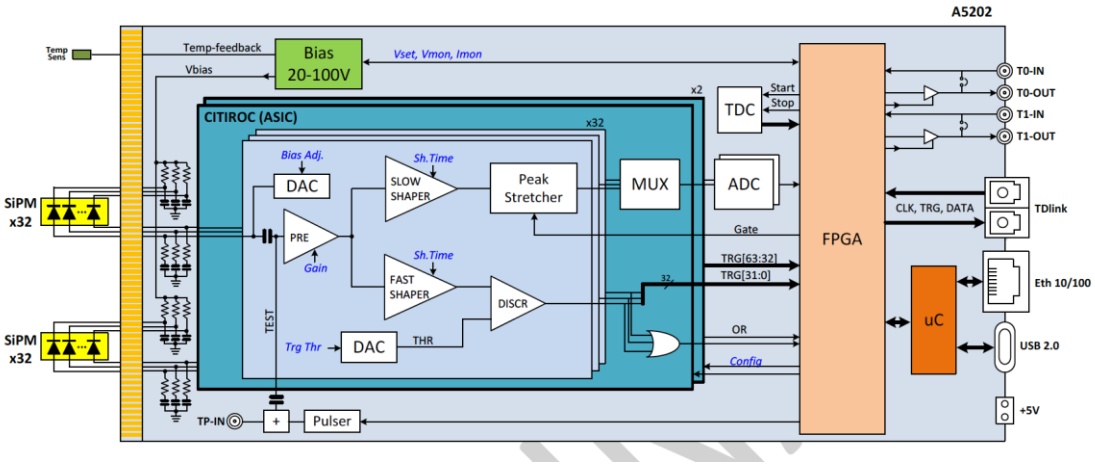


The evaluation boards

A1702 / DT5702

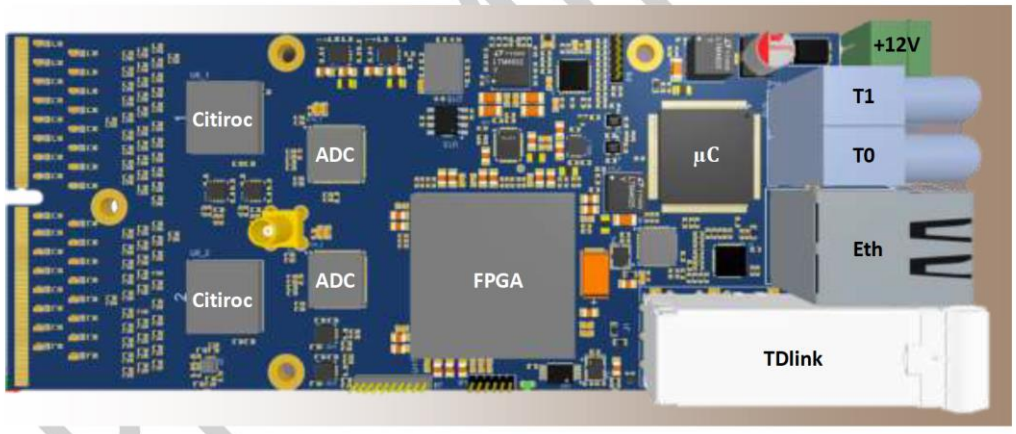
DT5550W

FERS unit - Citirorc: block scheme



The basic principle

- 2 Citiroc1A (64 ch)
- Timing with a TDC implemented into the FPGA (≈ 0.5 ns)
- 2 ADC to measure the charge
- 1 HV power supply (20 – 100V) with temperature compensation
- Interface for readout

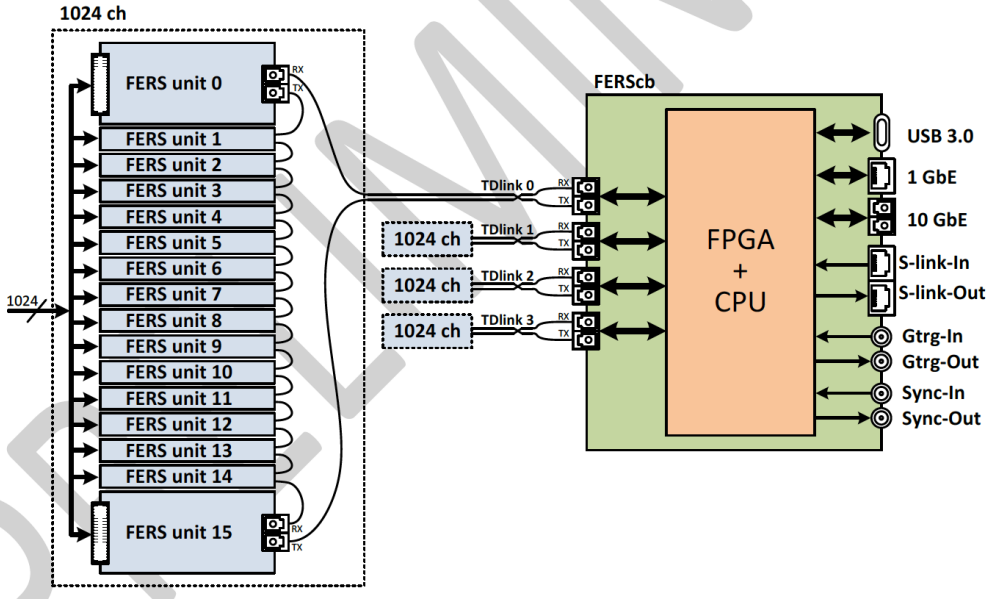


60 mm

150 mm

How to handle a "medium-size" calorimeter?

If the Citirorc1A qualification will fulfils our requirements we still need a compact and scalable solution for a test beam



The basic principle

- FERS-unit can be used in standalone or connected to the system
- Up to 16 FERS-unit can be connected in daisy-chain (FERSnet)
- The FERSnet data throughput is up to 200 MB/s
- The FERScb is a data collector housing 4 high speed optical link (TDLink)
- The connection to the host PC is performed with a 10 Gbit ethernet
- The FERScb has an embedded ARM processor (Quad Core) running Linux for data processing / data compression