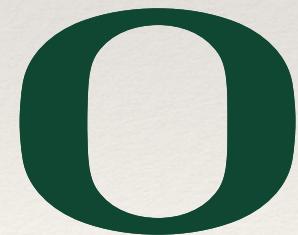


May 16, 2022

# The SiD Digital ECal based on Monolithic Active Pixel Sensors

Jim Brau,  
University of  
Oregon



UNIVERSITY OF  
OREGON

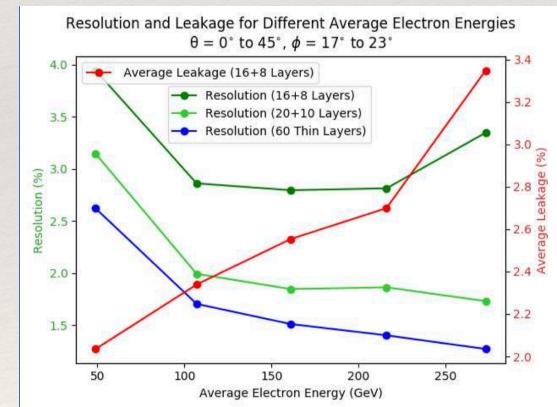
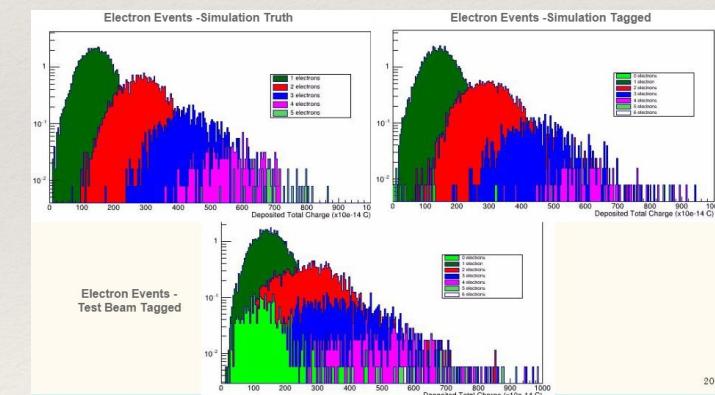
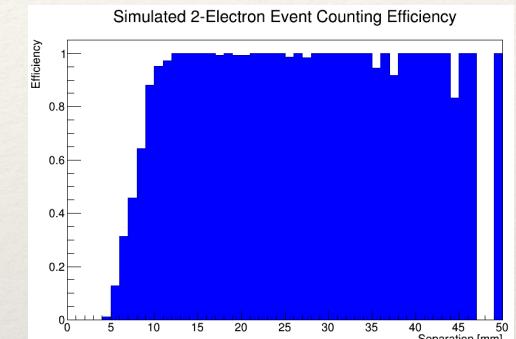
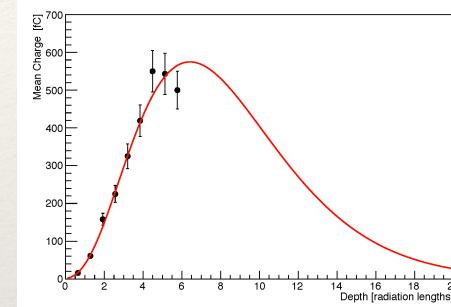
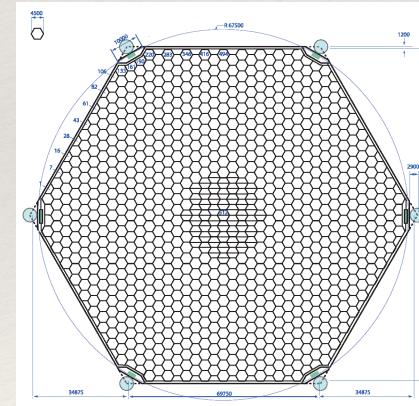
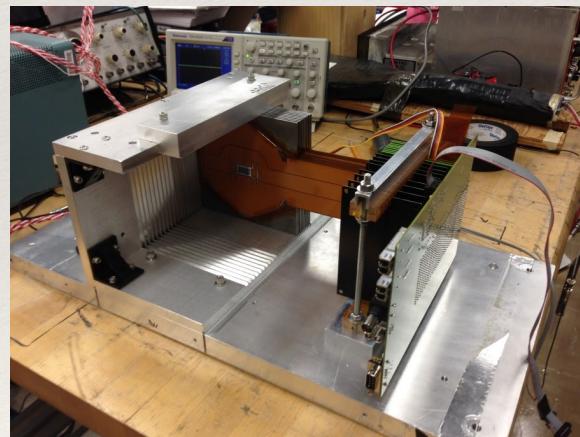
Research partially supported  
by the U.S. Department of Energy

on behalf of  
the SiD MAPS Collaboration  
(M. Breidenbach, L. Rota,  
C. Vernieri et al.)

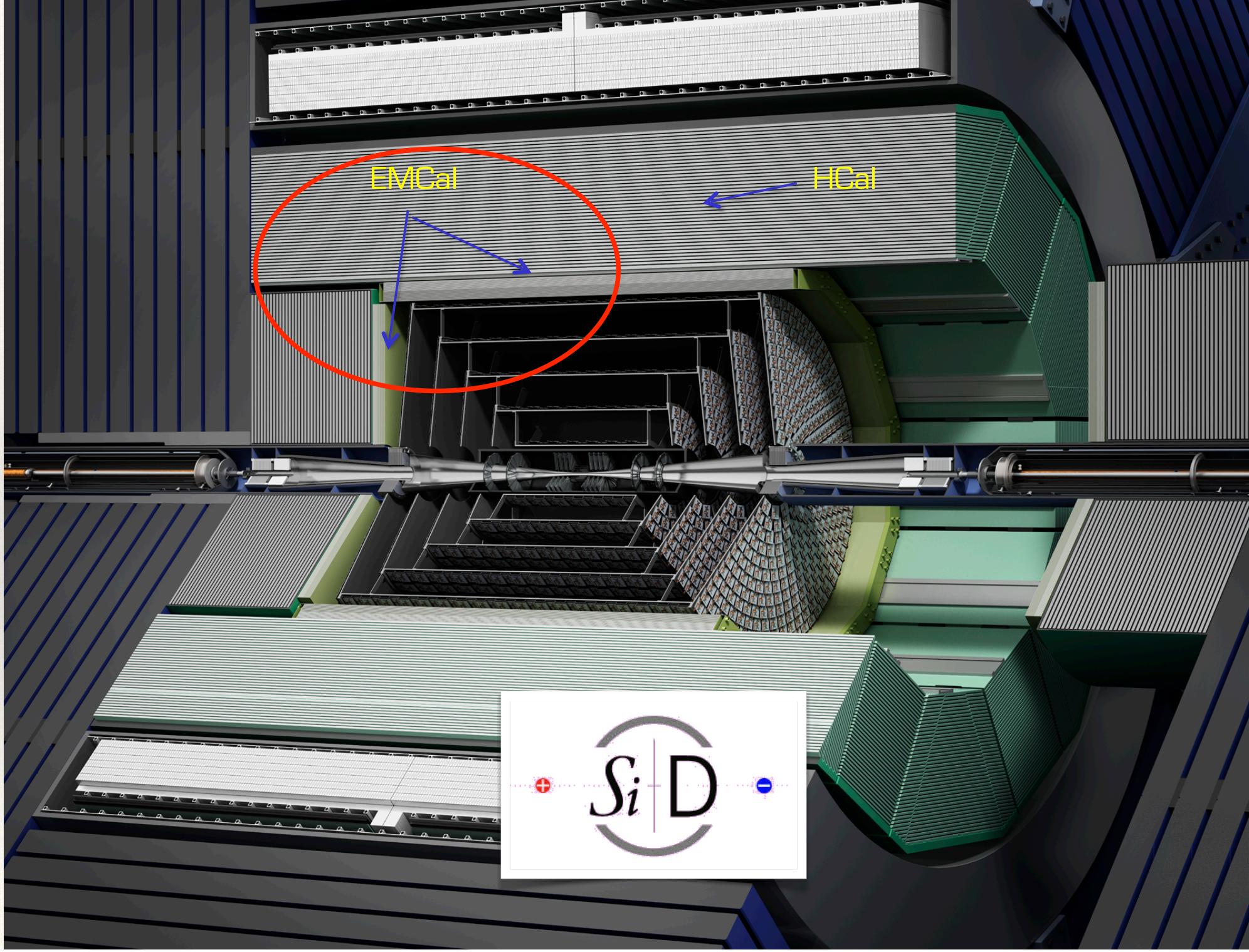
Reference: [arXiv:2203.07626](https://arxiv.org/abs/2203.07626) [physics.ins-det]

# SiD TDR Design Based on Analog Silicon Pixels

- ❖ SiD ILC TDR ECal design successfully tested in 9 layer SLAC beam test.
  - ❖ 13 mm<sup>2</sup> pixels on 6 inch wafers
  - ❖ 1024 pixels per wafer
  - ❖ KPiX readout bump-bonded to sensor



New development to improve design based on 25 μm x 100 μm digital MAPS.  
 Calorimetry application largely emphasizing Particle Flow Analysis.



# Large area MAPS for SiD tracker & ECal

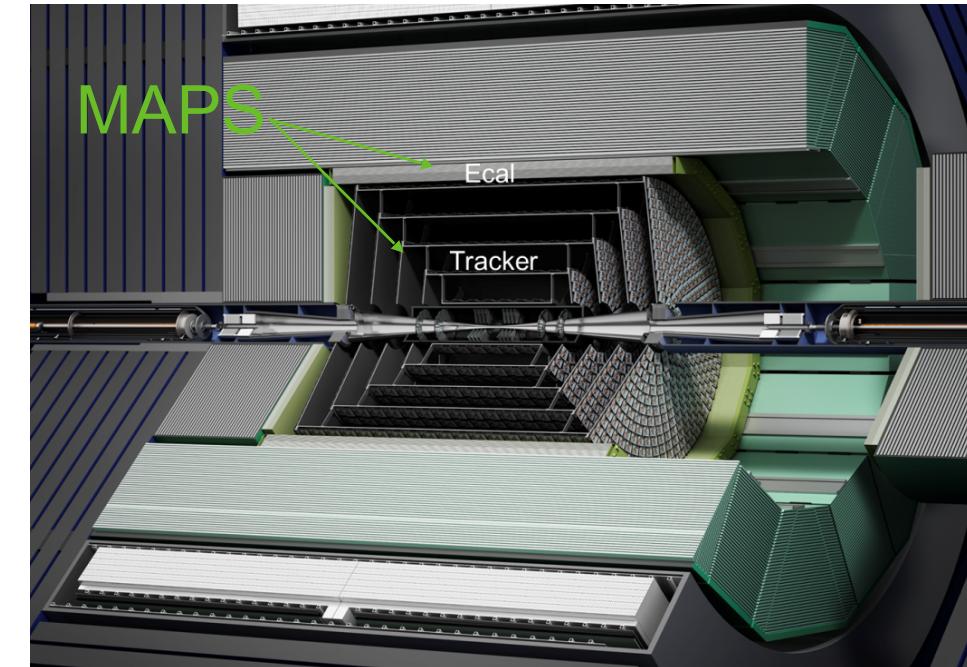
SLAC

## Benefits of large-area MAPS:

- Standard CMOS foundry, low resistivity: **cost ↓**
- Sensing element and readout electronics on same die
  - In-pixel amplification: **noise ↓, power ↓**
  - No need for bump-bonding: **cost ↓**
- Area  $> 10 \times 10 \text{ cm}^2 \rightarrow$  enable  $O(1) \text{ m}^2$  modules

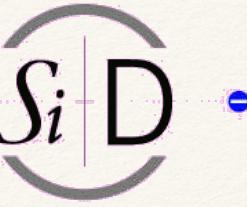
## Several design challenges:

- Large on-die variations, mismatch
- Yield
- Stitching layout rules
- Distribution of power supply
- Distribution of global control signals/references



An example of the SiD Tracker and the ECal overall design

**Goals of R&D: find solutions and explore novel design techniques**

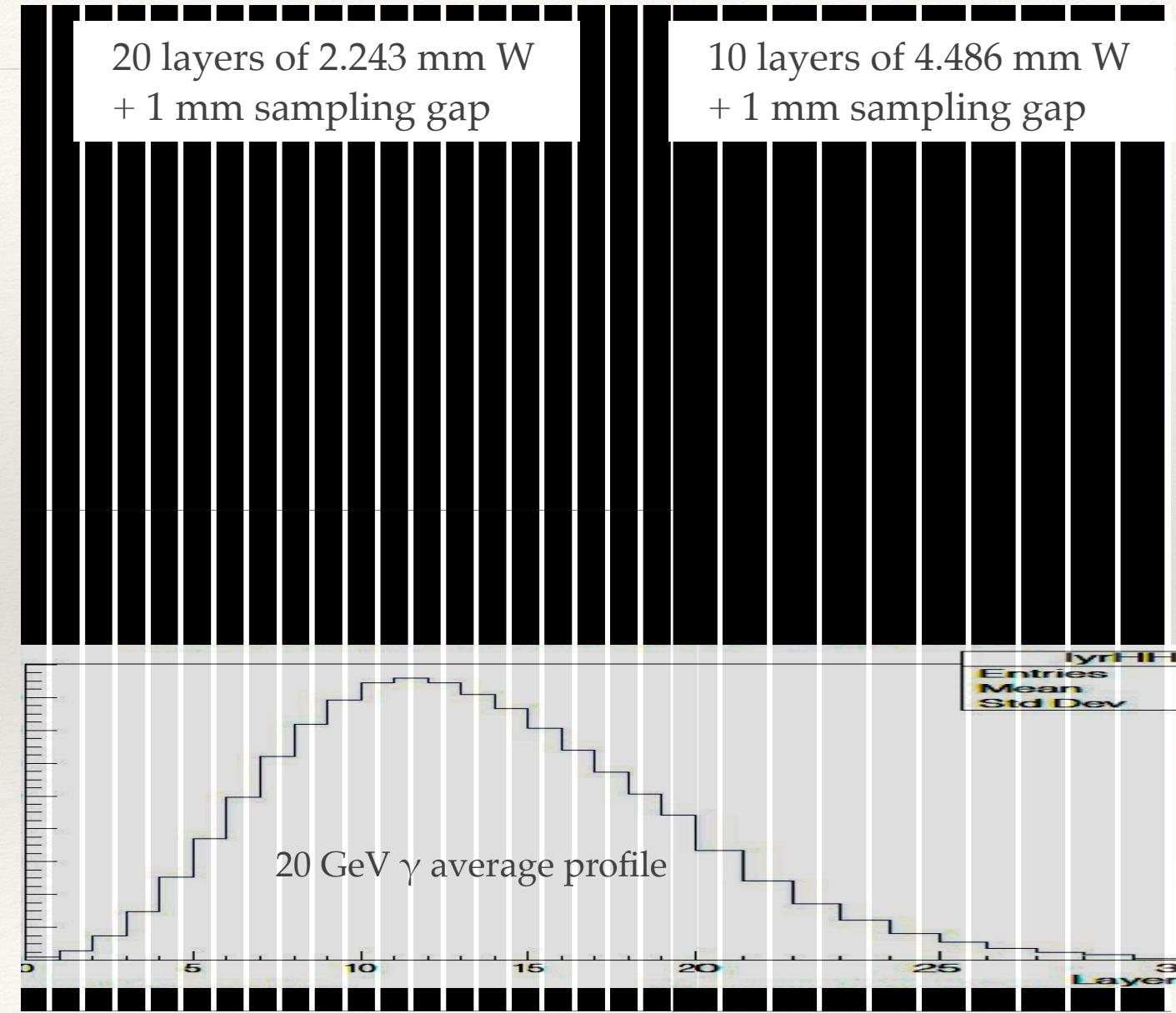


# Model of longitudinal structure of SiD ECal

Total = 27  $X_0$



Minimize sampling gap to achieve optimal Moliere radius and shower separation

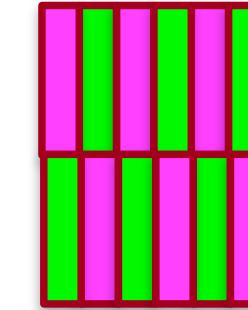


HCAL

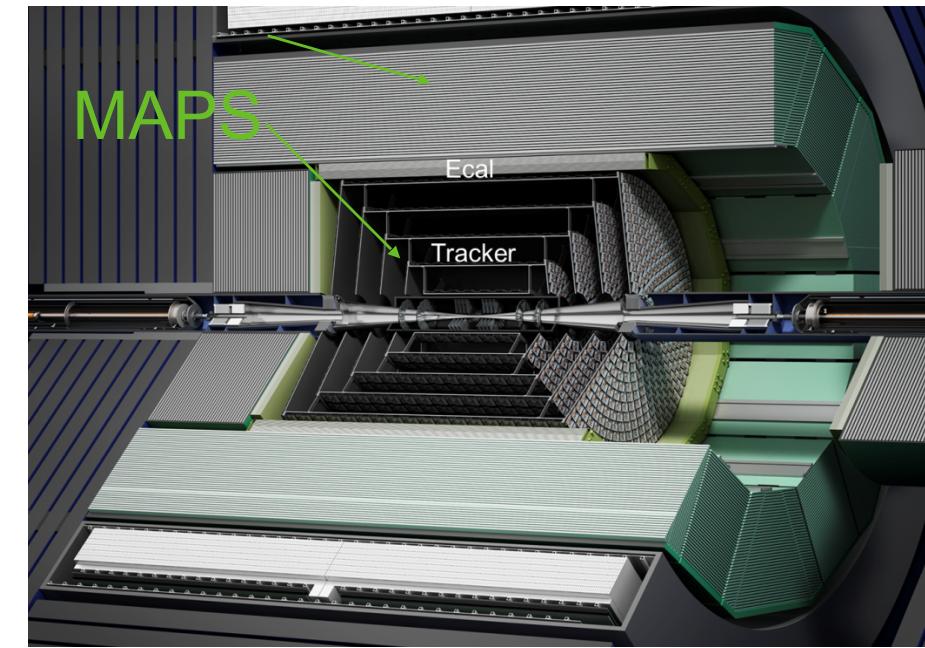
# Main specifications for Large Area MAPS development

TID-AIR **SLAC**

Parameter	Value	Notes
<b>Min Threshold</b>	140 e <sup>-</sup>	0.25*MIP with 10 $\mu\text{m}$ thick epi layer
<b>Spatial resolution</b>	7 $\mu\text{m}$	In bend plane, based on SiD tracker specs
<b>Pixel size</b>	25 x 100 $\mu\text{m}^2$	Optimized for tracking
<b>Chip size</b>	10 x 10 cm <sup>2</sup>	Requires stitching on 4 sides
<b>Chip thickness</b>	300 $\mu\text{m}$	<200 $\mu\text{m}$ for tracker. Could be 300 $\mu\text{m}$ for EMCal to improve yield.
<b>Timing resolution (pixel)</b>	~ ns	Bunch spacing: C <sup>3</sup> strictest with 5.3->3.5 ns; ILC is 554 ns
<b>Total Ionizing Dose</b>	100 kRads	Total lifetime dose, not a concern
<b>Hit density / train</b>	1000 hits / cm <sup>2</sup>	
<b>Hits spatial distribution</b>	Clusters	Due to jets
<b>Balcony size</b>	1 mm	Only on one side, where wire-bonding pads will be located.
<b>Power density</b>	20 mW / cm <sup>2</sup>	Based on SiD tracker power consumption: 400W over 67m <sup>2</sup>



25 x 100  $\mu\text{m}^2$   
Ecal performance  
same as  
50 x 50  $\mu\text{m}^2$

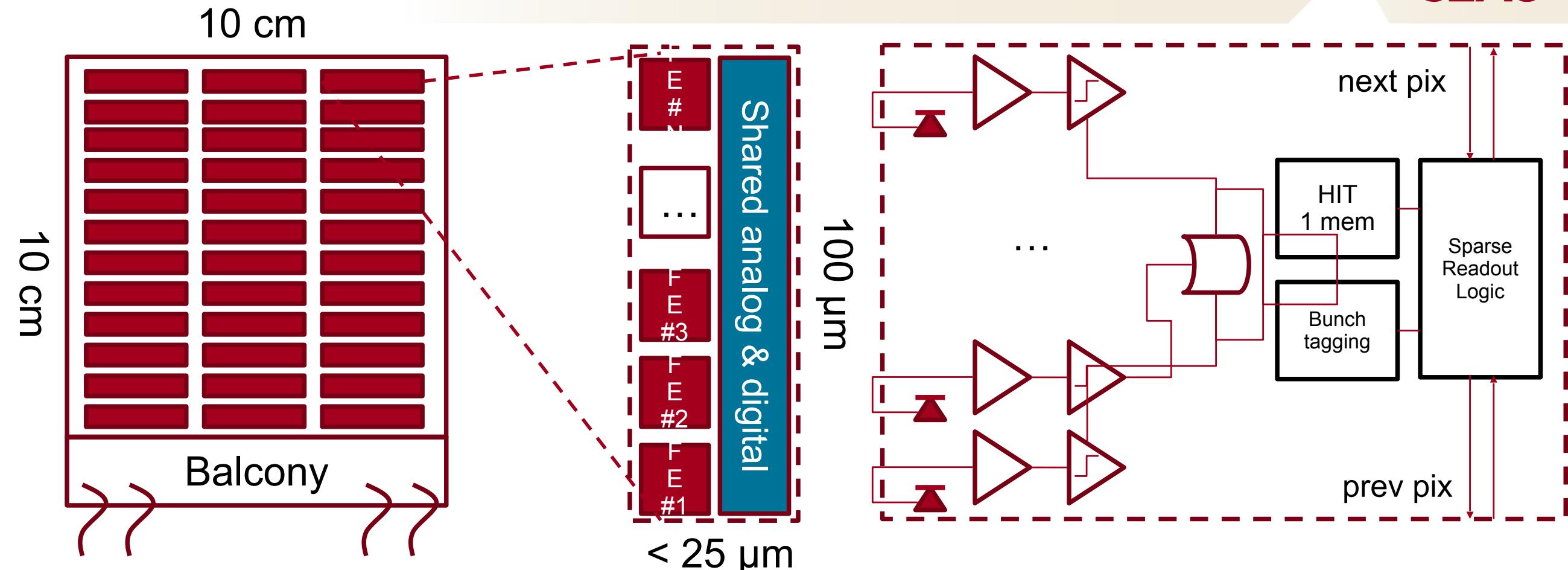


SiD Tracker and the ECal

L. Rota

# Overall architecture

SLAC



- Expected 1 hit/pixel/bunch train → integrate charge through whole bunch train → store 1 hit/pixel
- Segmentation of pixel front-end connected to common digital logic. See also CLIC TDR [1]
- Optimal segmentation of pixel front-ends will depend on sensor performance

[1] <https://cds.cern.ch/record/2643766/files/CLICdp-Conf-2018-008.pdf>

# Power during integration phase

SLAC

Phase:



- Avg power consumption reduced by power-cycling  
... but **peak** current draw is not!
- Assuming 1 $\mu$ A/pixel, current draw is ~16 A
- Resistance of metal lines not negligible over 10 cm → significant voltage drop

Possible strategies:

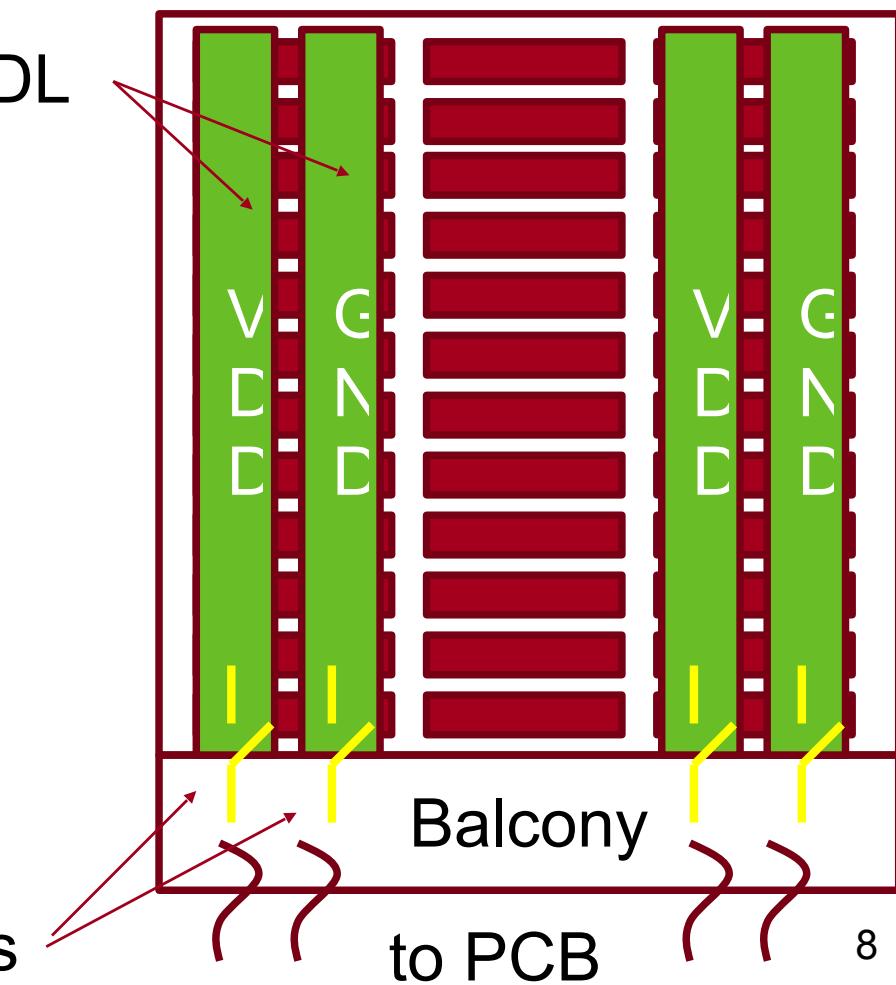
- Bypass caps distributed over sensor
- EMCAL flat cable distributes power to all reticule bump connections
- Re-distribution layer with thick metal deposited on-top
- Discuss with foundry about having more/thicker metal layers

Need to investigate strategies on how to cope with shorts:

Add “switches” for each column/cluster → if a short detected, DAQ disables the column during initial power-up sequence

L. Rota

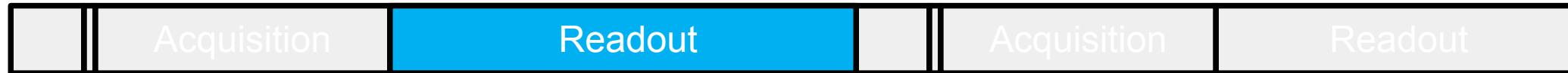
Switches



# Power during readout phase

SLAC

Phase:



Design an **asynchronous** readout logic with **zero-suppression**:

- Only pixels with HIT information are read-out by balcony
- Need to transmit data from pixel to balcony over ~10 cm lines, with large interconnection RC → minimize bit transitions → **power ↓**
- Remove clock → **power ↓**
- Handshaking between pixel and balcony ensures proper data transmission even with large on-die variations
- First simulations done, data throughput meets specs: ~200 ns to transmit one “hit” from pixel to balcony

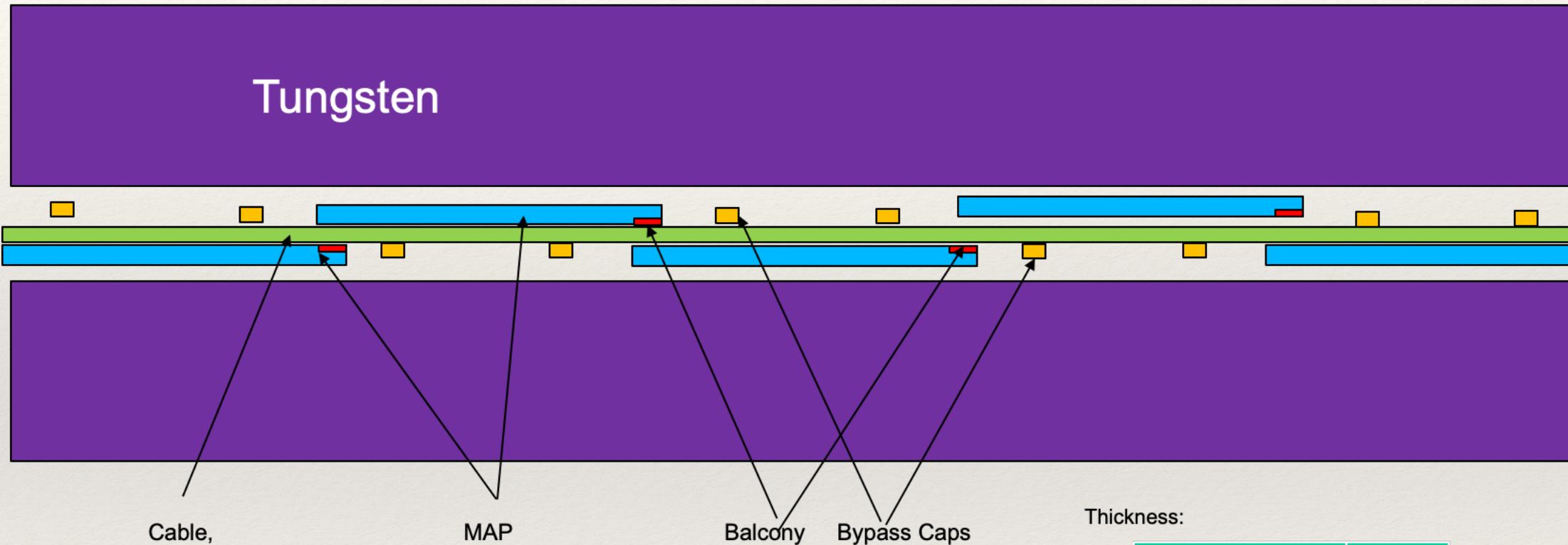
# Large area MAPS: next steps



- SLAC working in WP1.2 collaboration at CERN
  - ALICE ITS3 upgrade main driver
- Design 1.5x1.5 mm<sup>2</sup> prototype with few pixels to test sensor + front-end
- Submission of first prototype in 2022
  - Small-scale prototype in late 2022
- Study sensor performance on TowerSemi 65 nm process
  - TCAD simulations to optimize sensor design
  - Feedback from WP 1.2 measurements done at CERN
- Study bunch-tagging strategy (linear collider specific)
  - Analog-based: ramp, with low-res ADC in balcony (~8 bits)
  - Digital-based: local DLL for Time-to-Digital Conversion

# Gap Structure with MAPS

*Not to scale*



ONE CABLE IN GAP DESIGN

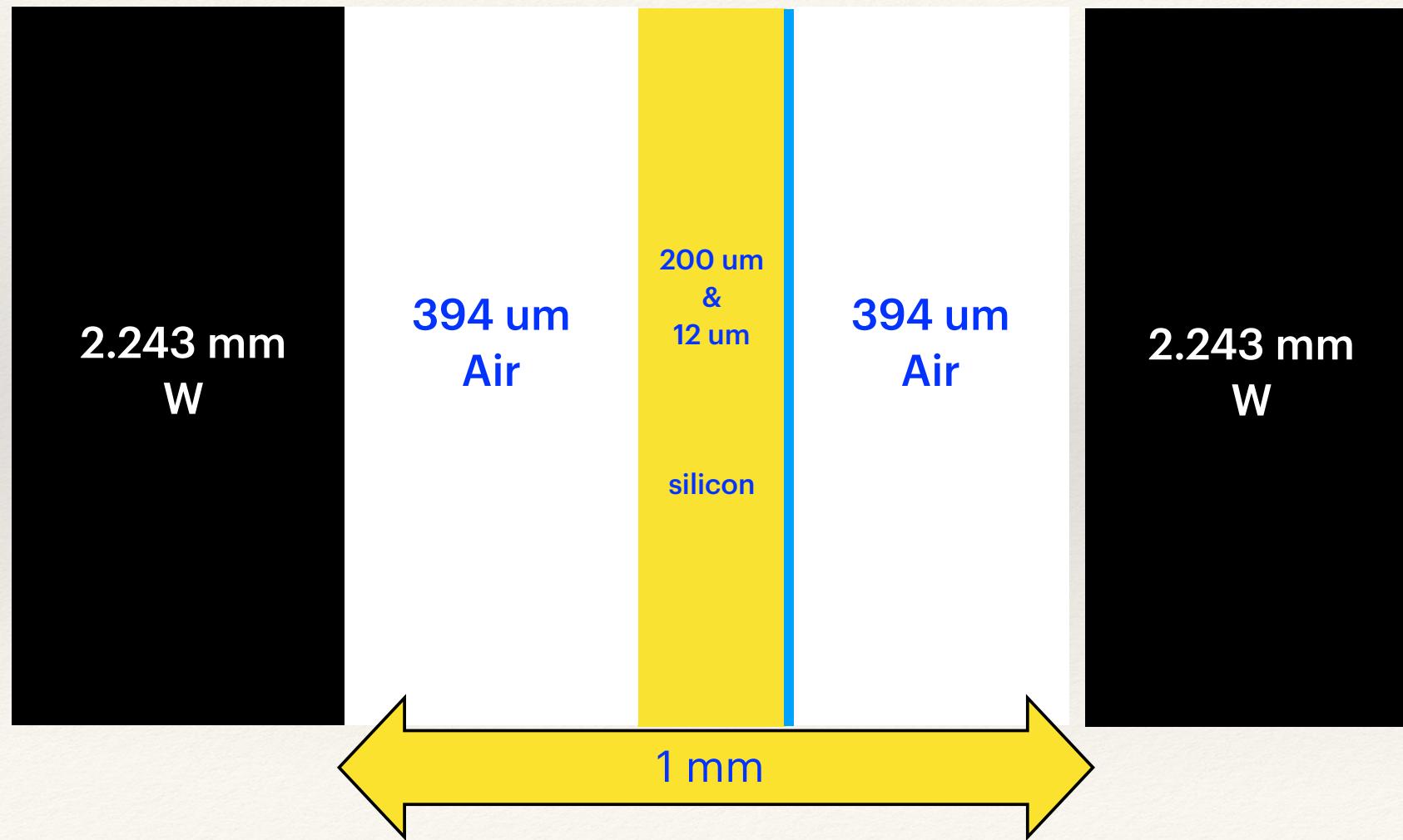
Gap structure with MAPs on one cable  
(or pcb). Requires bump bonding

This may well need  
adjustment following more  
cable design

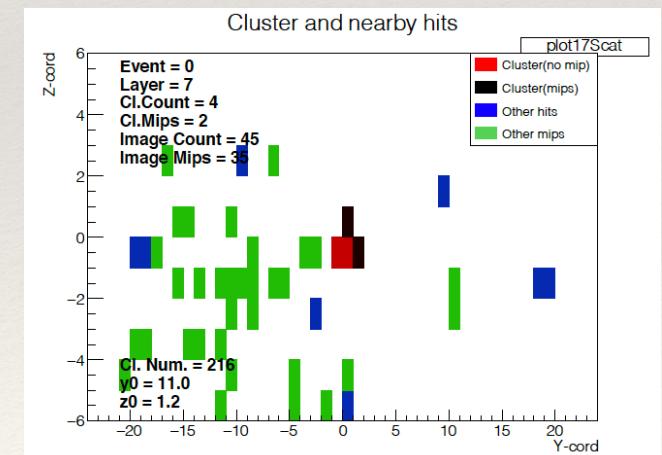
M. Breidenbach

# Sampling Gap Simulation - SiD MAPS Digital ECal

Geant4 simulated silicon gap structures



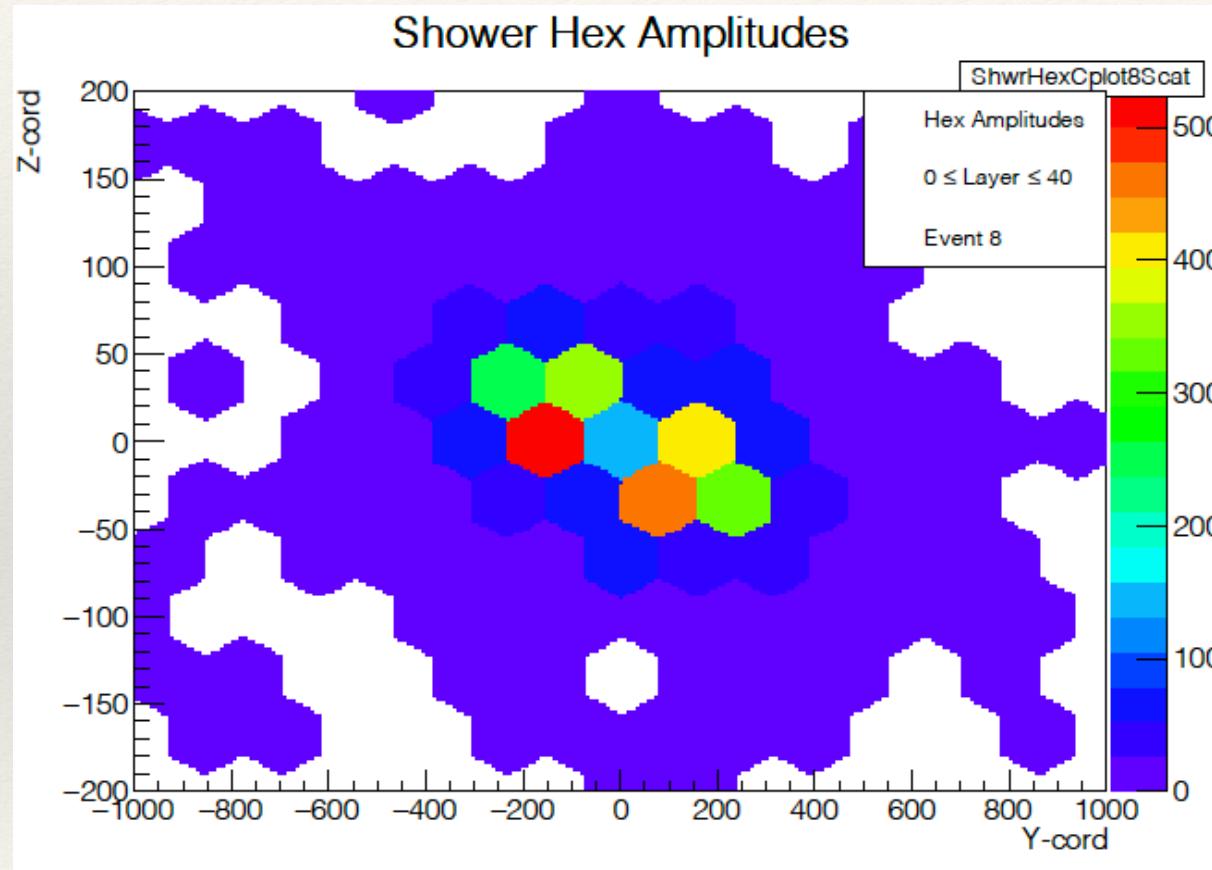
**Assumption:**  
**Pixel threshold =**  
 $1 \text{ keV} \approx 270 \text{ e's}$   
**Future:**  
**More detailed**  
**gap model**



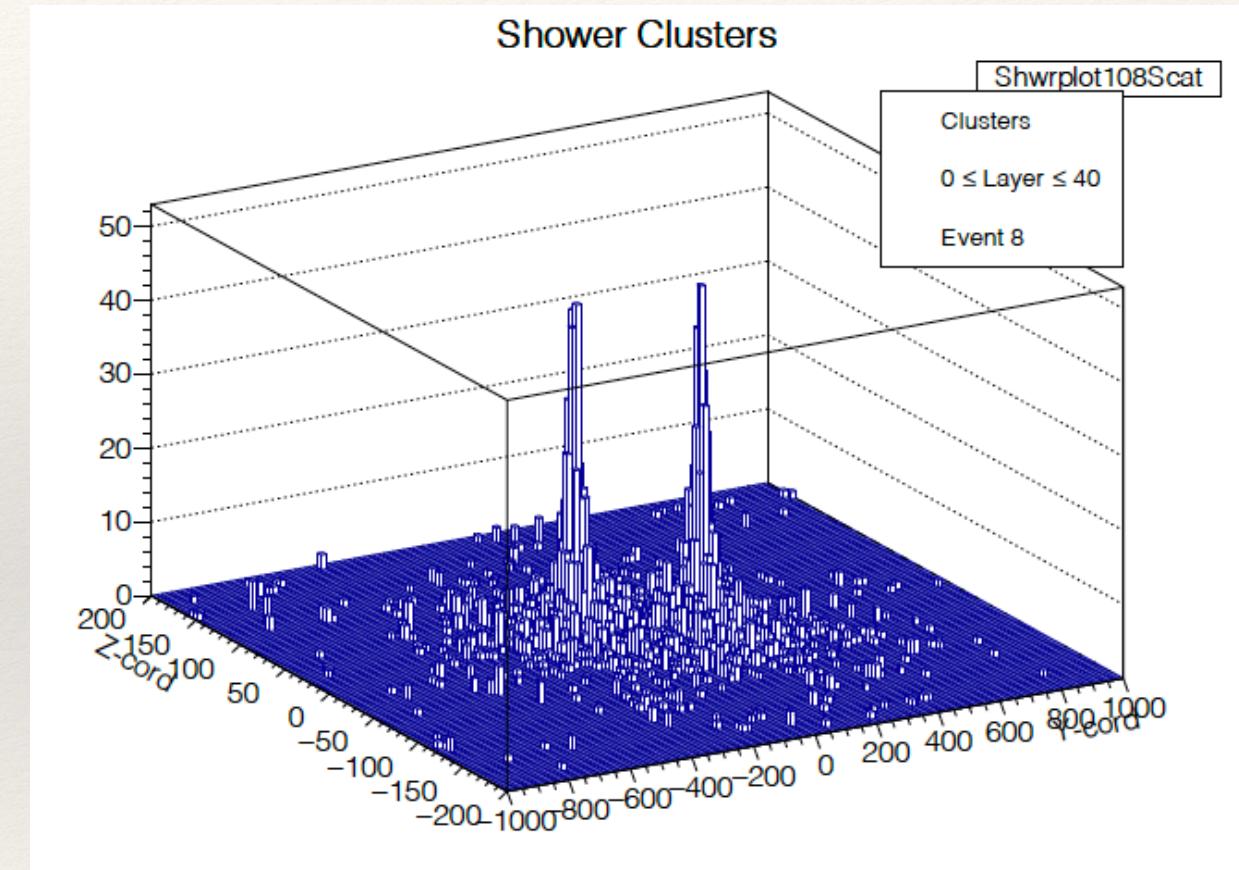
Typical hits distribution

# Multi-shower of SiD MAPS compared to SiD TDR

$40 \text{ GeV } \pi^0 \rightarrow \text{two } 20 \text{ GeV } \gamma's$



SiD TDR hexagonal sensors  
13 mm<sup>2</sup> pixels



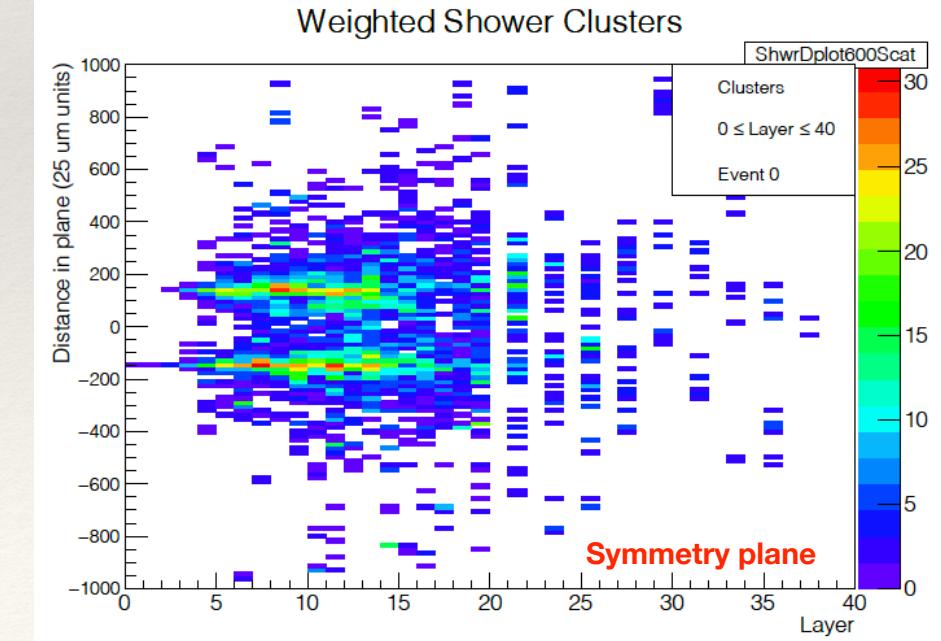
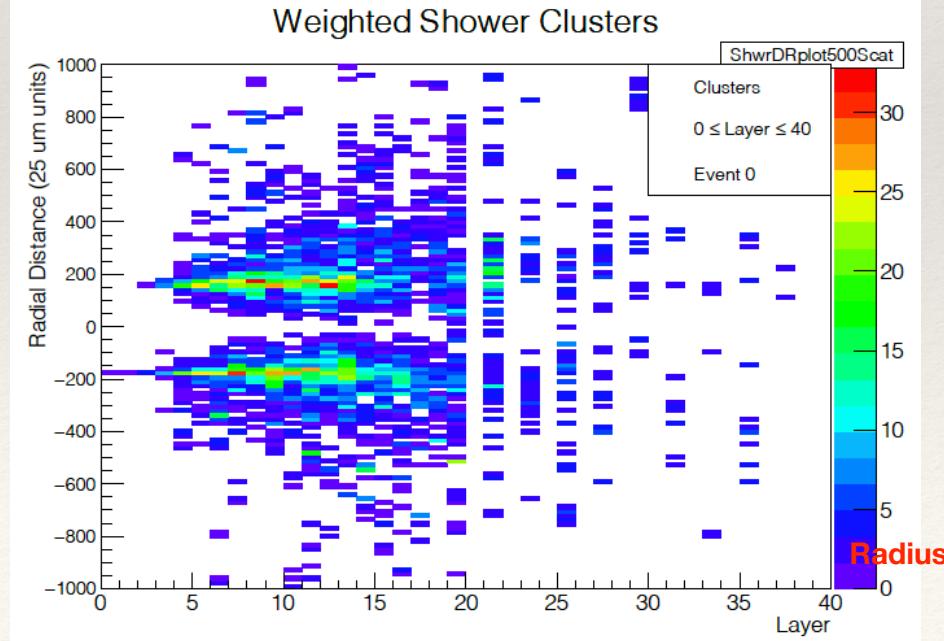
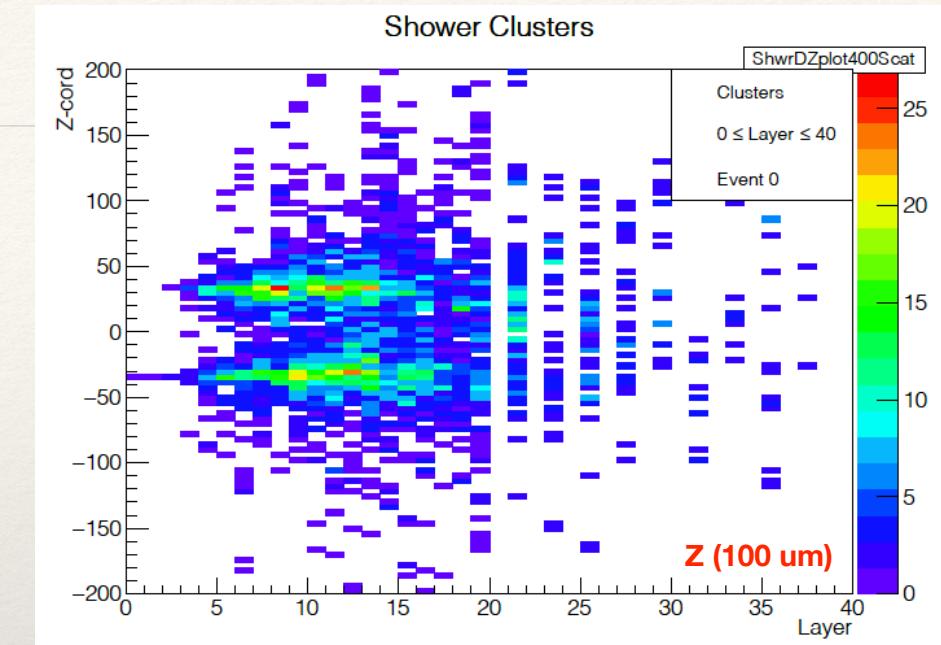
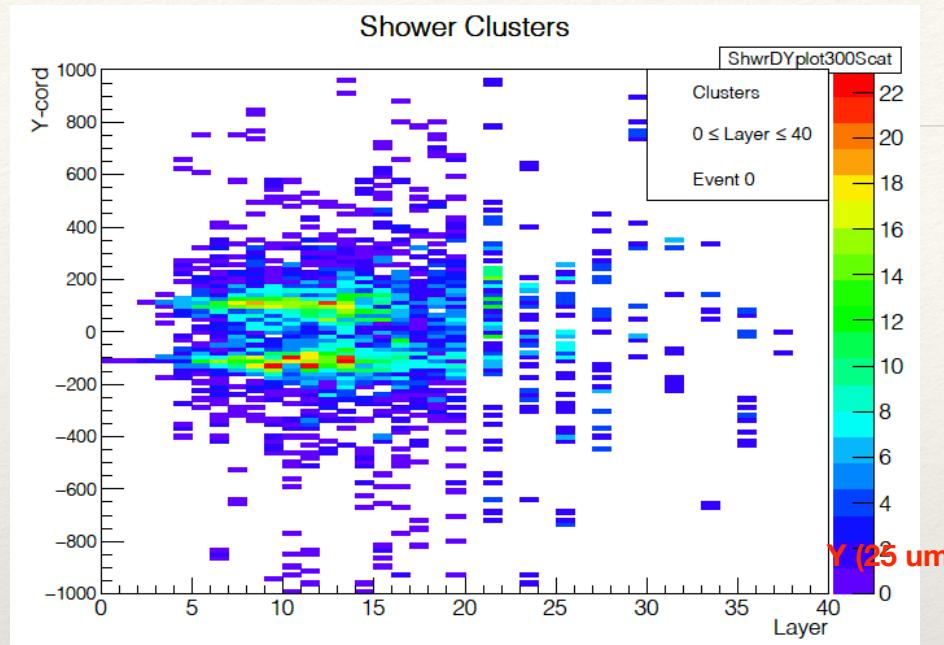
New SiD fine pixel sensors  
25 μm x 100 μm pixels

# 40 GeV $\pi^0 \rightarrow$ two 20 GeV $\gamma$ 's

Vertical bin  
400  $\mu\text{m}$

J. Brau - 16 May 2022

SiD Digital ECal based on Silicon MAPS

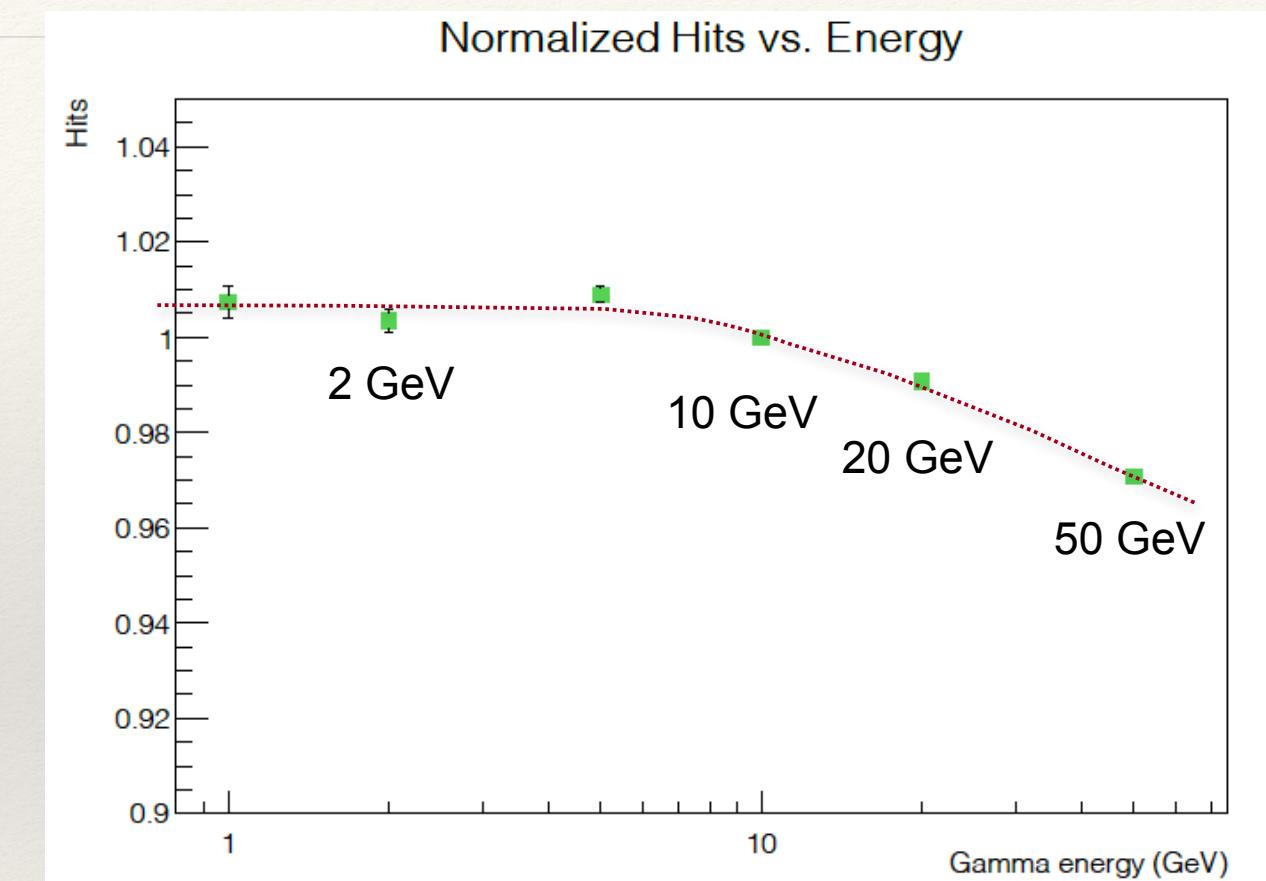
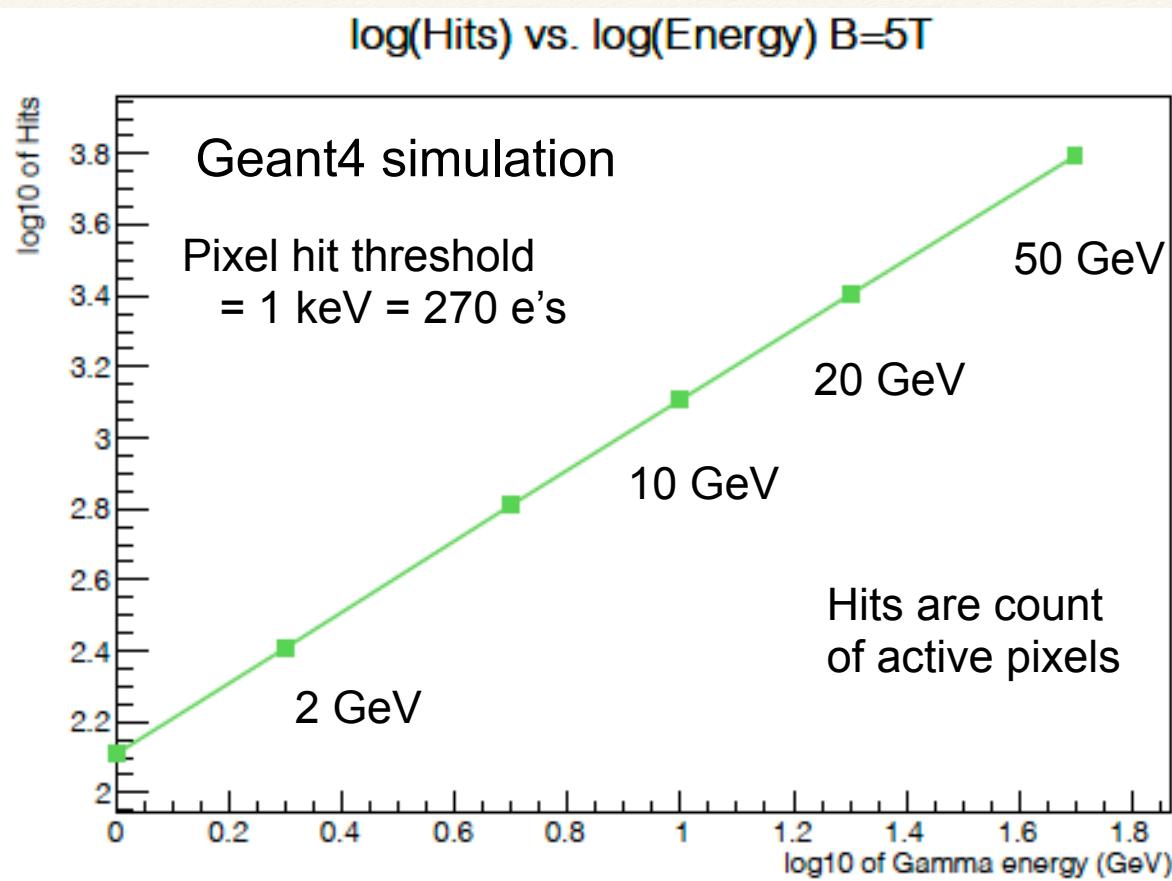


# Performance simulation - Overview

## Geant4

- ❖ Linearity
- ❖ Energy resolution
  - ❖ Ideal - count mips - sets unreachable goal
  - ❖ Simplest approximation to mips - count digitized hits
  - ❖ Improvement - count clusters of hits - reduce fluctuations
  - ❖ Optimized - apply weights cluster counts from cluster properties
- ❖ Localization
  - ❖ Multiple shower separation
- ❖ Note - SiD's 5 T B field degrades resolution ~5%

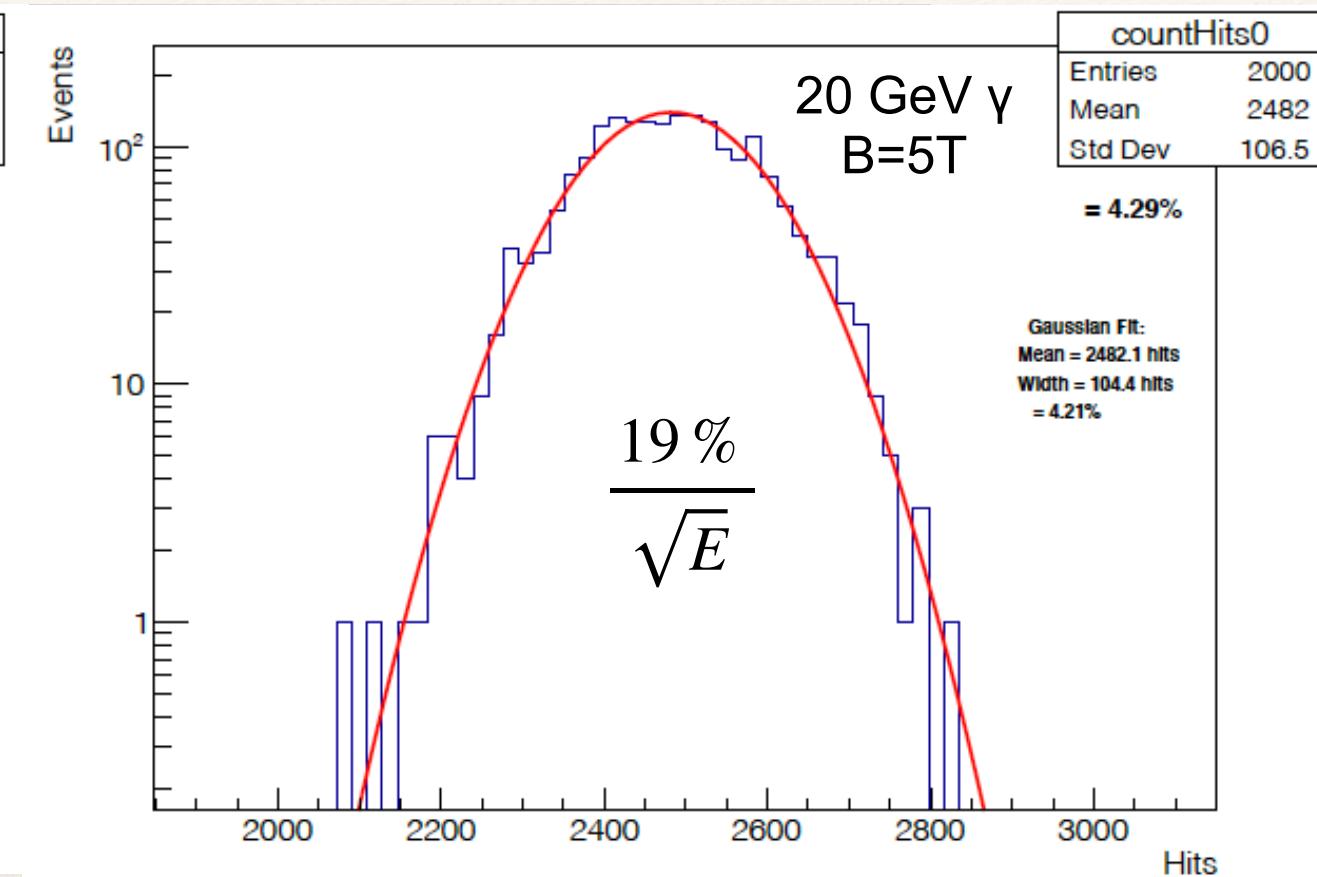
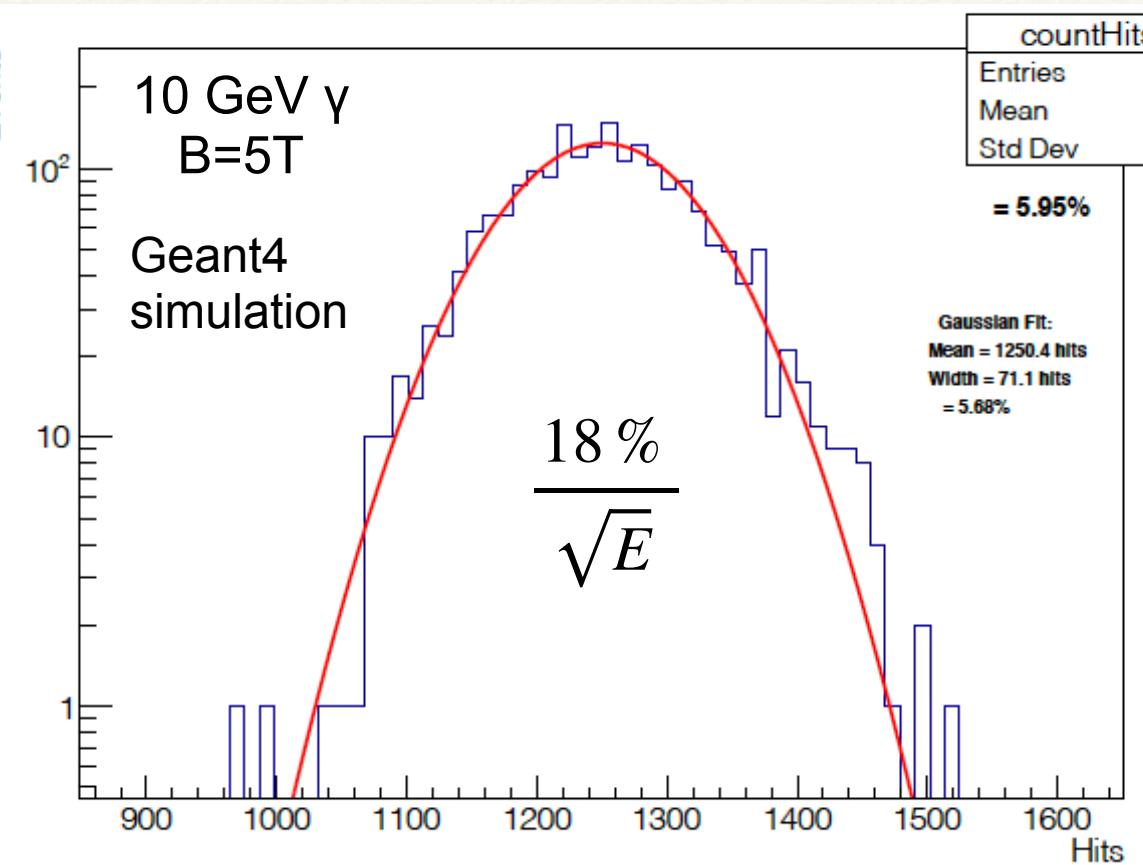
# Linearity of response (counting hits in $\gamma$ showers)



Non-linearity due to differing response and counting in thin ( $0.7 X_0$ ) and thick ( $1.4 X_0$ ) layers (and uncorrected leakage).

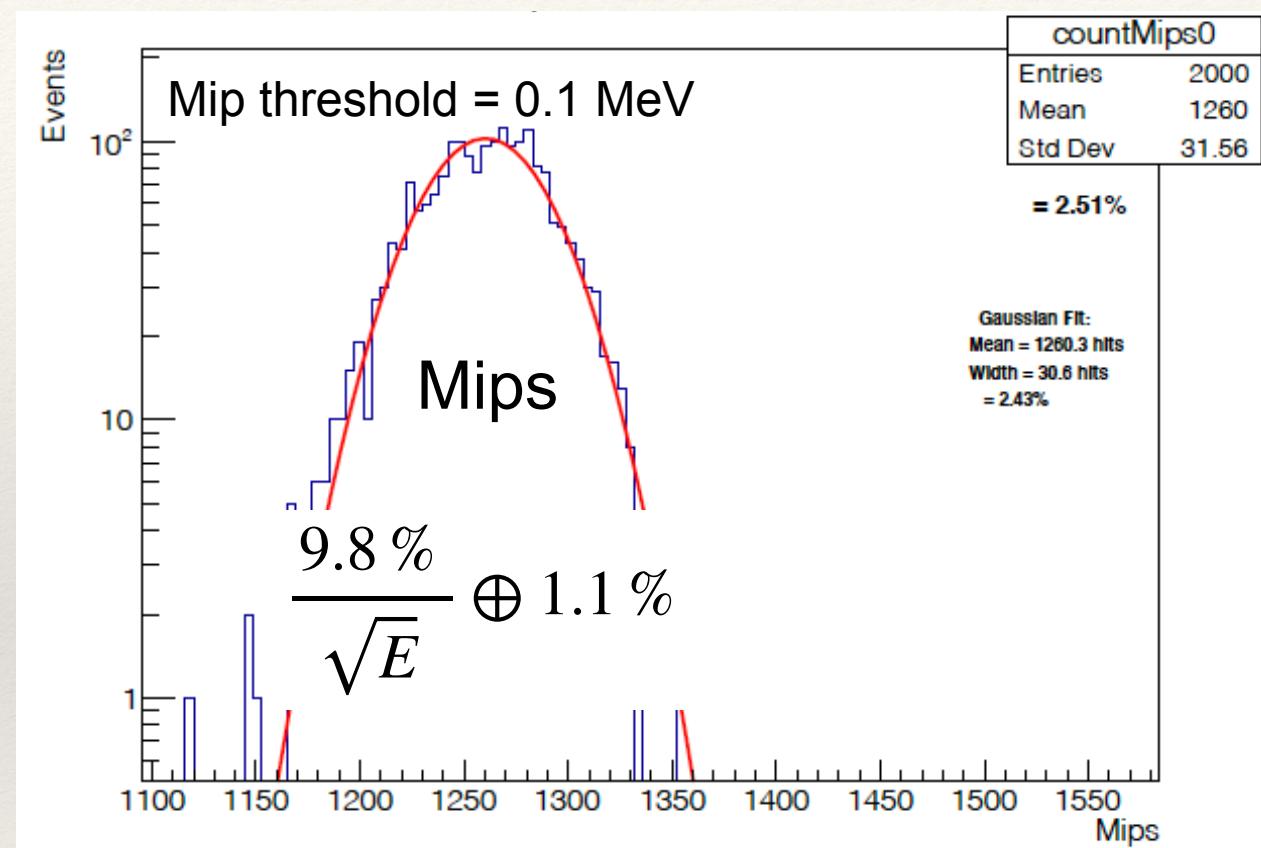
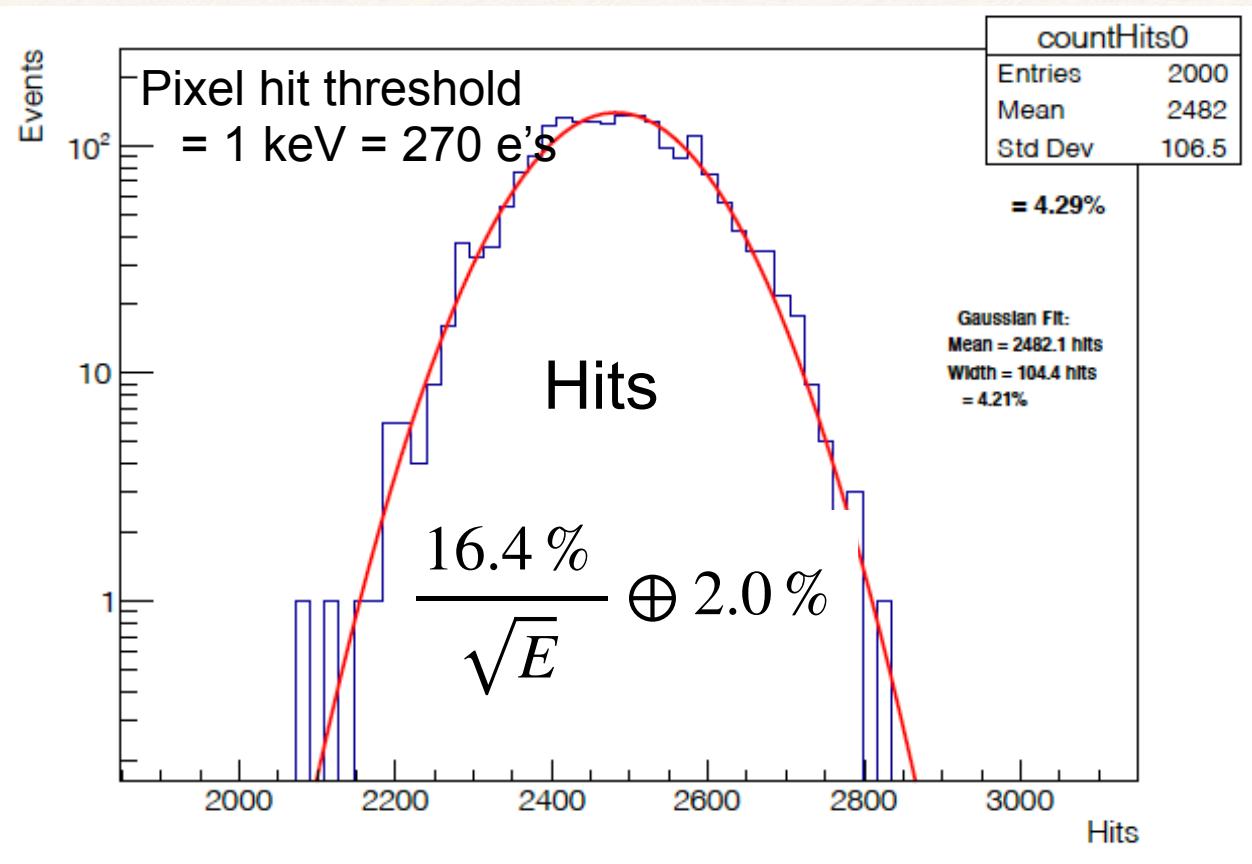
Pixel hit threshold  
= 1 keV = 270 e's

## Hits resolution - count active pixels



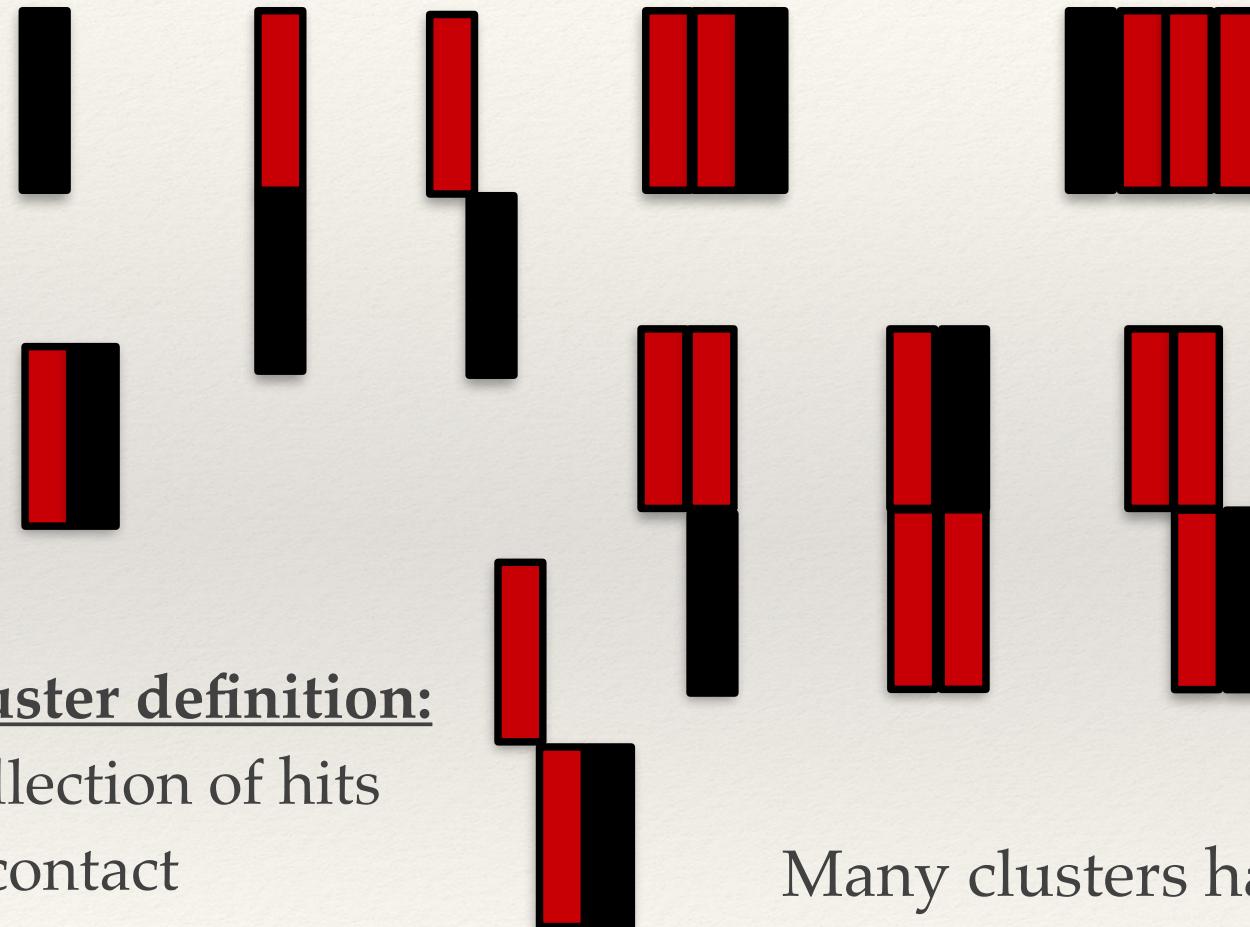
ILC TDR anticipates  $\frac{17 \%}{\sqrt{E}} \oplus 1 \% \quad$  for the SiD SiW ECal; **but we can do better.**

# Pixel counts (hits & mips) - 20 GeV $\gamma$ (B=5T)



Ultimate goal is to count mips based on hit distribution.  
Potential to improve resolution compared to hit count.

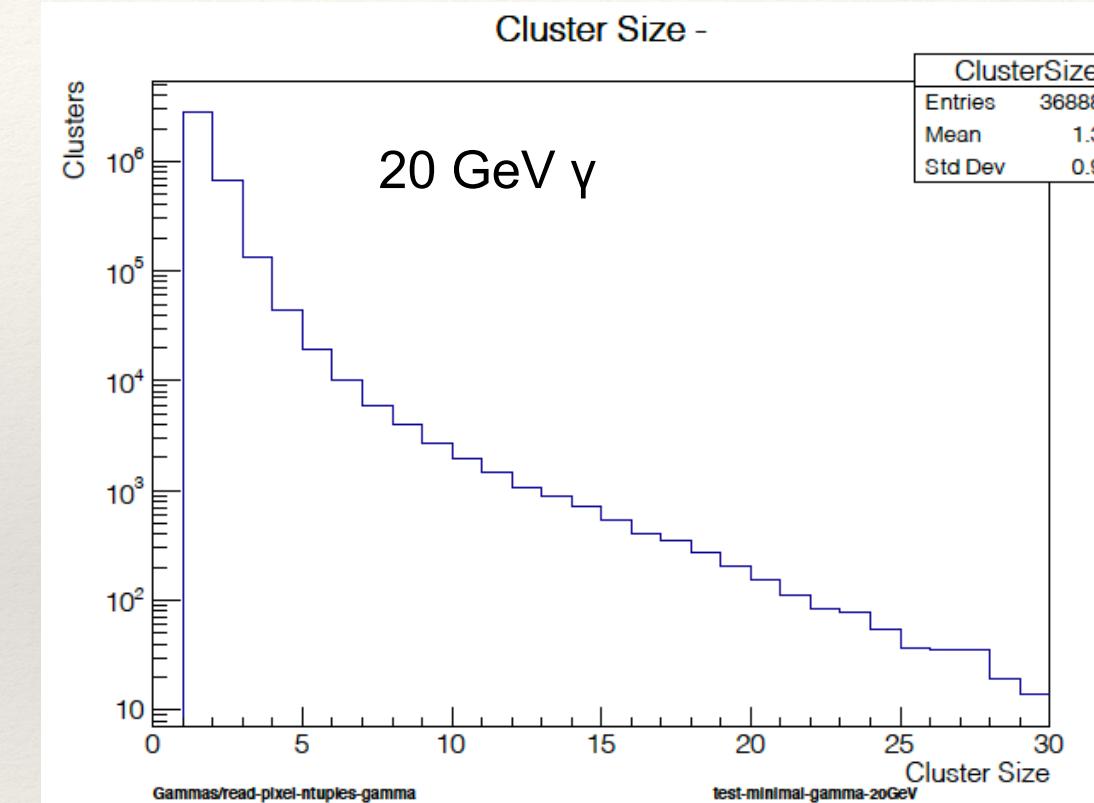
# Hits appear in clusters (size 1, 2, 3,...)



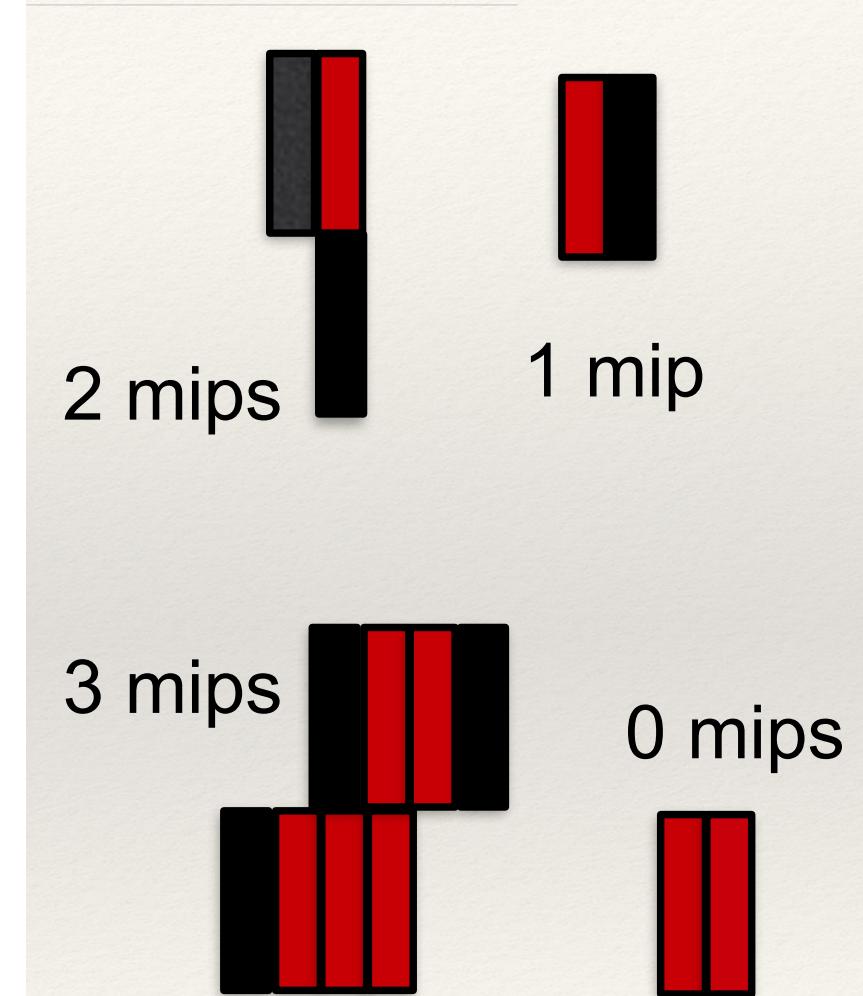
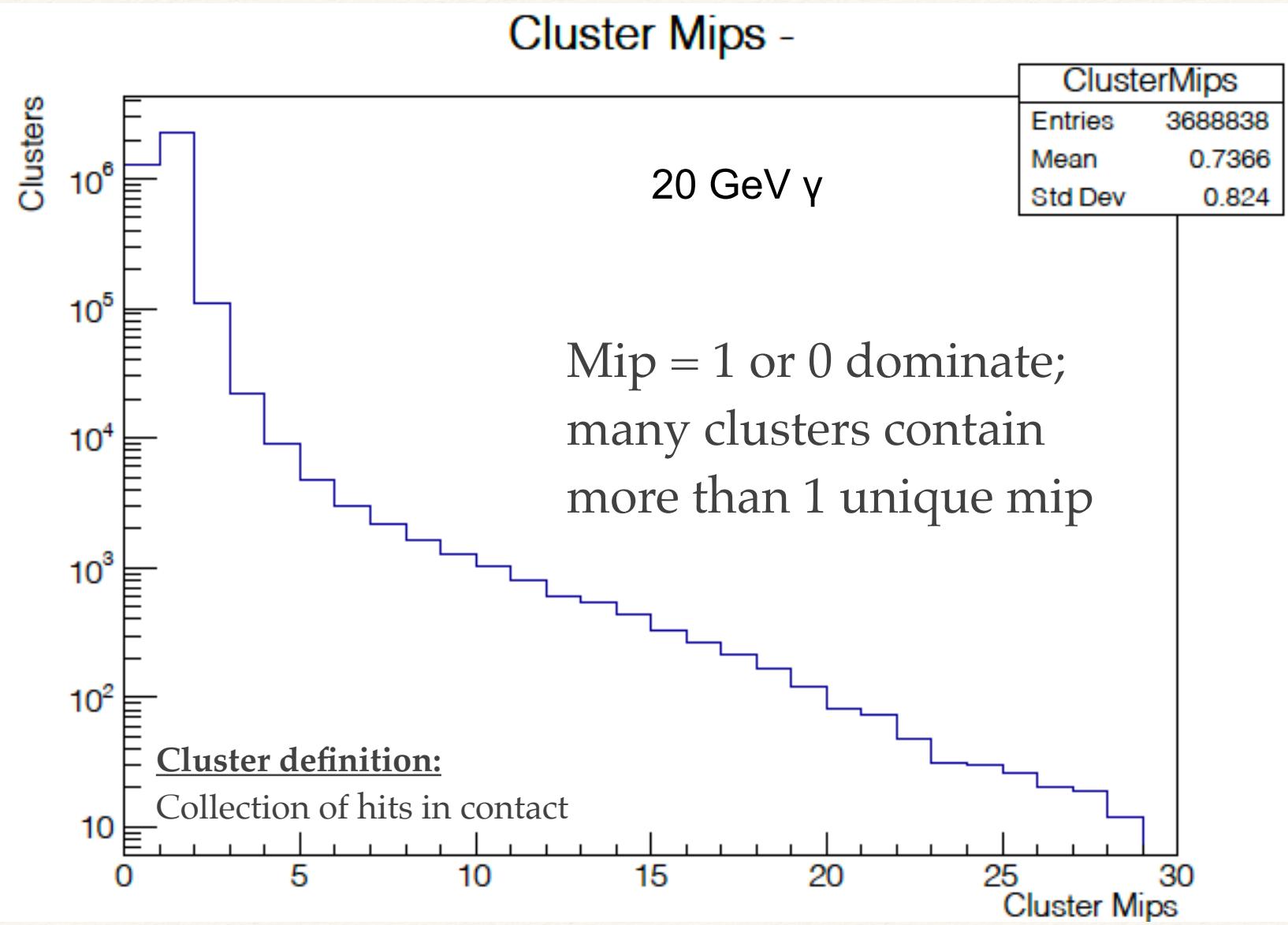
## Cluster definition:

Collection of hits  
in contact

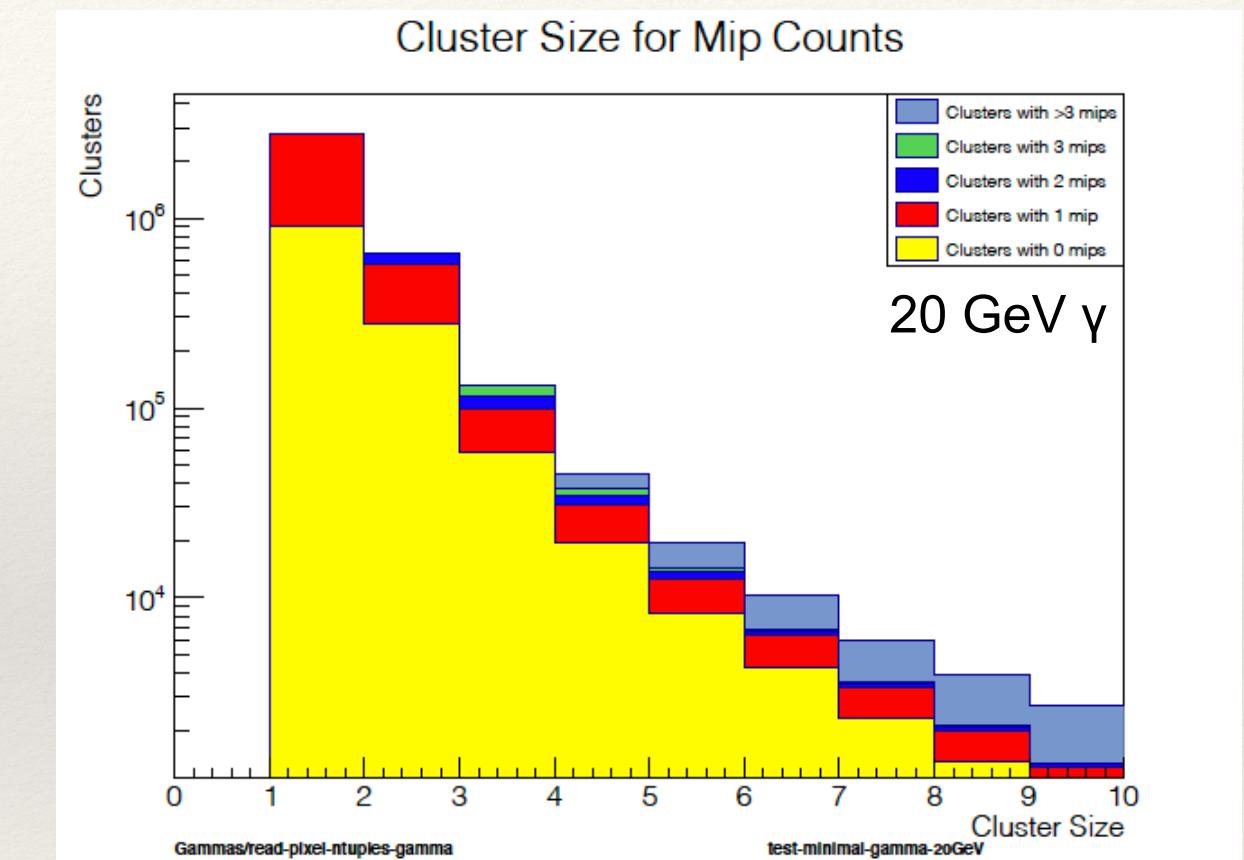
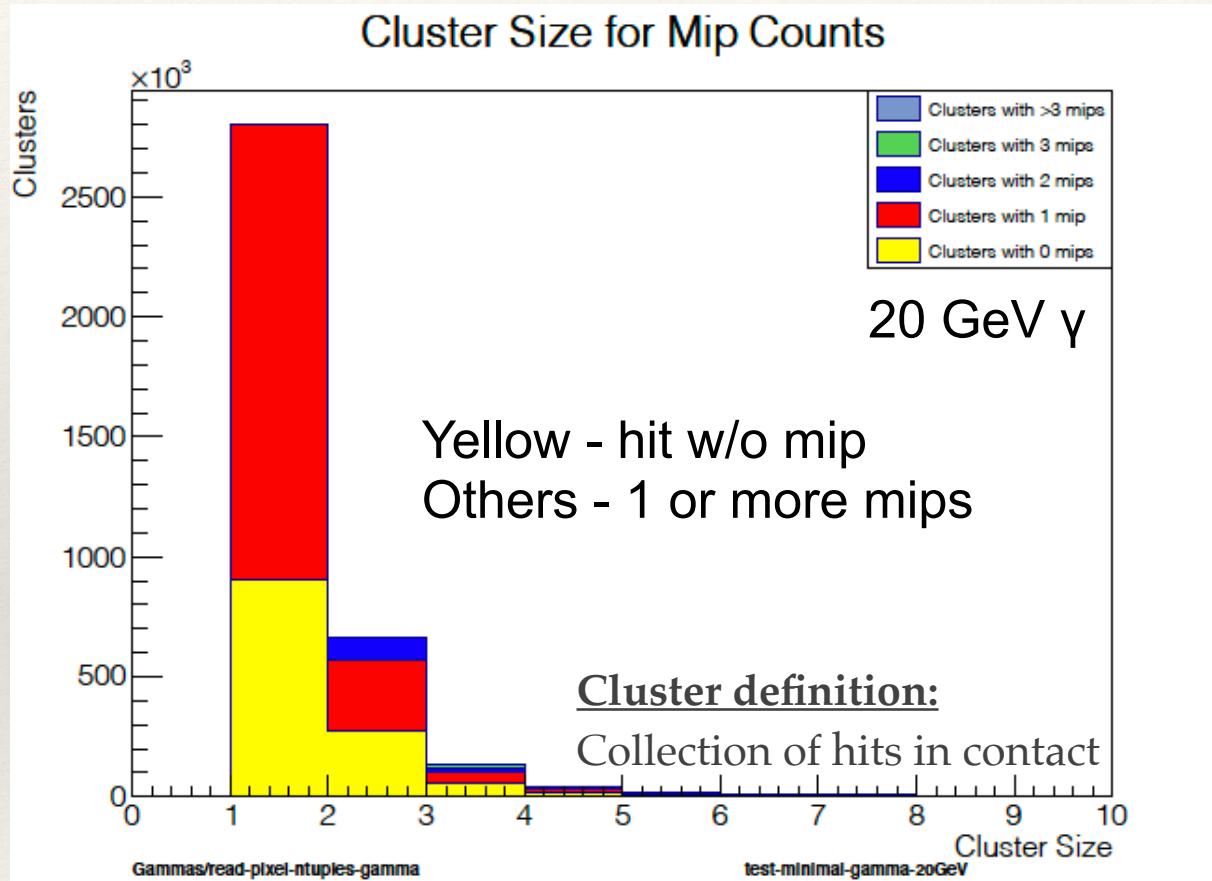
Many clusters have 1 mip  
(black - first appearance of mip)



# Mips per cluster

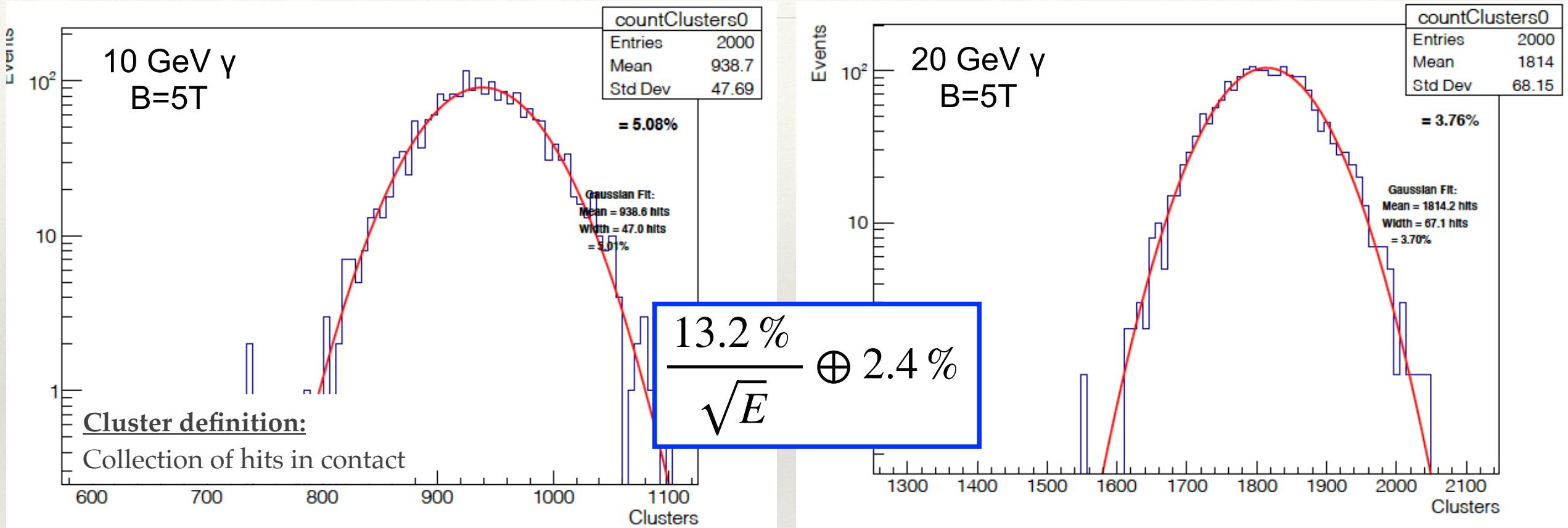


# Cluster summary (20 GeV $\gamma$ )



Cluster count is closer to mip count, reducing fluctuations from multiple hits.

# Energy resolution from counting clusters



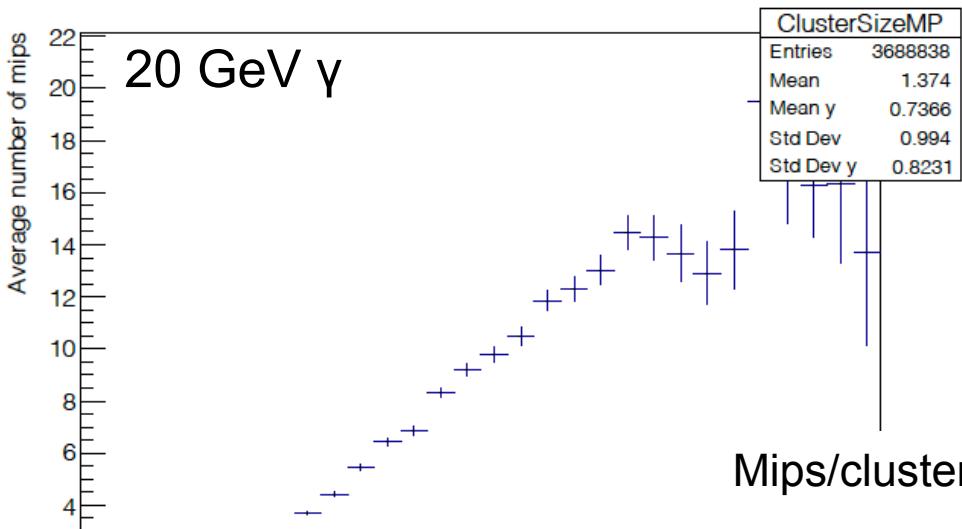
Improved compared to hit resolutions:

$$\frac{16.4\%}{\sqrt{E}} \oplus 2.0\%$$

But, cluster properties can improve more.

# Mips/cluster and shower radius dependence

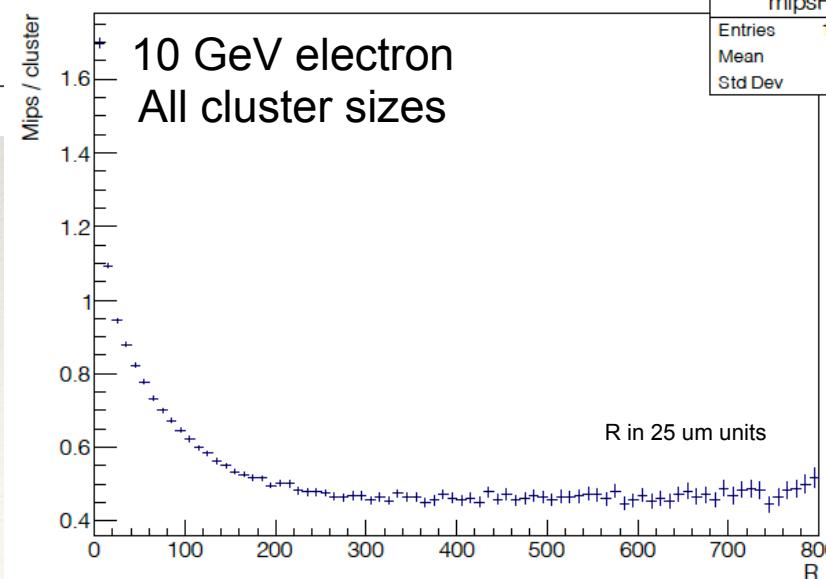
Average mips vs. Cluster Size



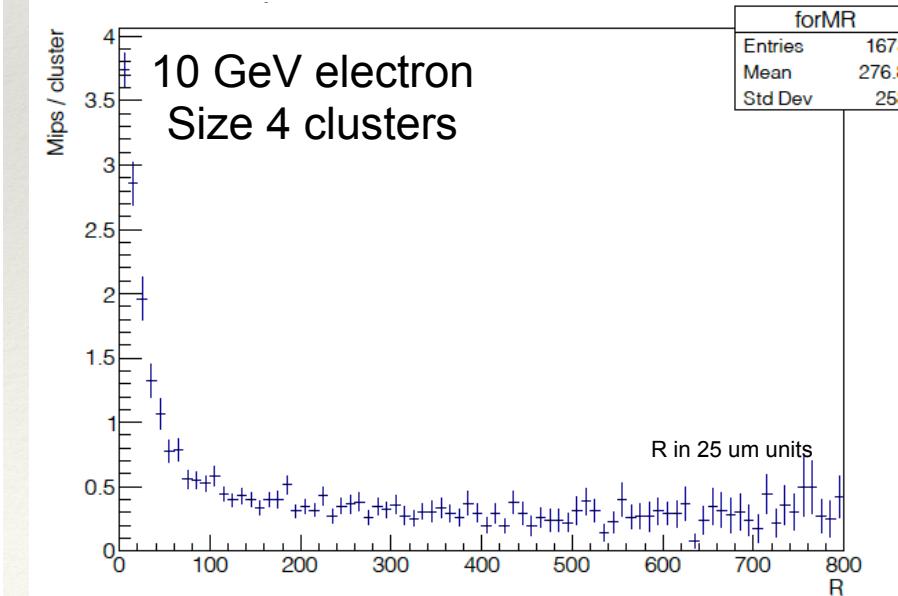
Cluster details “sense” number of mips:  
 Position (radius from shower axis);  
 Cluster size.

Analysis using these parameters improves  
 cluster resolution in our studies.

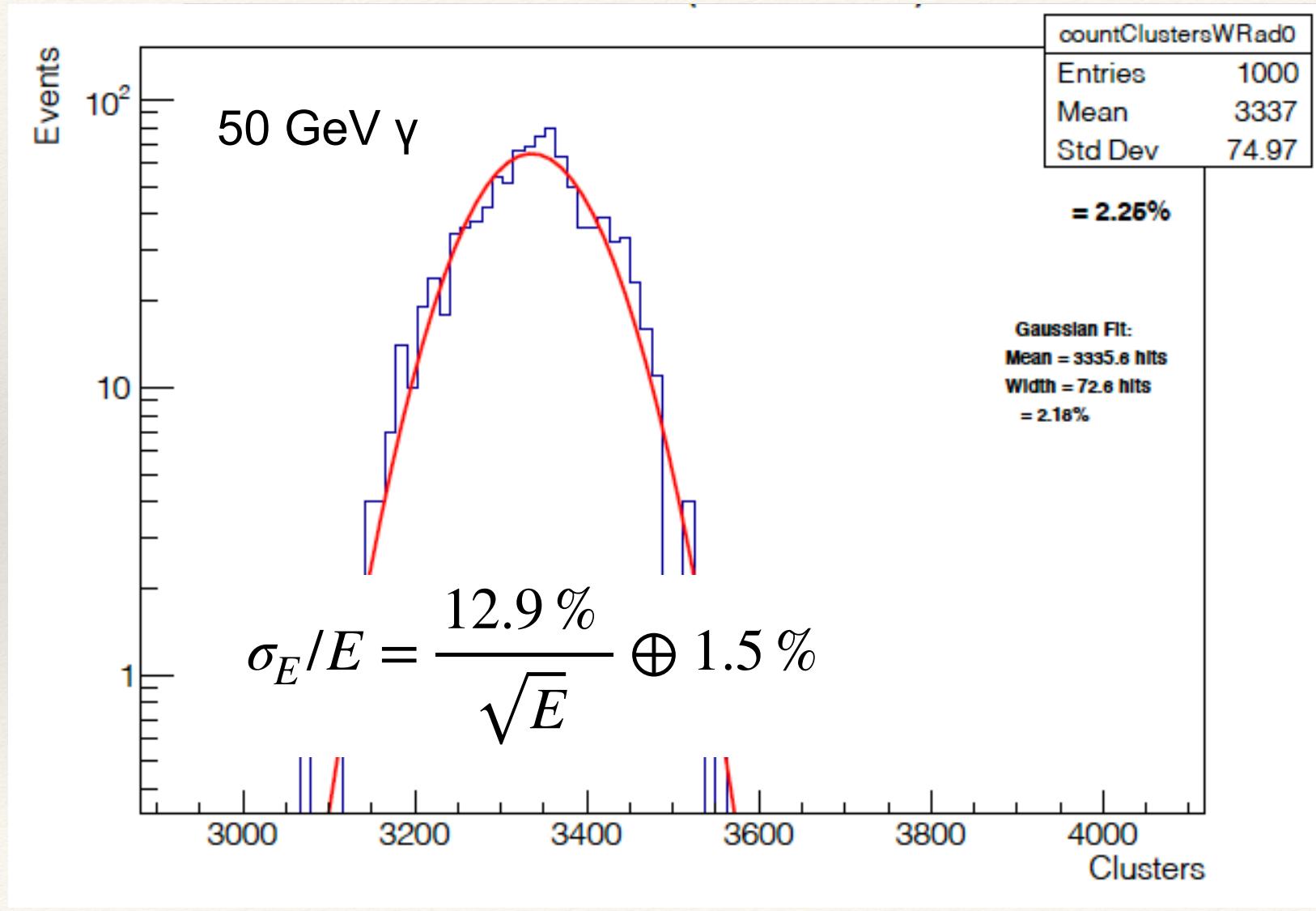
Mips/cluster vs. Radius from shower axis



Mips/cluster vs. Radius from shower axis



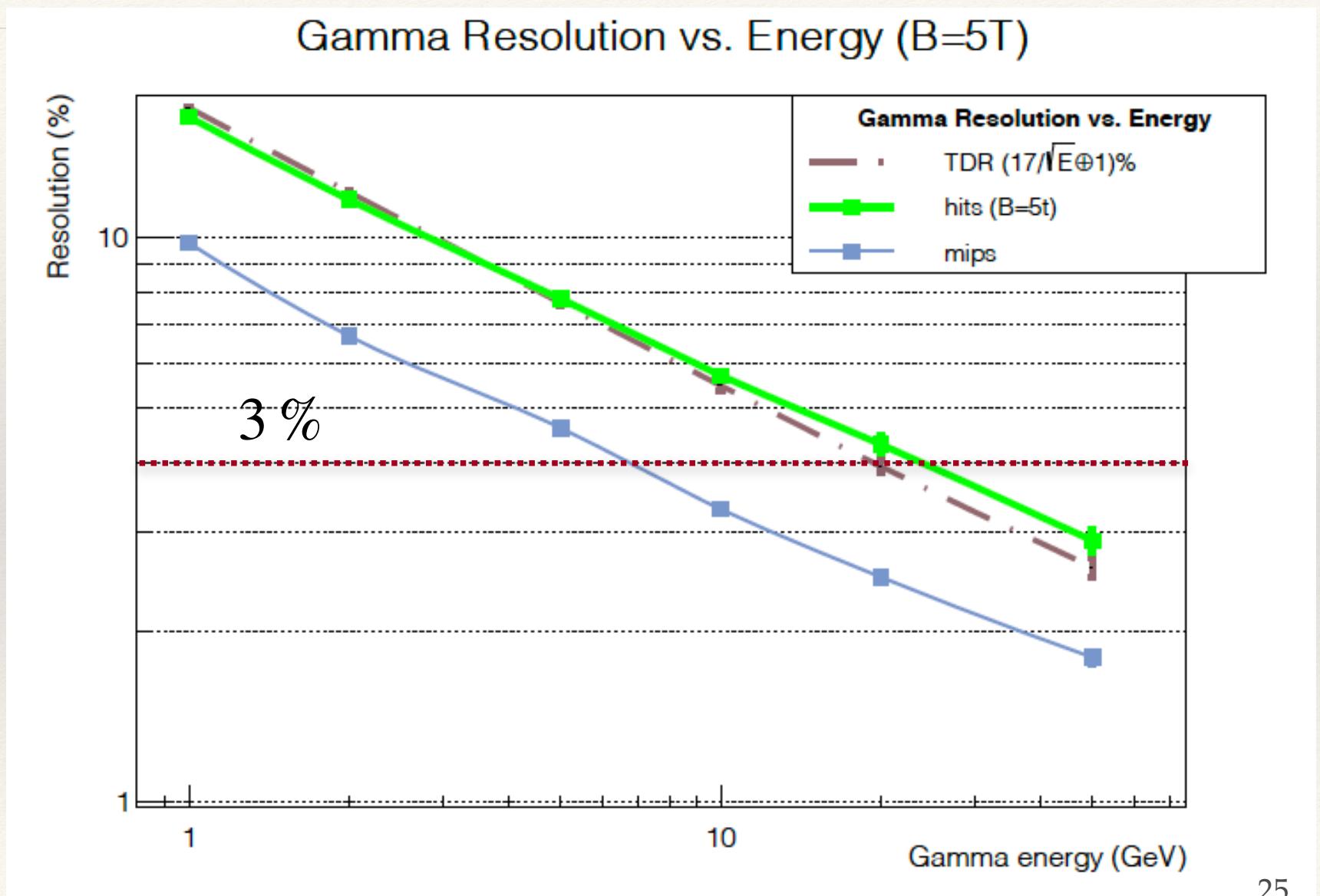
# Clusters weighted by radius & size



When cluster properties are taken into account with weighting, performance improves.

# Resolution vs. Energy (hits/clusters/mips)

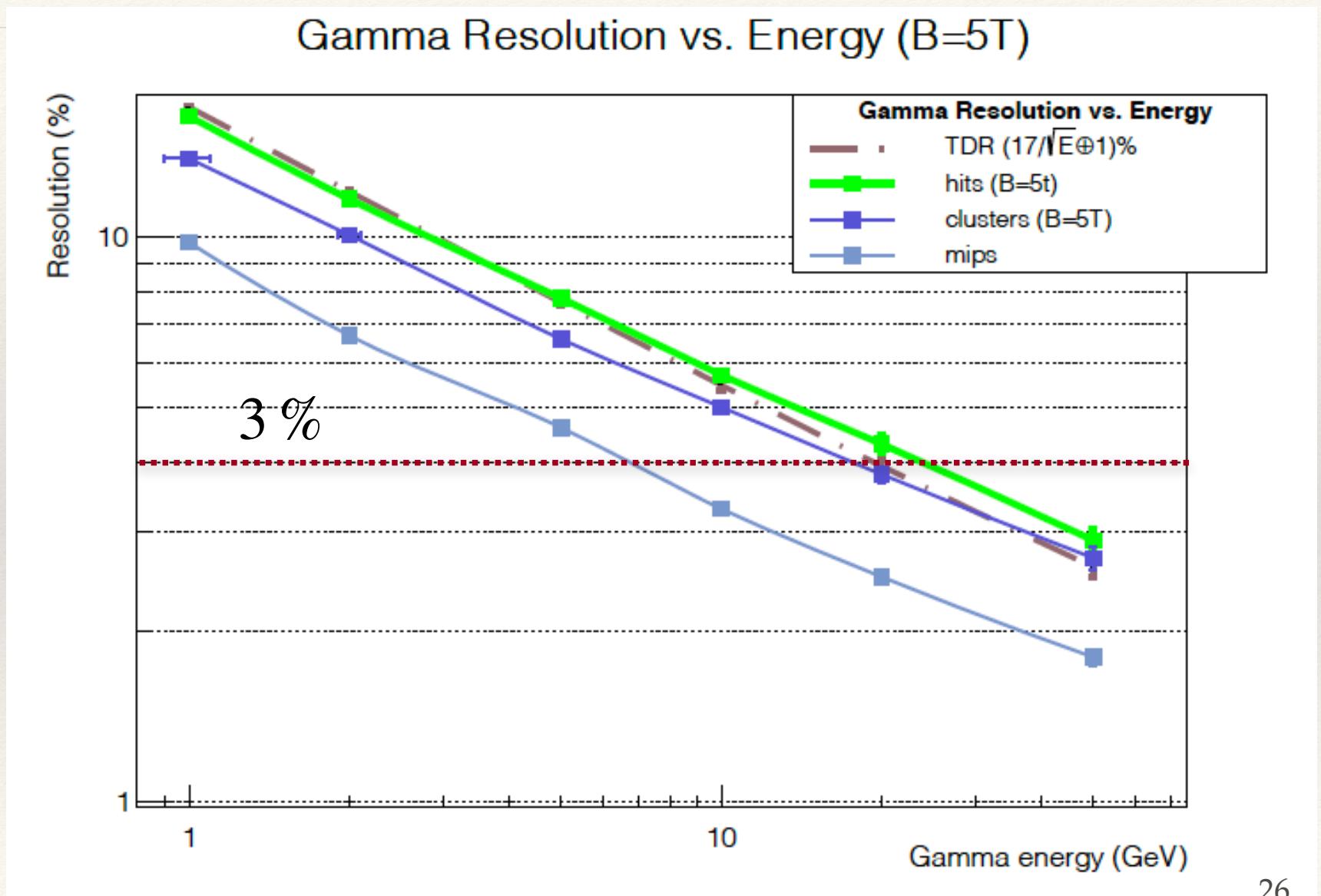
Resolution vs. Energy  
(hits and mips)



# Resolution vs. Energy (hits/clusters/mips)

Resolution vs. Energy  
(hits / clusters / mips)

Simple cluster  
performance is better  
than hit counting.

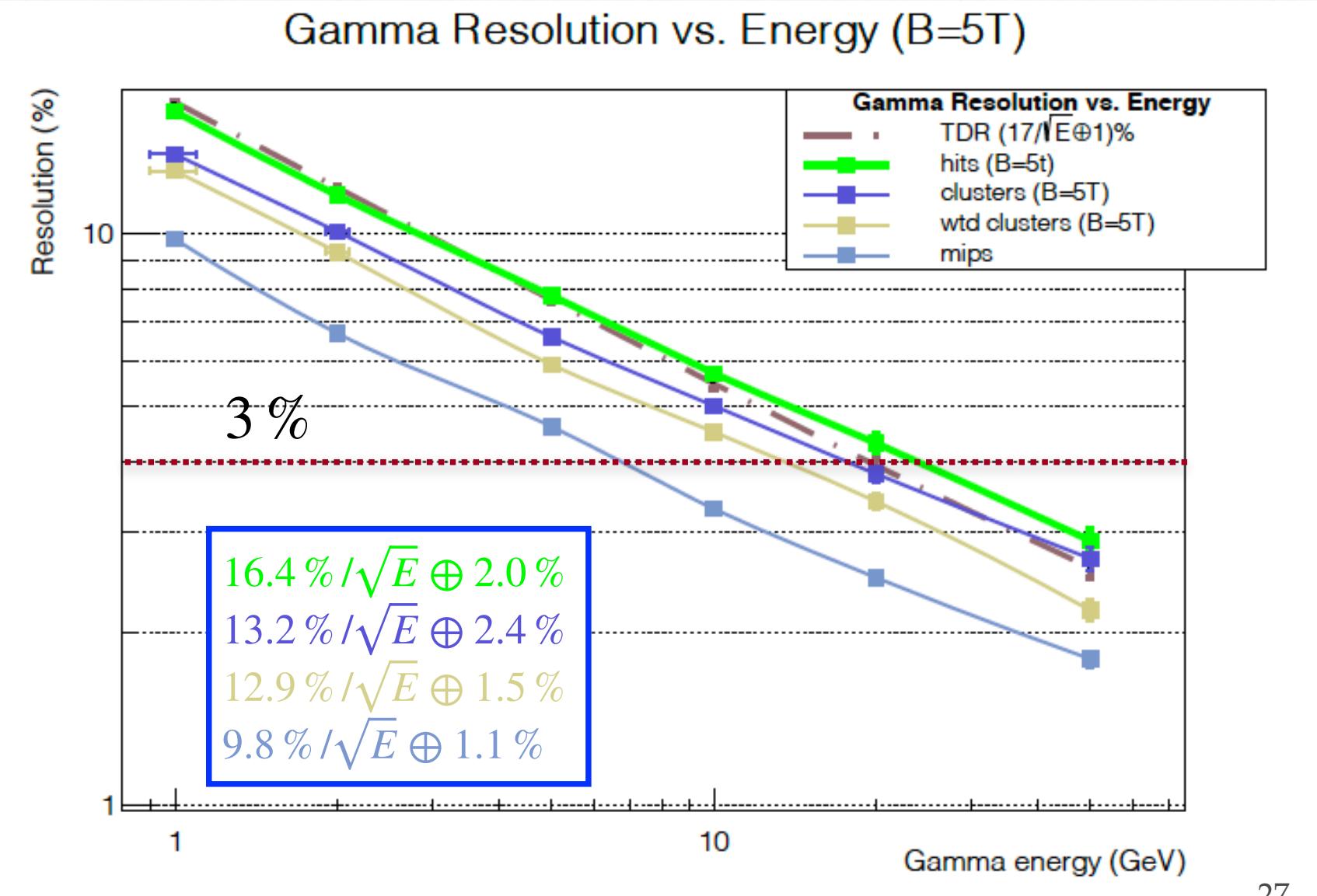


# Resolution vs. Energy (hits/clusters/mips)

Resolution vs. Energy  
(hits / clusters / mips) &  
weighted clusters.

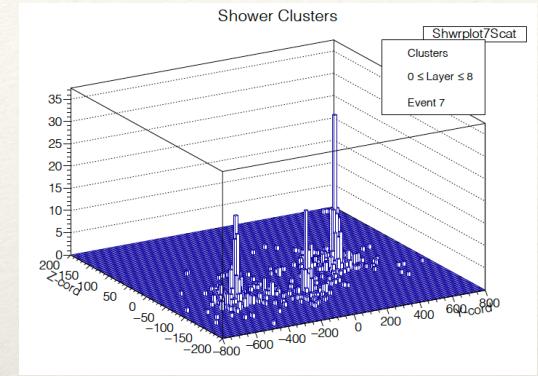
Simple cluster  
performance is better  
than hit counting.

When cluster properties  
are taken into account  
with weighting,  
performance improves.



# Other performance offered by MAPS and demonstrated in Geant4 studies

- ❖ Precise location of EM showers
- ❖ Multiple shower separation.
  - ❖ Two nearby showers - excellent separation to few mm.
  - ❖ Multiple nearby showers or showers / tracks
    - ❖ excellent counting and measurement.
- ❖ Pi0 reconstruction in busy environment.



# MAPS for SiD Tracking



- ◆ Size similar to that described for SiD in the ILC TDR,  $10 \times 10 \text{ cm}^2$  devices.  
Constructed by stitching  $2 \text{ cm} \times 2 \text{ cm}$  reticles.
- ◆ Exceptional granularity of  $25 \mu\text{m}$  by  $100 \mu\text{m}$  pixels, with  $25\mu\text{m}$  in bend direction resolution of  $25\mu\text{m}/\sqrt{12} \approx 7 \mu\text{m}$  without charge sharing.
- ◆ The  $25\mu\text{m}$  pixel matches KPiX-readout, silicon-strip width of the SiD TDR design recently assembled, tested, and shown to achieve  $7\mu\text{m}$  resolution<sup>†</sup>.
- ◆ The depleted  $10\mu\text{m}$  thick epi layer charge collection of the MAPS allows a minimum threshold of  $1/4$  MIP, ensuring high efficiency.
- ◆ The pixel nature provides vastly improved pattern recognition for track finding over the strip devices.
- ◆ For the endcaps, such a sensor would eliminate the need for two sensors in a small-angle-stereo configuration, reducing both the material budget and cost.

<sup>†</sup> J. Brau et al., “Lycoris – a large-area, high resolution beam telescope,” 2021 JINST 16 P10023, arXiv:2012.11495 [physics.ins-det]

# Ongoing effort

## Sensor development and shower analysis

- ◆ Sensor development progressing.
  - ◆ Anticipating first small-scale devices later in 2022.
- ◆ Shower performance studies advancing:
  - ◆ Various cluster features “sense” mip count in “large” clusters.
  - ◆ Cluster features improve performance:
    - ◆ Based on radial position in shower;
    - ◆ Based on longitudinal position in shower;
    - ◆ Based on shape of cluster.
  - ◆ Simulated energy resolution exceeds TDR performance.

Reference: [arXiv:2203.07626](https://arxiv.org/abs/2203.07626) [physics.ins-det]

# Extra



# Normalized Signal vs. Energy (B=5T)

