



# Commissioning of SiW ECAL Prototype

Roman Pöschl



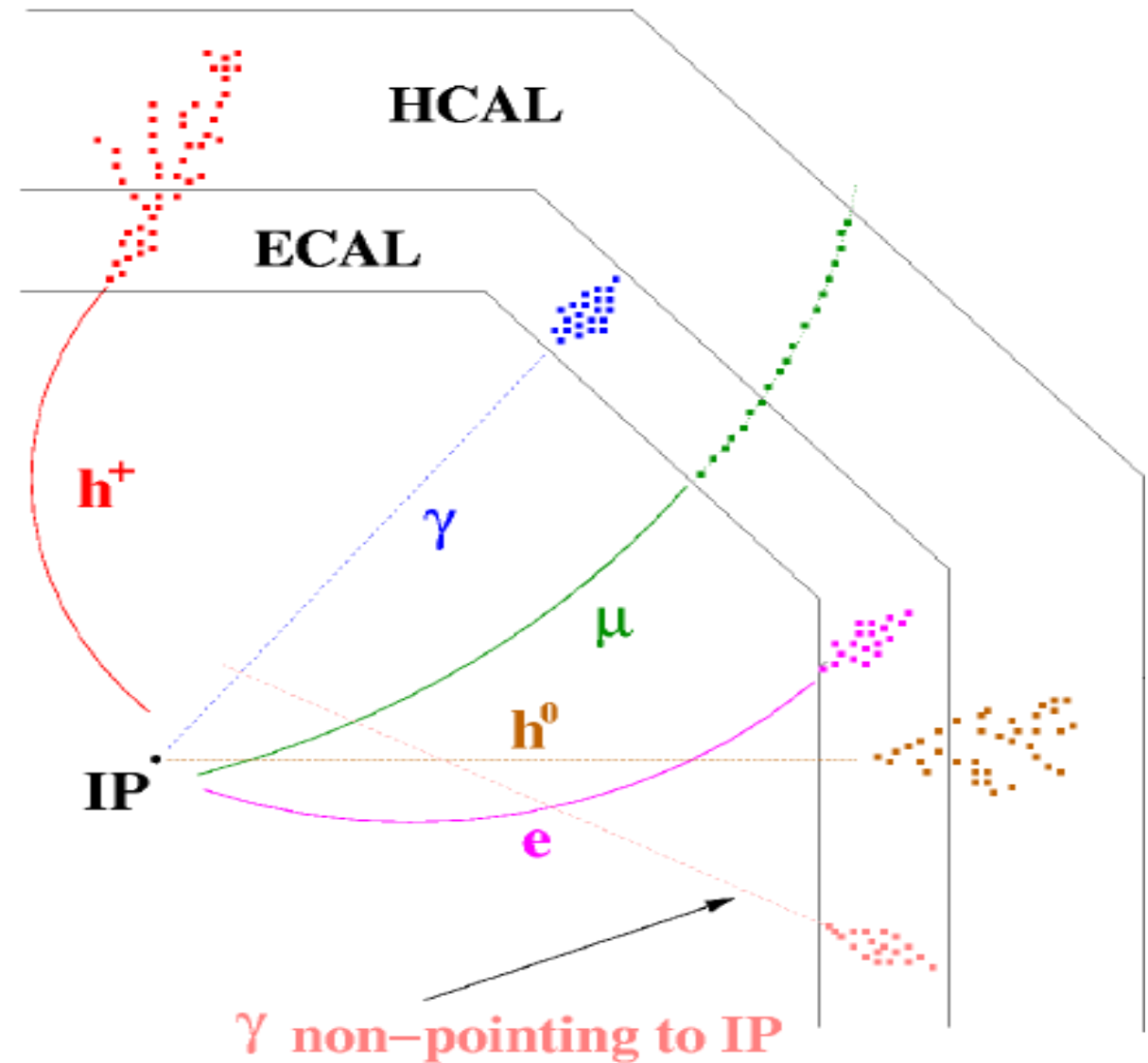
On behalf of the SiW ECAL Groups in CALICE:



CALOR 2022 – May 2022

Jet energy measurement by measurement of **individual particles**  
 Maximal exploitation of precise tracking measurement

- large radius and length
  - to separate the particles
- large magnetic field
  - to sweep out charged tracks
- “no” material in front of calorimeters
  - stay inside coil
- small Molière radius of calorimeters
  - to minimize shower overlap
- **high granularity of calorimeters**
  - to separate overlapping showers

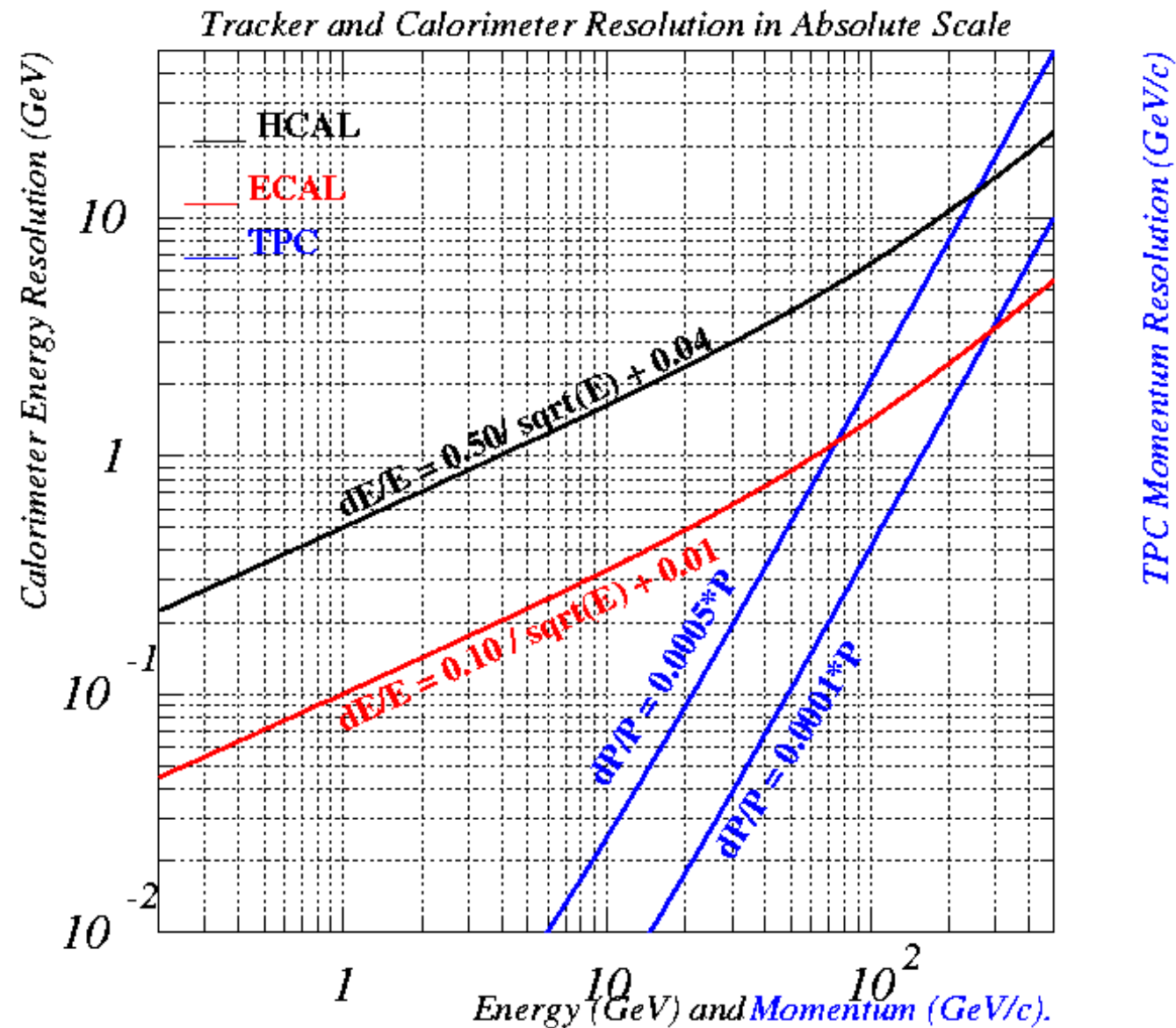


Particle flow as privileged solution for experimental challenges

=> **Highly granular calorimeters!!!**

Emphasis on tracking capabilities of calorimeters

Final state contains high energetic jets from e.g. Z,W decays  
 Need to reconstruct the jet energy to the utmost precision !  
 Goal is around  $dE_{jet}/E_{jet} - 3-4%$  ( e.g. 2x better than ALEPH)

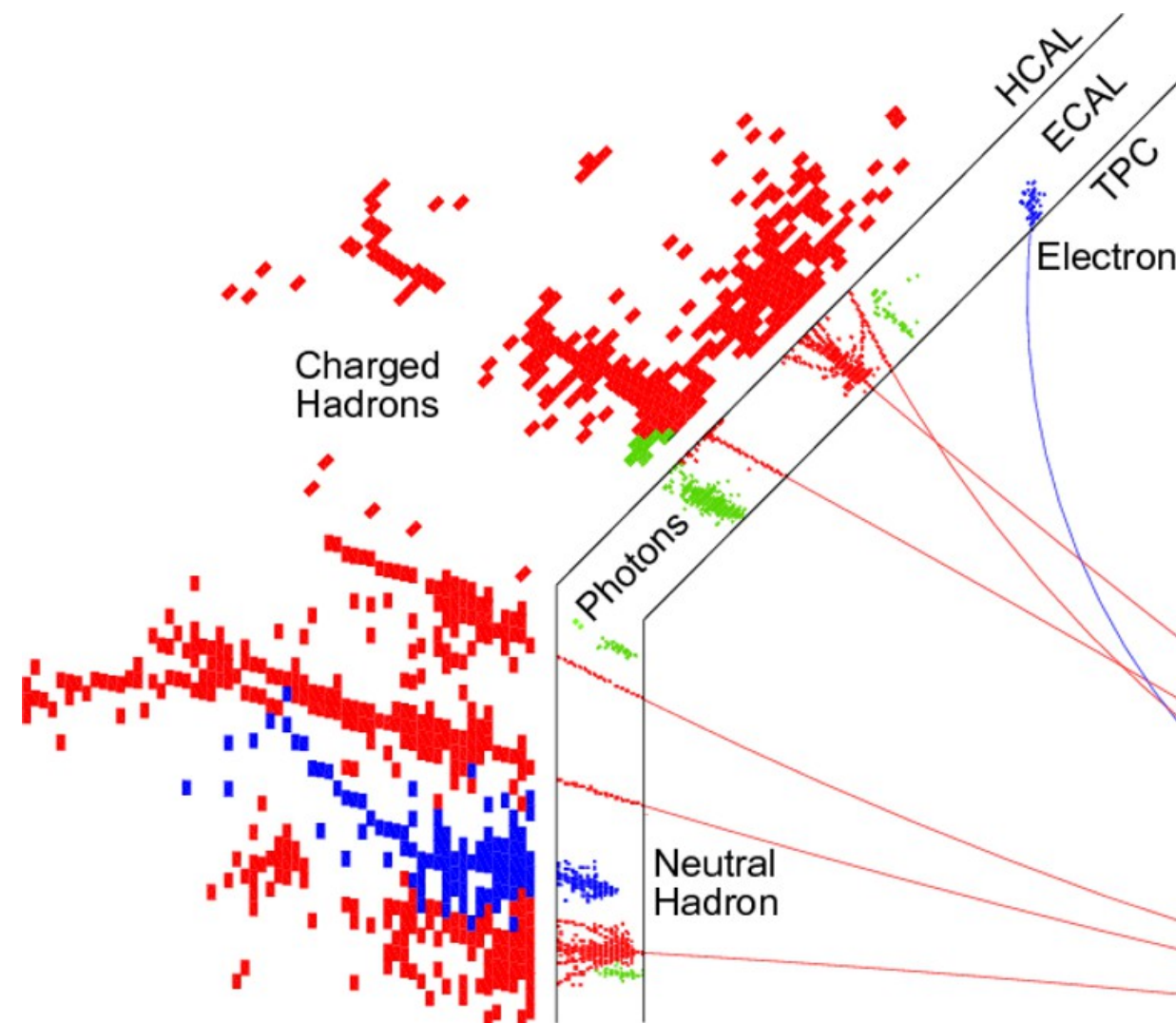


Jet energy carried by ...

- Charged particles ( $e^\pm, h^\pm, \mu^\pm$  65% :((  
 Most precise measurement by Tracker  
 Up to 100 GeV
- Photons: 25%  
 Measurement by Electromagnetic  
 Calorimeter (ECAL)
- Neutral Hadrons: 10%  
 Measurement by Hadronic  
 Calorimeter (HCAL) and ECAL

$$\sigma_{Jet} = \sqrt{\sigma_{Track}^2 + \sigma_{Had.}^2 + \sigma_{elm.}^2 + \sigma_{Confusion}^2}$$

- Base measurement as much as possible on measurement of charged particles in tracking devices
- Separate of signals by charged and neutral particles in calorimeter



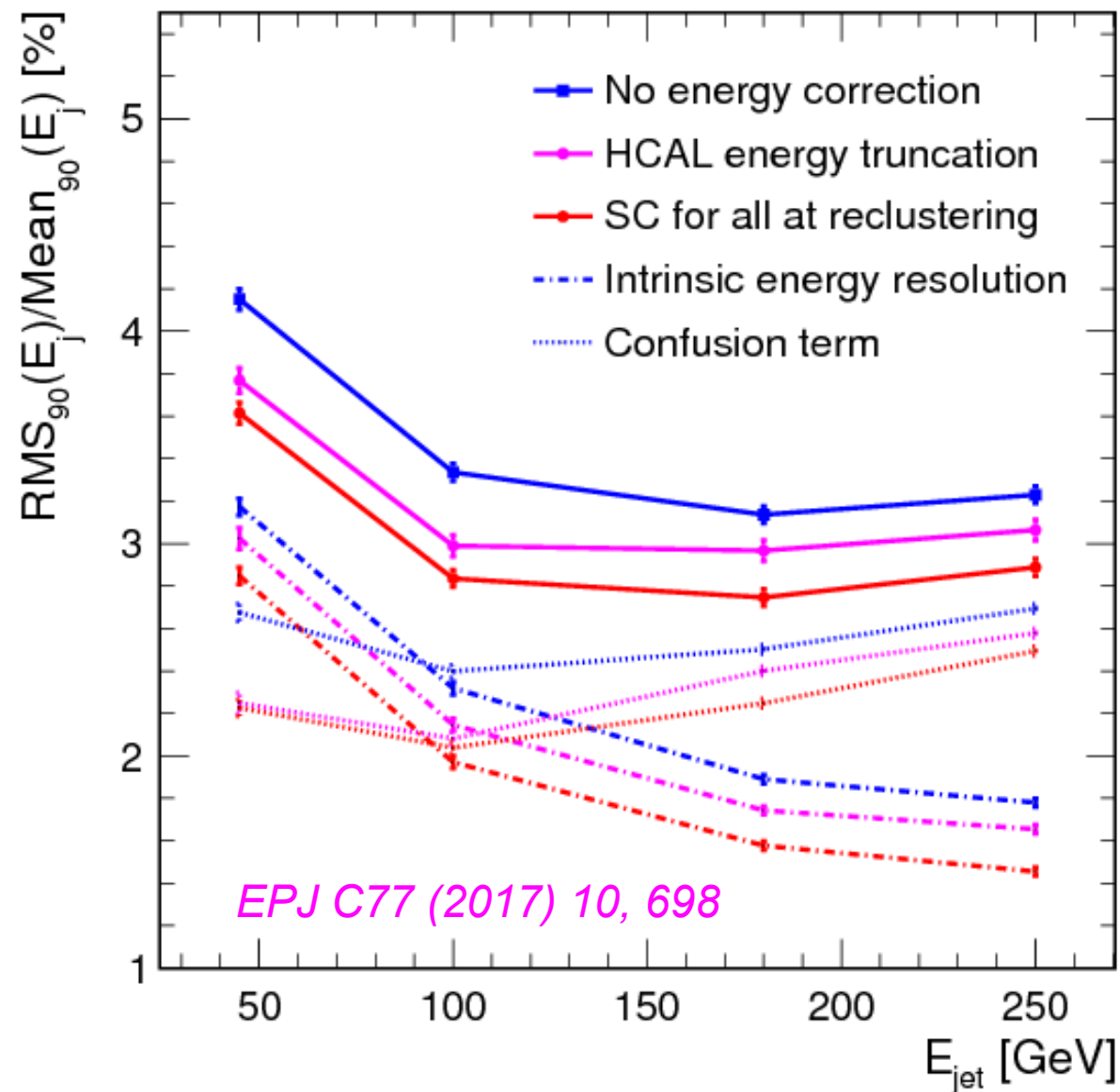
- Complicated topology by (hadronic) showers
- Overlap between showers compromises correct assignment of calo hits

## □ **Confusion Term**

Need to minimize the confusion term as much as possible !!!



## Pandora PFA jet energy resolution



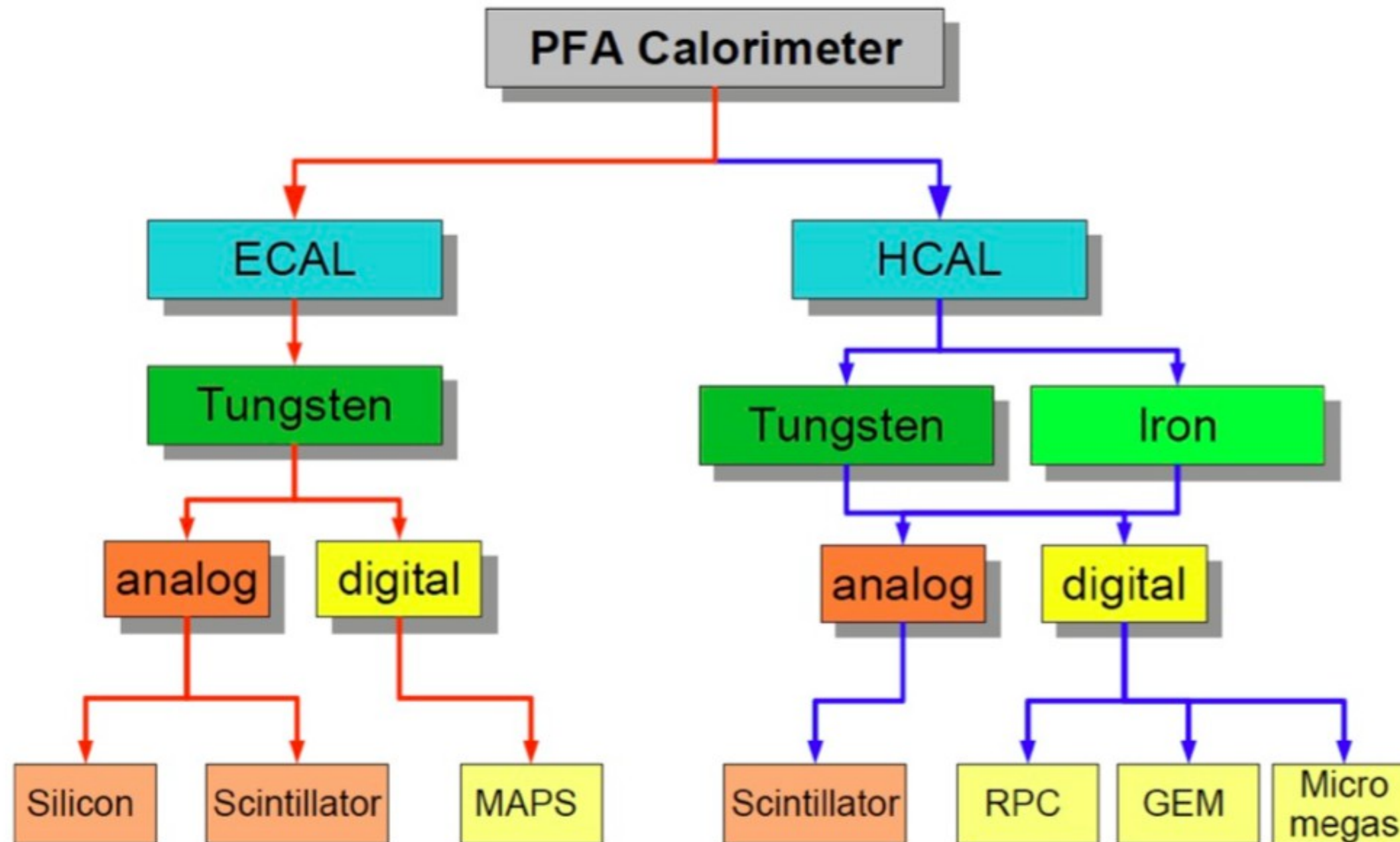
## Study within ILD Concept

- **Design goal:  $30\%/\sqrt{E}$  at 100 GeV**
  - $\sim 3\text{-}4\%$  over entire jet energy range
- **At lower energies  $< 100$  GeV resolution is dominated by intrinsic calorimeter resolution**
- **At higher energies have more particles and higher boost**
  - Smaller distance between particles
  - More overlap between calorimeter showers
  - Pattern recognition becomes more challenging

**=>Confusion**
- **Note particularly the gain by software compensation**
  - i.e. exploiting the wealth of information available through high granularity

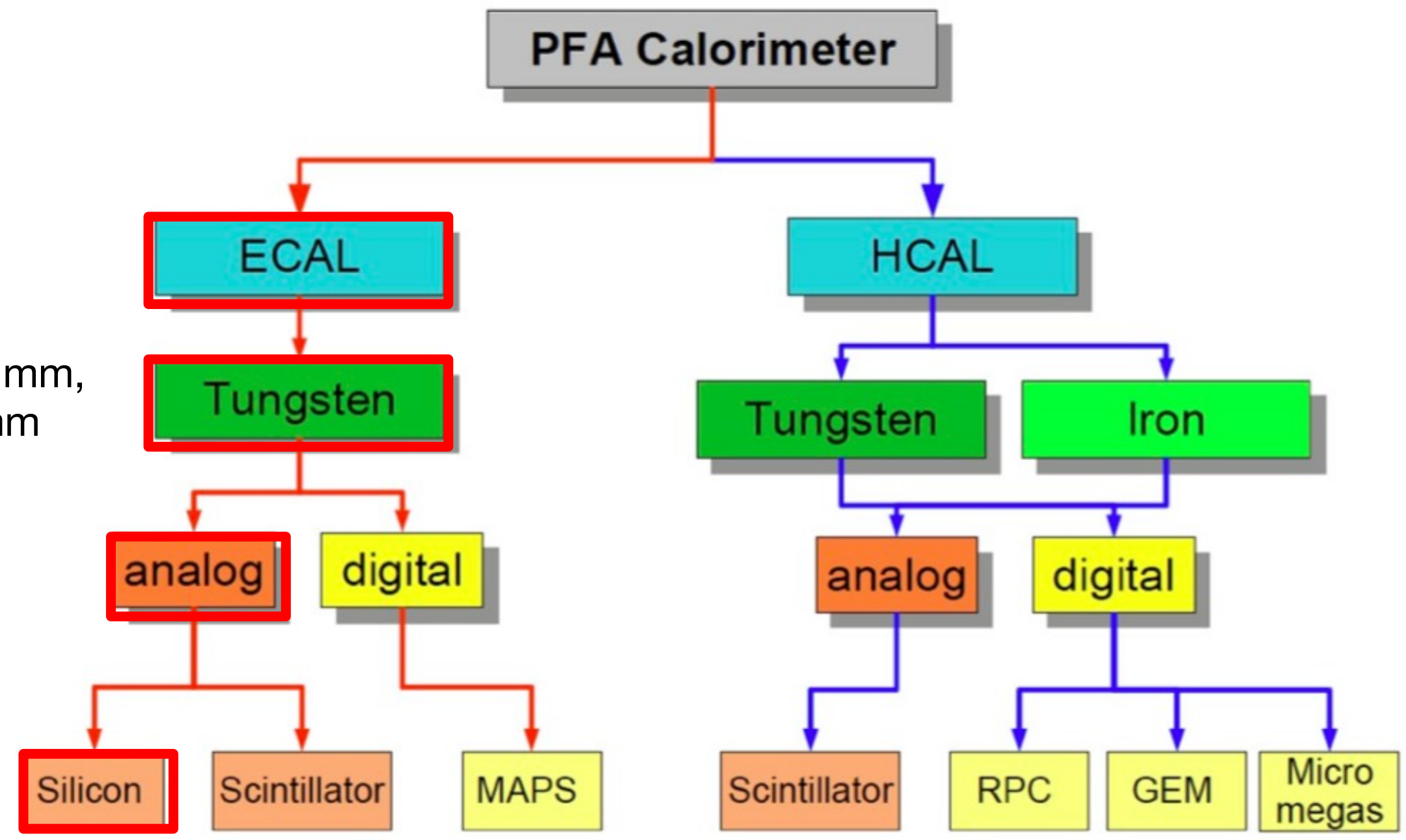
PFA ARBOR is algorithm of choice for CEPC Detector with similar performance

Mainly organised within the:  Collaboration



Mainly organised within the:  Collaboration

$X_0 \sim 3.5 \text{ mm},$   
 $\rho_M \sim 9 \text{ mm}$





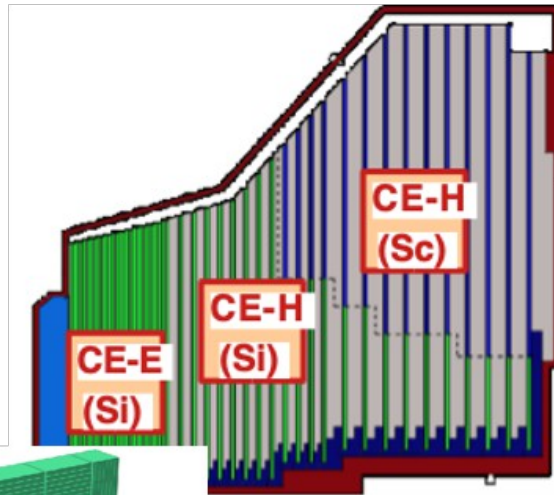
- Grouped into two categories:

## Main calorimeters of collider experiments

(barrel and / or endcap)

CMS HGCAL

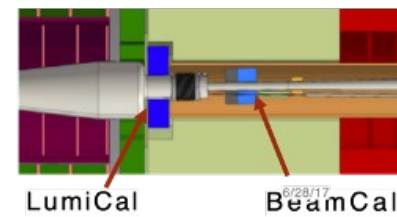
(ECAL, part of HCAL)



## Smaller, specialized calorimeter systems

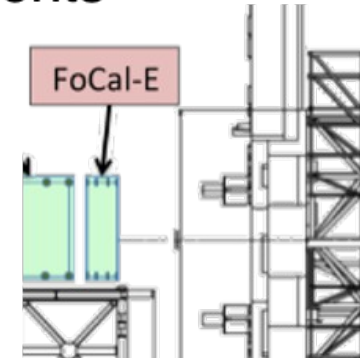
in collider and non-collider experiments

Very forward calorimeters: ALICE



Luminosity

measurement at  $e^+e^-$



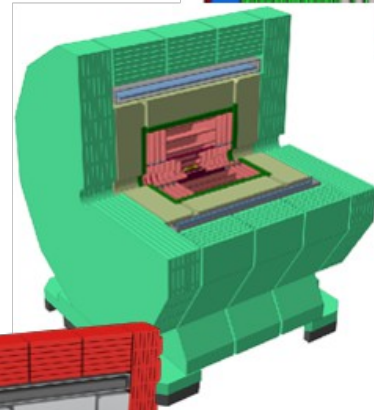
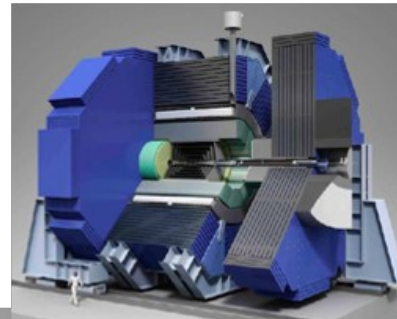
Non-collider experiments: LUXE, Satellites,

...

### Main arguments for adopting silicon:

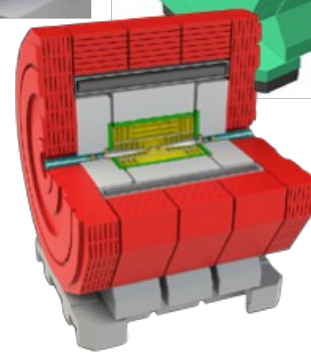
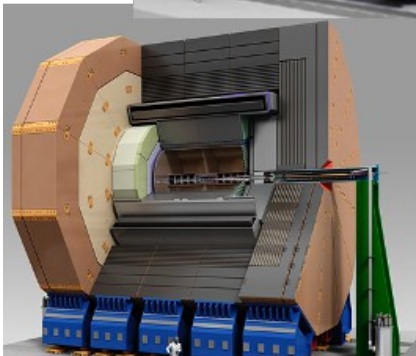
- Finely segmentable: High granularity
- Robust and stable performance
- Compact design, high density
  - typically combined with W absorbers for maximum compactness, small  $\rho_M$

*Main challenge: Cost*



ECALs of Higgs Factory detectors  
(linear and circular colliders);

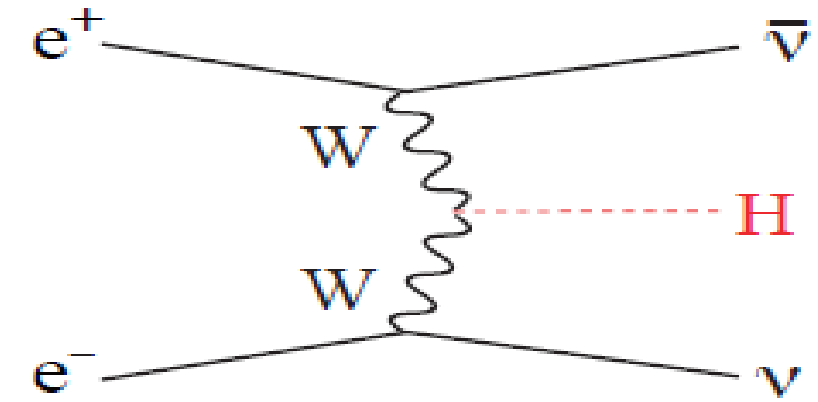
Muon colliders



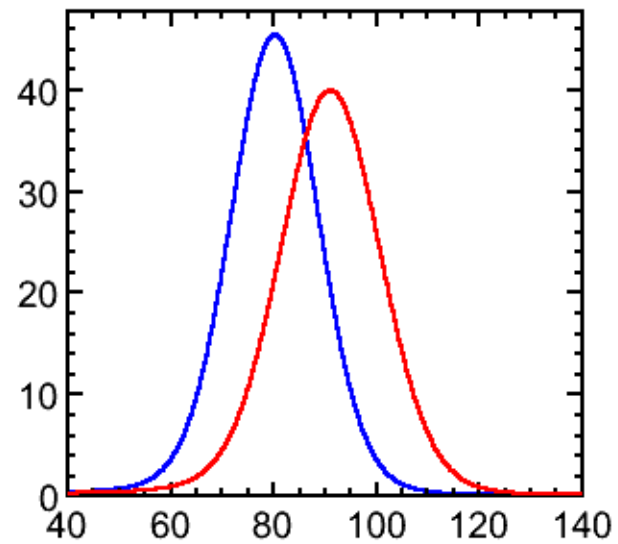


## Examples:

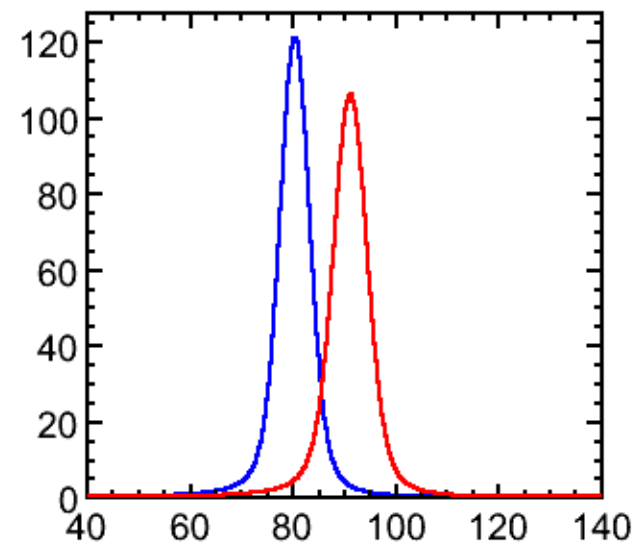
- W Fusion with final state neutrinos requires reconstruction of H decays into jets
- Jet energy resolution of  $\sim 3\%$  for a clean W/Z separation



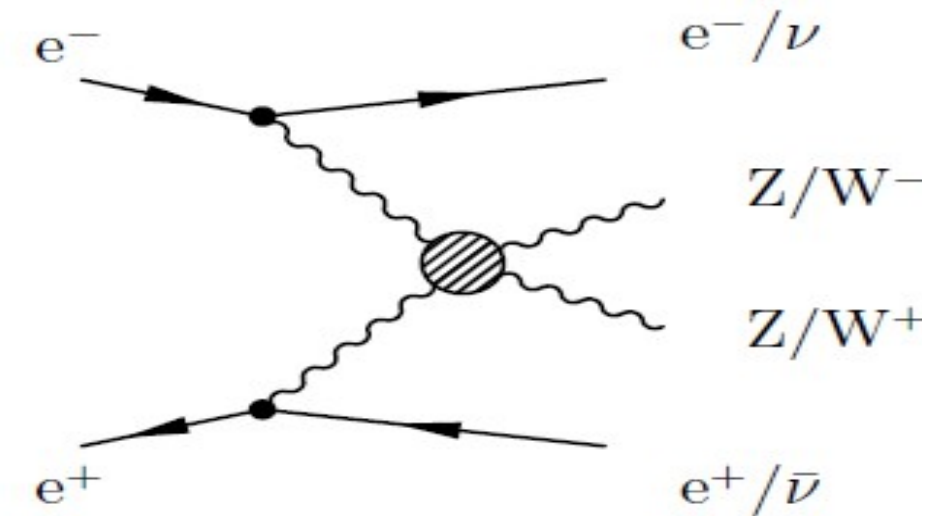
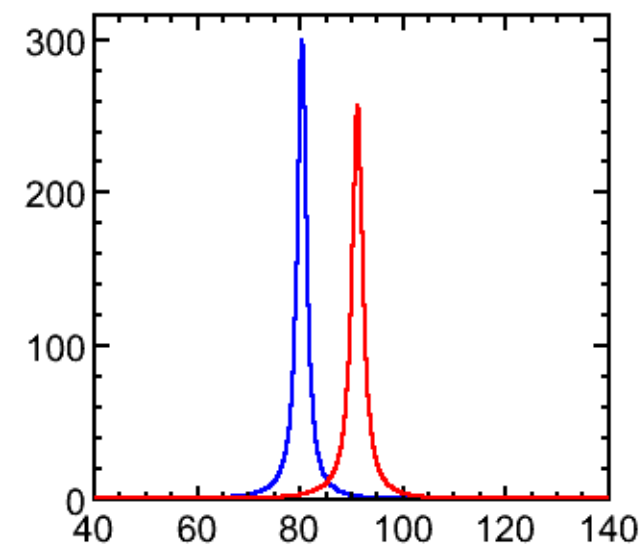
## Jets at LEP



## 3%

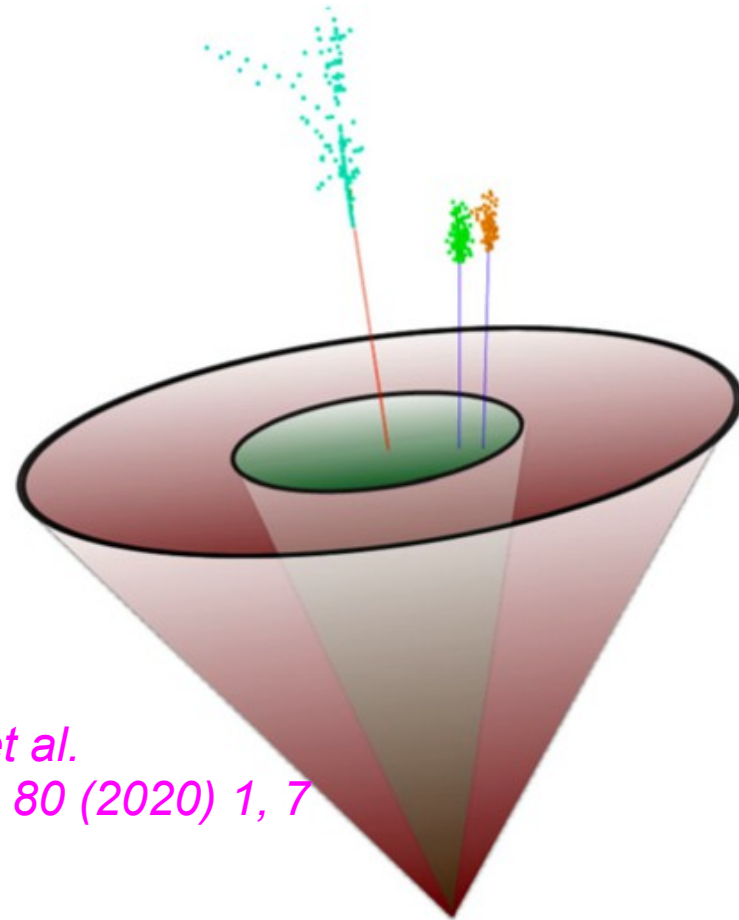


## Perfect



M. Thomson

Slide: F. Richard at International Linear Collider – A worldwide event



From D. Yu et al.  
 Eur.Phys.J.C 80 (2020) 1, 7

Available Tau Finders:

- TAURUS (for CEPC)
- Tau-Finder in ILD Marlin

- **Features on  $\tau$   $\tau$  final states**
  - Small multiplicity
  - => Can cut on small number of Particle Flow objects
- **Assets of granular calorimeters**
  - High granularity allows for counting of PFO
  - Clean separation of charged pion from photon clusters
  - Spatial resolution of close-by photons (at reasonable energy resolution)

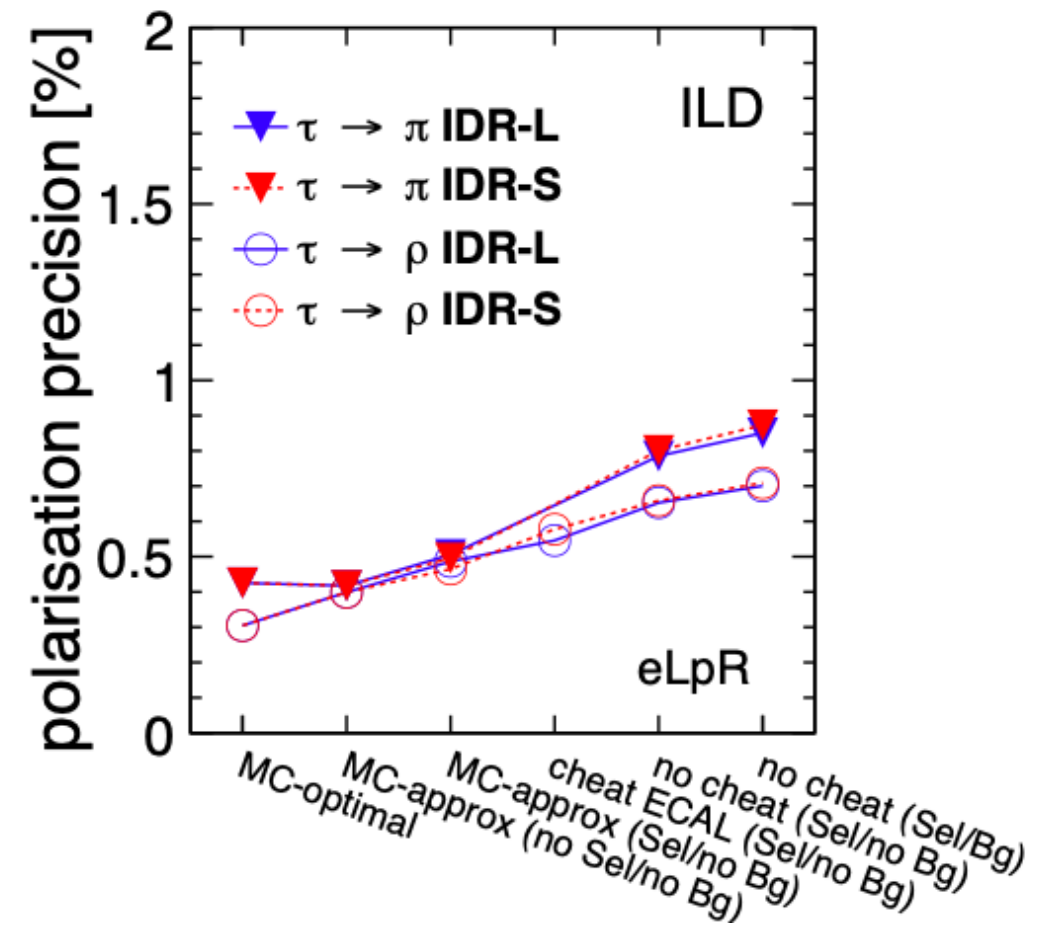
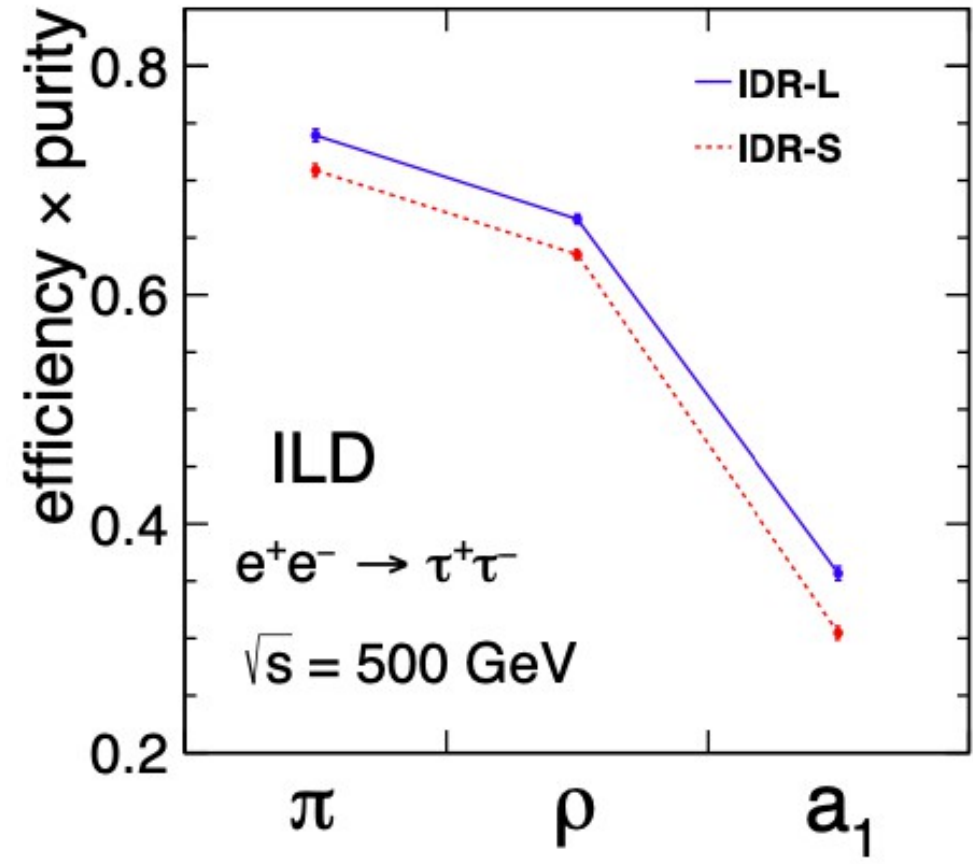
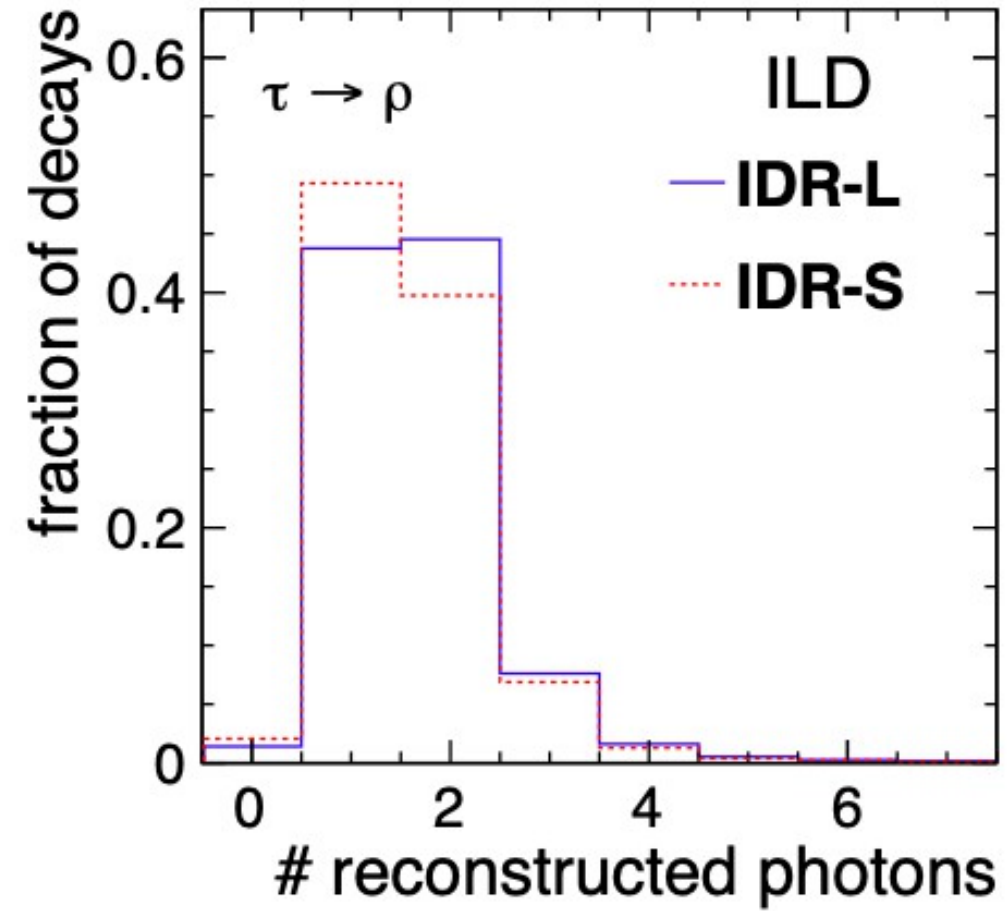
- Prominently used  $\tau$  decays

$$\tau^{\pm} \rightarrow \pi^{\pm} + \nu \text{ (} \text{''}\pi\text{'')}$$

$$\tau^{\pm} \rightarrow \pi^{\pm} + \pi^0 + \nu \text{ (} \text{''}\rho\text{'')}$$

$$\tau^{\pm} \rightarrow \pi^{\pm} + \pi^0 + \pi^0 + \nu \text{ (} \text{''}a_1\text{'')}$$

$e^+e^- \rightarrow \tau^+\tau^-$  Recent study at 500 GeV for ILD IDR



- Photon separation gets involved at high energies
- Still often only one photon reconstructed

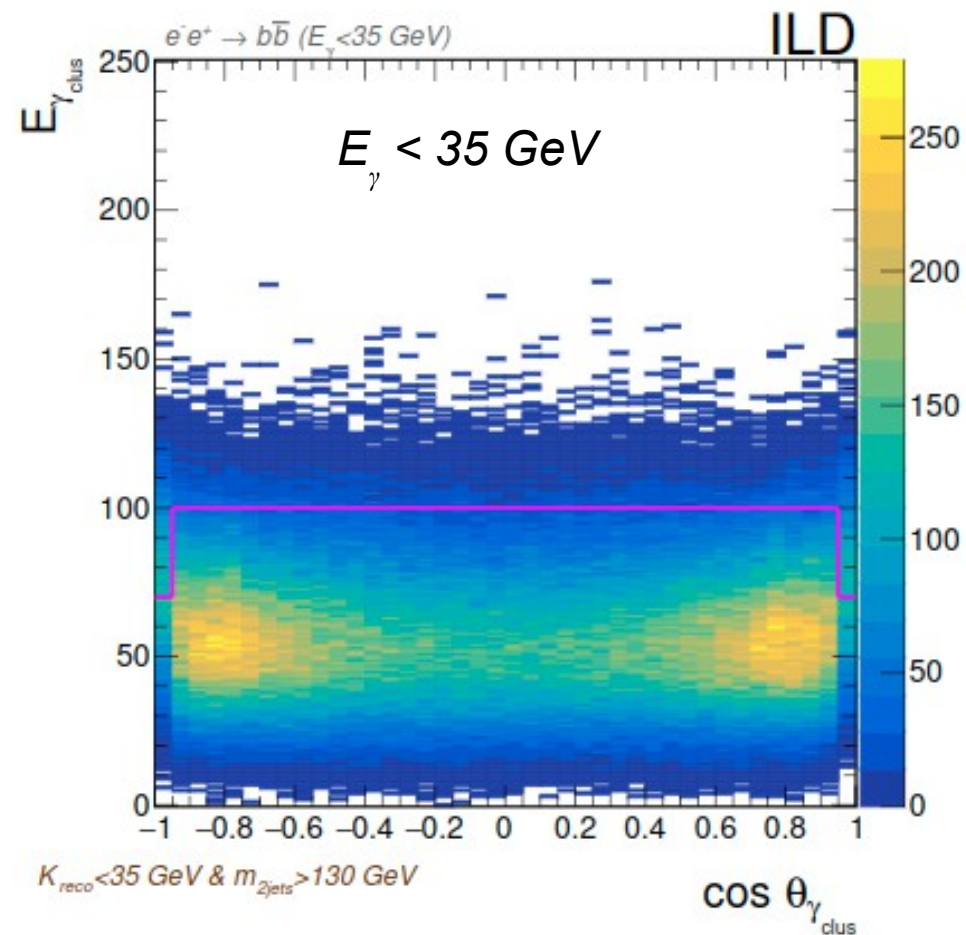
- Efficiency x Purity drops with increasing photon multiplicity

Precision of tau polarisation of order 0.3%-1%

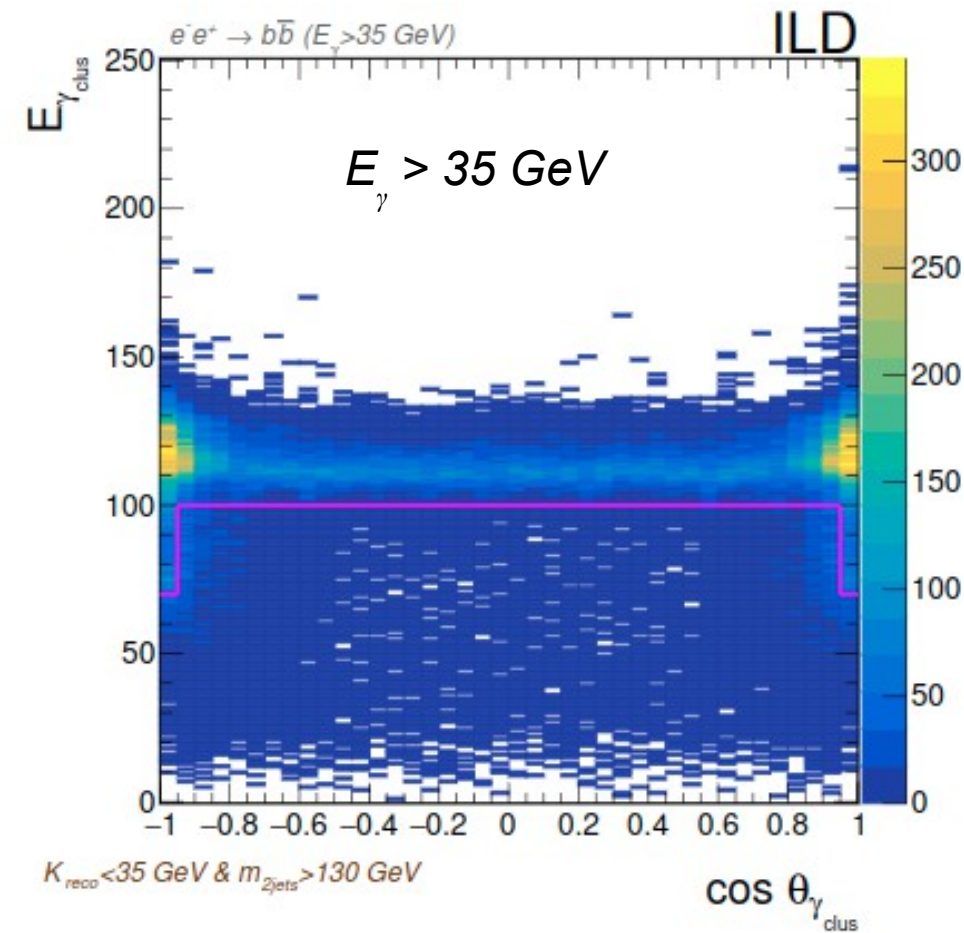
- Close-by photons are challenge for highly granular calorimeters (in particular Ecal) at high-energies
- Ideal benchmark for detector optimisation
- Maybe still room for improvement, better algorithms?

- Most ISR Photon are radiated collinearly but lead to a boost -> Check for acolinearity of dijet event
- Method doesn't work when photon is radiated into detector acceptance
  - ... and merged with a jet --> Busy environment

No or mild ISR



“Strong? ISR



- Excellent photon ID in granular calorimeter is key
- Identification of ISR photon within detector (jet) reduces ISR background by nearly a factor of six
- Would be interesting to carry out this analysis with less granular calorimeters

ILD: Irls, Richard, R.P.



## Physics Prototype

2003 - 2012

- Proof of principle of granular calorimeters
- Large scale combined beam tests

## Technological Prototype

2010 - ...

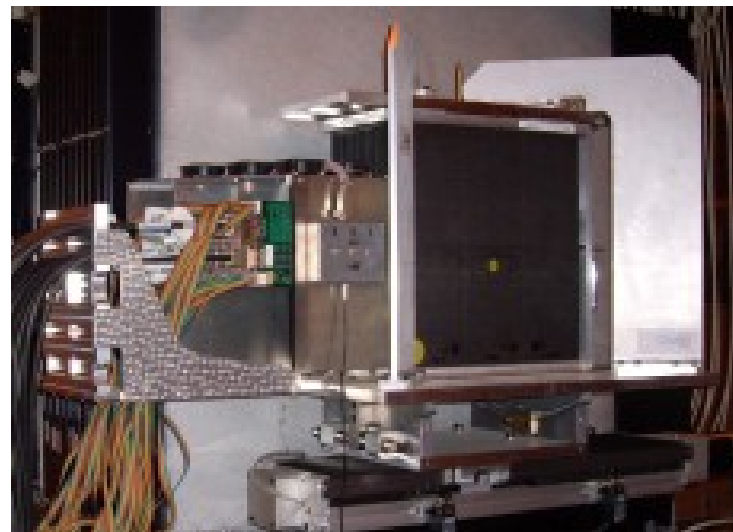
- Engineering challenges
- Higher granularity
- Lower noise
- **Today**

## LC detector

- The goal
  - Typically  $10^8$  calorimeter cells
- Compare:
  - ATLAS LAr  $\sim 10^5$  cells
  - CMS HGCAL  $\sim 10^7$  cells

## Physics Prototype

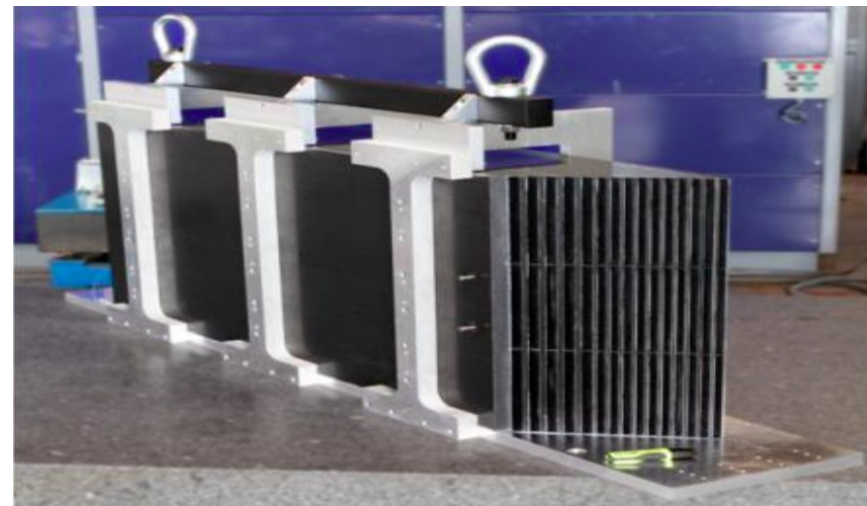
2003 - 2012



- Proof of principle of granular calorimeters
- Large scale combined beam tests

## Technological Prototype

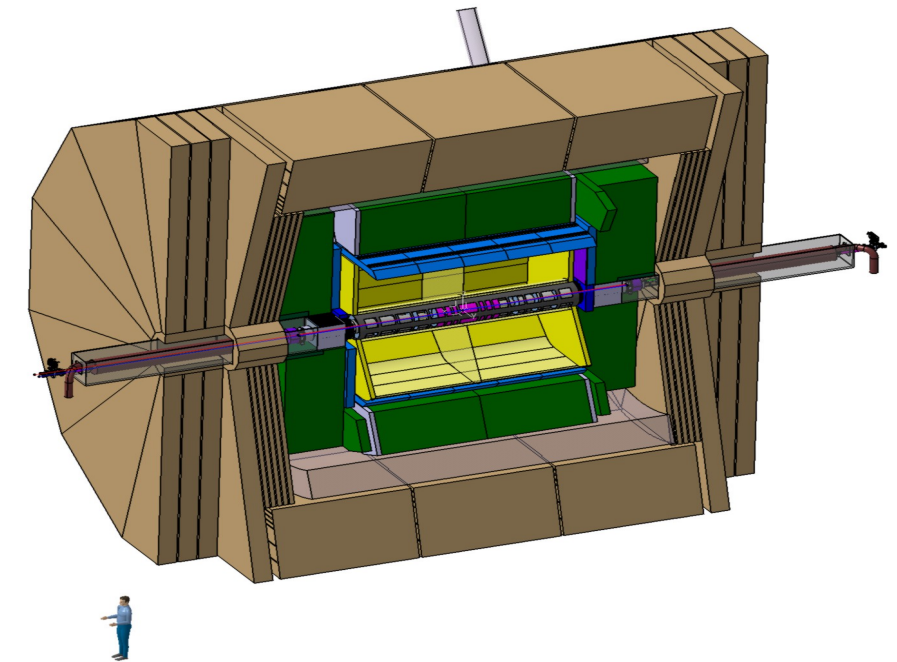
2010 - ...



- Engineering challenges
- Higher granularity
- Lower noise

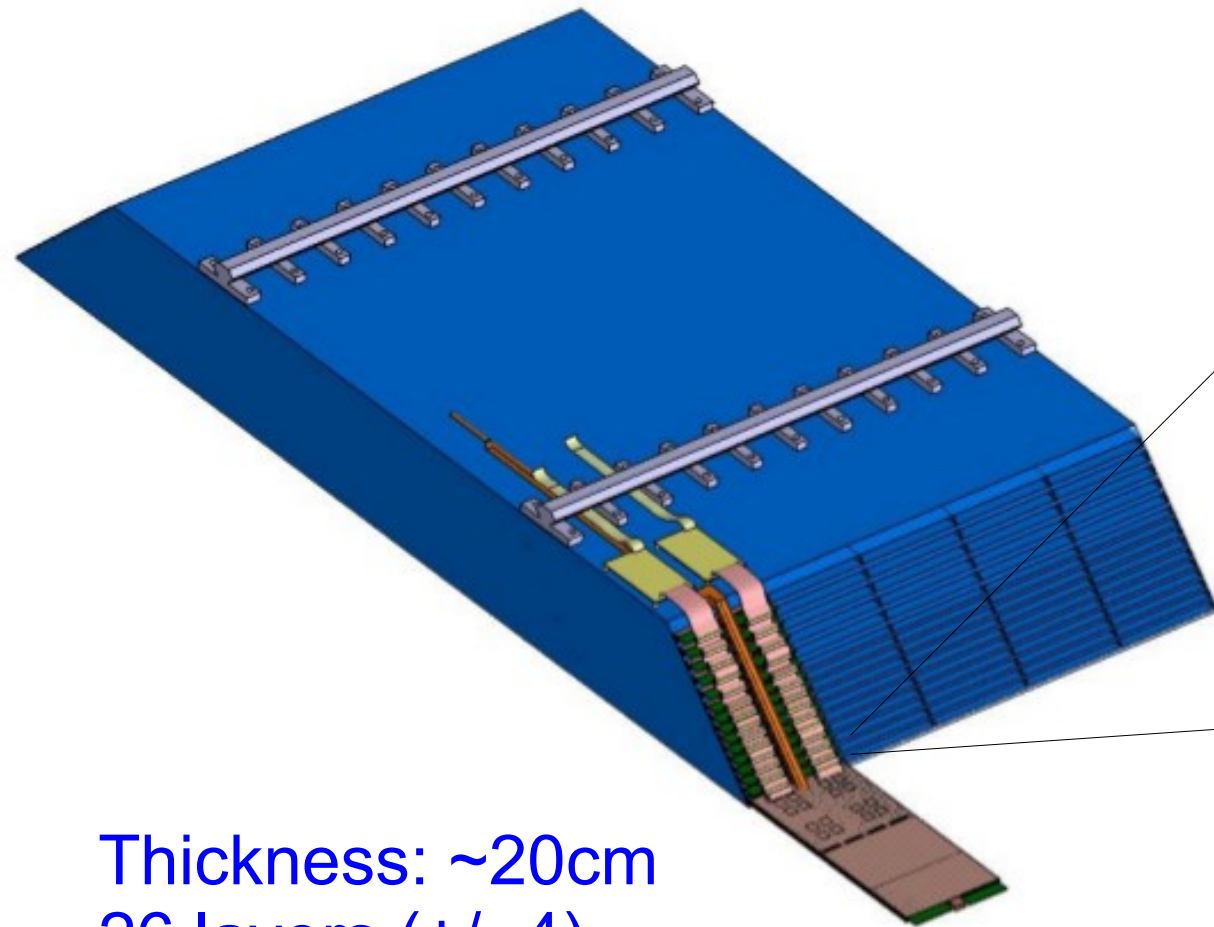
• **Today**

## LC detector



- The goal
  - Typically  $10^8$  calorimeter cells
- Compare:
  - ATLAS LAr  $\sim 10^5$  cells
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## Ecal alveolar structure

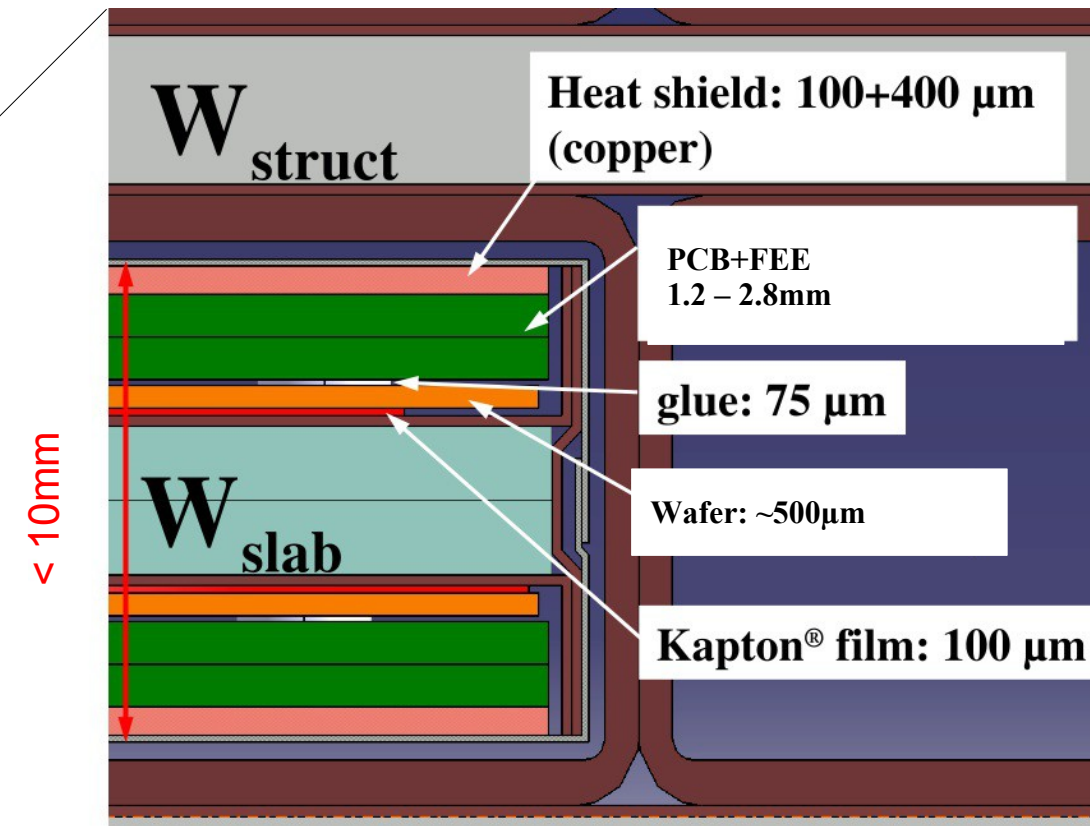


Thickness: ~20cm

26 layers (+/- 4)

$24 X_0 / 1 \lambda_1$

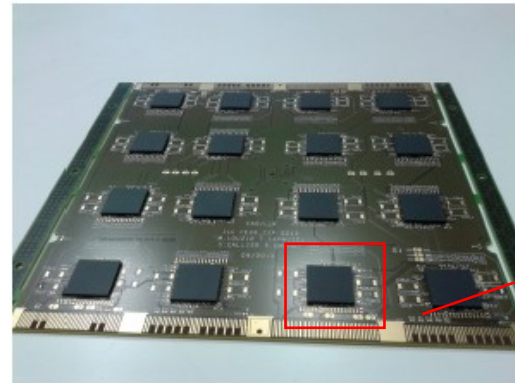
Expected elm. energy resolution  $15-20\%/\sqrt{E}$



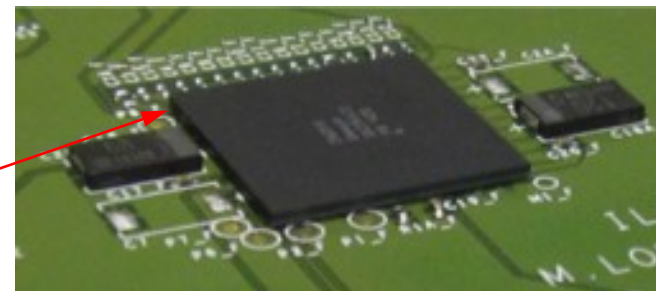
- Sandwich calorimeter
  - Si sensors as active material
  - W as absorber material
- Highly integrated design
  - ASICs in detector volume
  - Compact readout system



**ASIC+PCB+SiWafer  
 =ASU**  
**Size 18x18 cm<sup>2</sup>**  
 (IJCLab, Kyushu, OMEGA, LLR, SKKU)

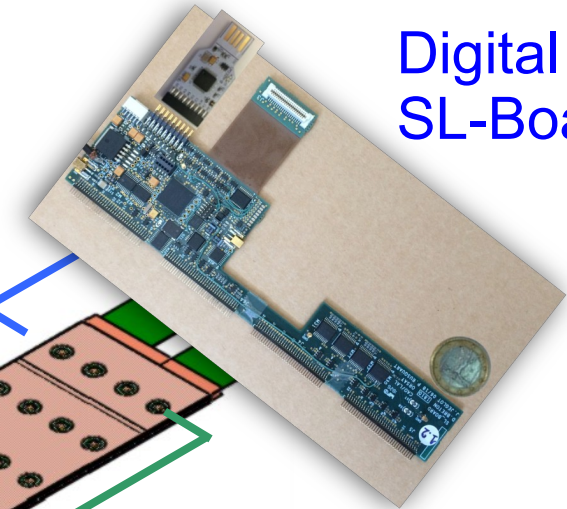


**ASIC SKIROC2(a)  
 (OMEGA)**  
**Wire Bonded or  
 In BGA package**  
 (IJCLab, Kyushu, LLR)

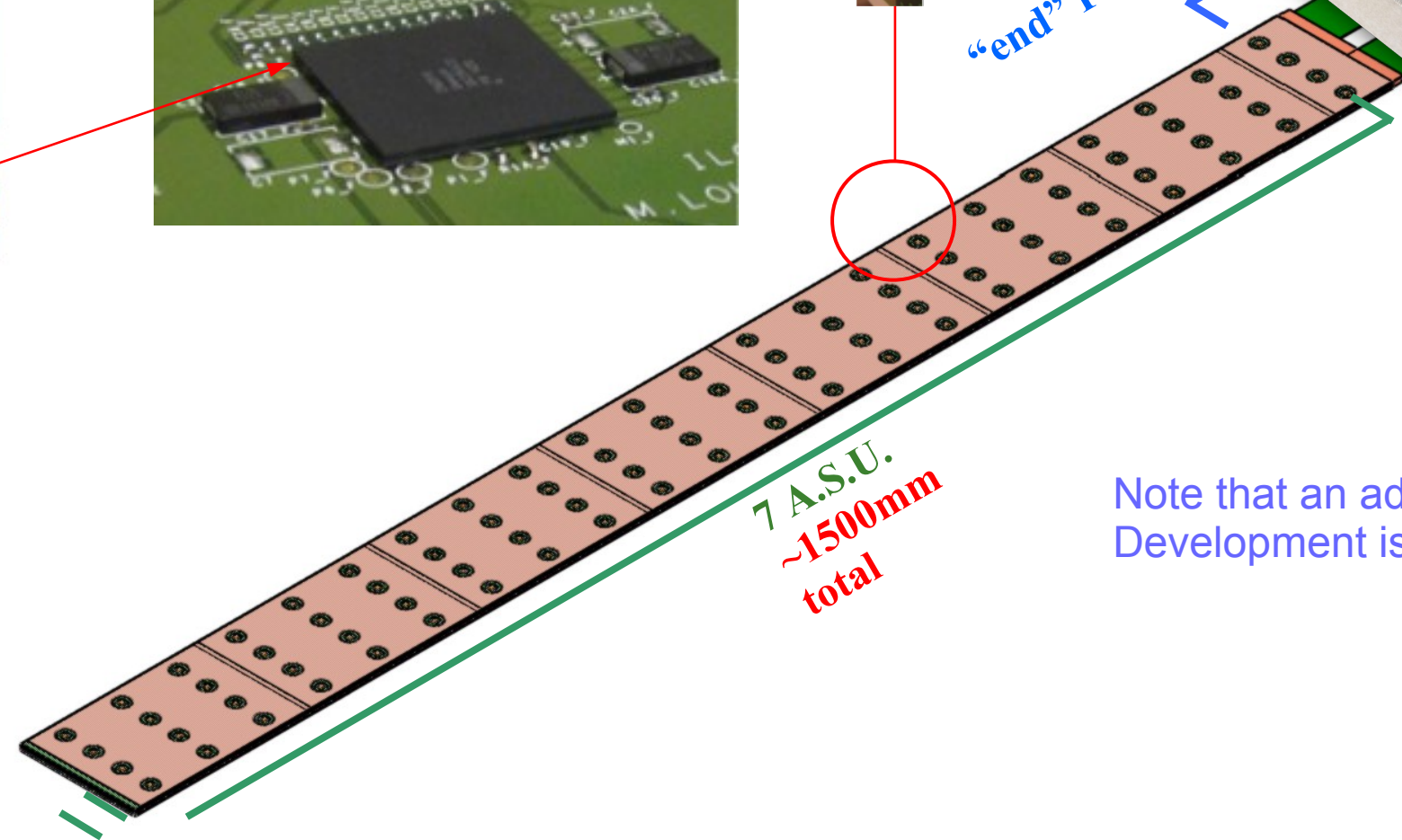


Interconnection  
 (IJCLab)

Digital readout  
 SL-Board (IJCLab)



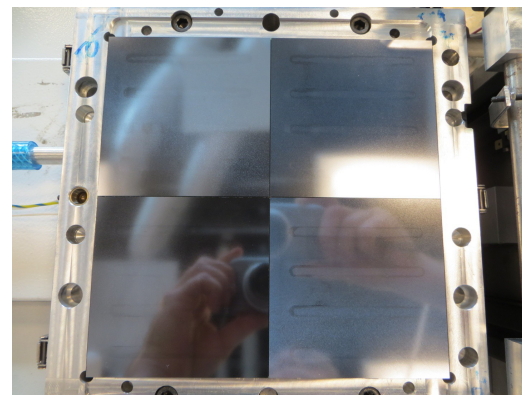
“end” PCB



7 A.S.U.  
 ~1500mm  
 total

Note that an additional hub for hardware Development is being set up at IFIC/Valencia

**SiWafers  
 glued  
 onto PCB**  
 Pixel size  
 5.5x5.5 mm<sup>2</sup>  
 (LPNHE)

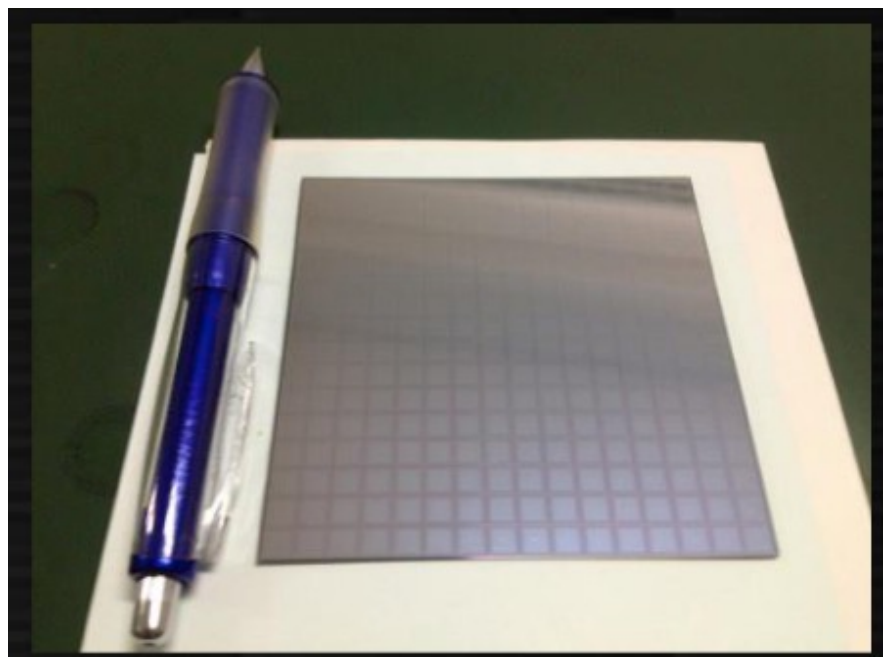


- The beam test set up will consist of a **stack of short layers** consisting of one ASU and a readout card each



## Si Sensor (9x9cm<sup>2</sup> from 6" wafer)

## Wafer specs



**Tab 1 : Summary of the substrate characteristics**

	Min.	Typ.	Max.
N type silicon	-	-	-
Resistivity (kOhms.cm)	4	5	-
Thickness (μm), option T1	310	320	<b>330</b>
Thickness (μm), option T2	490	500	<b>510</b>
Width (mm), option S1	89.7	89.8	89.9
Width (mm), option S2	44.7	44.8	44.9

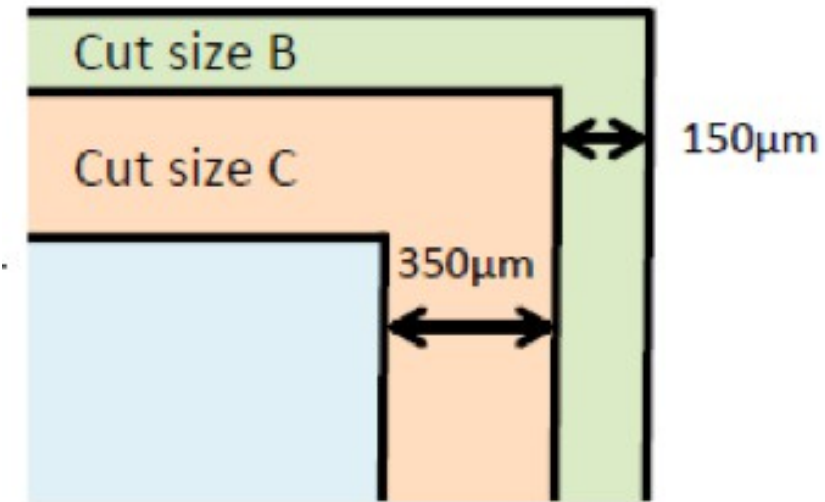
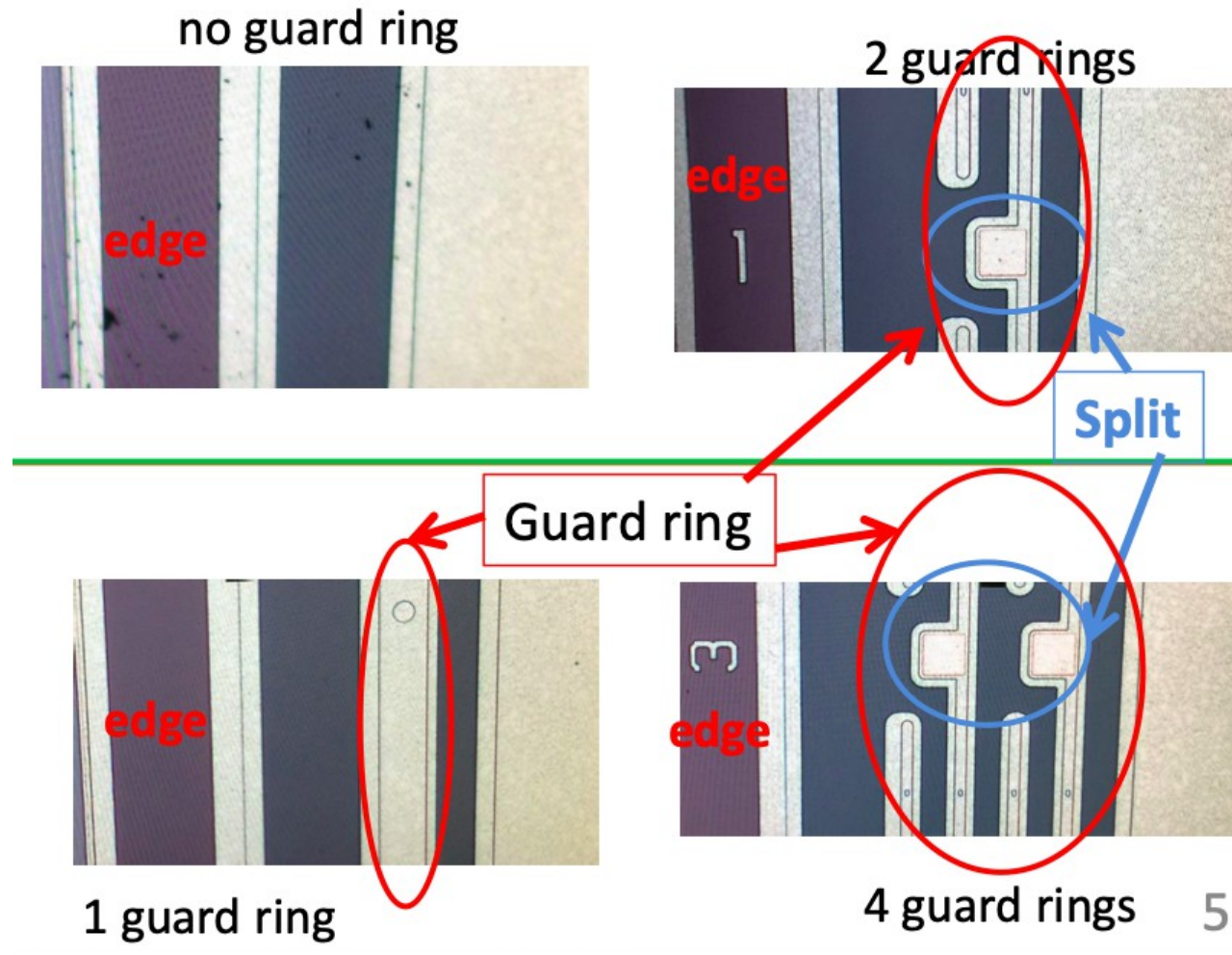
Definition of specifications for different wafer types:  
 Resisitvity: > 5 kΩxcm

N-type silicon

Crystal Orientation: <100> or <111>

- In addition we require small leakage current:s under full depletion a few nA/pixel but for cost reasons we tolerate a certain fraction of pixels with higher leakage currents
- **Vendors:** OnSemi (CZ) and Russian company for physics prototype (~2003)  
[Hamamatsu for technological prototype \(since ~2010\)](#)  
 Contacts with other vendors (e.g. LFoundry) hibernating mainly for funding reasons

We (i.e. Mainly Kyushu) have tested several wafer types in previous years



- Cut size determine the actual sensitive area of a wafer
- Different designs mainly on test samples of “baby wafers”
- The “Hamamatsu” standard is still 0 or 1 full guard ring
  - 0 is “fake 0” guard ring, in fact there is still a small guard ring

## Observations in recent years (see also backup for more details)

- Split or no guard ring lead to suppression of square events
- In prototype we still use full wafers with 0 or 1 guard ring
- General trend of reduction of bias voltage
- Can operate 500mm wafers at 60-80 V in full depletion

## Towards 8” wafers?

- General trend (e.g. CMS) is to use 8” wafers
- Larger surface/wafer => smaller cost
- Standard thickness 725mm

## SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

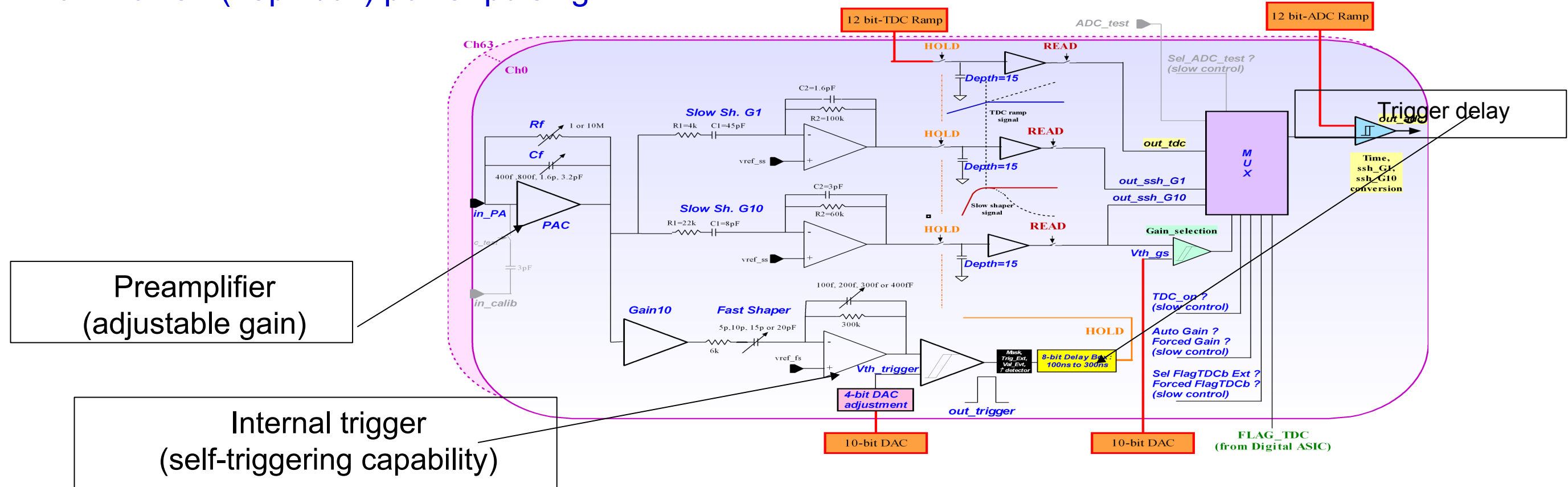
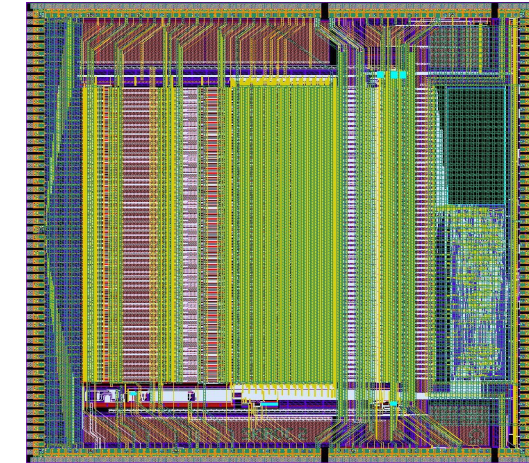
SiGe 0.35 $\mu$ m AMS, Size 7.5 mm x 8.7 mm, 64 channels

High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)

Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)

Auto-trigger at 1/2 MIP, on chip zero suppression

Low Power: (25 $\mu$ W/ch) power pulsing





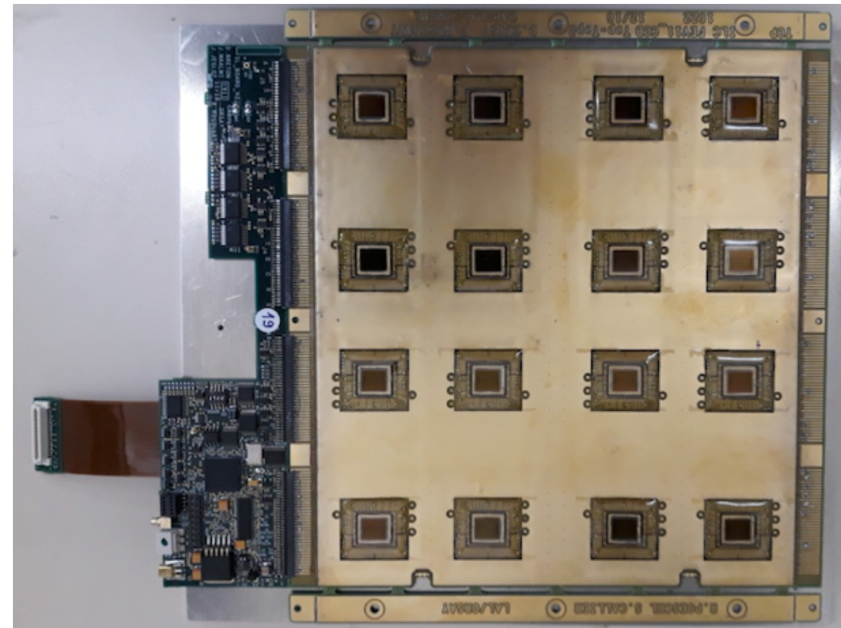
- In recent years the SiW ECAL has developed and used several PCB variants
  - To make sure that you don't get lost, here comes an introduction

FEV10-12



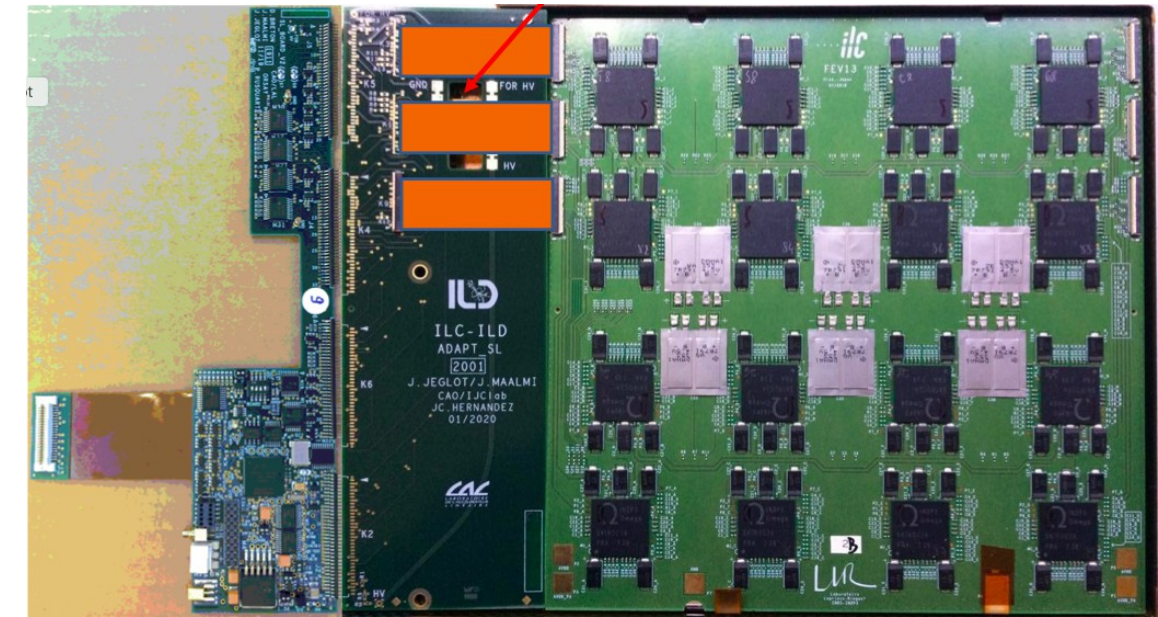
- ASICs in BGA Package
- Incremental modifications  
From v10 -> v12
- Main “Working horses” since 2014

FEV\_COB



- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- Current version FEV11\_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

FEV13

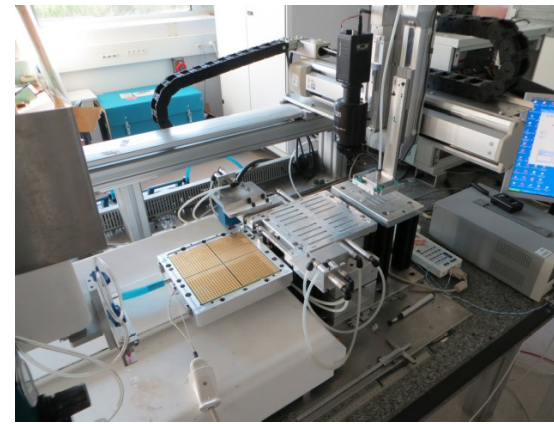
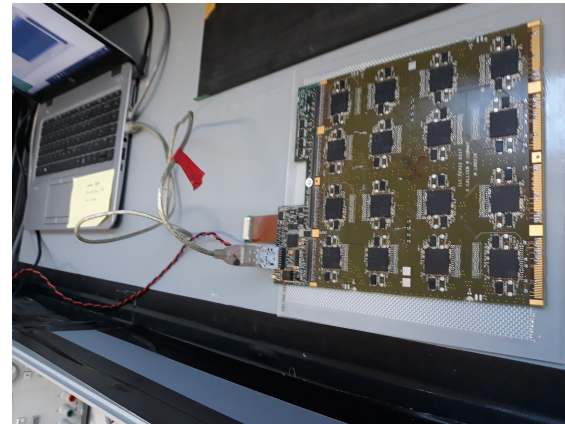


- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

Current prototype (see later) is equipped with all of these PCBs

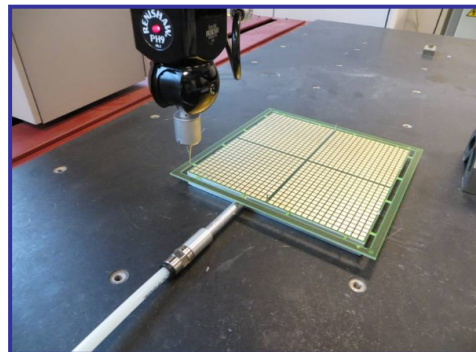


(In house) cabling and electronics tests with highly mobile DAQ system

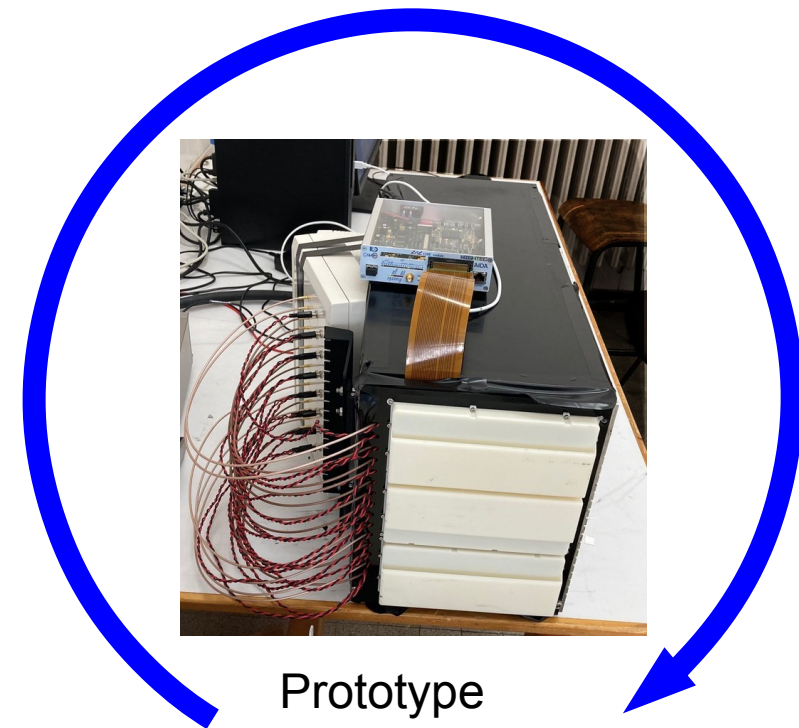


Wafer Gluing with robot

Metrology of PCBs



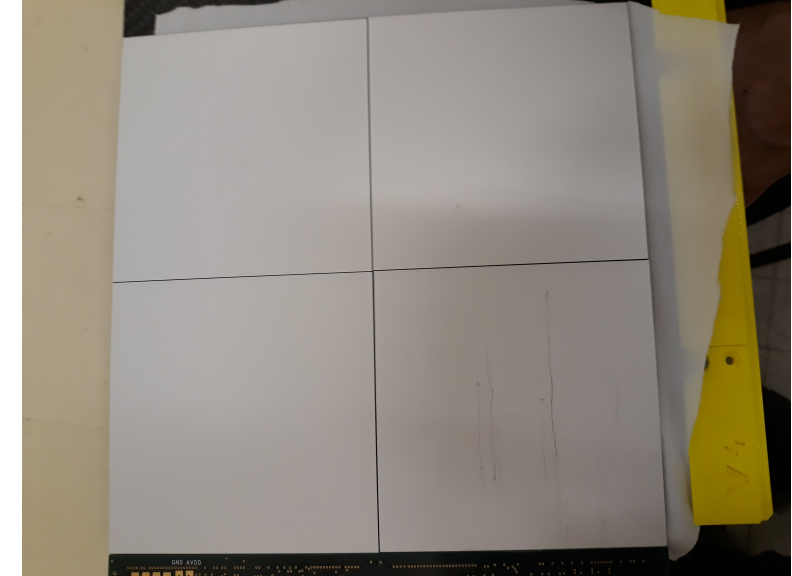
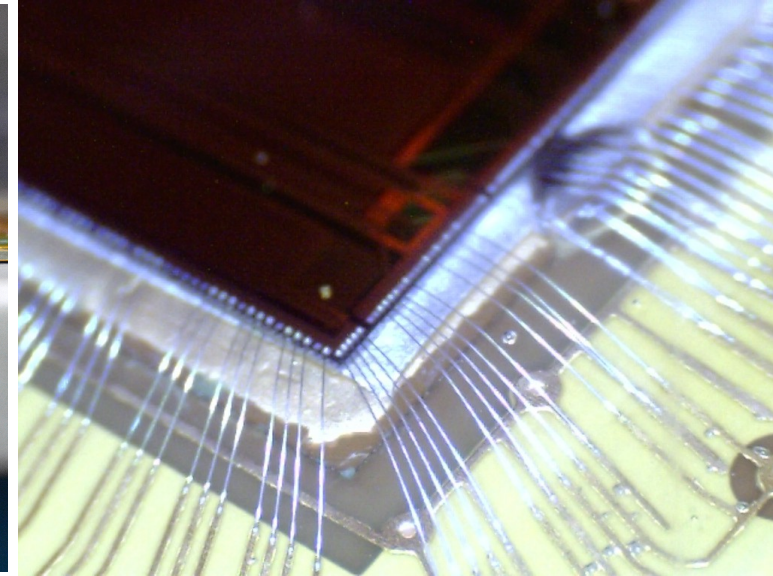
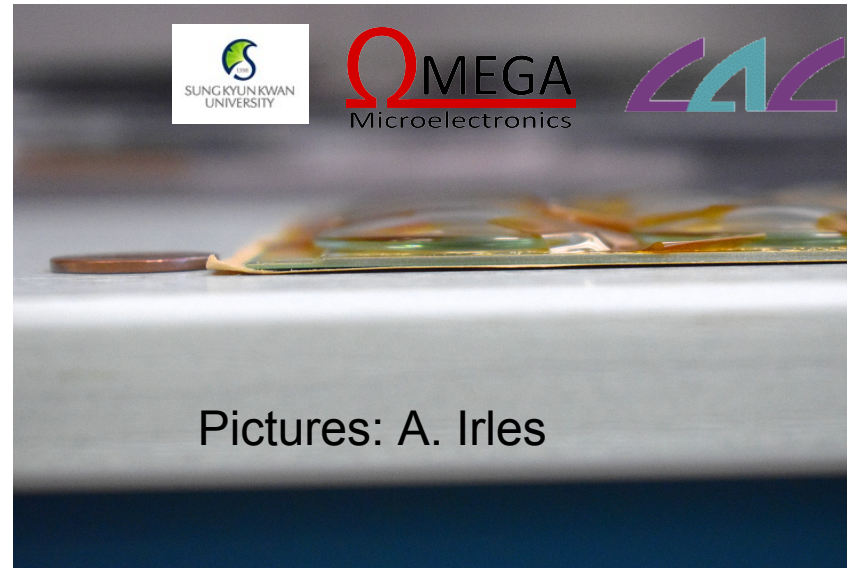
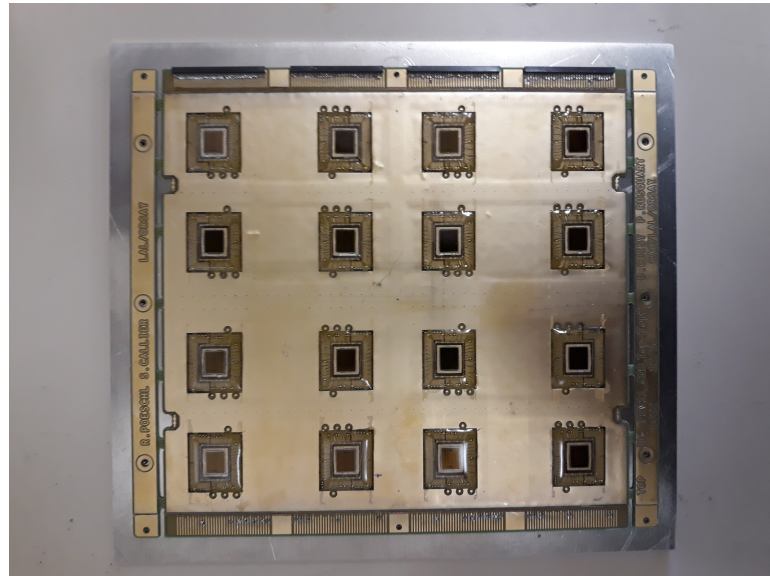
Si sensor tests



Detector assembly

Operational assembly chains in France and Japan

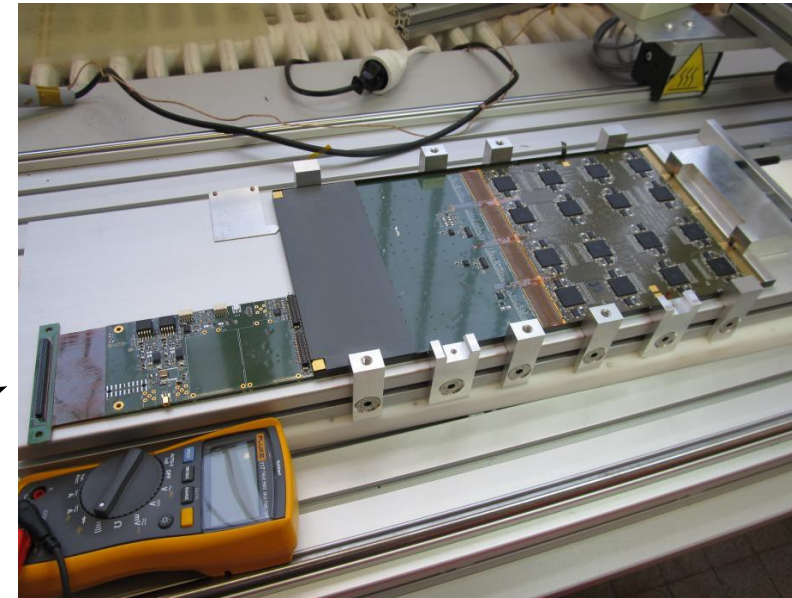
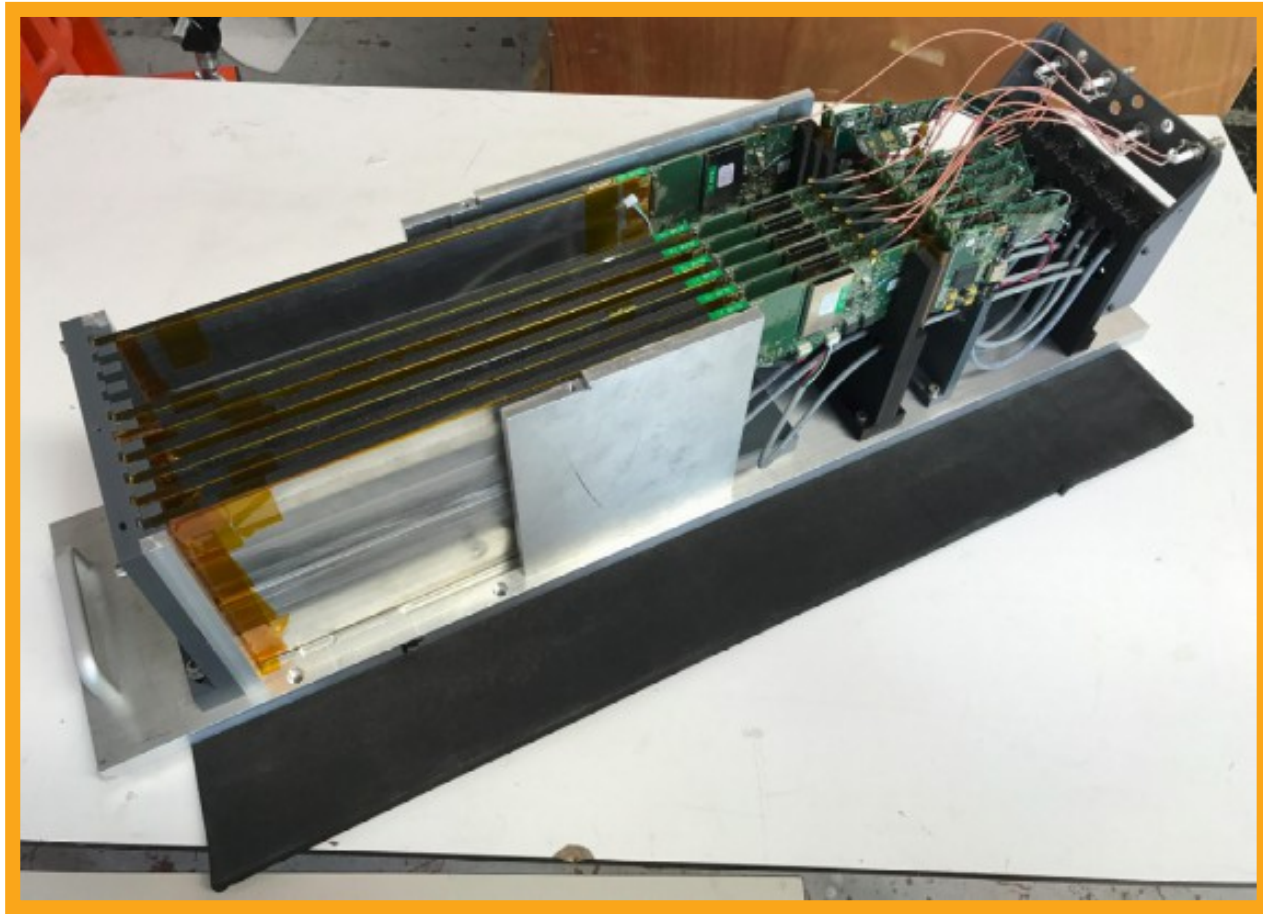




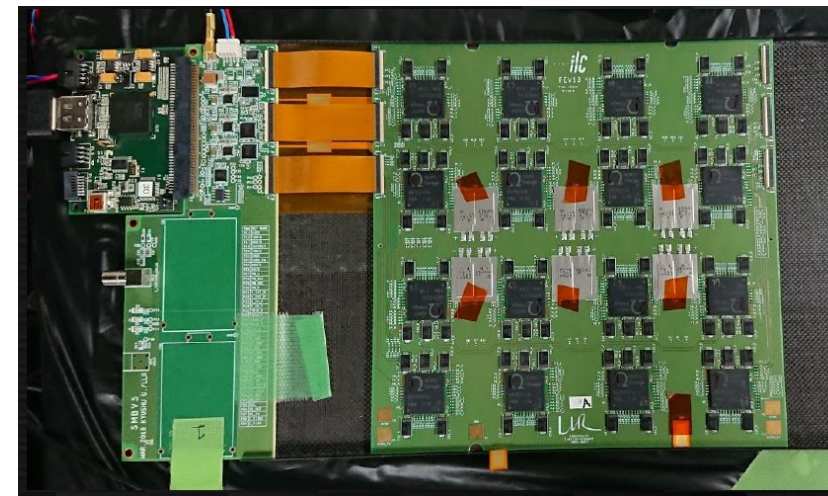
- **Height 1.2mm**
  - Thin multilayer board => Thermal stress during board production => Planarity was an issue
  - Less than 0.5mm bending after production for 8-% of the board
- **ASICs on COB have to be protected**
  - Successful “in house” application of Epoxy (Loctite Hysol) on several boards
- **Gluing of four sensors onto two boards during winter 2021/22**
  - After first test with one sensor in 2019
- First beam test in Summer 2019 with two boards (after many years of development)
- Only one wafer per board
- Full equipment for beam tests 2022



# Prototypes until ~2018



**PCB FEV10-12**  
 with long adapter card  
 Wafer thickness  
 325  $\mu\text{m}$



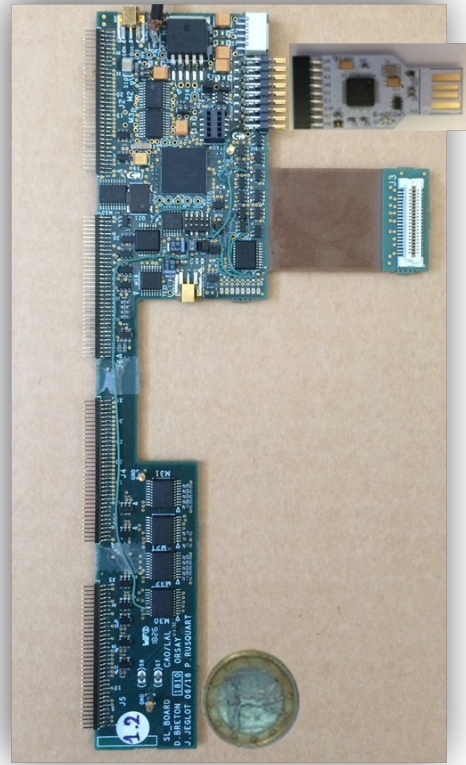
**PCB FEV13**  
 with small(er) adapter  
 card  
 Wafer thickness  
 650  $\mu\text{m}$

- Total ~15 layers constructed
  - Max of ten tested within one stack
- 1024 channels per layer
- Beam tests at DESY and CERN since 2016

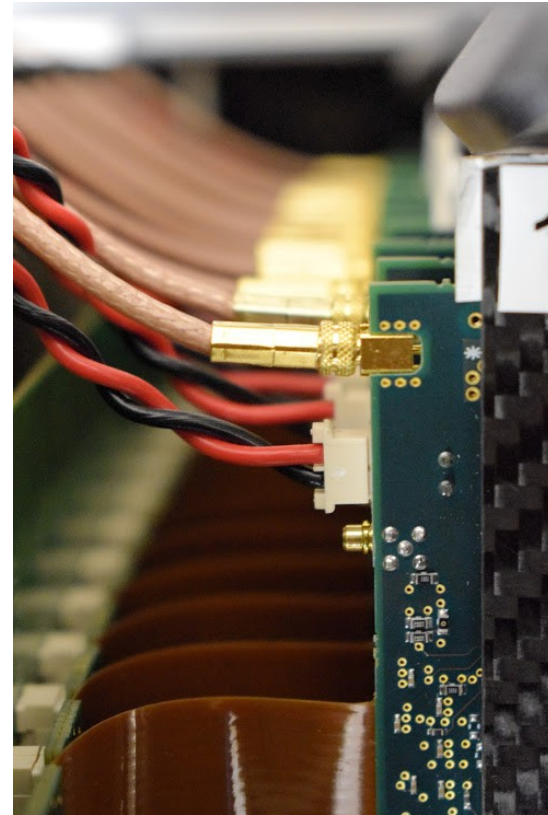
R&D for thin PCB see backup



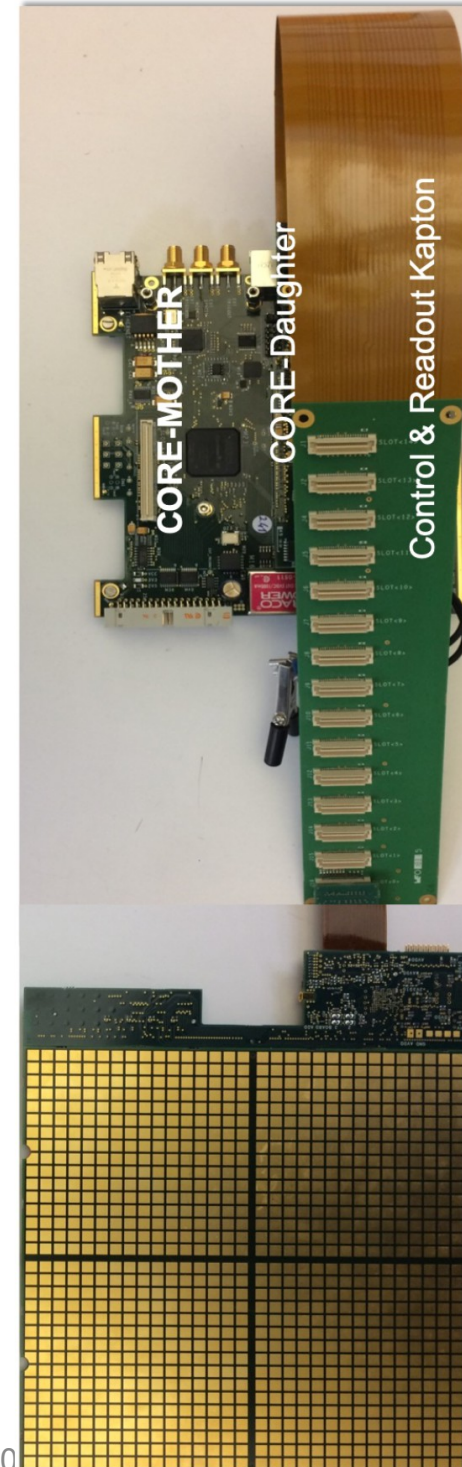
## Current detector interface card (SL Board) and zoom into interface region



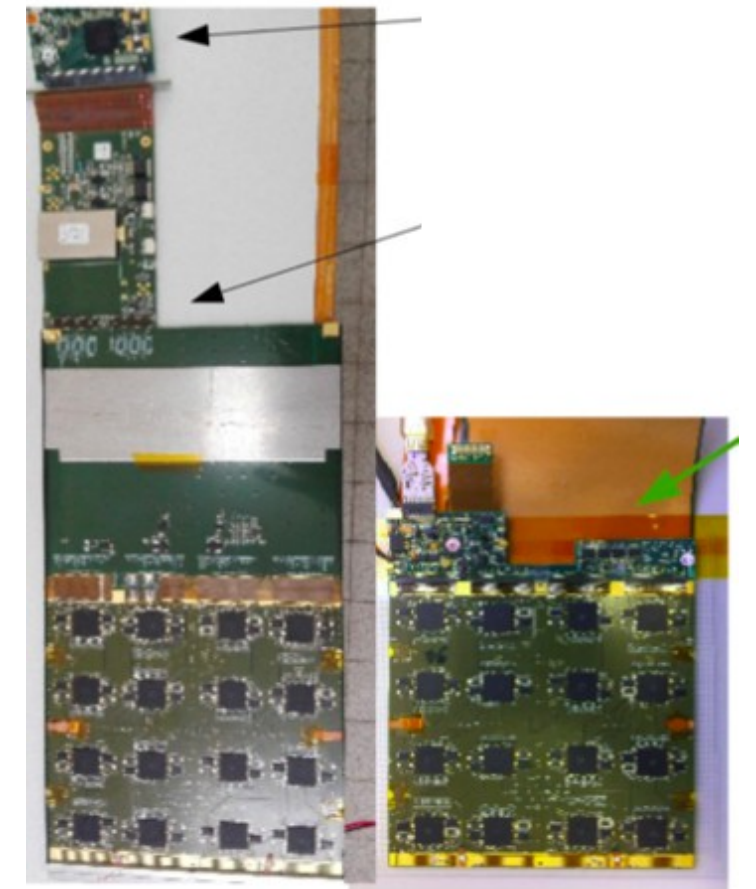
SL Board



## Complete readout system

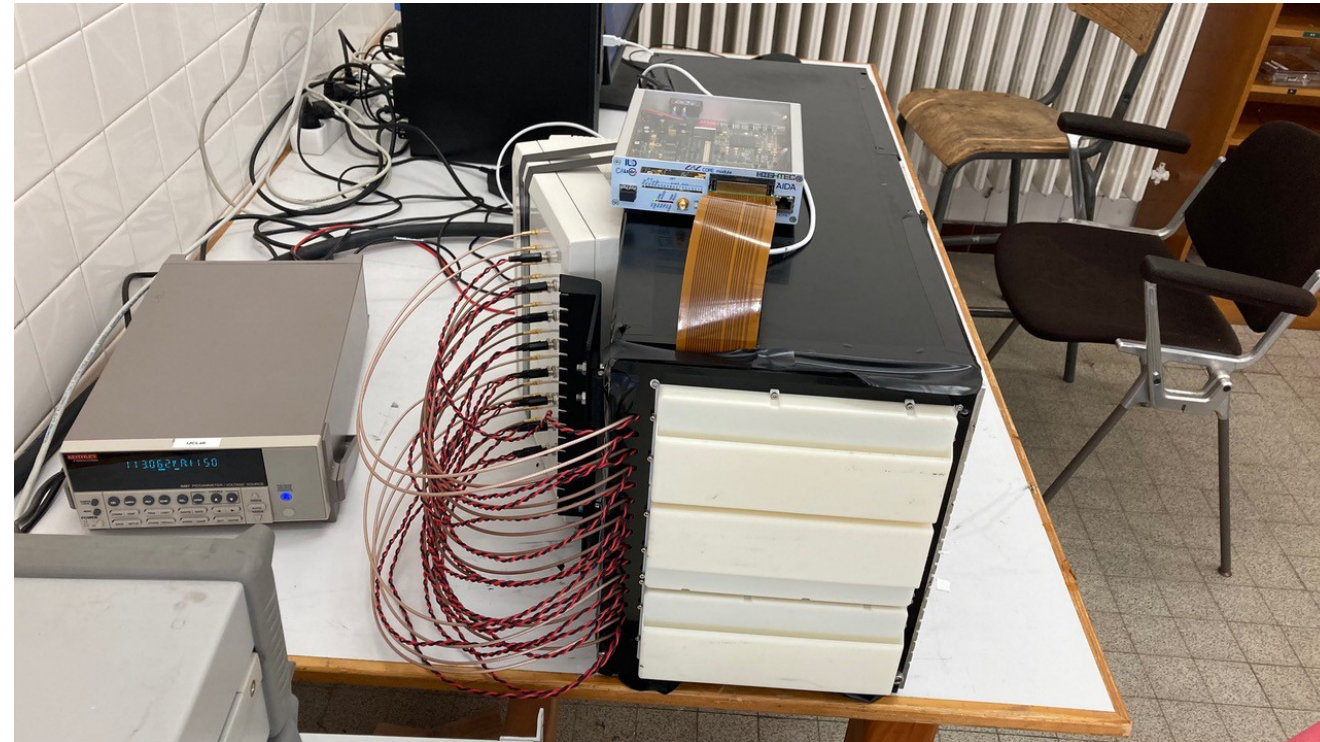
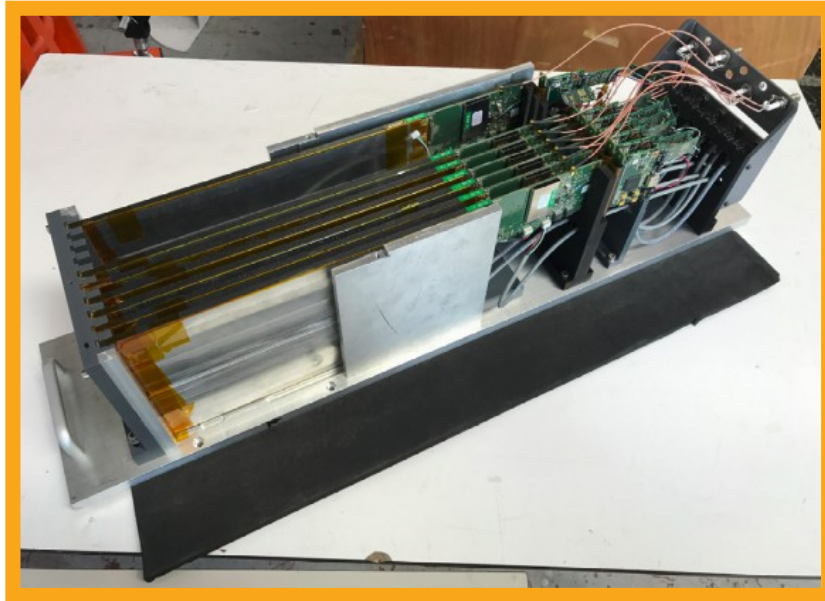


For reference  
Comparison old/new r/o system



- “Dead space free” granular calorimeters put tight demands on compactness
  - Current developments in for SiW ECAL meet these requirements
- System allows to read column of 15 layers <-> to be expected in ILD
  - Important that full readout system goes through scrutiny in beam tests



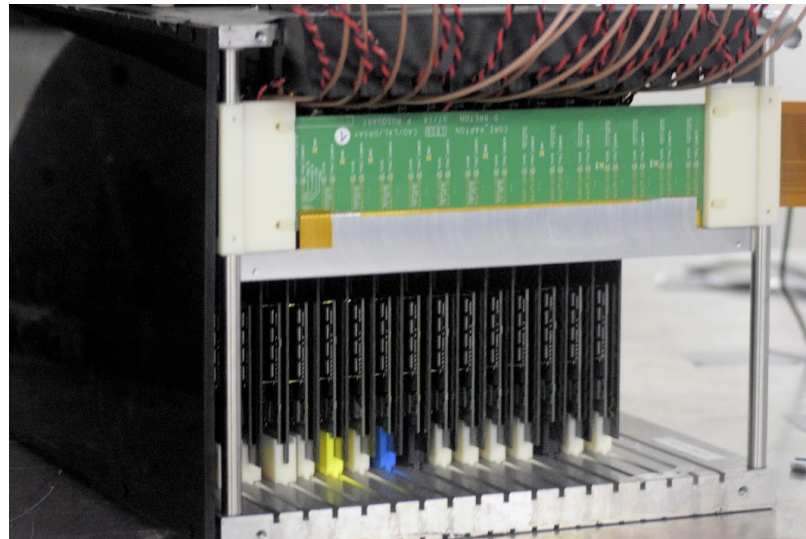


- 7 short layers ( $18 \times 18 \times 0.5 \text{cm}^3$ )
- 1024 channels per layer => 7186 cells
  - Assembly chains in France and Japan
  - Beam tests at DESY and CERN since 2016

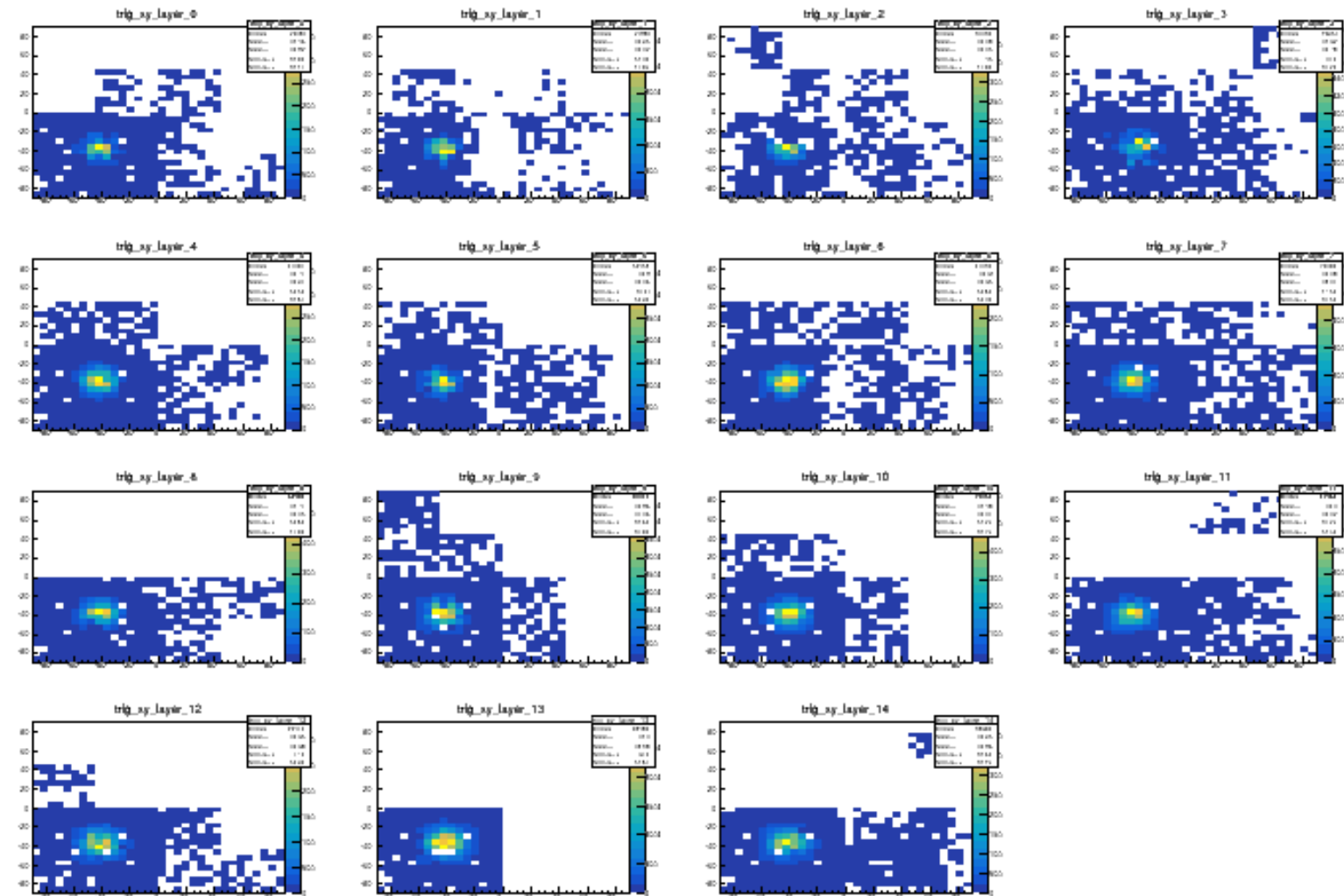
- 15 layers equivalent to 15360 readout cells
- Overall size  $640 \times 304 \times 246 \text{mm}^3$ 
  - Commissioned in 2020 and 2021
  - Testbeams (finally) in November 2021 and March 2022
  - 1.5 years in waiting loop due to pandemic



## Detector Setup



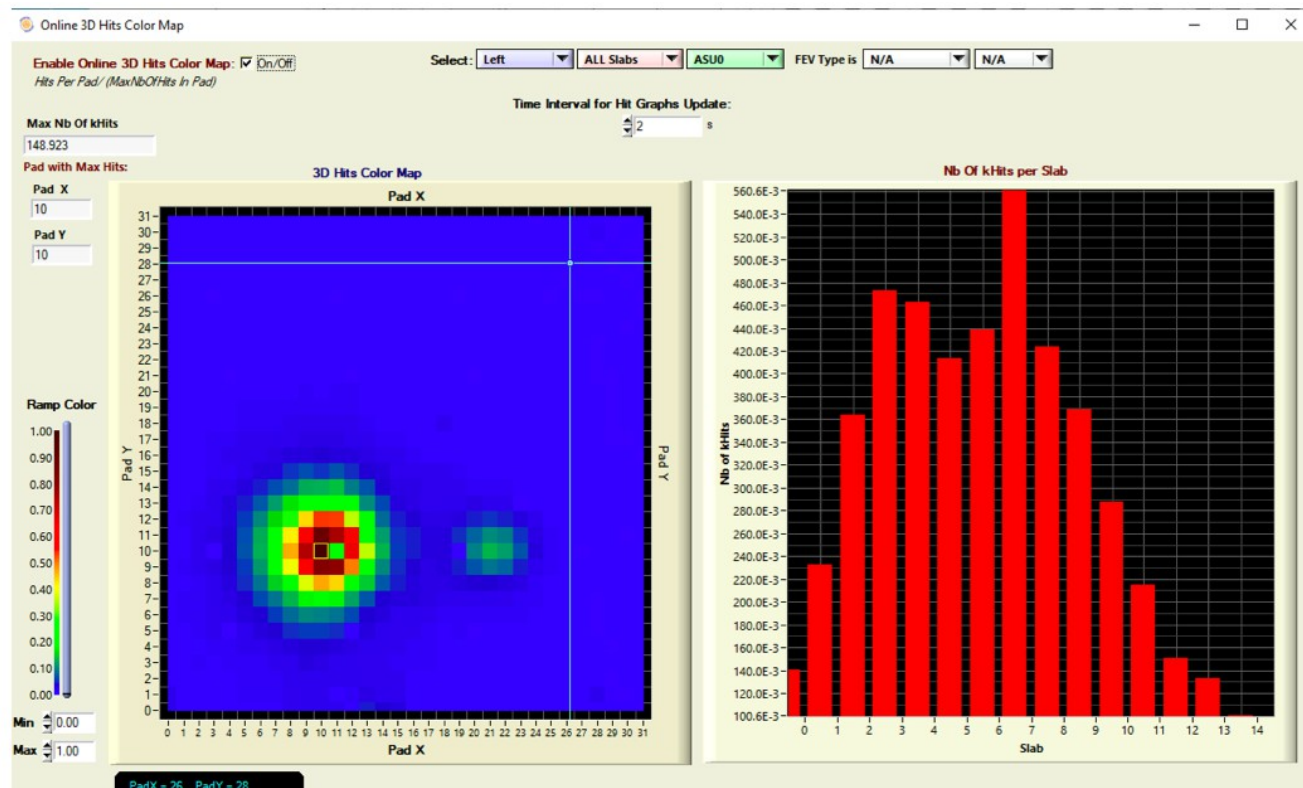
## Detector in beam position



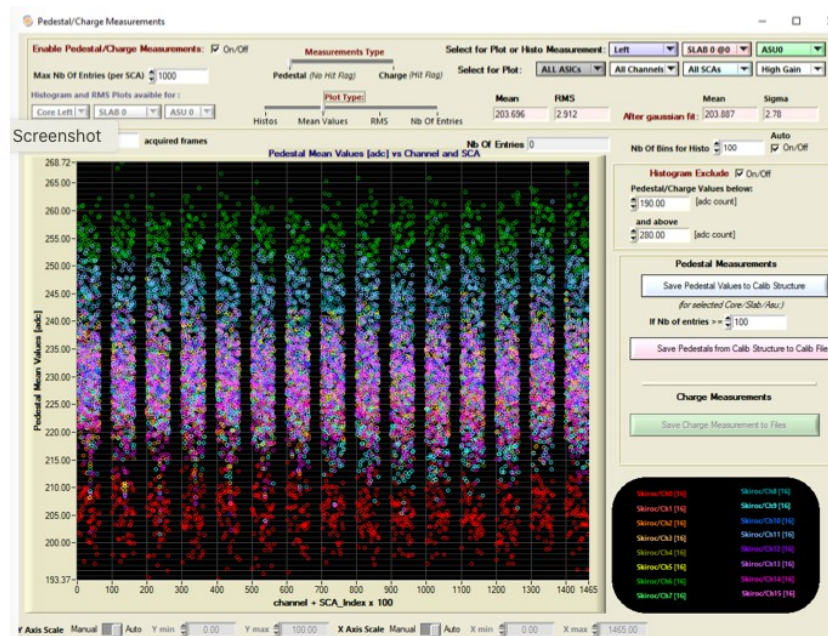
- Stack operational
- Beam spot in 15 layers

More on performance see next talk by Adrian

Jihane Maalmi, CALICE Meeting Valencia



- Online Hit Maps and shower profiles
- Allow for real time beam and detector tuning e.g. Adaptation of beam rates or thresholds

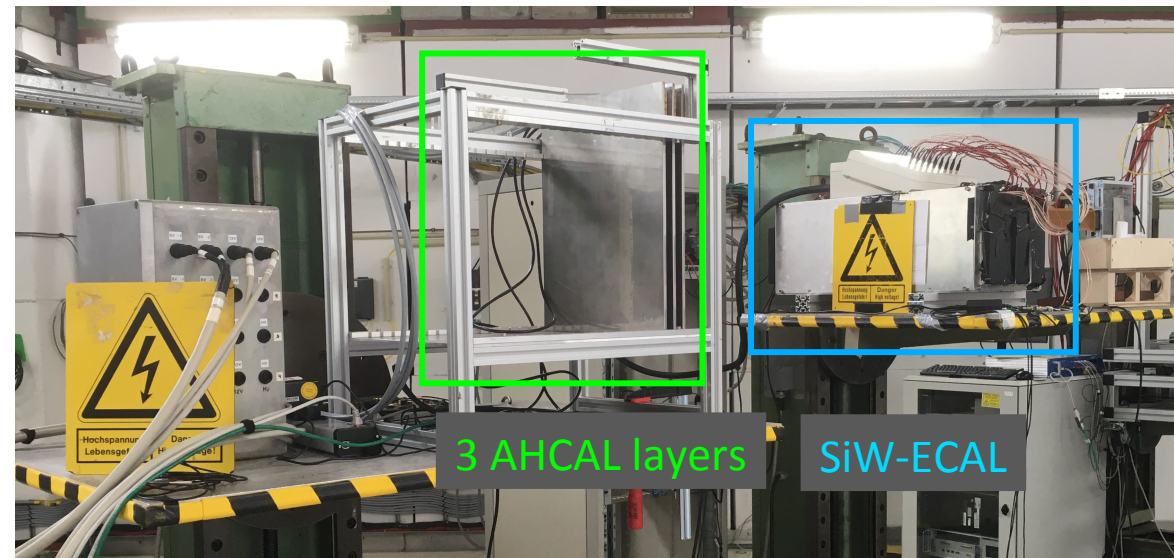


- Further online tools
- Pedestal measurement and subtraction
- Charge measurement and histogramming
- MIP gain correction

These are just a few examples from the powerful online suite



## Preparation for common SiW-ECAL AHCAL beam test



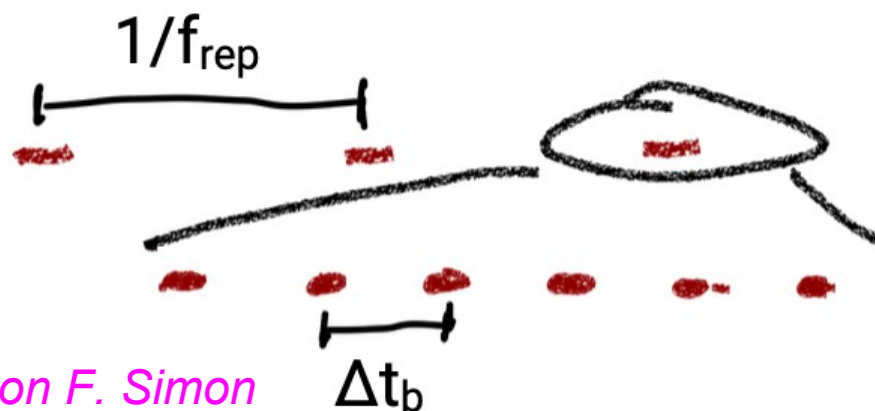
SiW-ECAL + AHCAL DAQ test @ DESY in March 2022



- Successful synchronisation of data recorded with SIW-ECAL and AHCAL
- Common running makes full use of EUDAQ tools (developed within European projects)

**Gearing up for common beam test at CERN in June**

- Linear Colliders operate in bunch trains



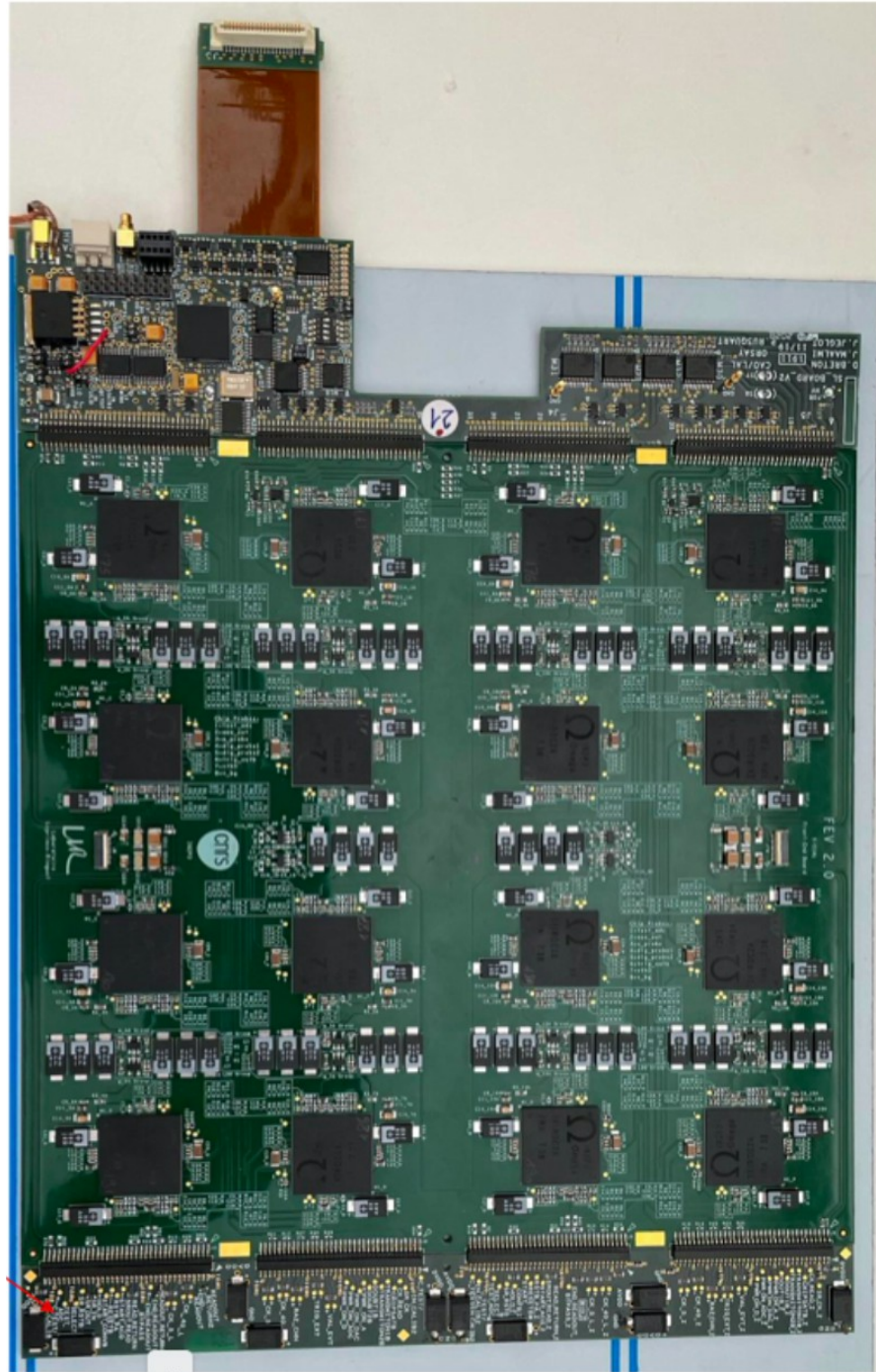
Cartoon F. Simon

CLIC:  $\Delta t_b \sim 0.5\text{ns}$ ,  $f_{\text{rep}} = 50\text{Hz}$

ILC:  $\Delta t_b \sim 550\text{ns}$ ,  $f_{\text{rep}} = 5\text{ Hz (base line)}$

- Power Pulsing reduces dramatically the power consumption of detectors
    - e.g. ILD SiECAL: Total average power consumption 20 kW for a calorimeter system with  $10^8$  cells
  - Power Pulsing has considerable consequences for detector design
    - Little to no active cooling
    - => Support compact detector design
  - Have to avoid large peak currents
  - Have to ensure stable operation in pulsed mode
- Upshot: Pulsed detectors face other R&D challenges than those that will be operated in “continuous” mode





- **Improved Layout**
  - Better shielding of AVDD and AVDD PA plans and minimisation of cross-talk between inputs and digital signals.
- **Power Pulsing Mode: new philosophy**
  - limiting the current through the Slab (current limiter present on the SL Board) to:
    - avoid driving high currents through the connectors and makes the current peaks **local** around the SKIROCs chips
    - avoid voltage drop along the slab
    - ensure temperature uniformity
  - We add large capacitors with low ESR for **local** energy storage (around each SKIROC chip)
  - Generate **local** power supply with LDO (Low Drop Out) to avoid voltage variations
- **Clean clock distribution all over the slab**
  - for Slow Control and Readout Clocks
- **Parallel configuration and readout over 2 partitions.**
- **Driving high voltage up to 350V for 750 $\mu$ m wafer (via the ASU connectors)**
  - Adding a filter for each wafer HV and limit the current in case of wafer failure

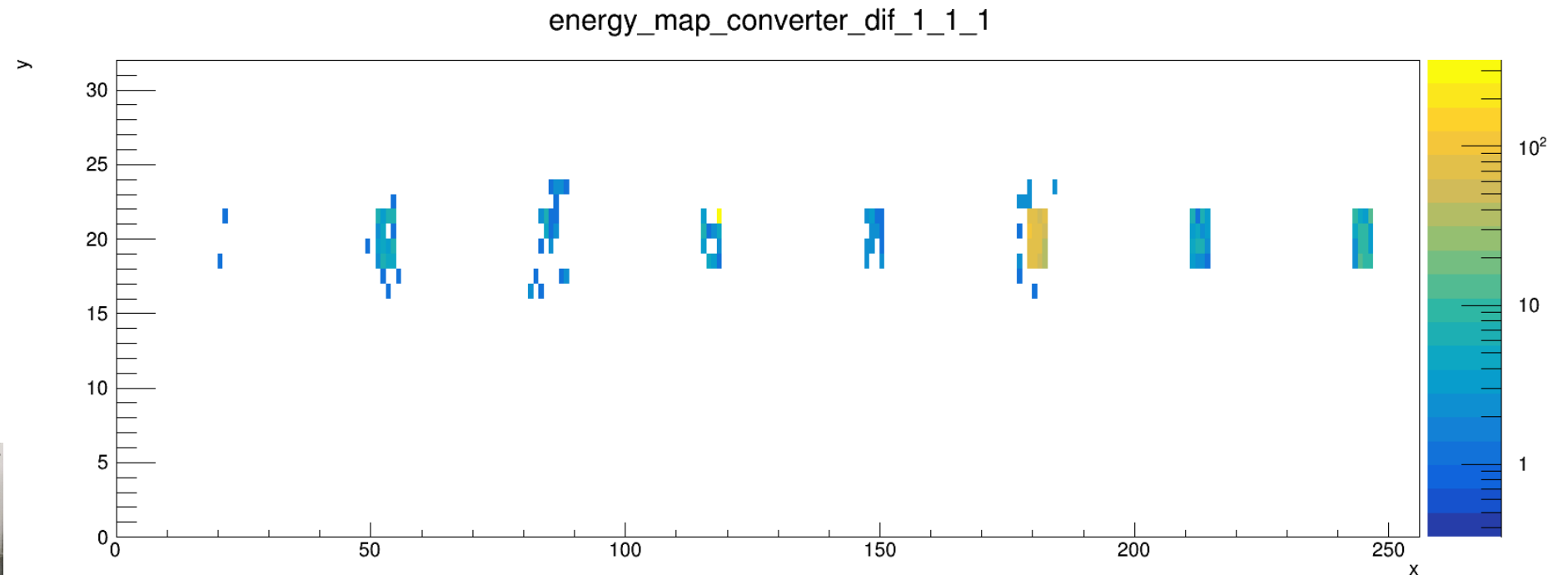


*LM*

Chain of  
8 detection elements  
~3m



Beam test at DESY June 2018



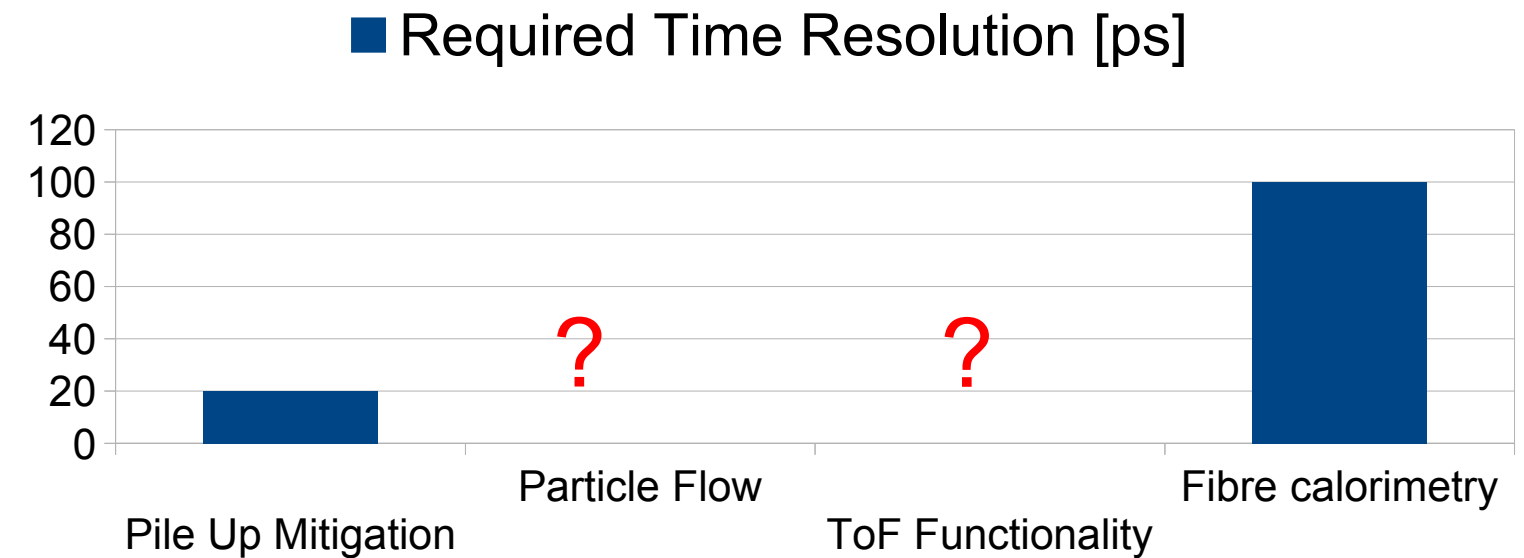
- **Very encouraging results in first beam test in 2018**
  - Credibility for concept as foreseen for e.g. ILD
  - Issues with signal drop towards extremities
- **Long slab studies will be resumed with new FEV**
  - Adapted for power pulsing, will avoid voltage drop, etc ...

## (Non exhaustive) “To do list” (for LC Detector)

	Today	LC Detector
#cells*	15360	10 <sup>8</sup>
Sensor surface/m <sup>2</sup>	0.5	2000-2500
Sensor type	9x9cm <sup>2</sup> based on 6” wafers	Size ? Based on 8” wafers?
Real size slabs	1 “electrical” long layer	~10000 detector slabs (5000 double layers)
Front end ASICs	SKIROC2, ns timing	SKIROC3, ps timing? Need 1.2-1.5M
Digital electronics	SL-Boardv2 (already quite close)	New versions, need 9k
DAQ	Highly performant system for prototype	Scaling to full detector
PCB	FEV2.x (already quite close)	Integration of new FE electronics, need ~75k
Slow control	Integrated in SL Board	Solution for full detector?
Mechanical Structures	1 barrel alveola structure (EUDET 2010)	40 barrel modules + <b>endcaps</b>
Carrier Boards	Simple carbon plates	“H Boards” with wrapped W (Studies date back to 2010-2016)
Cooling	Advanced studies (AIDA-2020)	Full detector integration Continuous powering would be a new world
Engineering (electrical and mechanics)	Advanced studies (for ILD IDR)	Require full revision and consolidation
Software	Few skillful people	Needs consolidation and person power

- **A lot has been achieved**
  - ... but the way is still long, as of today the team is too small and the funding is very (too) volatile
  - We are good in engineering but too few (young) physicists

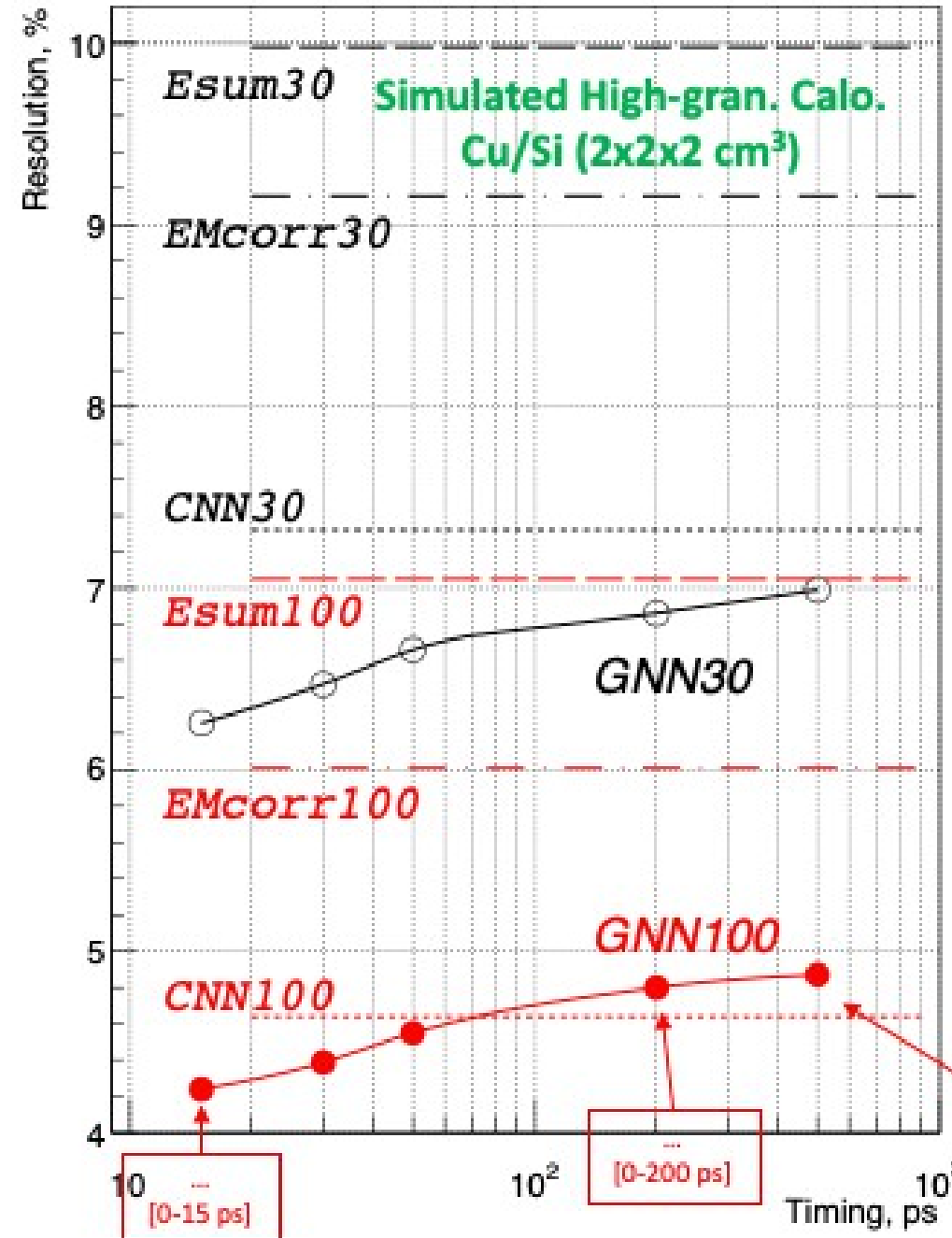
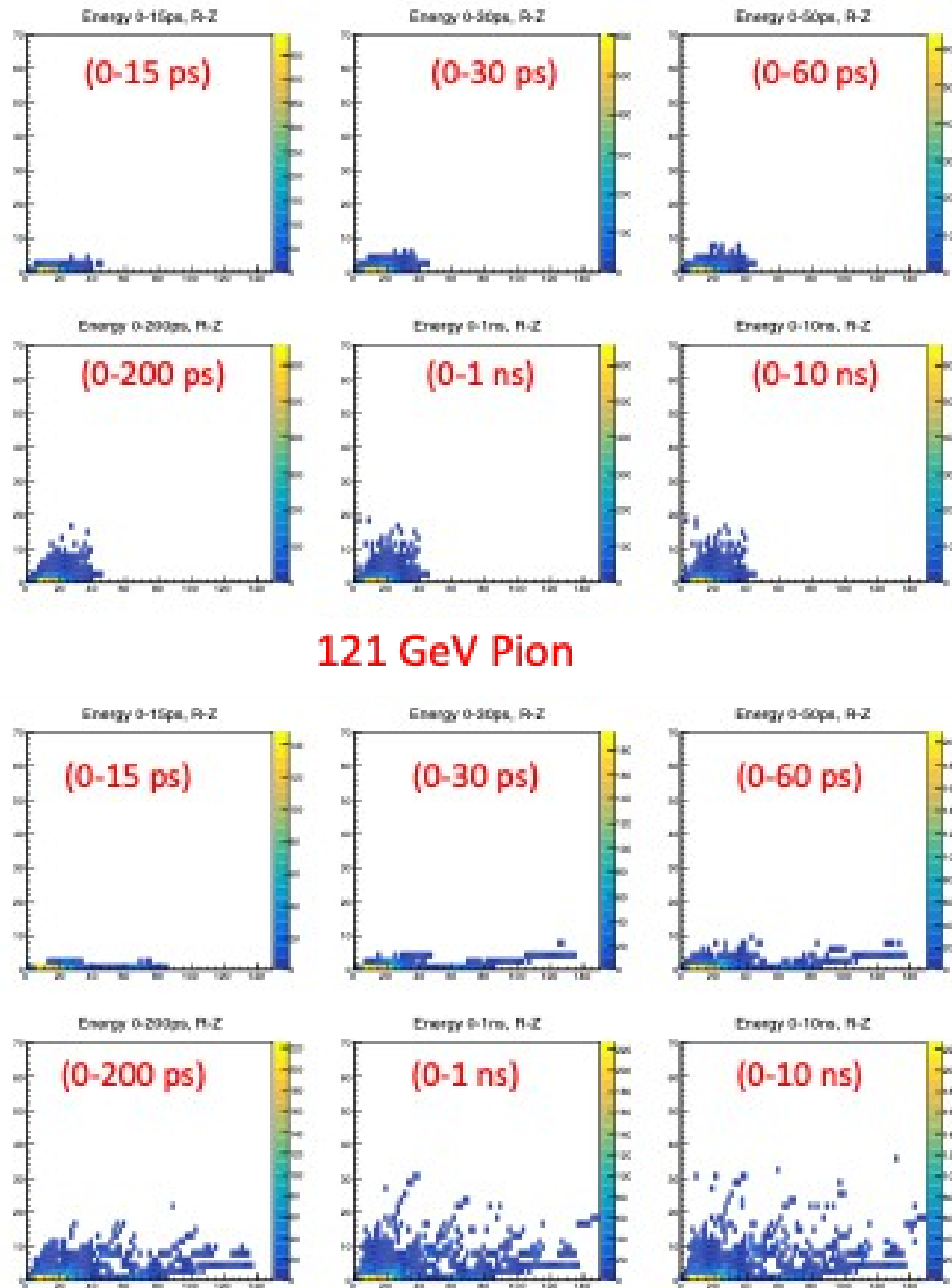
- Timing is a wide field
- A look to 2030 make resolutions between 20ps and 100ps at system level realistic assumptions
- At which level: 1 MIP or Multi-MIP?
- For which purpose ?
  - Mitigation of pile-up (basically all high rate experiments)
  - Support of PFA – uncharted territory
  - Calorimeters with ToF functionality in first layers?
    - Might be needed if no other PiD detectors are available (rate, technology or space requirements)
    - In this case 20ps (at MIP level) would be maybe not enough
  - Longitudinally unsegmented fibre calorimeters
- A topic on which calorimetry has to make up it's mind
  - Remember also that time resolution comes at a price -> High(er) power consumption and (maybe) higher noise levels





# Timing in calorimeters

Features that emerge in the time domain can help distinguish particle types and, with GNNs, enhance  $\sigma(E)/E$



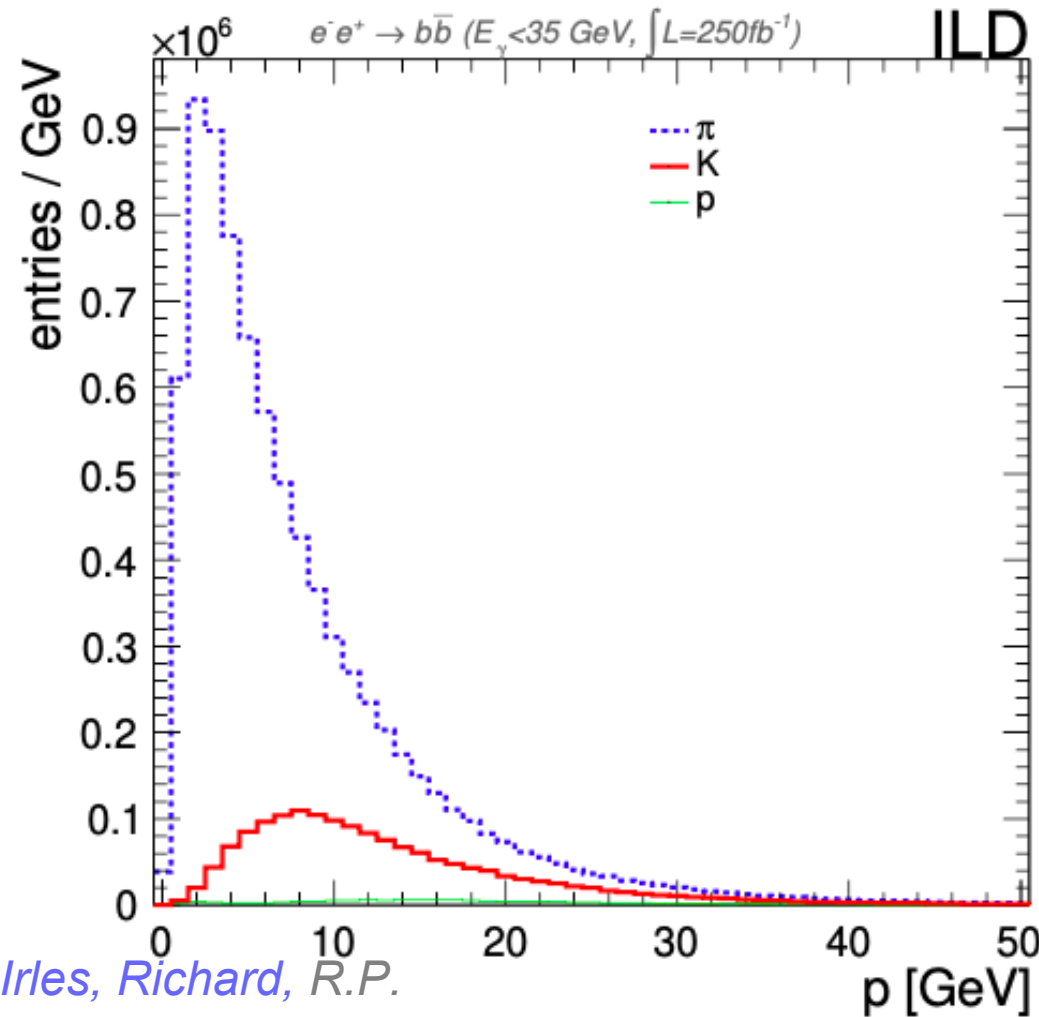
**CNN** trained on pions achieves marked improvement over the conventional approach while maintaining performance for photon reconstruction

**GNN**, with edge convolution (PointNet), with shower development timing information further improves energy resolution when shorter time slices are included

[0-10 ns]  
[0-4 ns]  
[0-1 ns]  
[0-0.5 ns]

[arxiv:2108.10963](https://arxiv.org/abs/2108.10963)

## Momenta and abundance of pi/K/p in ee->bb @ 250 GeV



ILD: Irlas, Richard, R.P.

## Available time resolution with calos

Available "now"

Doable with Intensive R&D in 5-10 years

Requires a new breakthrough

## Difference in ToA at ILD Calos

Barrel, R=1.6m, B=4T, cosθ=0

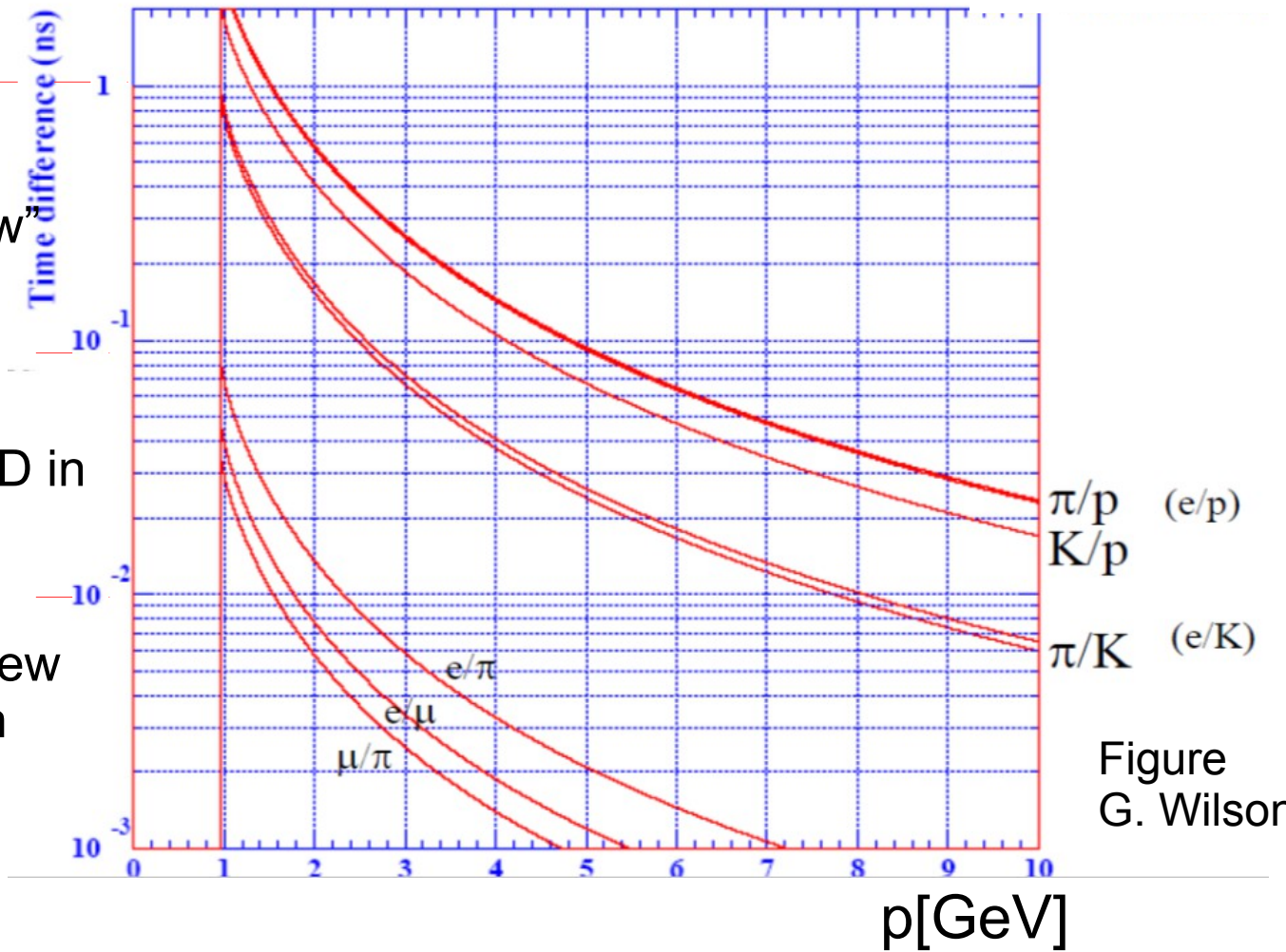


Figure G. Wilson

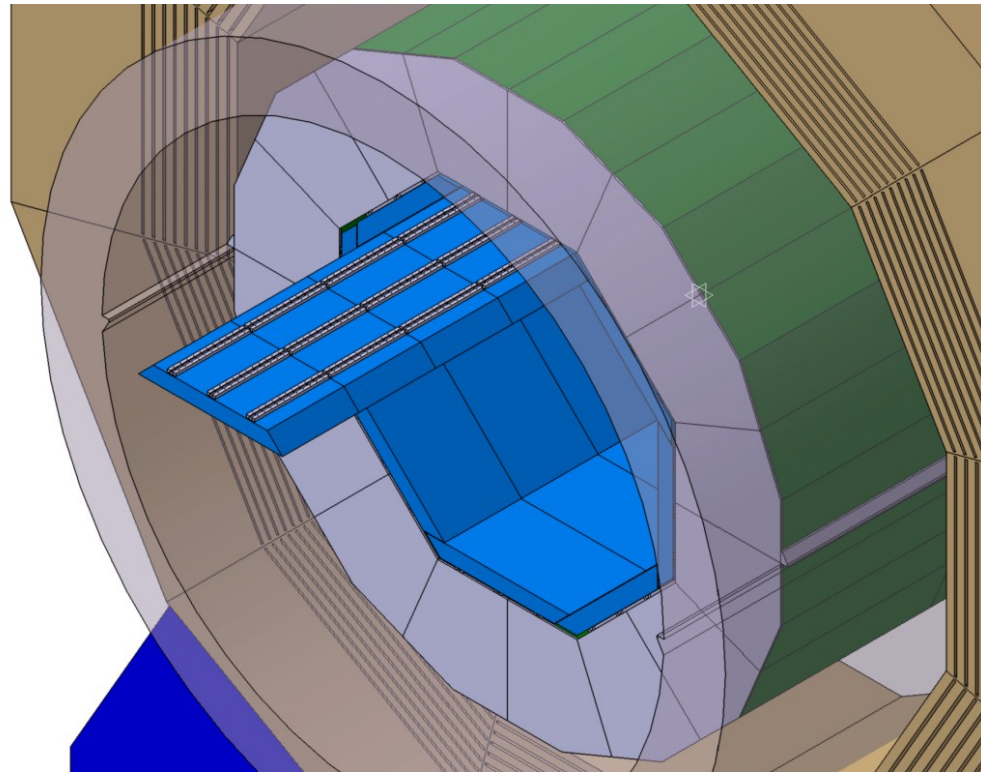
- Particle momenta (at 250 GeV) have peak below 10 GeV but long tail to higher energies
- Realistically ToF measurements will be (in foreseeable future) limited to particles below 10 GeV
  - Note that, apart from power consumption, in a final experiment one needs to control full system
- **Momenta above 10 GeV require a real breakthrough and maybe even radically new approaches**
  - Mandatory if ToF should work at and well above 250 GeV i.e. at Linear Collider energies

- **Successful operation of a fifteen layer stack in two beam tests at DESY**
  - Major milestone for technological prototype
  - Demonstration of performance of compact DAQ
  - Rich set of data to study detector performance
  - Have already precious feedback on strong points but also of weak spots
    - The inhomogeneity in the layer response is a matter of concern
    - Debugging has started
- **Powerful infrastructure to conduct conclusive system tests now and in coming years**
- **New type of PCBs will allow for finalising the R&D in terms of power pulsing and for bringing us to the “eve” of an engineering prototype in the next around two years**
  - Sufficient support provided ... the team is working at the limit
  - We need in particular more people for data analysis
- **Have to make up our minds on the requirements for timing in PFA calorimeters**



# Backup

- Optimized for Particle Flow: Jet energy resolution 3-4%, Excellent photon-hadron separation



The SiW ECAL in the ILD Detector

- $O(10^8)$  cells
- “No space”
- => Large integration effort

## Basic Requirements:

- Extreme high granularity
- Compact and hermetic
- (inside magnetic coil)

## Basic Choices:

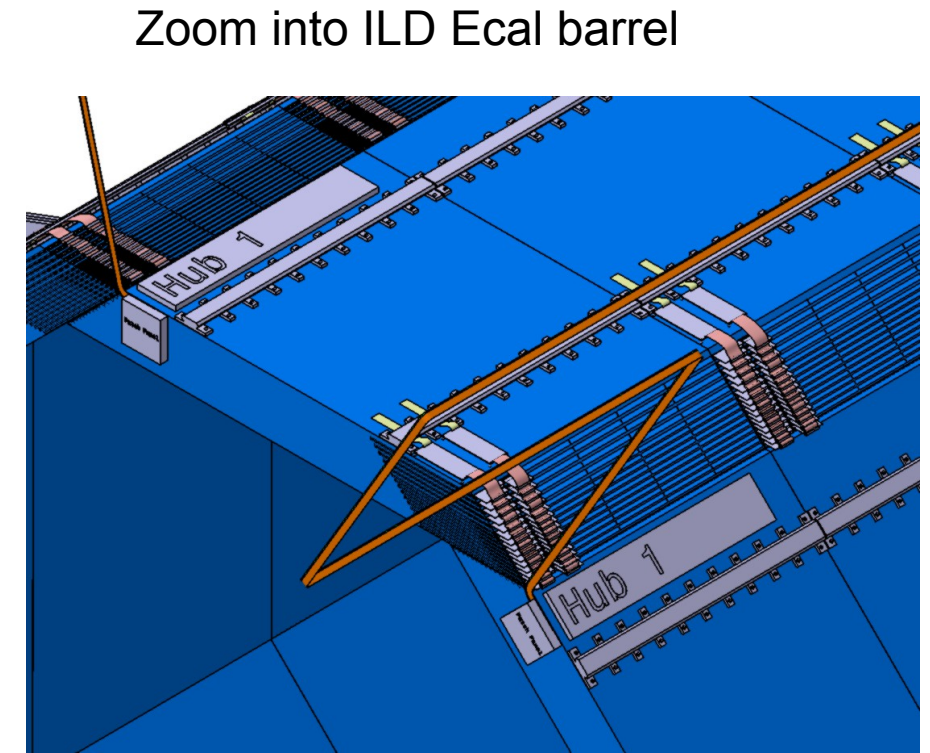
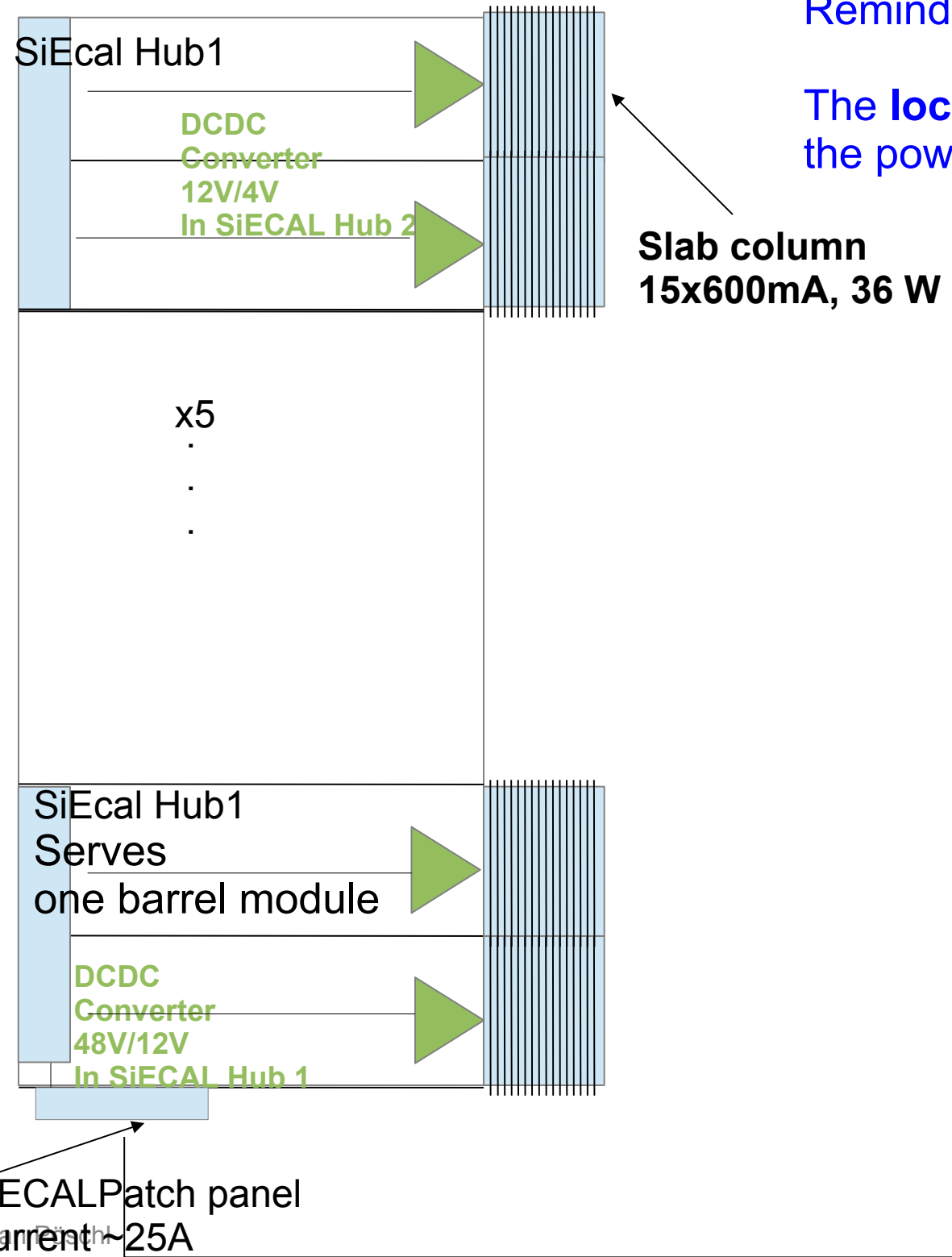
- Tungsten as absorber material
  - $X_0=3.5\text{mm}$ ,  $R_M=9\text{mm}$ ,  $\phi=96\text{mm}$
  - **Narrow showers**
  - **Assures compact design**
- Silicon as active material
  - **Support compact design**
  - **Allows for pixelisation Robust technology**
  - **Excellent signal/noise ratio: 10 as design value**

- **All future e+e- collider projects feature at least one detector concept with this technology**
  - Decision for CMS HGCal based on CALICE/ILD prototypes

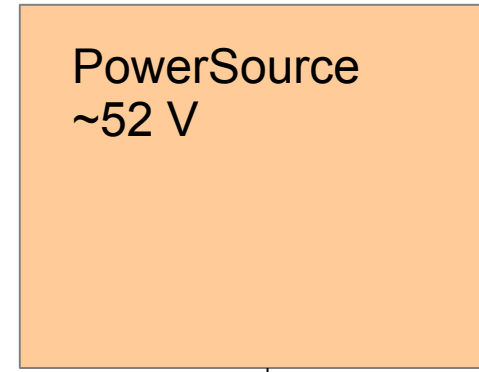


Reminder IDR

The **local** power storage is at the heart of the powering concept of the ILD SiECAL



Power cable trailer <-> SiECAL Patch panel



- Total average power consumption **20 kW** for a calorimeter system with  $10^8$  cells\*
- Only possible through PP
- The art is to store the power very locally
- Issue for upcoming R&D

\*Compare with 140 kW for CMS HGAL FEE  $6 \times 10^6$  cells

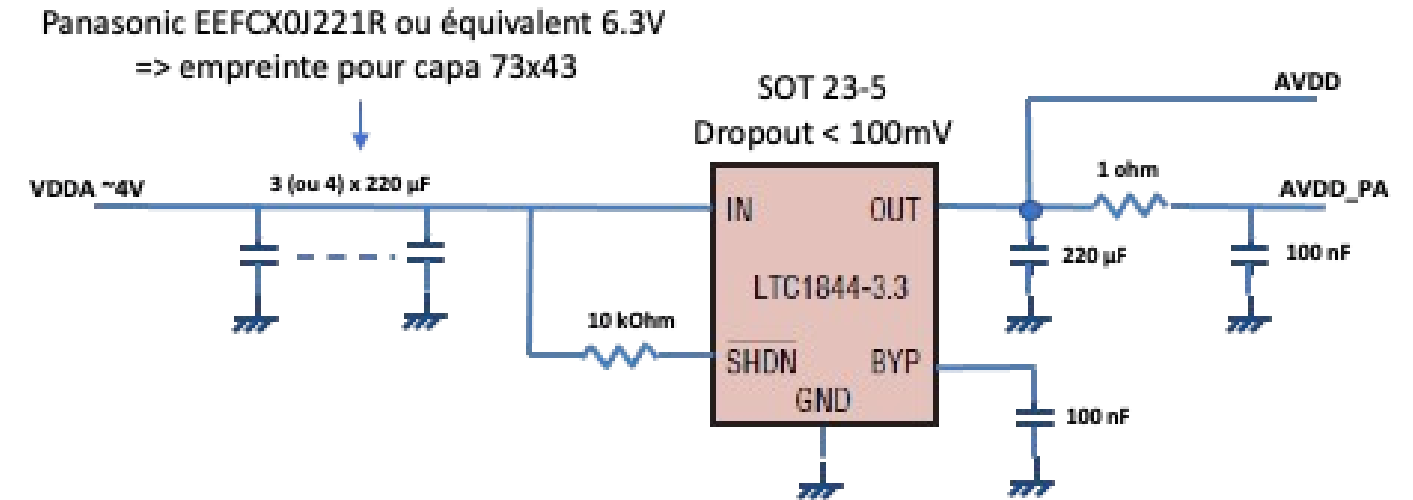
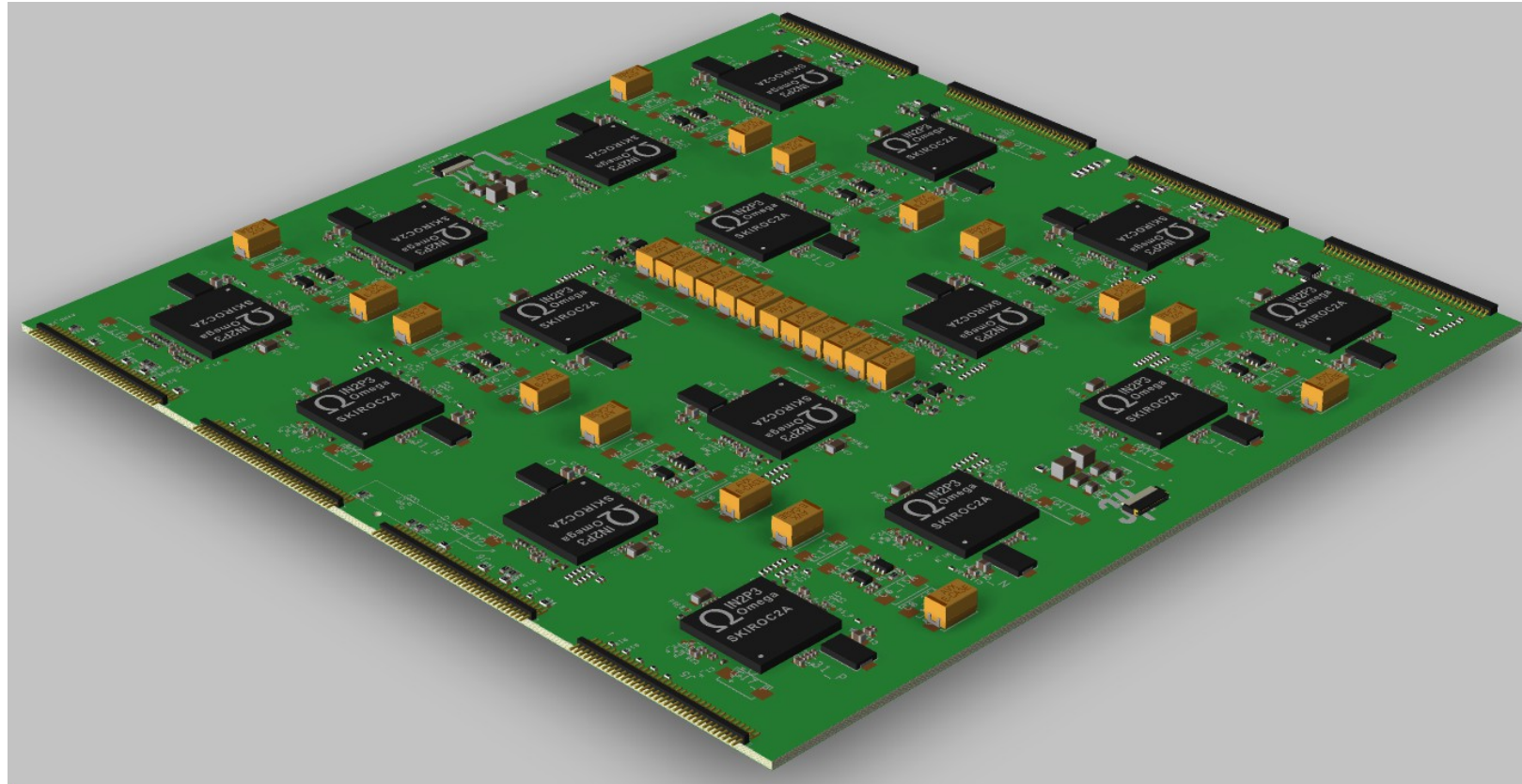
- Dynamic gain preamp or TOT ?
- 200 ns shaping, 10 MHz ADC, several samples on the waveform
- Timing capability ? Auto-trigger and zero suppression
- Target ~1 mW power/ch and possible power pulsing
- I<sup>2</sup>C slow control ? New readout protocol ?
- Include 2.5V LDO inside VFE ?
- Compatible with FCC LAr. SiPM/RPC tbd

	experiment	Sensor	capacitance	shaping	power	data	techno	Vdd	slow control	
→	SKIROC2	CALICE	Si	30 pF	300 ns	5 mW/ch	5 MHz	SiGe 350n	3.3 V	SPI
	HGCROC	CMS	Si	50 pF	20 ns	20 mW/ch	1.2 Gb/s	TSMC 130n	1.2 V	I <sup>2</sup> C
	FCC	LAR	Lar	50-200 pF	200 ns	<1 mW	Gb/s	TSMC 130n	1.2 V	I <sup>2</sup> C
→	SKIROC3	CALICE	Si	50 pF	200 ns	<1 mW	Mb/S	TSMC 130n	1.2 V	?

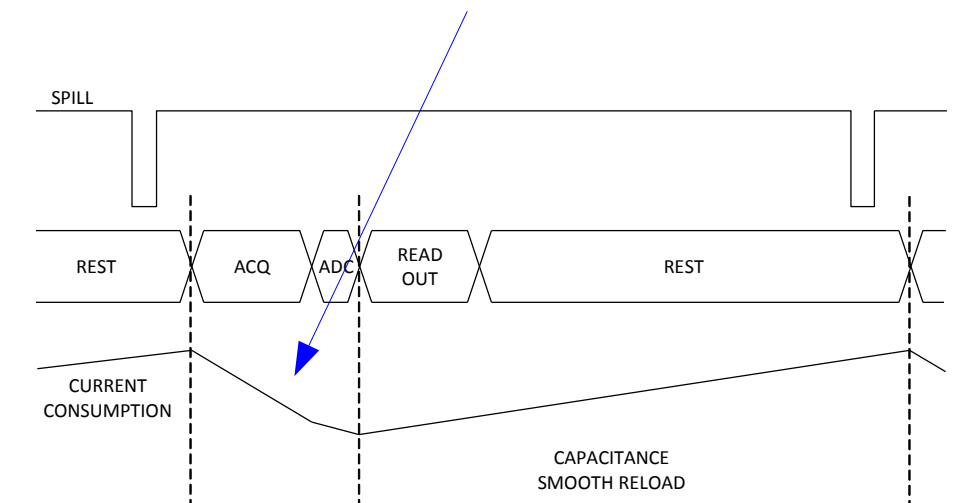
CdLT CALICE meeting 20 apr 2022



Status after regular discussions between engineers of LLR, IJCLab, LPNHE and OMEGA



With 600  $\mu\text{F}$ , we ensure 100mA during 3ms with a voltage drop of 0.5V ( $\Delta V = I.t/C$ ).

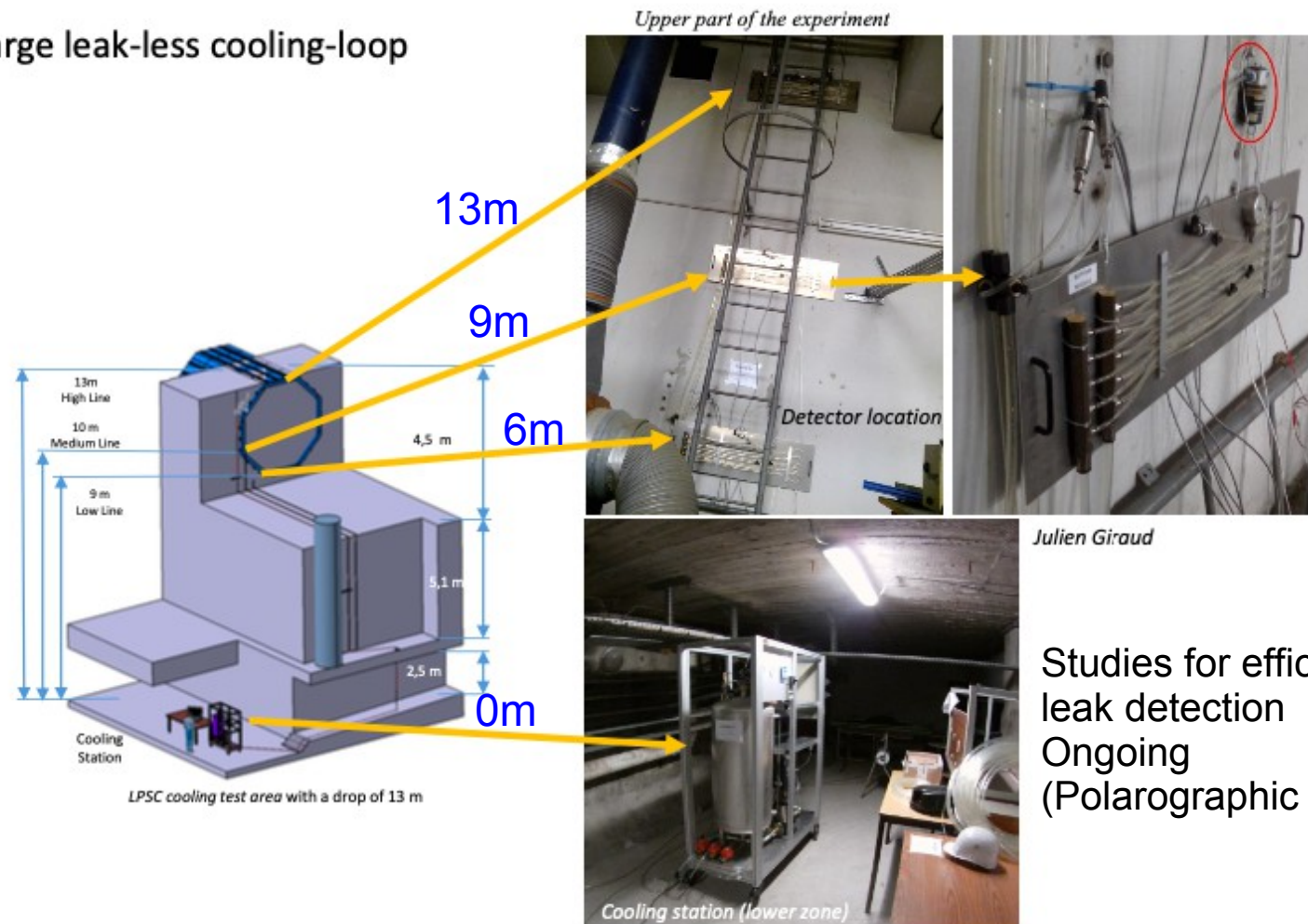


- **New board for next step of technical realisation of power pulsed Ecal layers**
  - Capacitances and LDO close to ASICs
- **Last month progress in design**
  - Stacking of PCB
  - Choice of components
- **Another important feature is that HV will be transported via connectors (i.e. On top of board)**
  - Wafer supply from bottom of board via plies (copper/kapton)
  - These plies are a delicate piece
  - Risk of shortcuts and wafer damage (the design of the kapton that goes below the board requires another design round)
- **Expect production either shortly before or shortly after the summer break (not in a hurry, carefulness comes before speed)**
- **The setup will be completed by a “Termination card” that will allow for flexible chaining of cards (i.e. No soldering of terminations)**
- **and for flexible adding of decoupling capacitances (to study noise behaviour of COBs)**

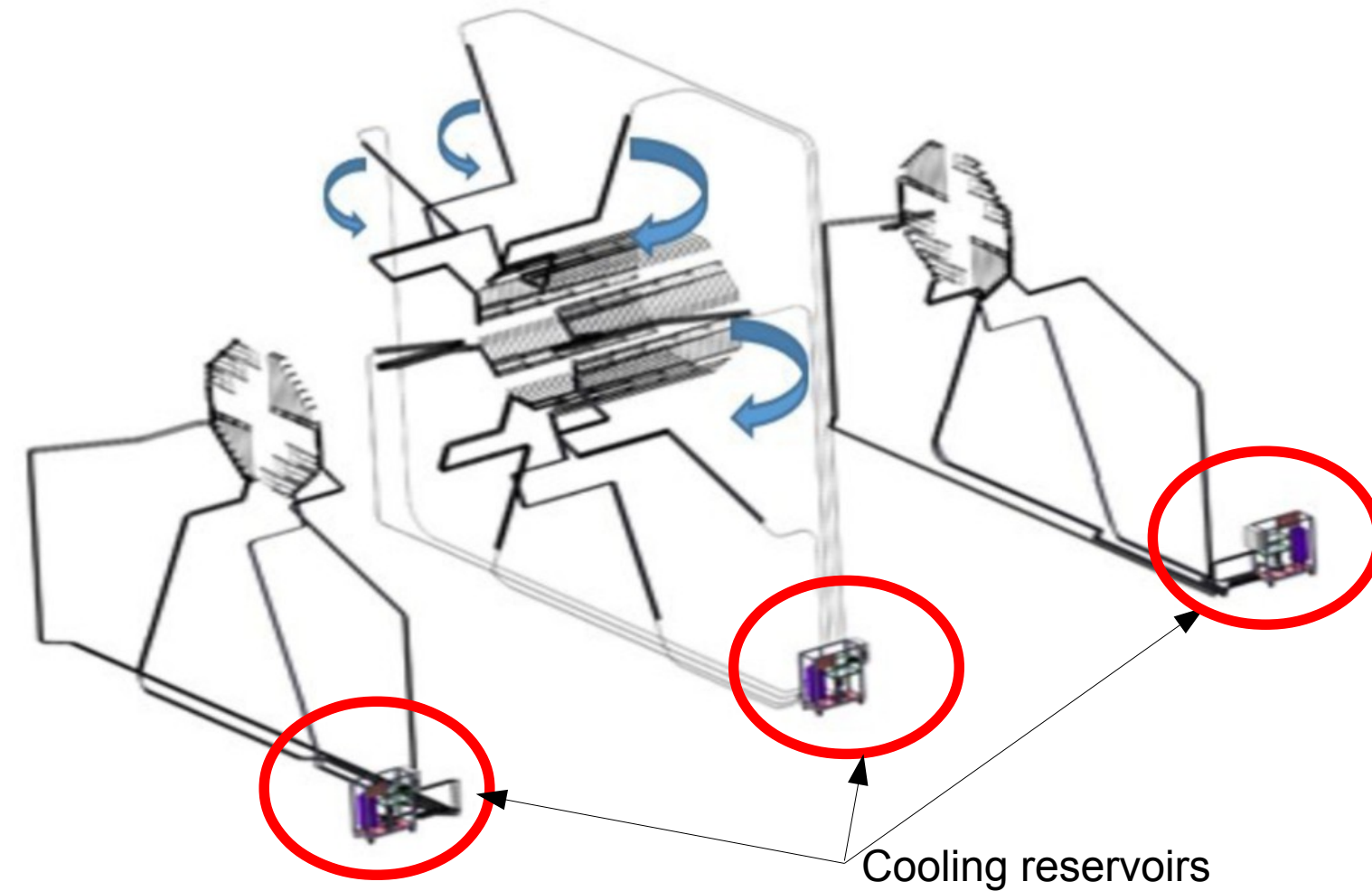
## Demonstrator of large leakless loop for CALICE/ILD ECAL

- Thermal model as milestone
- Probes at different heights to establish full model of Cooling system for large detectors

a large leak-less cooling-loop



Studies for efficient leak detection  
 Ongoing  
 (Polarographic probe)





## Power pulsed systems

Numbers from Vincent

### ILC “Standard”

$$\begin{aligned}
 T_{\text{Bunch}} &\sim 1\text{ms} \\
 f_{\text{rep}} &\sim 5\text{Hz} \\
 \Rightarrow \Delta T_{\text{Bunch}} &= 200\text{ms}
 \end{aligned}$$

### HL-ILC:

$$\begin{aligned}
 &- \mathcal{L} \times 4 (6) \\
 &- N_{\text{bunches}} \times 2 : \tau_{\text{Train}} : 1 \rightarrow 2 \text{ ms} \\
 &- f_{\text{rep}} \times 2 (3) : 5 \rightarrow 15 \text{ Hz} \\
 \Rightarrow \Delta T_{\text{Bunch,min}} &= 66\text{ms}
 \end{aligned}$$

### HL-CLIC:

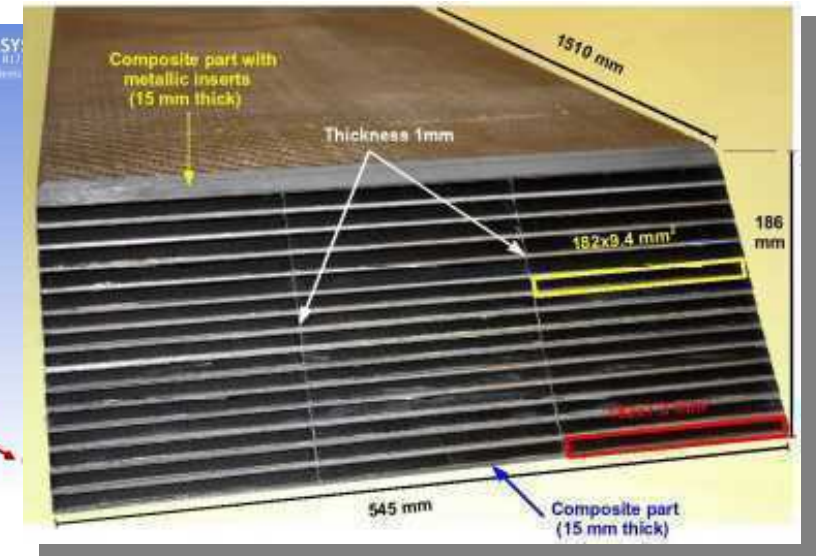
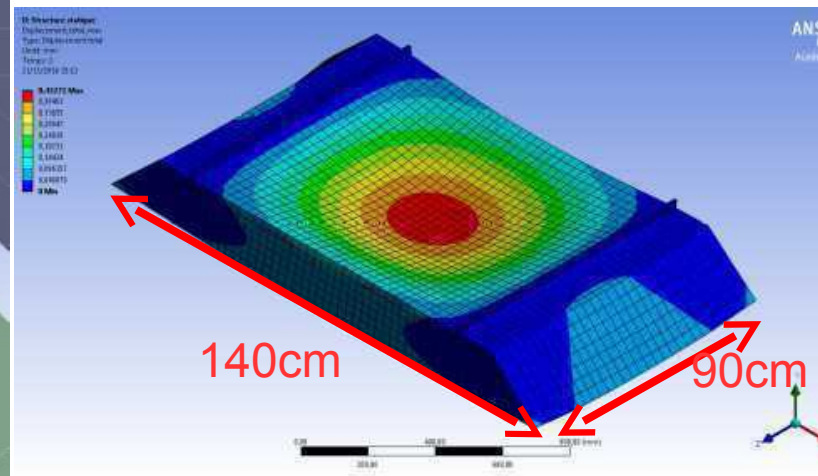
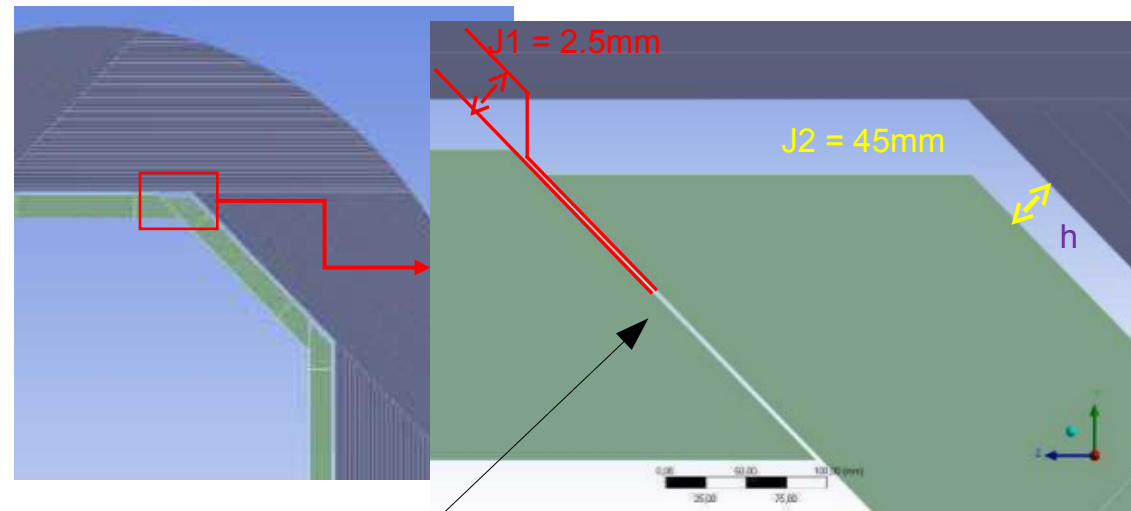
$$\begin{aligned}
 &- \mathcal{L} \times 2 \\
 &- N_{\text{bunches}} \rightarrow : \tau_{\text{Train}} : 176 \text{ ns} \\
 &- f_{\text{rep}} \times 2 : 50 \rightarrow 100 \text{ Hz} \\
 \Rightarrow \Delta T_{\text{Bunch,min}} &\sim 10\text{ms}
 \end{aligned}$$

All faults are mine

- In the (local) powering scheme the power is reloaded between the bunch trains with a small constant charging current
- As long as one manages to charge the capacitances between the bunch trains, the overall power consumption will not increase with increasing luminosity
  - The step from ILC Standard to HL-ILC doesn't look too big, CLIC may require a further look
  - Of course, the front-end electronics will still dissipate heat, passive cooling should still work

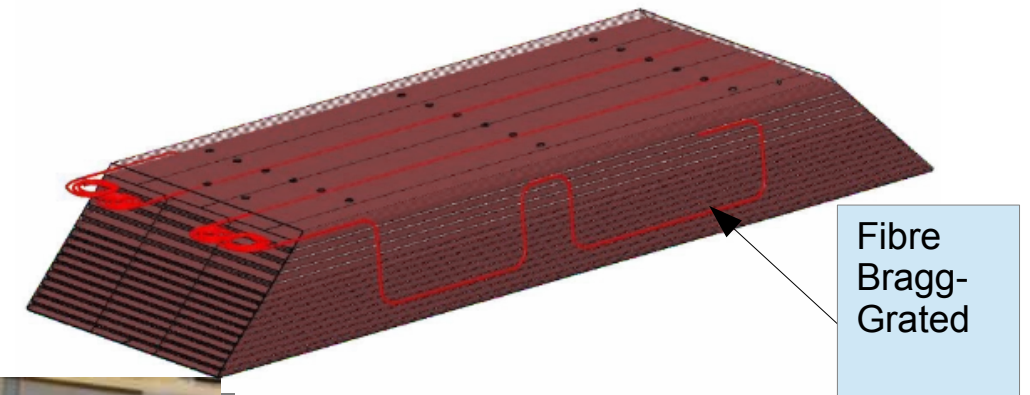
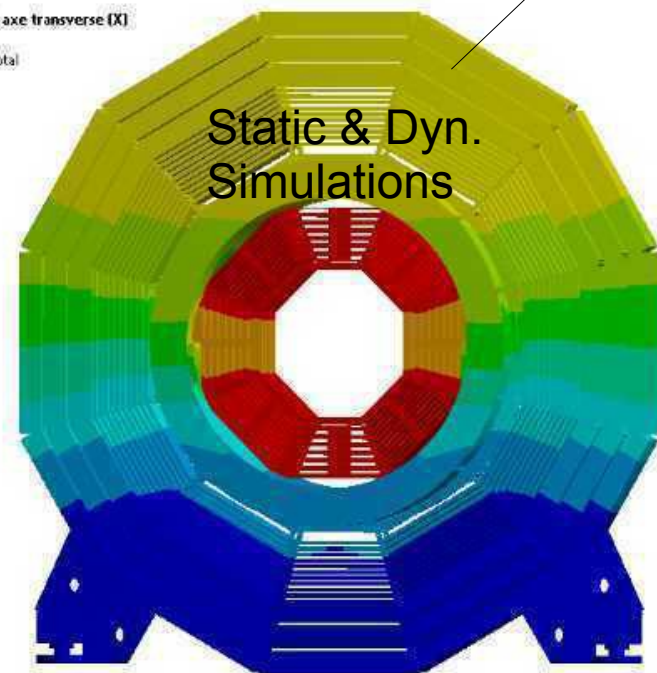
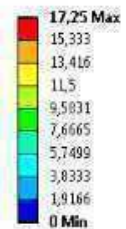
## Continuously powered systems:

- Typical consumption of FEE (as of today) 5-10mW/channel
  - CMS HGCR0C has 20mW/channel due to sophisticated digital part
- This translates directly into power consumption of detector
- 5mW: For  $10^8$  channels this leads to 500 kW power consumption of full detector
  - This is the pure consumption of the front-end electronics (e.g. no ohmic losses in power transfer etc.  $U=RI$  and  $I$  would be high)
  - $\Rightarrow$  Active cooling



J1 = clearance between modules for the ECAL  
 J2 = Clearance at ECAL edges between ECAL and HCAL  
 h = height of the rails 30mm

J: Réponse spectrale axe transverse (X)  
 Déplacement total  
 Type: Déplacement total  
 Unité: mm  
 Temps: 0  
 04/09/2017 10:31



measurements still to be done...





## Shower reconstruction



It is known that the more dimensions, the easiest to reconstruct patterns

### Using the time-space

To figure out the pattern of a shower developed by a charged track or a neutral

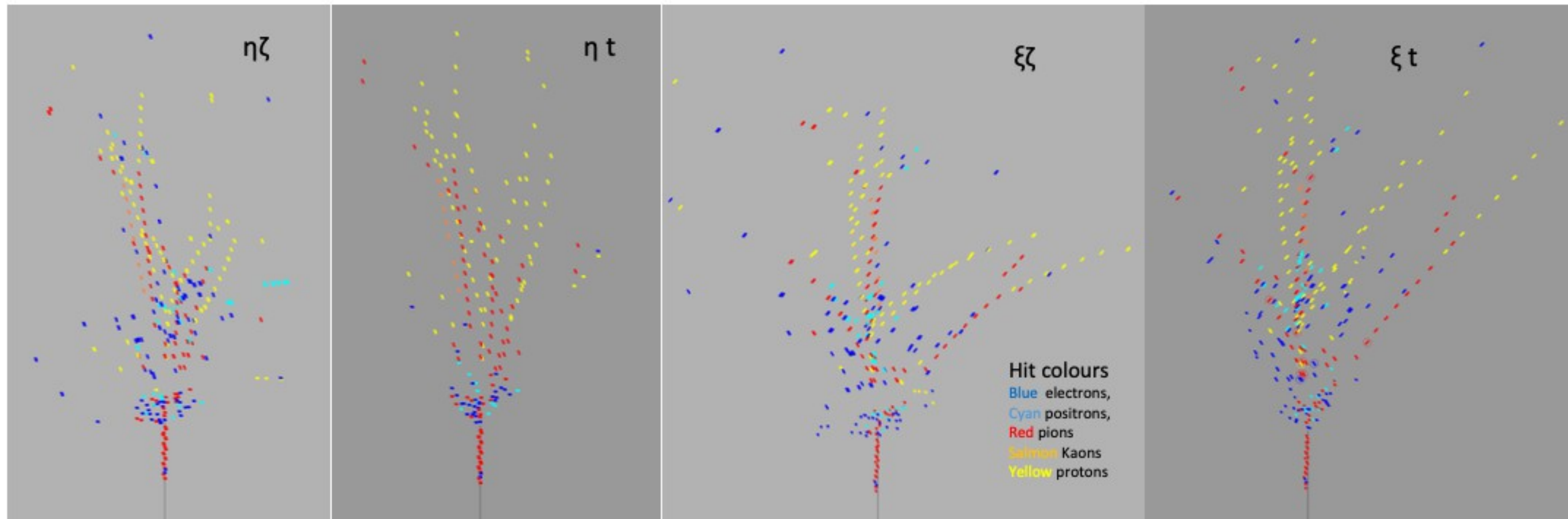
We assume that the main direction of the shower, called  $\zeta$ , is

- along the flight line from interaction to the earliest hit in the Ecal (or globally) for a neutral
- along the track direction at the position of the earliest hit for a charged track

Two perpendicular coordinates,  $\xi$  and  $\eta$ , are chosen to optimise the match with the detector axes, mostly for visualisation.

Then  $t$  which is much correlated to  $\zeta$ .

You see immediately the role of the  $\beta$  and how the protons slow down when the pions do not



15/05/2021

Henri Videau | LCWS March 2021

12

*H.Videau et al., LCWS2021*

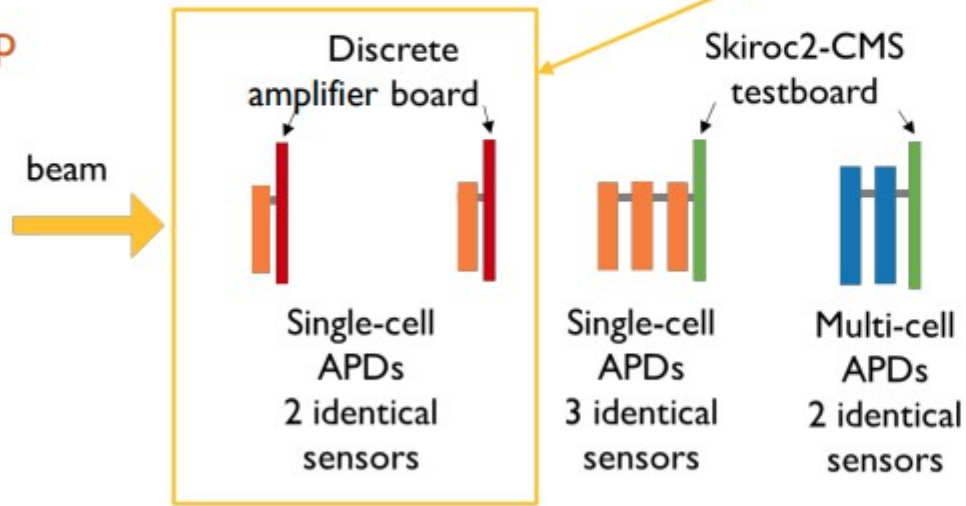
*arxiv:2108.10963*



6-8 Oct. 2021 at ELPH, Tohoku University

- 3 days × 12 hours positron beam: ~770 MeV

Setup



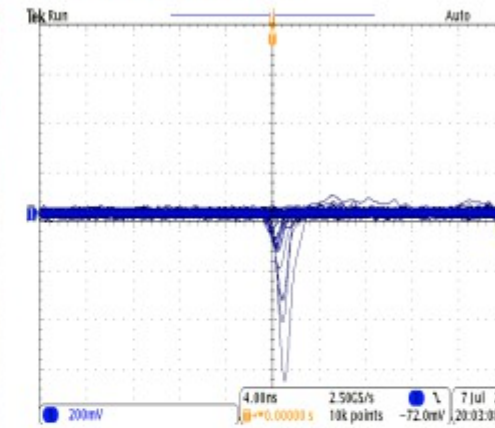
APD

amplifier board



2 stages

Waveform output from the amp. board



Rising time  
~1 nsec

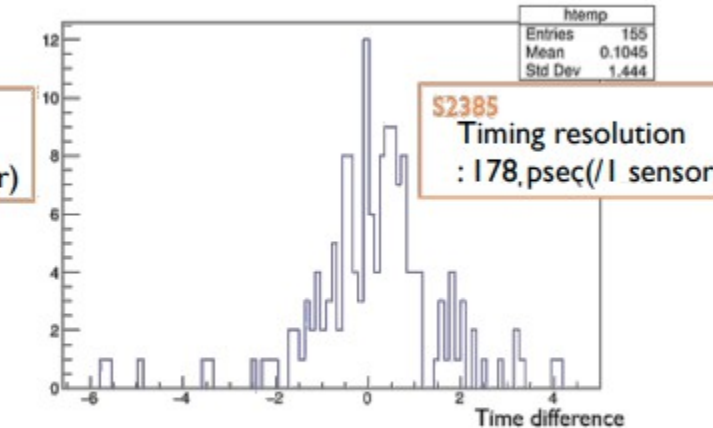
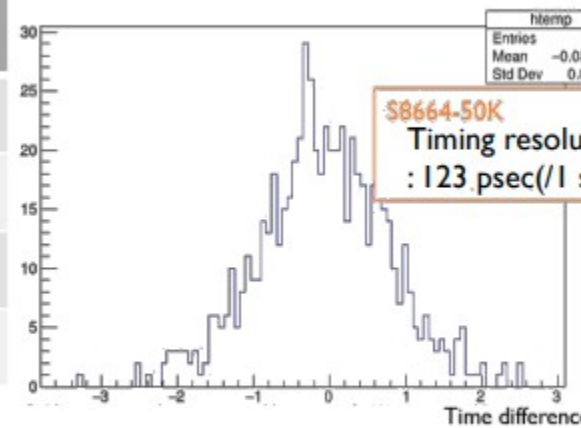
Amplifier chip



- GALI-S66+ (Mini-circuit)
- Gain: 20 dB
- Wide bandwidth 3GHz

Time difference between the two APDs (charge > 18 fC)

APD sensor	Cut of charge	Timing resolution
S8664-50K (Inverse type)	> 18 fC	123 ps
	> 36 fC	63 ps
S2385 (reach through type)	> 18 fC	178 ps
	> 36 fC	89 ps

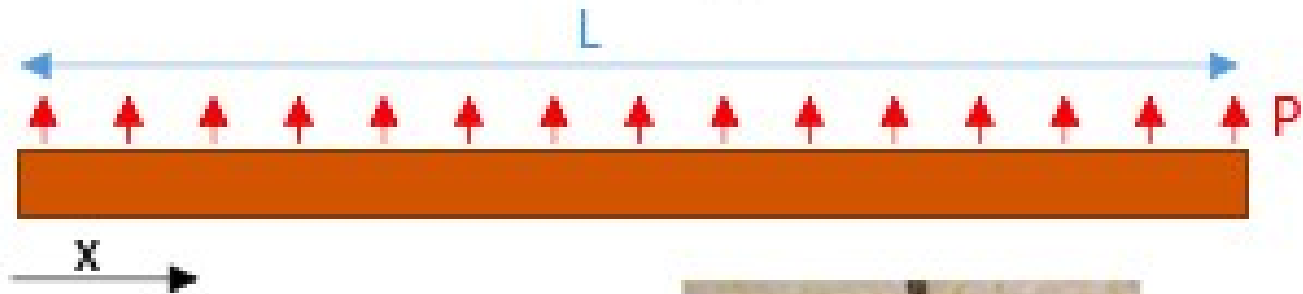


- Timing resolution of S8664-50K is better

→ Difference in capacitance related to signal rising time (S8664-50K: 55 pF S2385: 95 pF)

*LM*

## Passive cooling

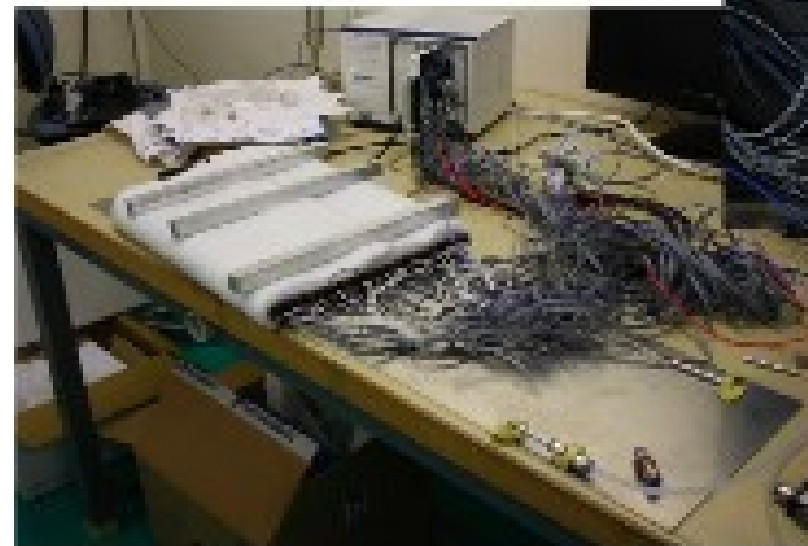
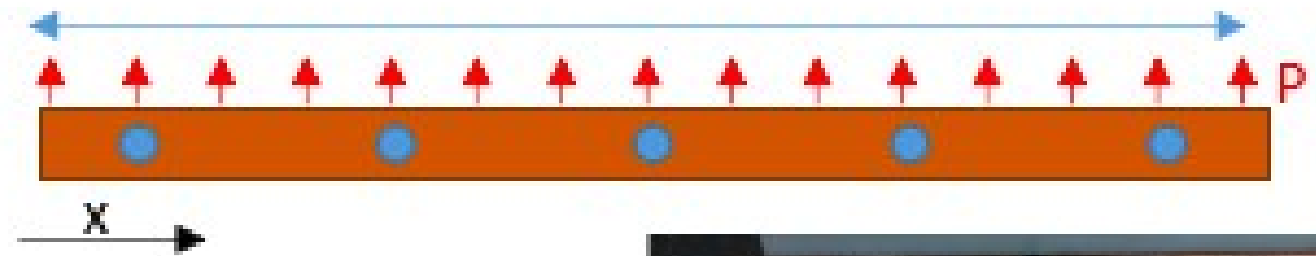


Passive cooling ramp example

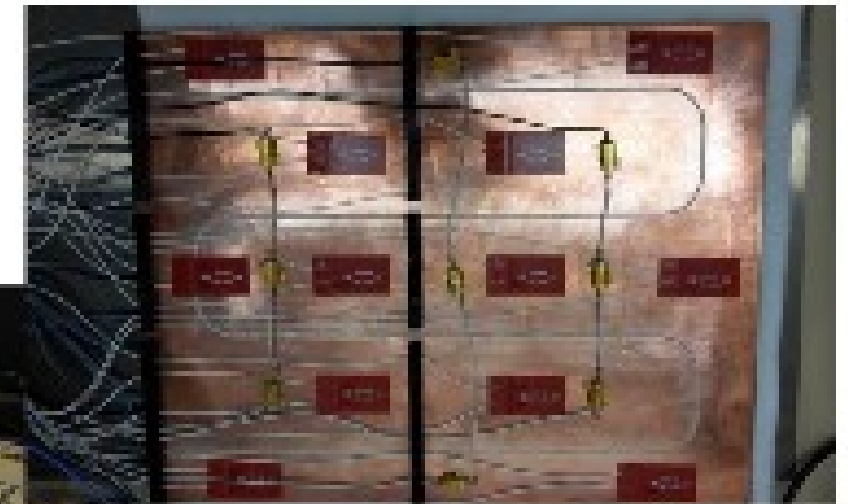


Passive cooling ramp set up test

## Active cooling



Active cooling set up test with water at room temperature



Active cooling test layout (400mm x 300mm x 3mm thick copper plate with 1800 pipes embedded)