

Performance at testbeam and simulation of the CALICE SiW ECAL prototype

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on behalf the SiW-ECAL team

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MATTER AND TECHNOLOGY

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CALICE

 **IJCLab**
Irène Joliot-Curie
Laboratoire de Physique
des 2 Infinis

 **LMR**
LPSC
Grenoble

 **LPNHE**
PARIS

 **OMEGA**
Microelectronics

 **CNRS**
IN2P3
Les deux infinis

 九州大学
KYUSHU UNIVERSITY

 東京大学
THE UNIVERSITY OF TOKYO

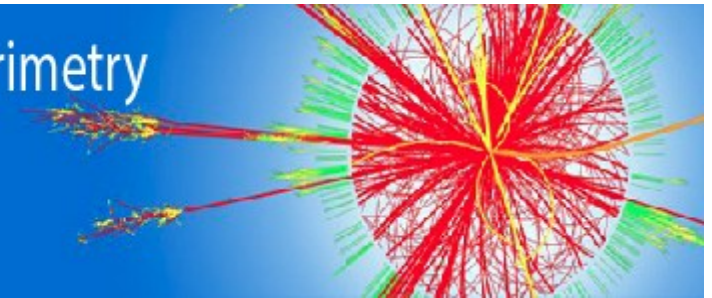


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Ciemat
Centro de Investigaciones
Energéticas, Medioambientales
y Tecnológicas

- ▶ The SiW-ECAL
 - Few slides taken from [R. Poeschl's talk](#)
- ▶ Testbeam setup at DESY2021-2022
- ▶ Detector commissioning and single cell performance
 - Pedestal & noise
 - MIP
- ▶ Low energetic electron showers
- ▶ Next step: high energy showers at CERN (with AHCAL)

CALOR 2020 – 19th International Conference on Calorimetry
in Particle Physics
University of Sussex, UK, 16-20 May, 2022



Thanks to R. Poeschl, Y. Okugawa, J. Kunath, V. Boudry, T. Suehara, F. Jimenez, H. García
for material for this talk

Thanks to the engineering teams of IJCLab, LPNHE and LLR

FEV zoo (see R. Poeschl's talk)

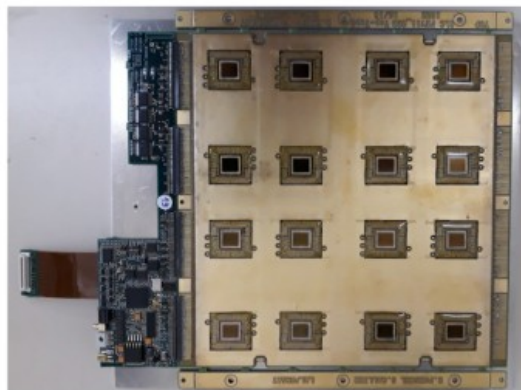
- In recent years the SiW ECAL has developed and used several PCB variants
- To make sure that you don't get lost, here comes an introduction

FEV10-12



- ASICs in BGA Package
- Incremental modifications
From v10 -> v12
- Main “Working horses” since 2014

FEV_COB



- ASICs wirebonded in cavities
 - COB = Chip-On-Board
- Current version FEV11_COB
- Thinner than FEV with BGA
- External connectivity compatible with BGA based FEV10-12

FEV13



- Also based on BGA packaging
- Different routing than FEV10-12
- Different external connectivity

Current prototype (see later) is equipped with all of these PCBs

Very Front End ASICs (see R. Poeschl's talk)

SKIROC (Silicon Kalorimeter Integrated Read Out Chip)

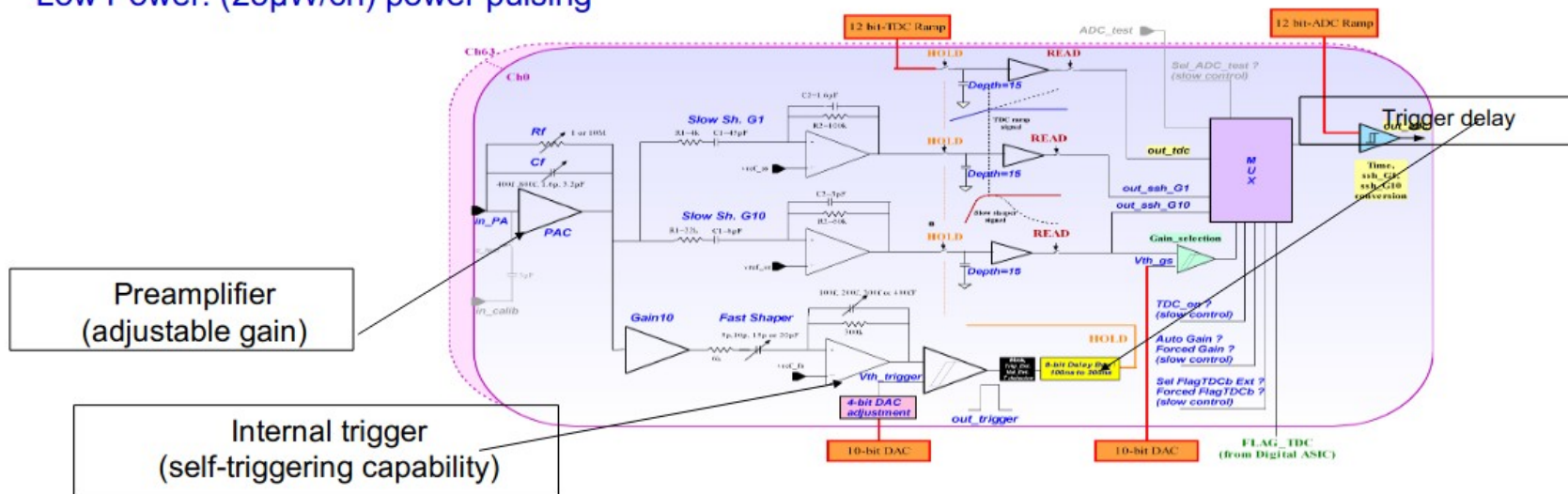
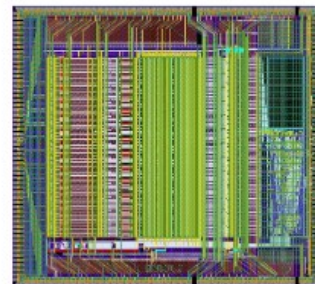
SiGe 0.35 μ m AMS, Size 7.5 mm x 8.7 mm, 64 channels

High integration level (variable gain charge amp, 12-bit Wilkinson ADC, digital logic)

Large dynamic range (~2500 MIPS), low noise (~1/10 of a MIP)

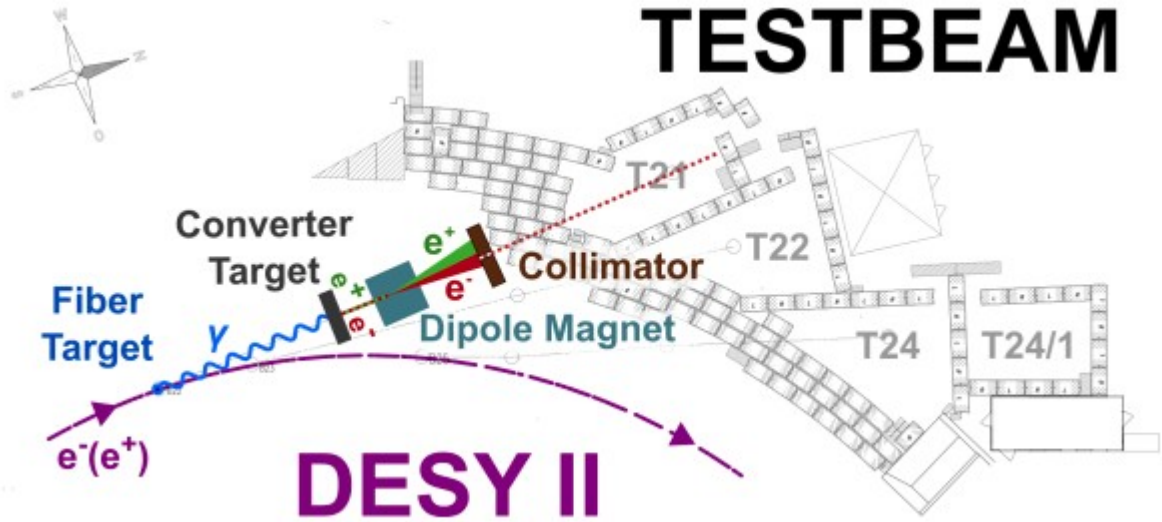
Auto-trigger at $\frac{1}{2}$ MIP, on chip zero suppression

Low Power: (25 μ W/ch) power pulsing



(see R. Poeschl's talk)

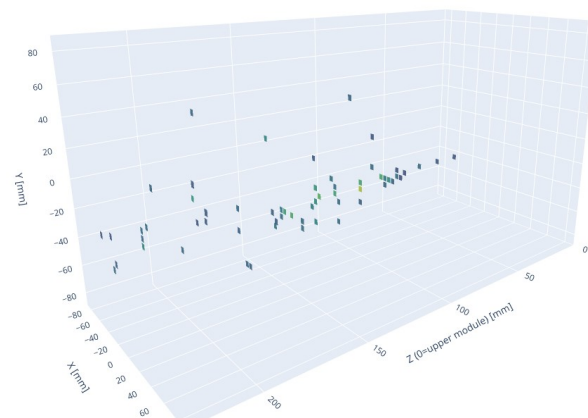
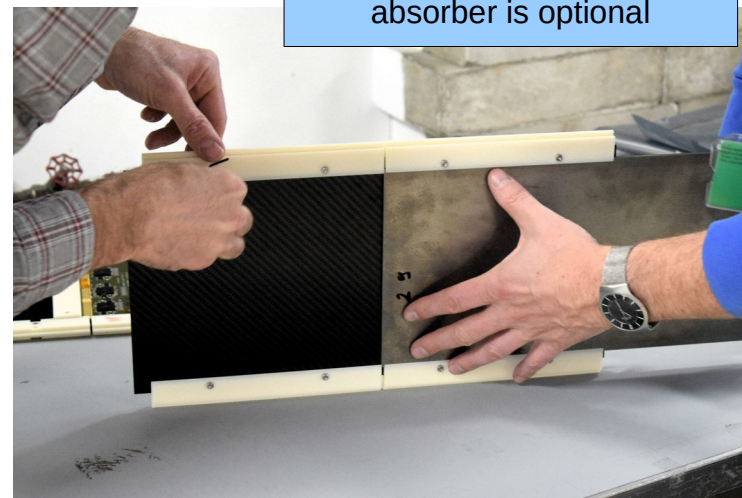
- ▶ Sensors
- ▶ DAQ
- ▶ Mechanics
- ▶ ... all in R. Poeschl talk this morning



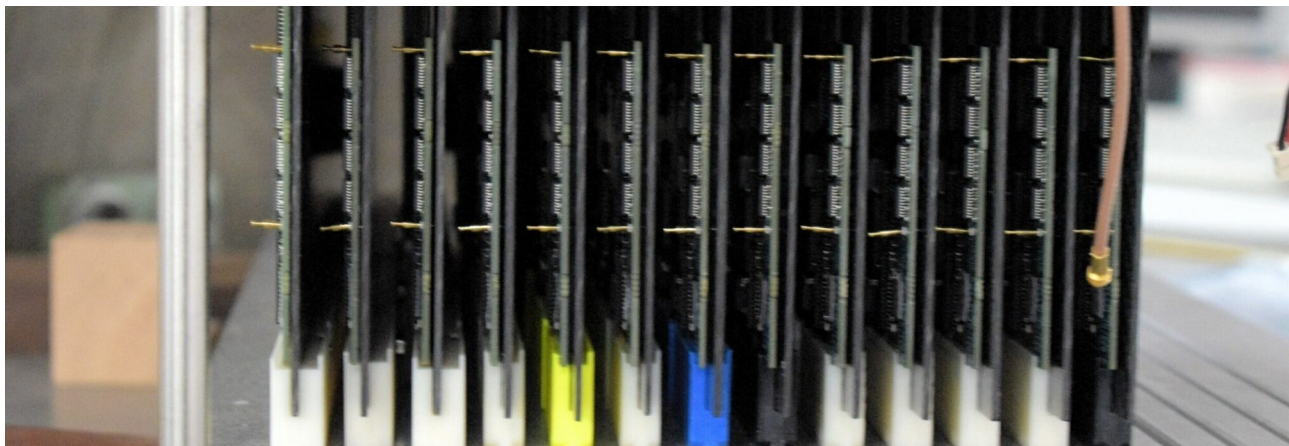
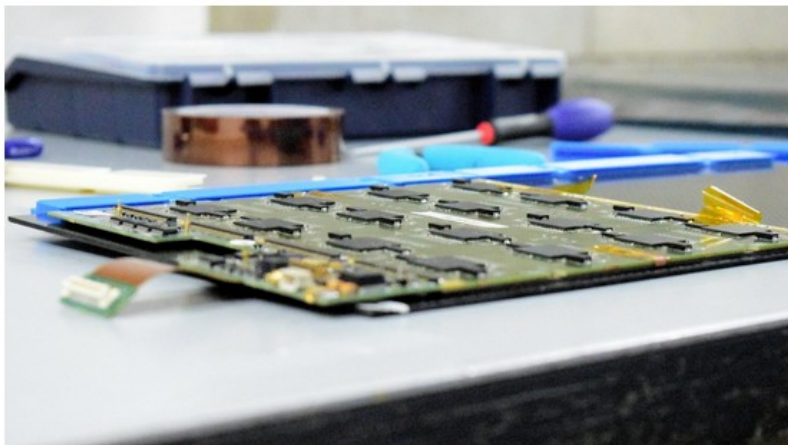
The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF)

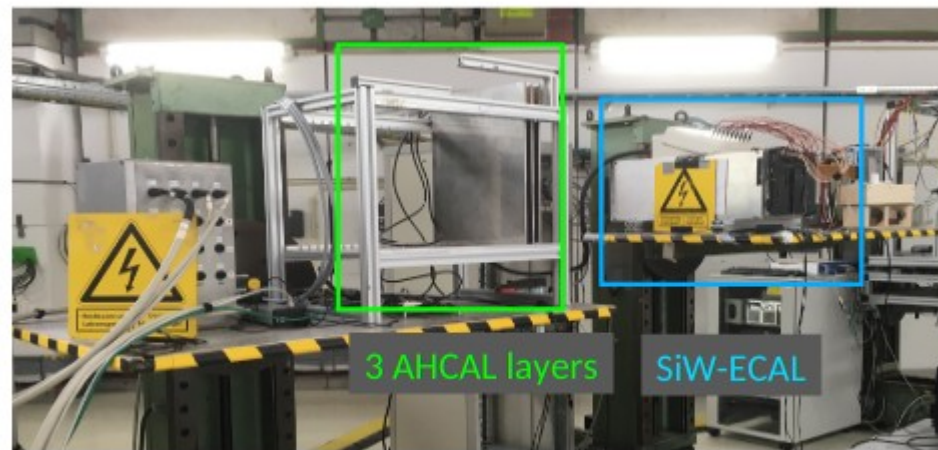
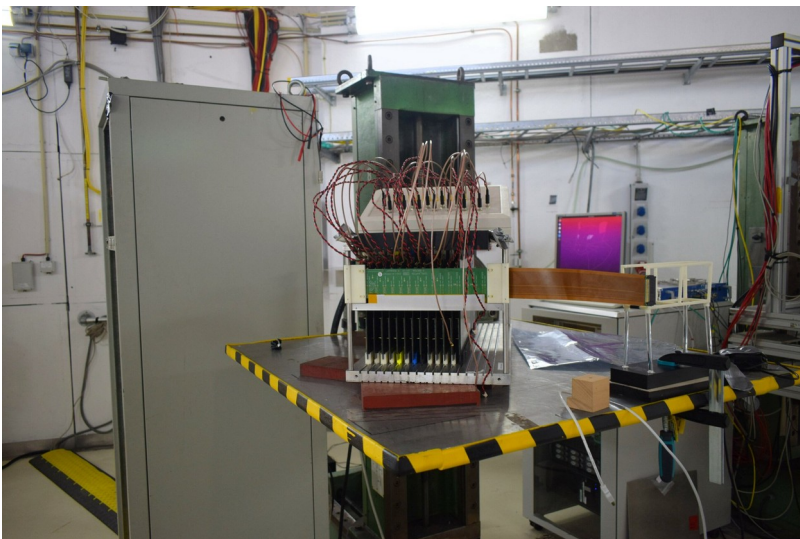
Test Beams DESY 2021-2022

- ▶ **DESY offers low-energetic beams of 1-6GeV (e-, e+)**
- ▶ **15 layers with 1024 readout cells each**
 - **5.5mm si pads**
 - LHC calorimeter scale
 - But it fits in a suitcase
- ▶ **4 weeks in total**
- ▶ **~3 weeks of commissioning and “training”**
 - Mechanical structure (adding or removing the tungsten plates)
 - New and continuously improving DAQ and online monitoring tools
 - New semi-online monitoring tools
 - Hold values, gain optimization, Threshold optimization, single cell calibration, etc



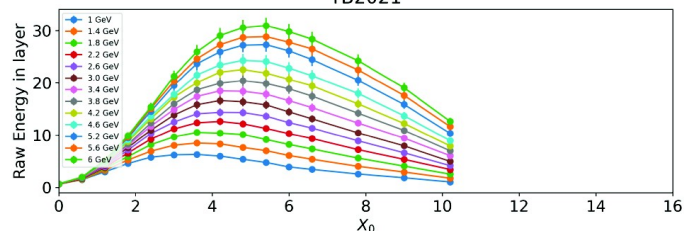
Test Beams DESY 2021-2022





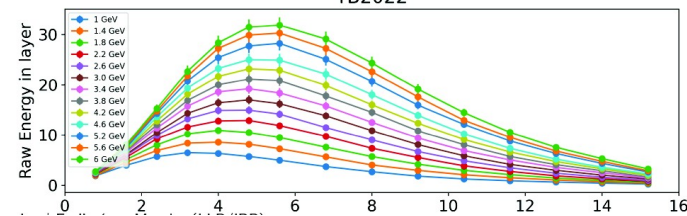
SiW-ECAL + AHCAL DAQ test @ DESY in March 2022

TB2021



Preliminary simulation

TB2022



Preliminary simulation

Coherent noise source identification in multi channel analysis

<https://arxiv.org/pdf/1401.7095.pdf>

T. Frisson*¹ and R. Poeschl¹

¹Laboratoire de L'accélérateur Linéaire (LAL), CNRS/IN2P3,
Orsay, France

May 4, 2021

- ▶ “The goal is to identify and characterize dissociable noise sources in a multi channel systems. This method cannot separated noise sources which affect exactly the same set of channels. In this case, the noises sources are processed as a single source. We consider a system with N channels. “
- ▶ “Each channel \mathbf{k} is affected by an incoherent noise source \mathbf{I}_k and N_c coherent noise sources ($\mathbf{C1}_k, \mathbf{C2}_k, \dots, \mathbf{CN}_k$). We assume that all noise source distributions are Gaussian and independant.”

Detector commissioning: pedestal and noise

Equation 1.10.

$$\sigma_i^2 = \sigma_{I_i}^2 + \sum_{j=1}^{N_c} \sigma_{C_i^j}^2 \quad (1)$$

The covariance matrix element from the two channels i and k is expressed by:

$$\text{cov}(i, k) = \delta_{ik} \sigma_{I_i} \sigma_{I_k} + \sum_{j=1}^{N_c} \sigma_{C_i^j} \sigma_{C_k^j} \quad (2)$$

where:

$$\delta_{ik} = \begin{cases} 1 & \text{if } i = k \\ 0 & \text{if } i \neq k \end{cases} \quad (3)$$

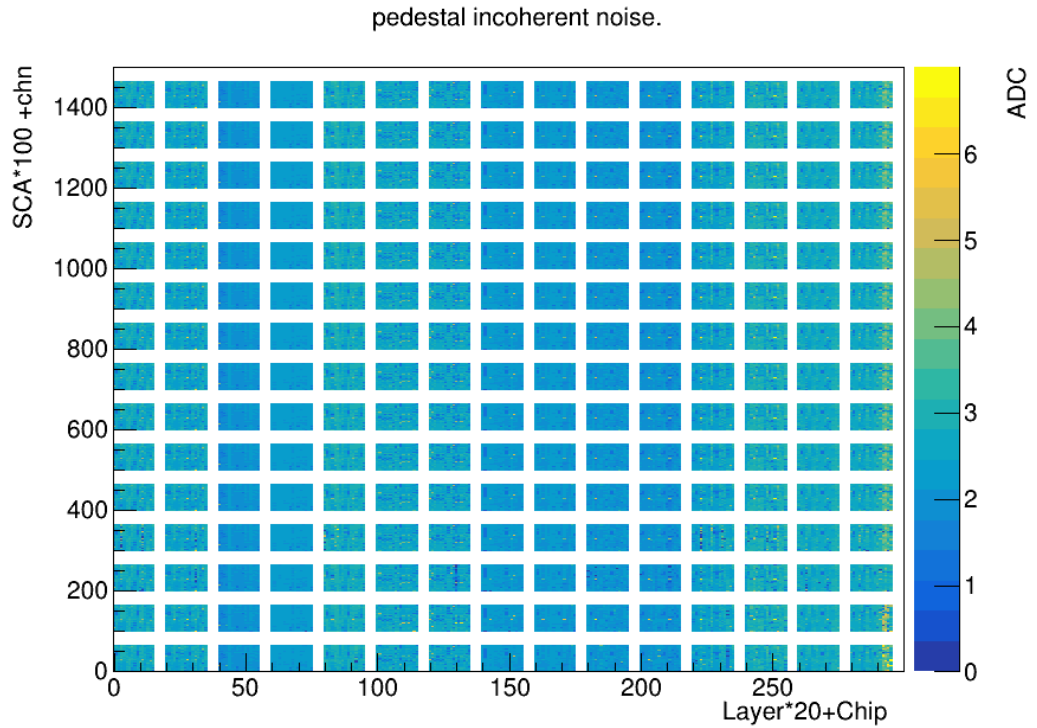
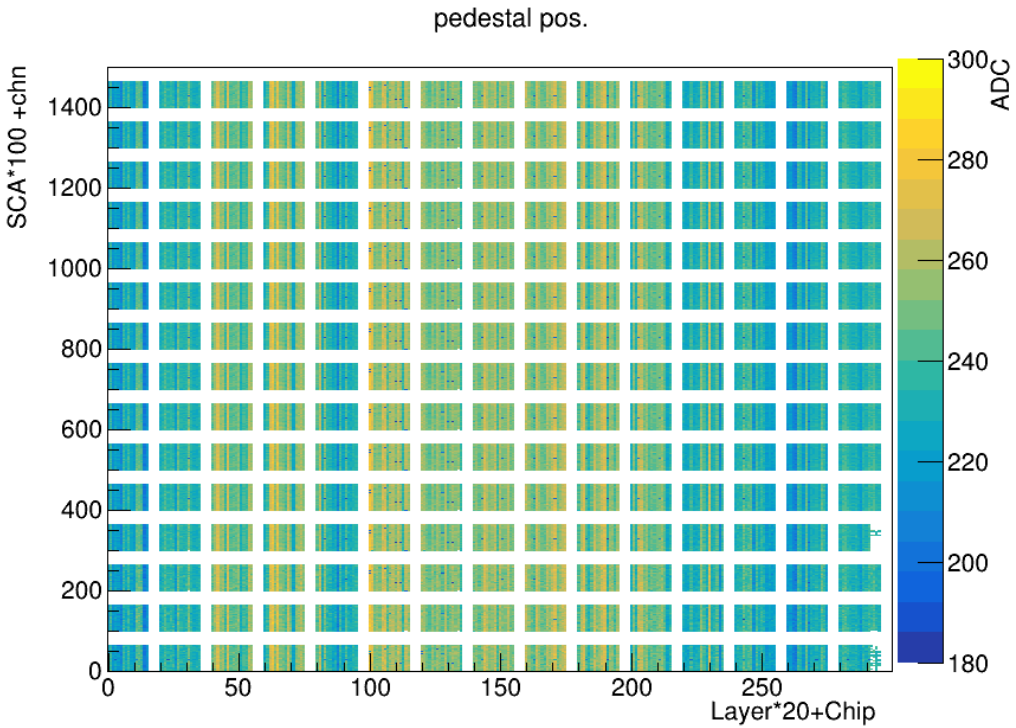
The covariance matrix element can also be determined from the data:

$$\text{cov}_{Data}(i, k) = \frac{\sum_{n=1}^{N_{event}} (A_i(n) - \mu_{A_i})(A_k(n) - \mu_{A_k})}{N_{event}} \quad (4)$$

Measured amplitude if no hit

Pedestal position → calculated as simple histogram Mean

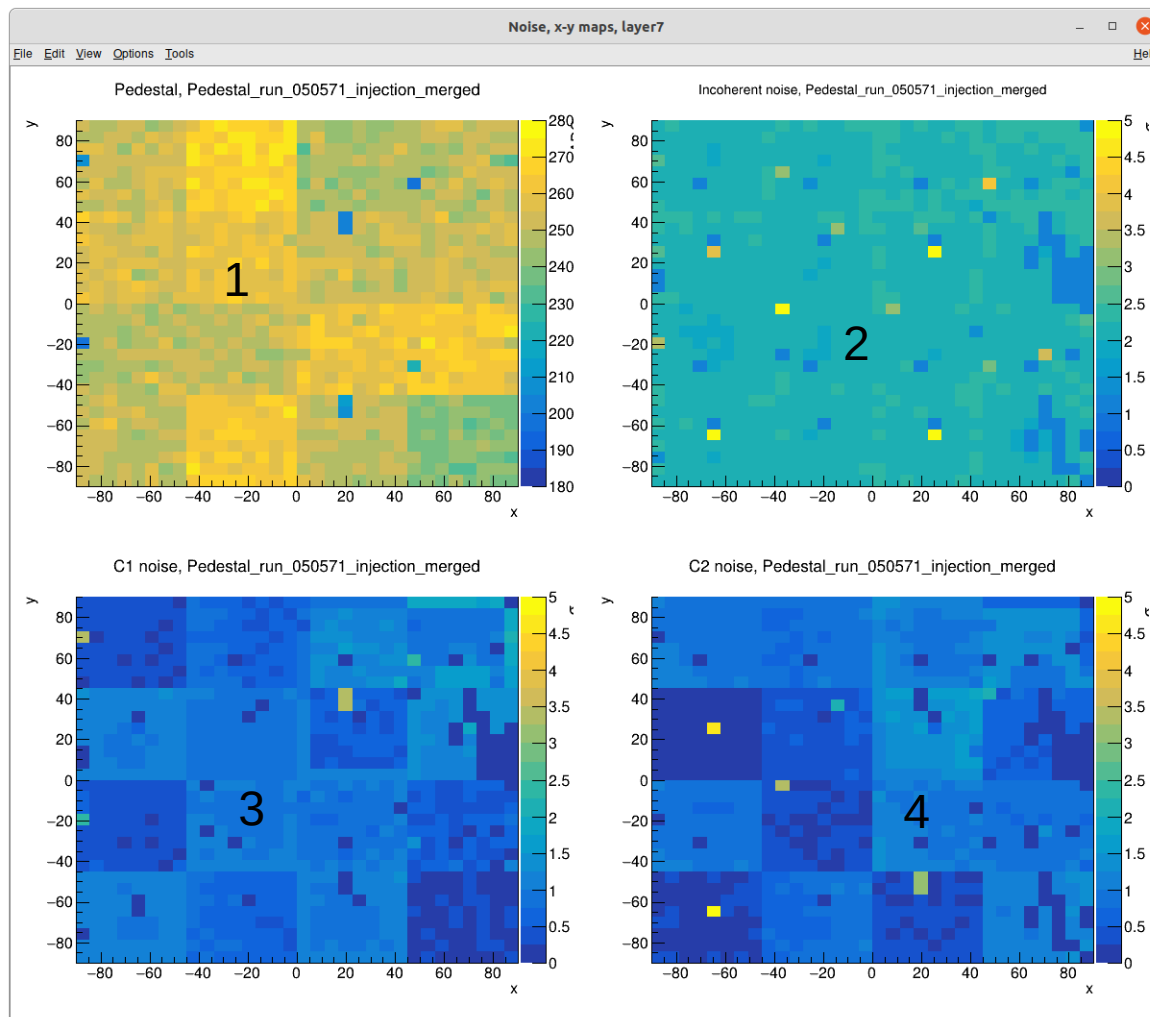
Pedestal position and incoherent noise



Layer 7, slab30 FEV12 sk2a, 500um

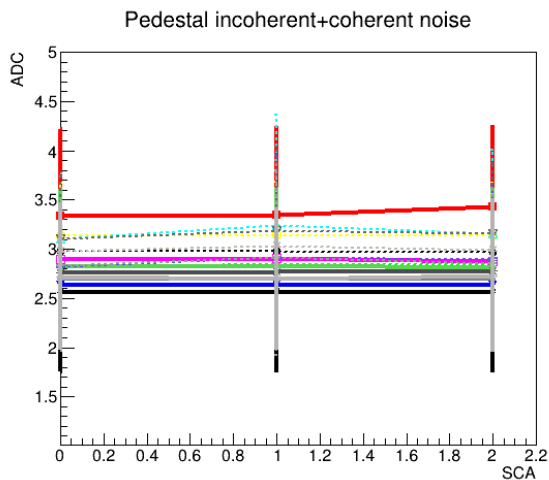
- ▶ 1) Pedestal map
- ▶ 2) Incoherent noise map
- ▶ 3) coherent noise map (c1)
- ▶ 4) coherent noise map (c2)

Few channels are off
These are usually seen as noise
sources (FEV10/11/22)
Routing issues (addressed in
next generation)
Only BGA

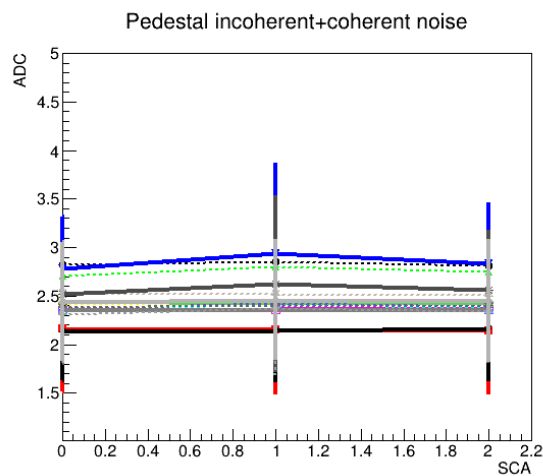


Noise: Chip on board vs BGA

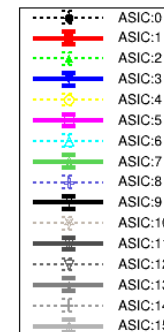
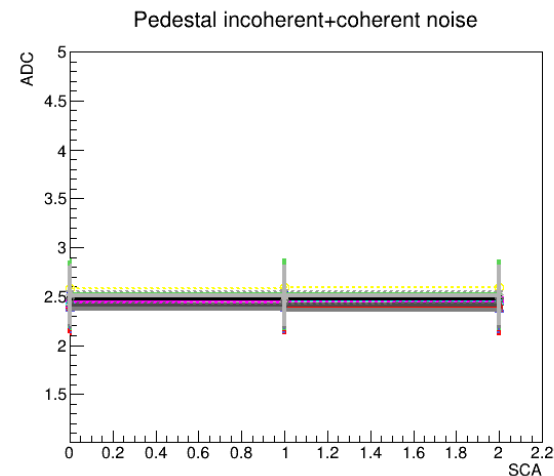
COB



FEV12



FEV13



► Average of sigma for all channels in the same chip

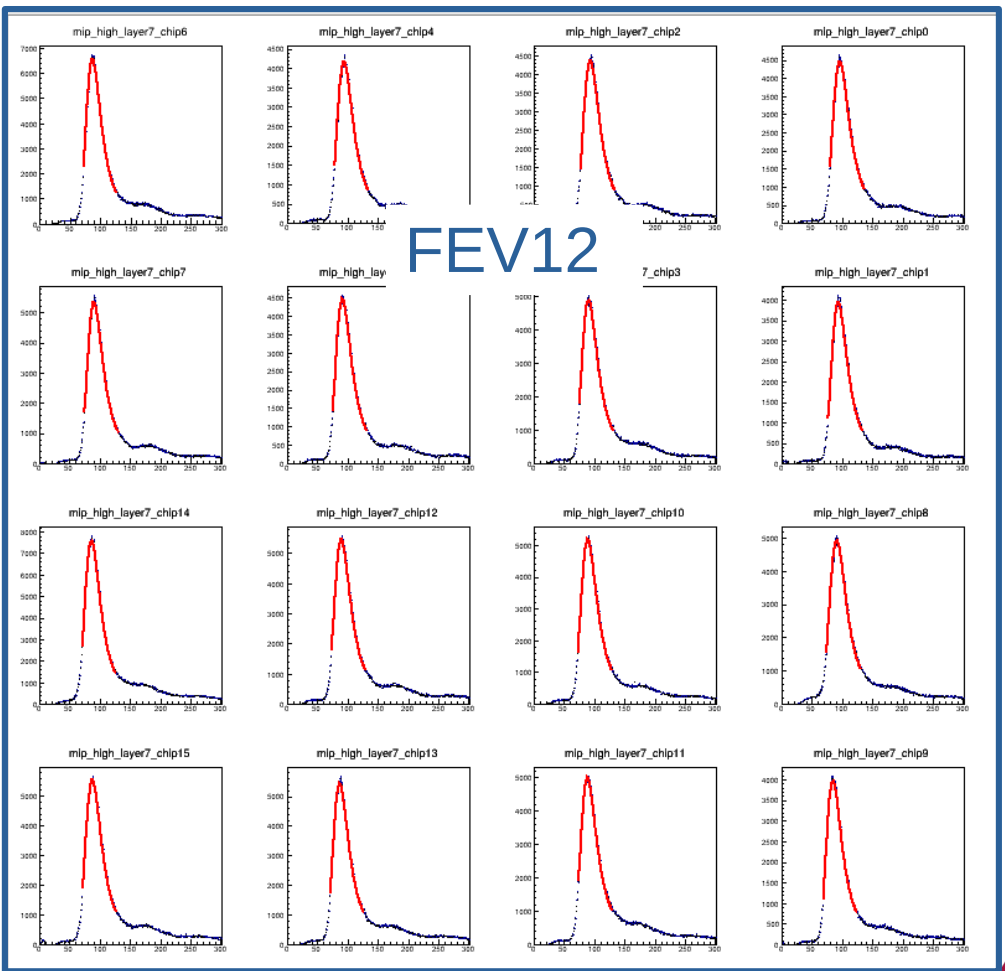
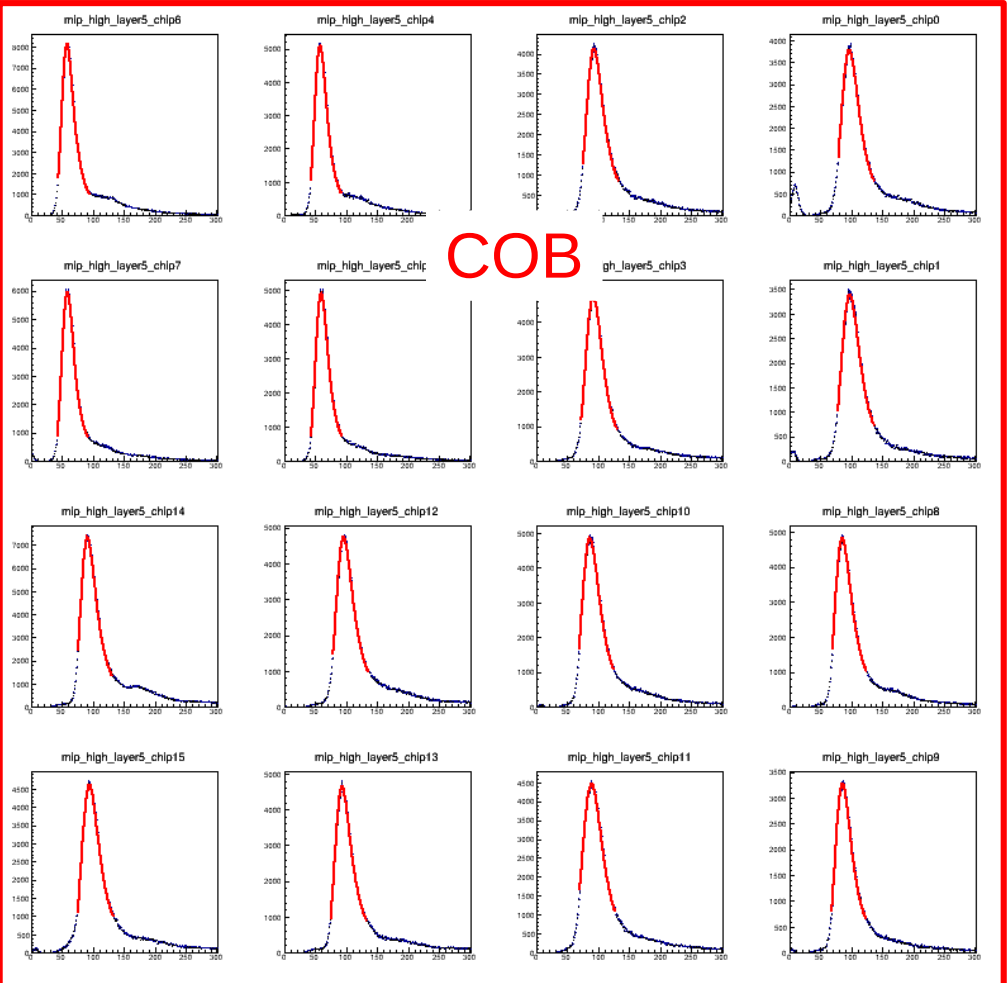
- The error bar is the std of these values

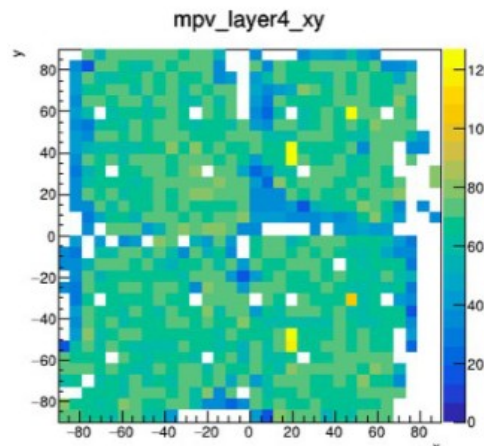
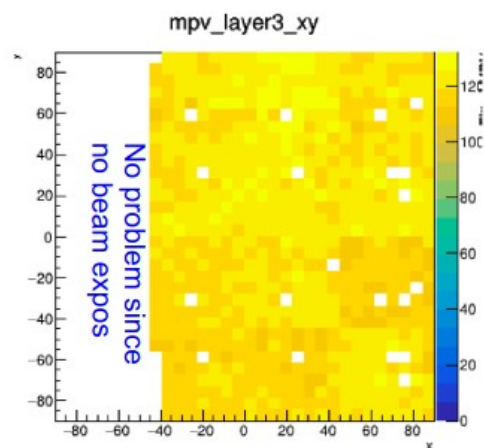
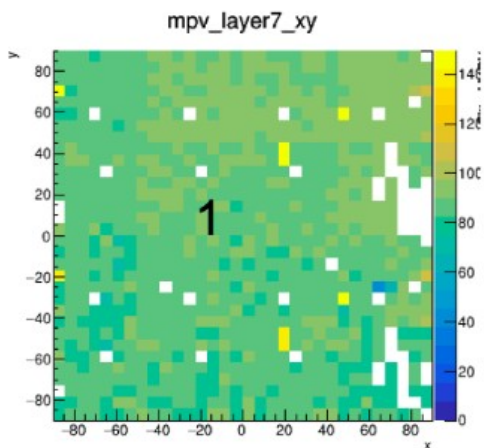
► Newer PCBs, with optimized power distribution shows better behavior

► COB has a competitive performance

- Despite being almost not equipped with passive components as decoupling capacitors

MIP calibration: COB vs BGA





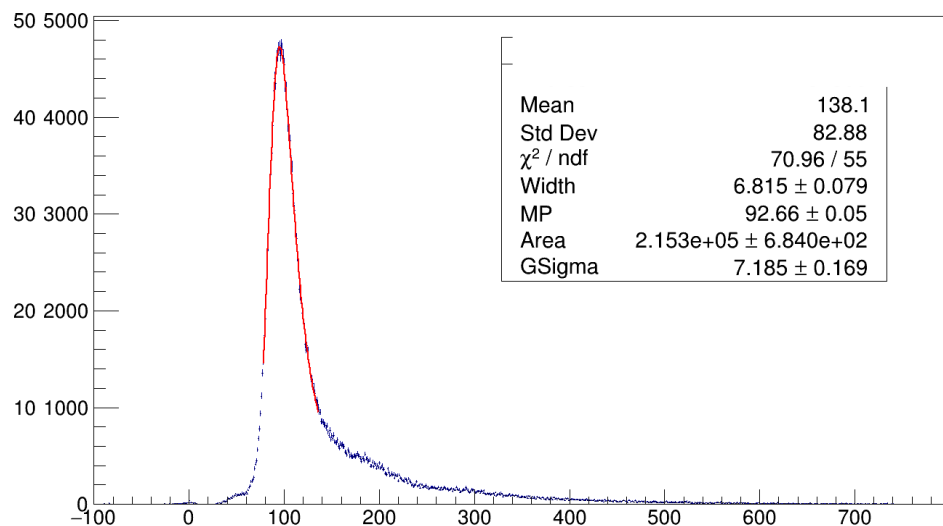
- We have good layers ...
 - Homogeneous response to MIPs over layer surface
 - Here white cells are masked cells due to PCB routing
 - Understood and will be corrected

... and not so good layers

- Inhomogeneous response to MIPs
 - Partially even no response at all, in particular at the wafer boundaries
 - To be understood, may require dedicated aging studies
- Have since last week access to the different stages of the ASICs
 - => major debugging tool
- In any case less good layers will be replaced in coming months

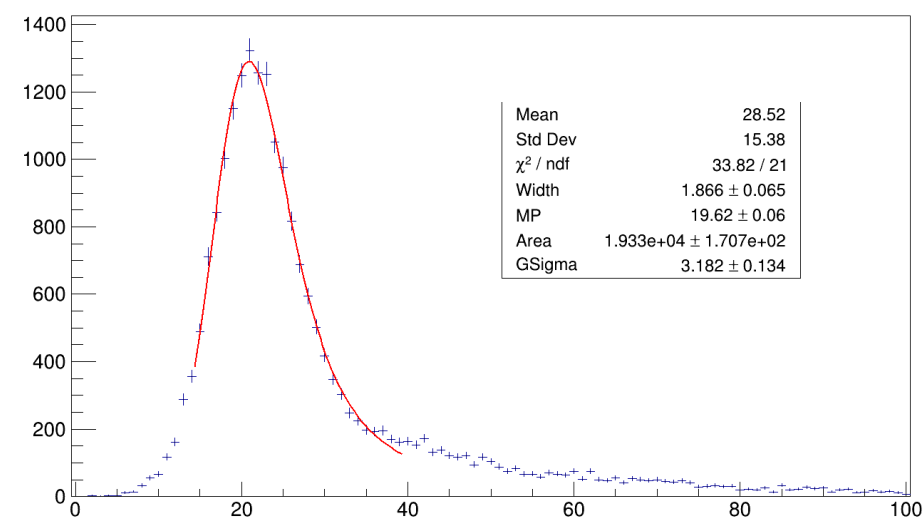
DESY gain

mip_high_layer5_chip12

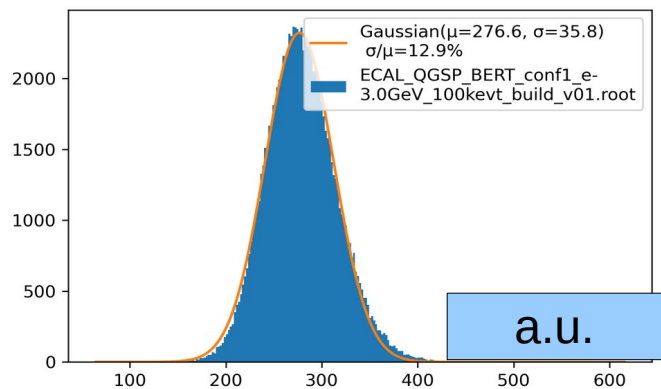
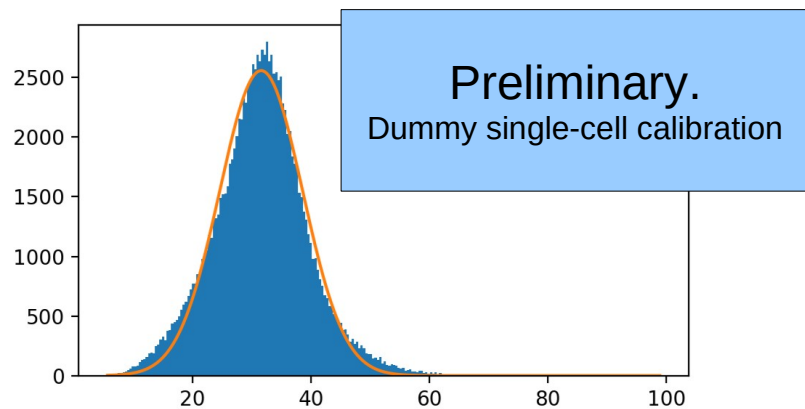


ILC gain

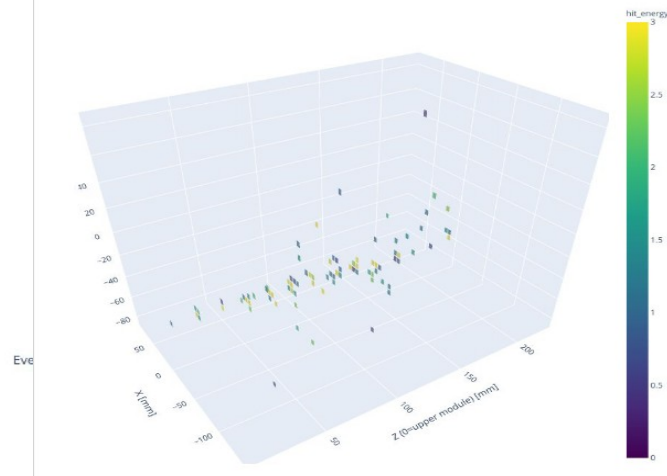
mip_high_layer5_chip12



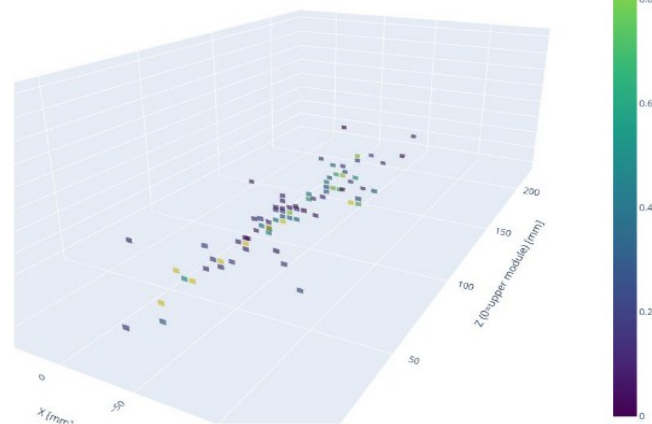
Preamplifier 1.2pF vs 6pF ~ x4.73



Event display Run_name_1 #Hits=86 #Coincidences=15



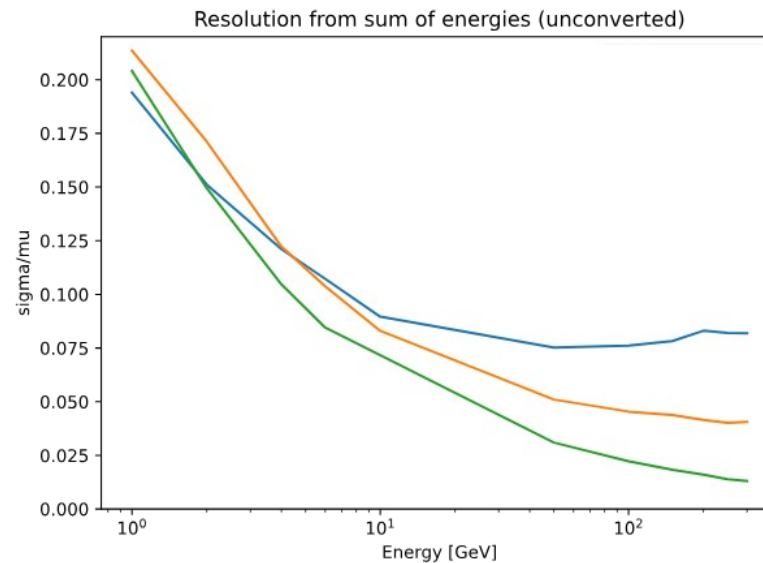
Real event



MC

Next step: CERN (together with AHCAL)

20



Simulation (only SiW-ECAL)

15 layers:

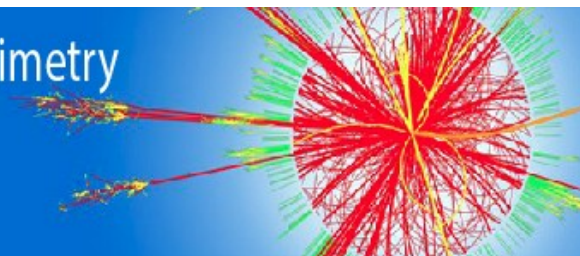
– 14.7 X0

– 21.2 X0

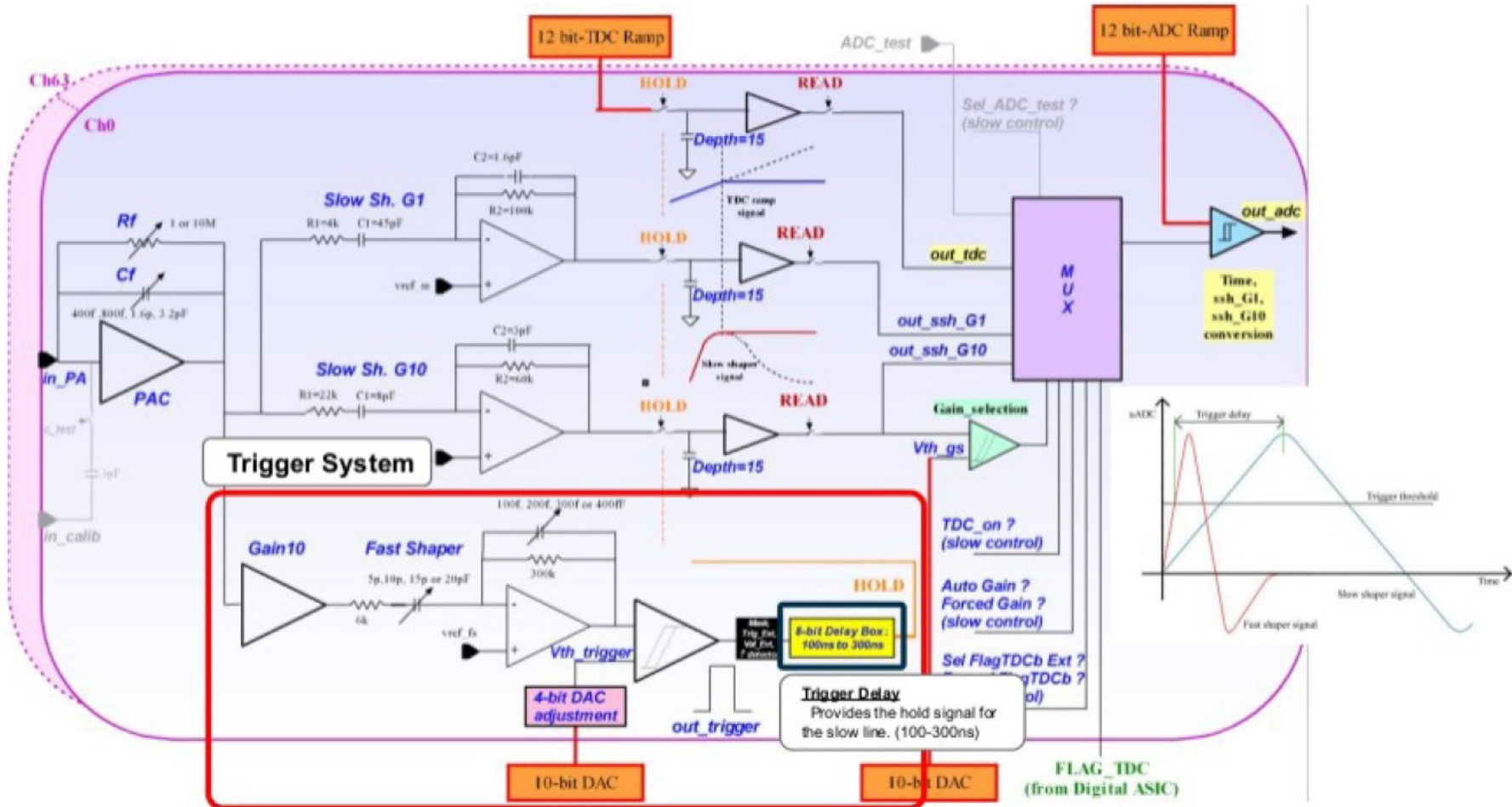
– 28.9 X0 (and 24 layers)

- ▶ The SiW-ECAL prototype
 - 15 layers of $180 \times 180 \text{ mm}^2$ with 1024 $5.5 \times 5.5 \text{ mm}^2$
 - Modular stack: accepts different tungsten distributions and different options for PCBs
- ▶ Intense campaign of BT 2021-2022
 - After a long hibernation due to COVID
 - Detailed commissioning at DESY (low energy electrons)
 - Detailed input obtained for the ongoing new optimized PCBs design and production
- ▶ Next stop at CERN
 - common running with Analogue Hadronic Calorimeter of CALICE
 - High energy leptons and hadrons

CALOR 2020 – 19th International Conference on Calorimetry
in Particle Physics
University of Sussex, UK, 16-20 May, 2022

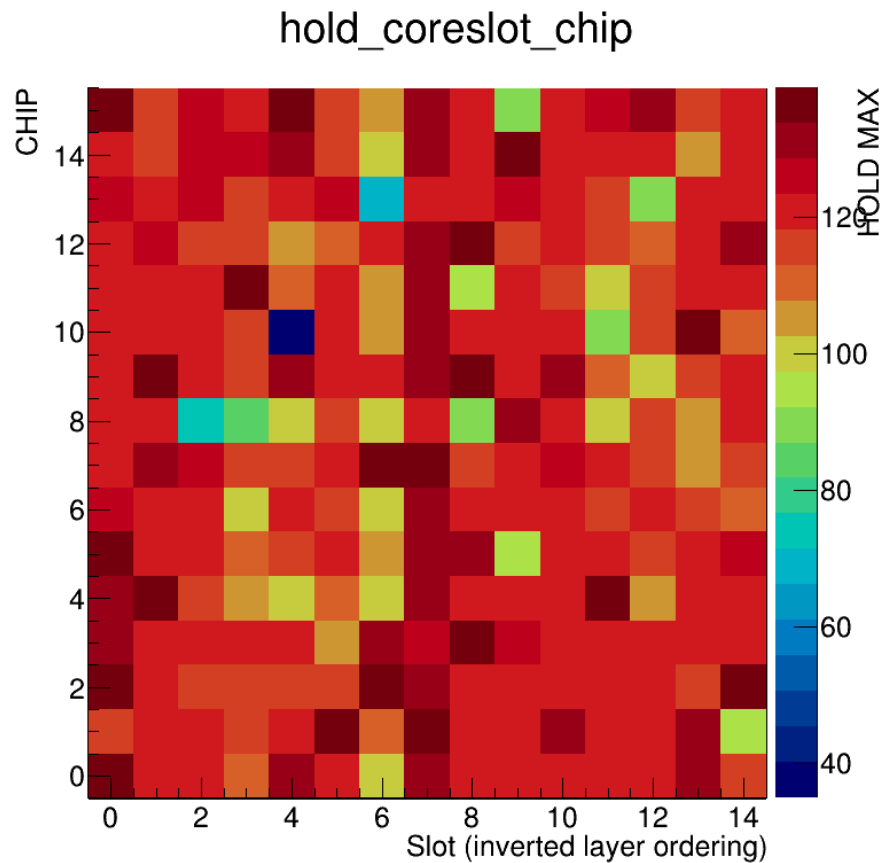
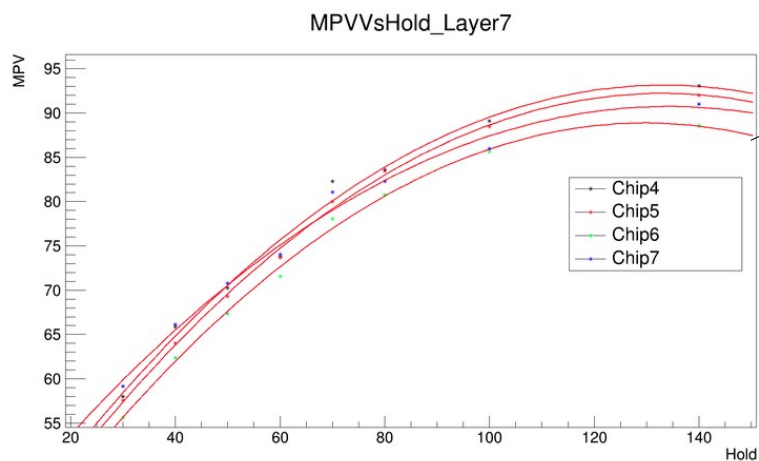


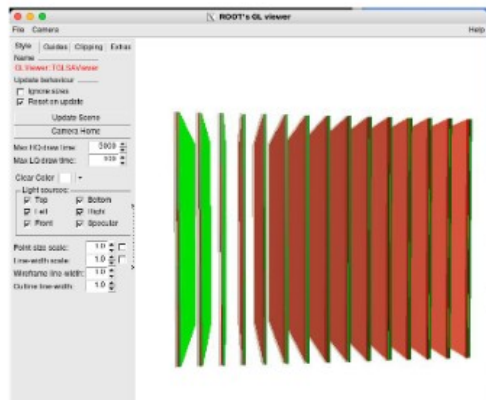
Detector commissioning: hold-value



Detector commissioning: hold-value

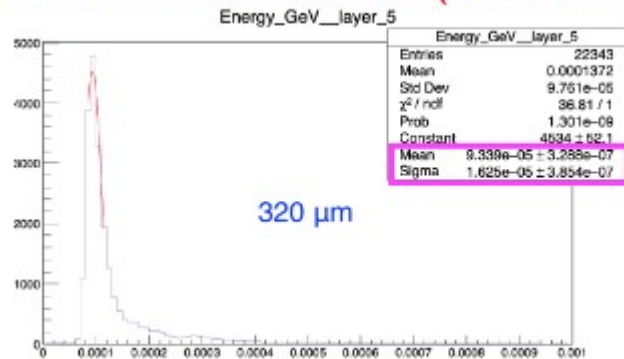
► Done at DESY with beam



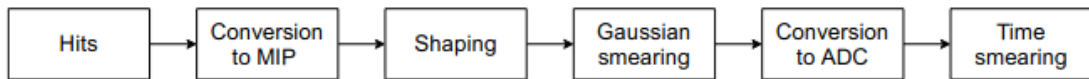


Digitization

Conversion to MIP scale (electrons @ 3 GeV)



Raw simulation \Rightarrow info. resembling detector output, including readout effects



- Hits: starting point from raw simulation.
- Map energy deposited to MIP scale.
- Simulate pulse shaping in the readout electronics + saturation effects.
- Add smearing: noise term in detector cells/readout.
- Conversion to ADC, time smearing

