Upgrade of CMS Barrel Electromagnetic Calorimeter for LHC Phase-II

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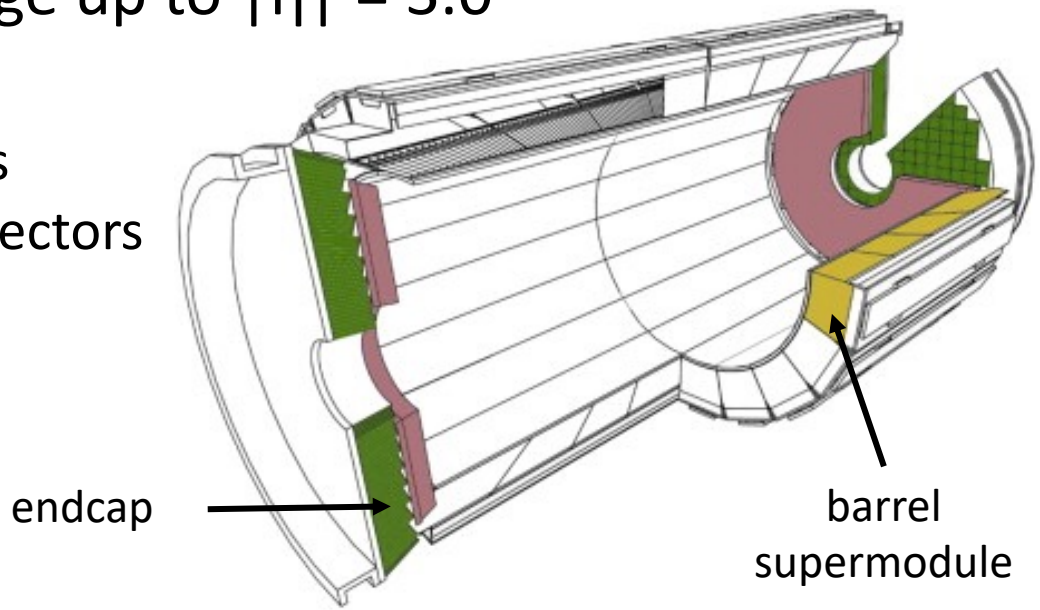
Phase I ECAL Overview

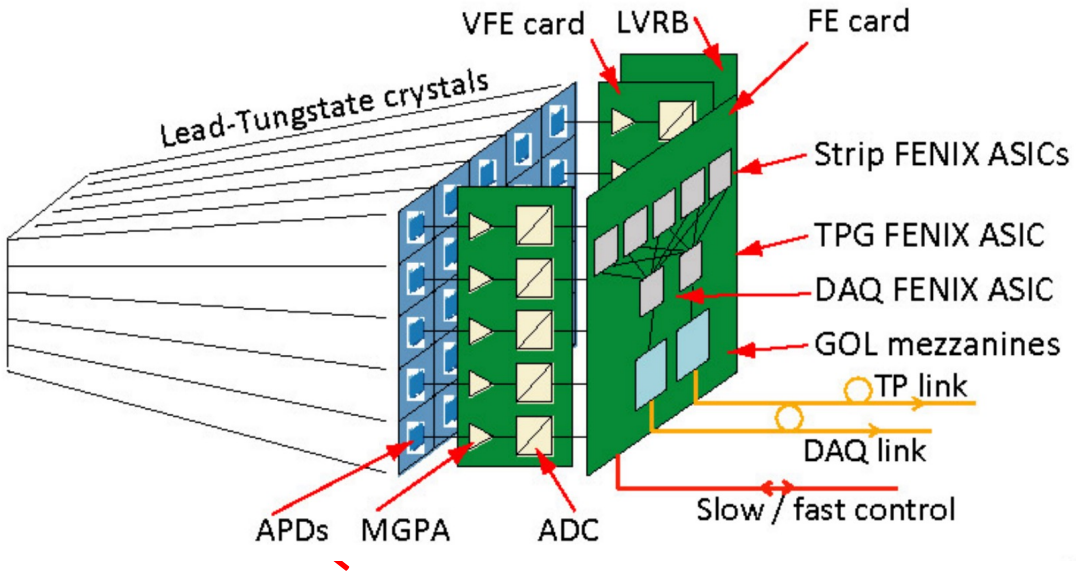
- Lead tungstate ($PbWO_4$) crystal calorimeter
- Provides excellent energy resolution in harsh radiation environment
  - Achieved 1% mass resolution for SM Higgs in γγ decay channel
  - Detailed in Simone and Federico's talk
- Hermetic and compact detector with coverage up to $|\eta| = 3.0$
- Barrel region:
  - Contains 61,200 crystals across 36 supermodules
  - Uses avalanche photodiodes (APDs) as photodetectors
- Endcap region:
  - Contains 14,648 in 4 half-disk "Dees"
  - Uses vacuum phototriodes



Phase II Challenges

- The main objective of High Luminosity LHC (HL-LHC) is to deliver a much larger dataset for physics to the LHC experiments
- ECAL will have to maintain physics performance for an integrated luminosity of 4500 fb^{-1}, a peak luminosity of 7.5 x 10^{34} $cm^{-2}s^{-1}$ and for 200 pileup interactions
- Implications of Phase II:
  - Increase trigger latency from 4 us to 12.5 us
    - This allows use of the track trigger at L1
  - Increase L1 trigger rate to 750 kHz, currently 100 kHz
    - HLT output bandwidth of up to 10 kHz
  - More challenging event reconstruction with much higher in-time and out-of-time pileup
  - More radiation
    - More noise (APD leakage current) and crystal transparency loss
  - Increased rate of anomalous signals ("spikes") caused by hadrons impacting directly on the APDs, affecting trigger rate

Phase I ECAL Electronics



VFE = very front end
FE = front end

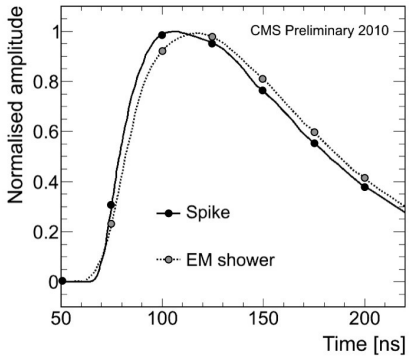
- Multi-gain pre-amplifier (MPGA):
  - Charge sensitive amplifier
  - 3 outputs, gain values: x1, x6 and x12
- Multi-channel ADC:
  - ADC resolution: 12 bit / gain value
  - ADC sampling frequency: 40 MS/s
- Front-End Card:
  - Data pipeline
  - Trigger primitive generation
  - Trigger data granularity: 5x5 crystals

ECAL Phase II Upgrade Overview

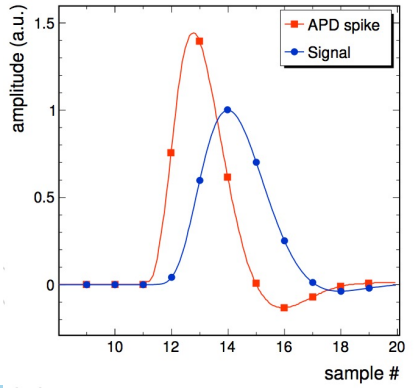
- Replace the endcaps with a high granularity calorimeter
- Refurbish ECAL barrel supermodules during Long Shutdown 3 (2026-2028)
- Keep the lead tungstate crystals and APDs in the barrel
  - Reduce temperature from 18^{O}C to 9^{O}C to keep noise below 250 MeV
- Replace the on and off detector electronics
  - Use new radiation hard ASICs with faster pulse shaping and factor of 4 increase in sampling rate:
    - Reduce impact of out of time pileup and limit increase in APD noise
    - Provide improved spike rejection via pulse shape discrimination
    - Provide 30 ps timing resolution for E > 50 GeV
  - Streaming Front-end board providing single crystal info to trigger via high speed radiation hard optical links (lpGBT)
    - More advanced algorithms in off-detector FPGAs

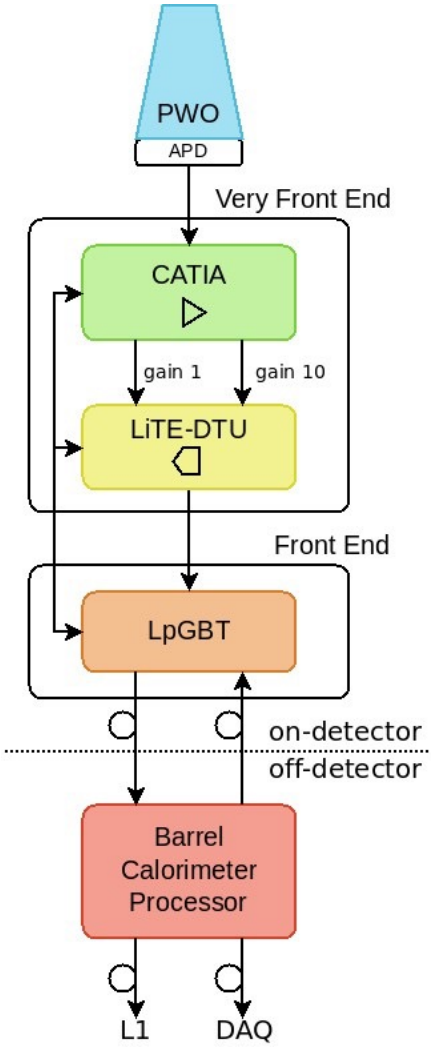
Zoltan Gecse's talk

Current



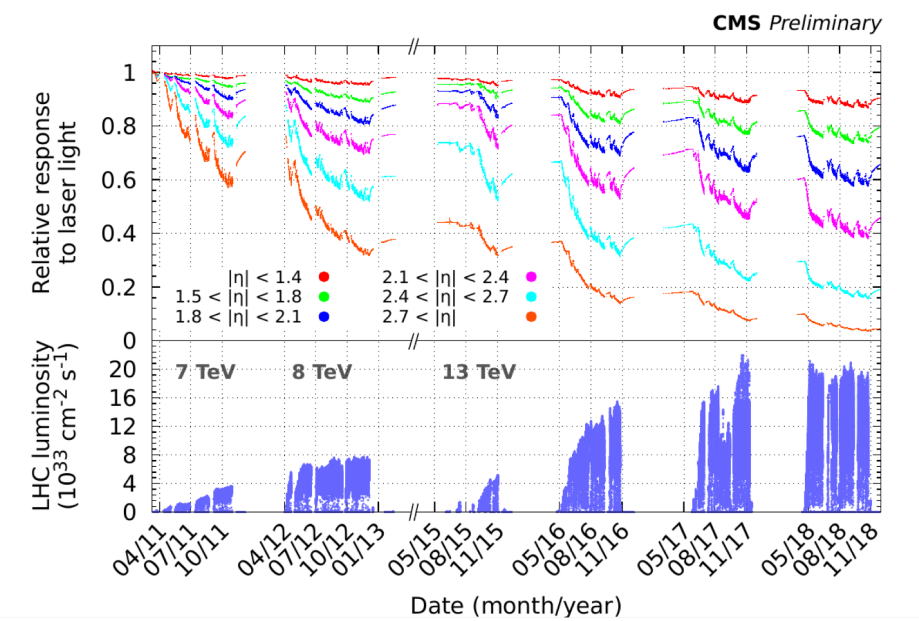
Upgrade





Lead Tungstate Crystal Longevity

- Main concern for ECAL crystals is ageing due to radiation
- Scintillation mechanism is not affected by radiation
  - Radiation creates crystal defects which reduce the crystal transparency and therefore light output
- Effect is monitored and corrected using a dedicated light injection system
- MC simulations have been used to predict the light output in Phase II
  - Validated using test beam data studying effect of hadron irradiation on crystals

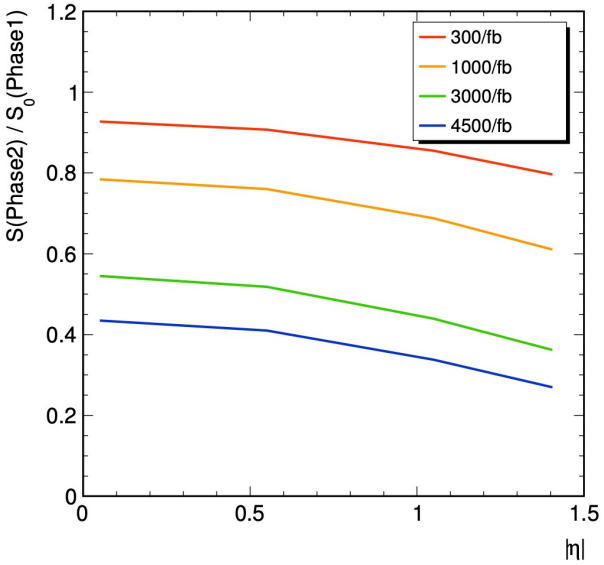


EB: 90%

EE low eta: 40-80%

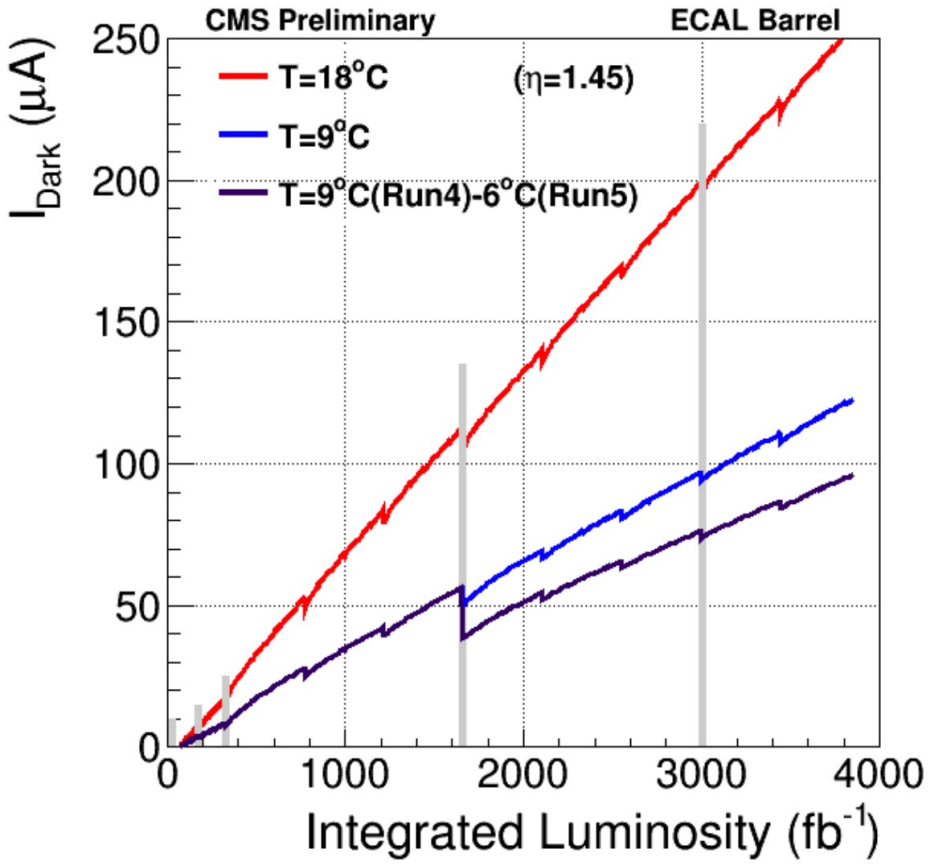
EE high eta: 5-20%

Left: ECAL laser response over Run 1 and Run 2 (2011-2018)
Right: Expected Phase II light output for 50 GeV photon showers with respect to CMS conditions in 2010



Avalanche Photodiode (APD) Longevity

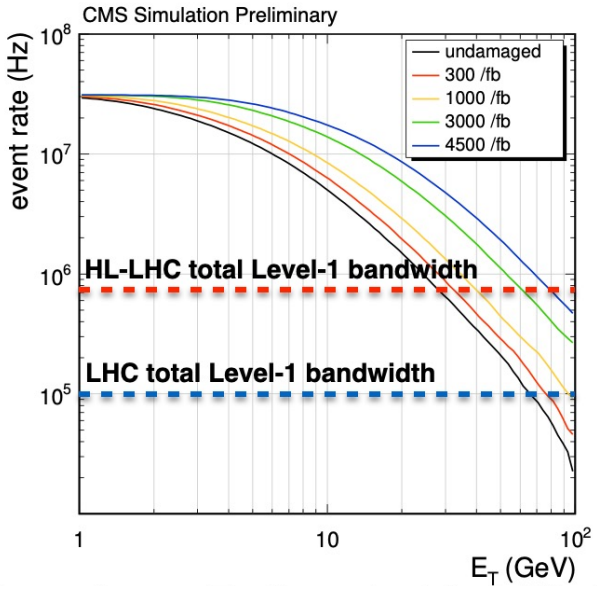
- Two causes of radiation damage to APDs:
  - Gamma rays creating surface defects
    - Increasing surface current
    - Reducing quantum efficiency
  - Hadrons creating bulk damage
    - Causing an increase in the bulk current
- Main concern for HL-LHC is the increase of dark current
  - Electronic noise depends on square root of bulk current
  - Can be mitigated by reducing the operating temperature



Spikes

Spike – large isolated signal due to hadron interactions within APD volume

Will **dominate** L1 trigger rate at HL-LHC if not suppressed

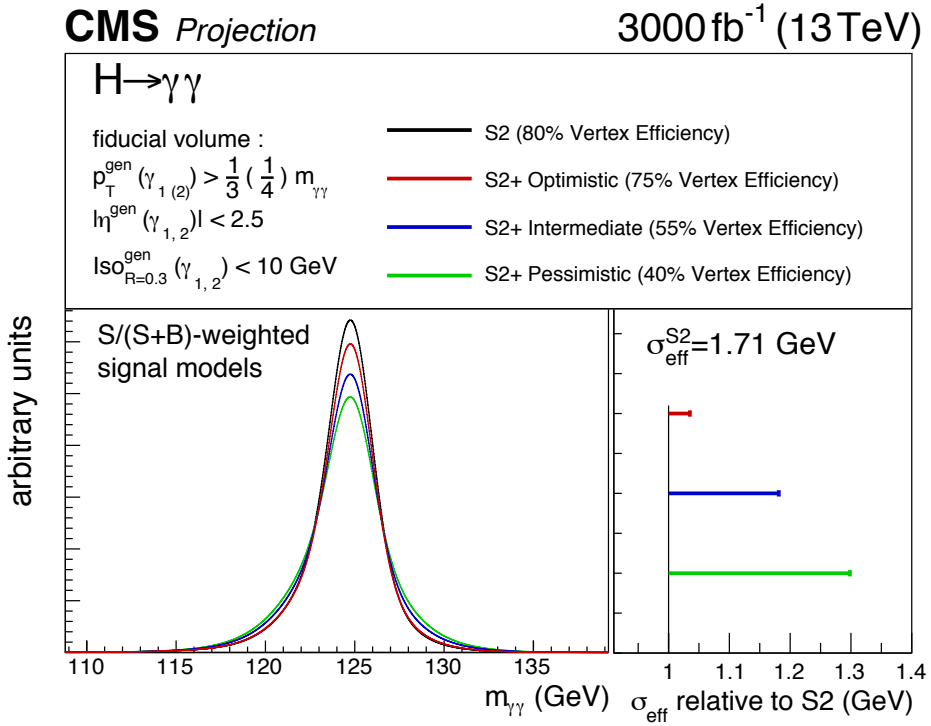


Spike rate vs Et threshold

Need spike killing algorithm in trigger primitives with >99% spike rejection for < 1 kHz residual spikes triggering L1 for signals with $E_T > 5$ GeV

Impact of Fast Timing

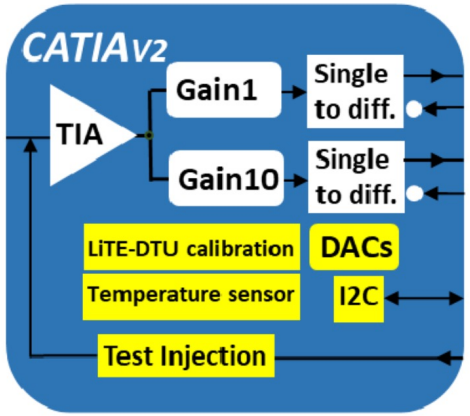
- Challenging to maintain reconstruction performance at 140-200 pileup
  - Reduced primary vertex efficiency (75%->30%) from H→γγ decays
- Improved vertex localisation possible with precise (~30ps) timing capabilities
  - Sensitivity gain (ECFA 2016): ~10% on H→γγ resolution and fiducial cross-section relative to no precise timing case at 140 pileup
- With precision timing (ECAL + MIP timing) we can obtain similar results to Run 2 conditions (S2)

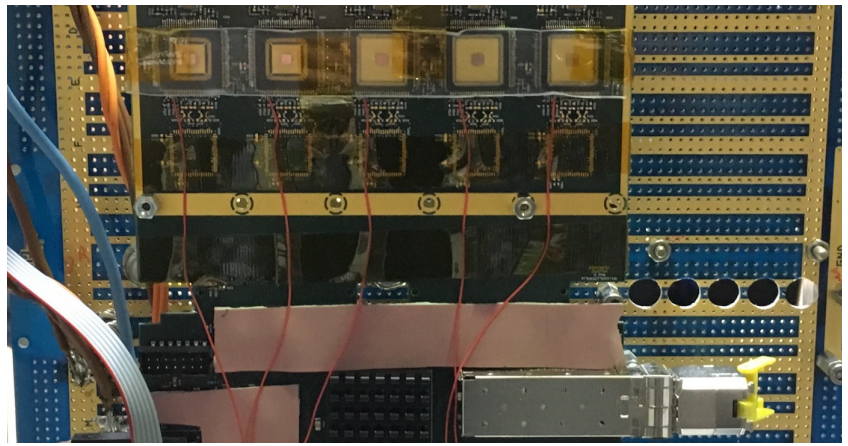


H→γγ mass resolution with different assumptions on vertex efficiency:
no precise timing
+ precise timing in calorimeter
+ precise MIP timing (timing layer)

CATIA

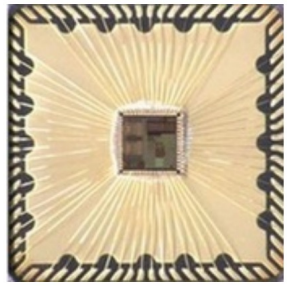
- Pre-amplifier ASIC
  - Trans-impedance Amplifier (TIA) architecture with minimal pulse shaping
    - Faster pulse shaping is important for precise timing and improved spike rejection capabilities
  - 2 output gain values: x1 and x10
- CATIA V1 has been used in test beam with good results
- Initial tests of CATIA V2.1 show very promising results

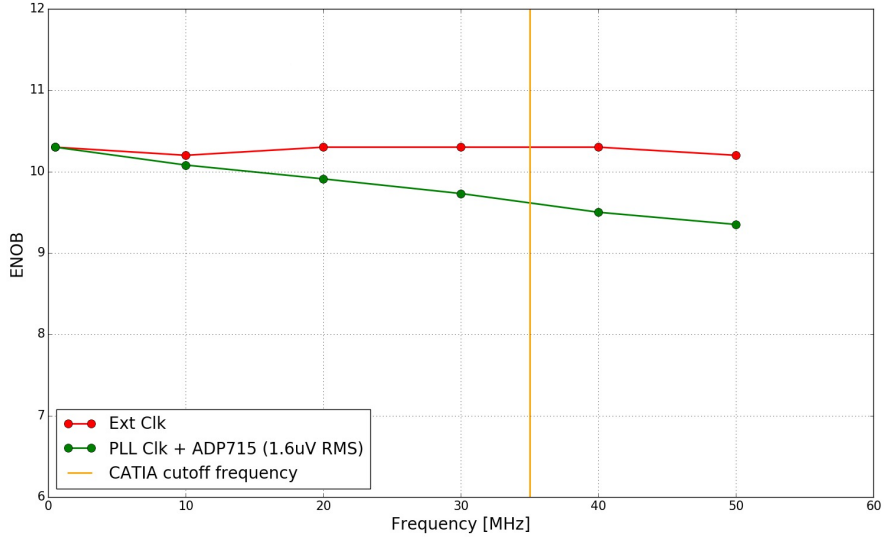




LiTE-DTU

- Data conversion, compression and transmission ASIC
  - Two 12-bits ADCs, 160 MS/s data conversion
  - Lossless data compression
  - Look-ahead algorithm
    - Sample saturation check prevents mixing samples from different gains in the same APD signal timeframe
- ENOB scan performed as function of frequency
  - Fits expected performance
- Received ~600 packaged LiTE-DTU v2 in February
- All 600 tested with 98% passing
- SEU test performed at CRC Louvain
  - No I2C errors, No PLL loss of lock
  - More SEU results to come
    - Including more ions tested at SIRAD LNL

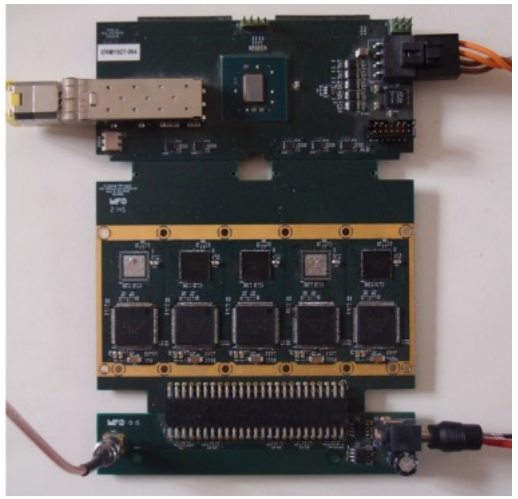




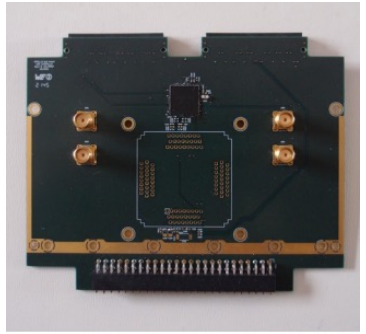
ENOB scan with LiTE DTU v1.2

CATIA and LiTE-DTU Combined Tests

- Have both single channel and multi channel test board
  - Using CATIA v2.0 and LiTE DTU v2.0
- Preliminary results show that the system is working
  - Initial noise and timing measurements are compatible with 30 ps timing for E > 50 GeV
- LiTE-DTU new features working
  - Test-pulse generation for CATIA
  - Enables secondary calibration scheme
  - ADC calibration with CATIA baseline-like levels
- Close to starting production for both ASICS



Multi channel test board

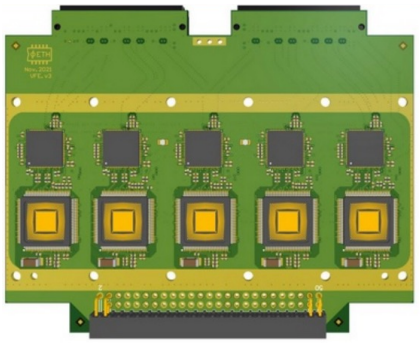


Single channel test board

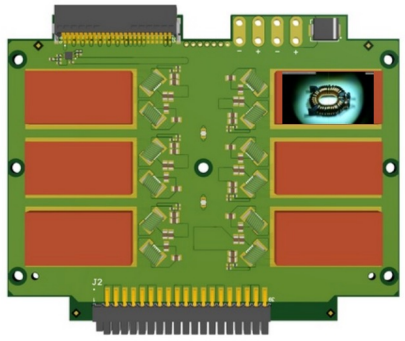
Very Front End (VFE) and Low Voltage Regulator (LVR)

VFE:

- Contains 5 x CATIA and LiTE DTU chips
- Calibration of ADC values using CATIA's reference voltage and embedded multiplexer
- Readout of temperature sensors (via FE)
  - APD, CATIA and PCBs
- Pilot run of 8 VFE v3 have been tested
  - Larger production launched at the beginning of this month



VFE v3



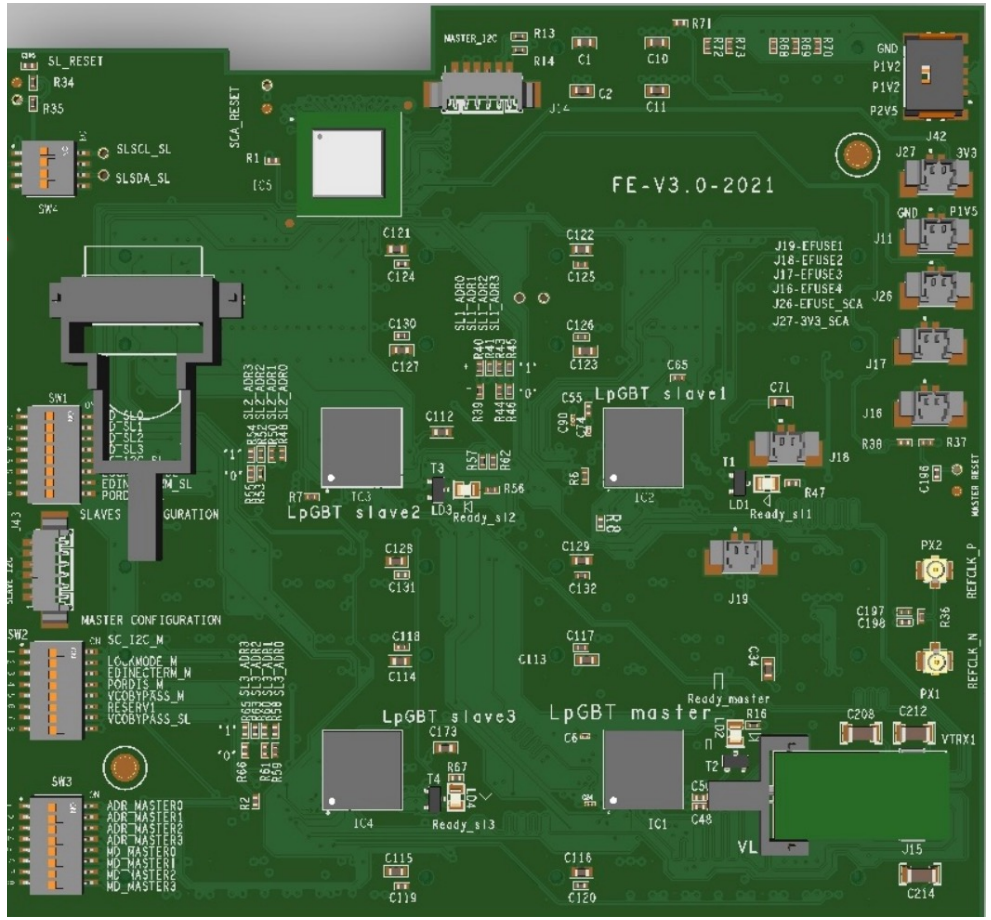
LVR v3.1

LVR:

- Supplies voltages to ASICS and FE board
- Radiation tolerant ASIC to readout APD leakage current
- Uses DCDC converters
  - bPOL12s and linPOL12
- Design is magnetic field tolerant and has low noise

Tentatively final versions of both VFE and LVR

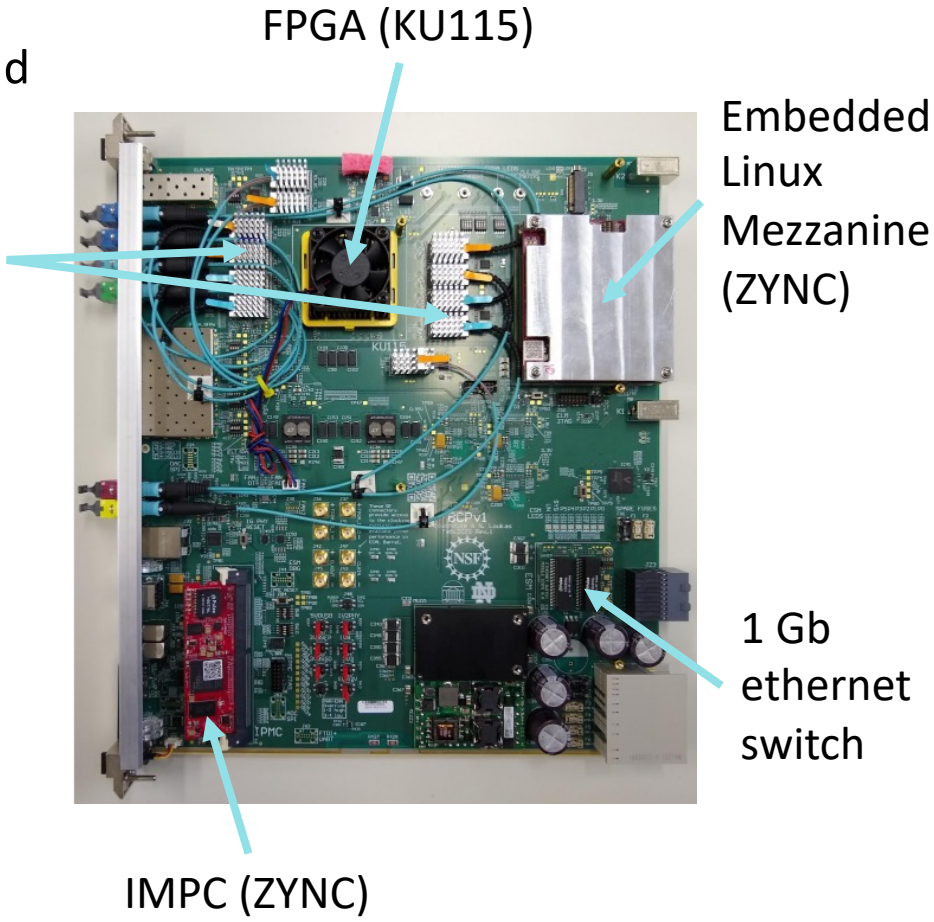
Front End (FE)



- Allows streaming of full granularity data off-detector at 40 MHz
  - Not possible in the current Phase I detector
- Sends clock to VFE directly from controller lpGBT
- I2C via controller-responder chain
- Monitors APD dark current
- FE v3 is close to the final version

Backend Electronics

- Barrel calorimeter processor (BCP)
  - Combines trigger and DAQ functionality and provides clock and control signals to the FE electronics
  - Each board handles signals from 600 crystals
  - Uses commercially available FPGAs
  - Algorithms being developed using high level synthesis to produce trigger primitives
- Currently have BCP v1
  - Uses one KU115 FPGA
  - Being used for integration tests with VFE/FE boards and DAQ
- BCPv2 will use one VU13P instead of 2xKU115 originally envisioned
  - Provides nearly 3 times the memory, 30% more logic cells and 11% more digital signal processing
  - Schematics under development
- Testing results (including timing performance) are good

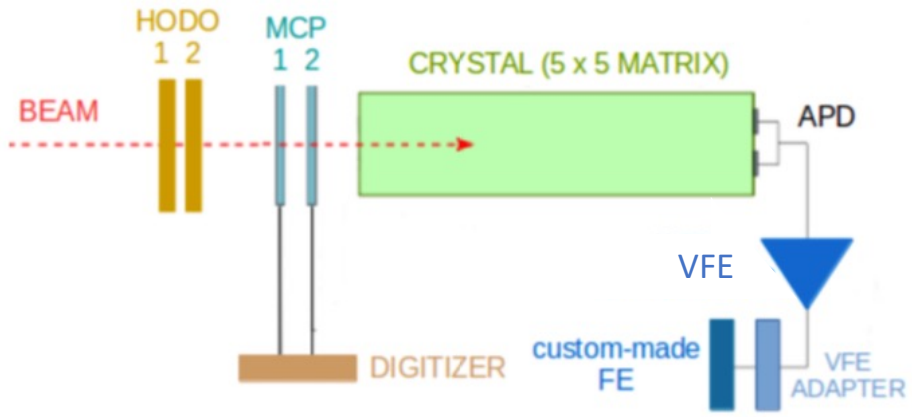


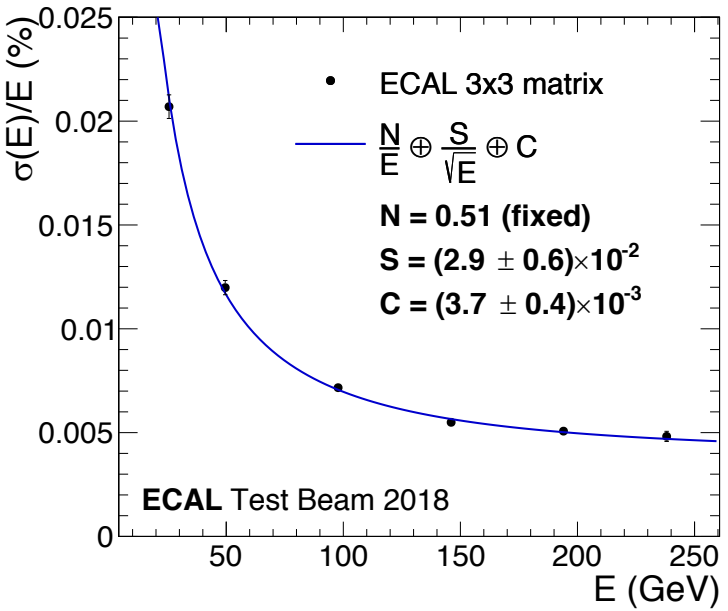
Test Beam to Date

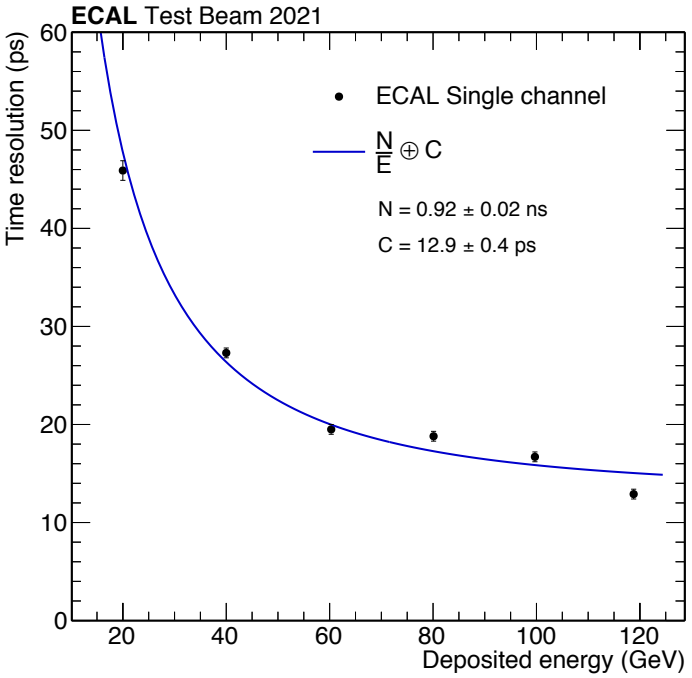
- In 2021 we tested a single ECAL tower (5x5 crystal matrix) with Phase II CATIA v1.2 and LiTE DTU v1.2
- Electron beam with energies from 25 to 250 GeV
- Energy and timing resolution meet requirements

Hodoscopes measure beam position

Microchannel plate detectors for external timing

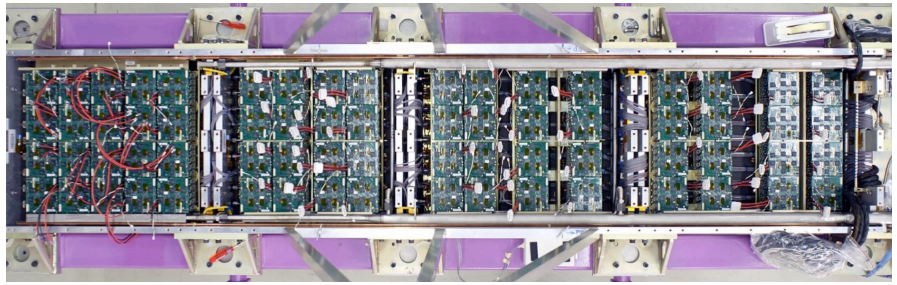






Energy resolution plot is from 2018, where we used CATIA v1 and a commercial 160 MHz ADC

Supermodule Refurbishment and Schedule



- 36 supermodules will be extracted at the start of LS3
- All Phase I electronics will be exchanged for their Phase II counterparts and associated services (e.g. optical cables) by dedicated teams on the surface
- Supermodules will be fully tested before reinstallation
- Whole procedure will take approximately one year

Plans for This Year

- Large scale (~400 channel) system tests planned for summer 2022
  - Using ECAL supermodule with 16/20 trigger towers
- Test full Phase II readout chain with lpGBT transmitters for front-end to back-end data streaming
  - Two BCP v1 will be used in sync
  - Need features of LiTE-DTU v2 for this scale test
- Beam test with this supermodule in late 2022:
  - Measure timing and energy resolution
  - Measure APD spikes using a pion beam
- Engineering design review in Oct 2022
  - Will give the go-ahead for the production of the front-end ASICs and electronics boards
  - System tests are an important input for this

Conclusion

- Both the on and off detector electronics will be replaced in the CMS ECAL for HL-LHC in order for the current performance to be maintained
- Full featured ASICs have been received
  - Initial test results are good
- Plans for this year:
  - System test (>400 channels) with spare supermodule
  - Supermodule test beam with electrons and pions
  - Engineering design review to provide green-light for the production of the front-end ASICs and electronics boards
  - Continue development of BCPv2 and associated firmware
- Will have production ready (and tested) versions of ASICs and on detector boards by the end of the year
- All barrel calorimeter components are on track for installation during LS3