Upgrade of ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC

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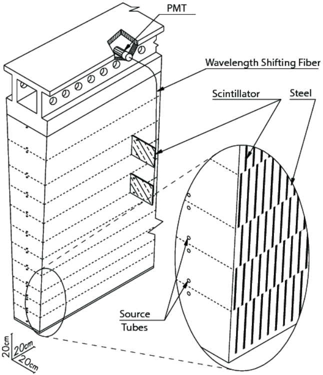
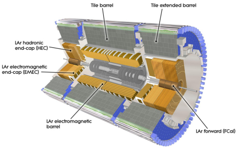
Introduction





- Central hadronic calorimeter ($|\eta| < 1.7$)
- Sampling calorimeter : plastic scintillators and steel absorbers
- 5182 cells (9836 PMTs) : double photomultiplier readout using wave length shifting fibres
- Readout granularity (η, φ) : 0.1×0.1 (in the outer layer 0.2×0.1)
- Energy resolution $\sigma/E \sim 50\%/E \oplus 3\%$
- Critical sub-detector for most physics signatures
  - jets and missing p_{T}
  - electrons and photons

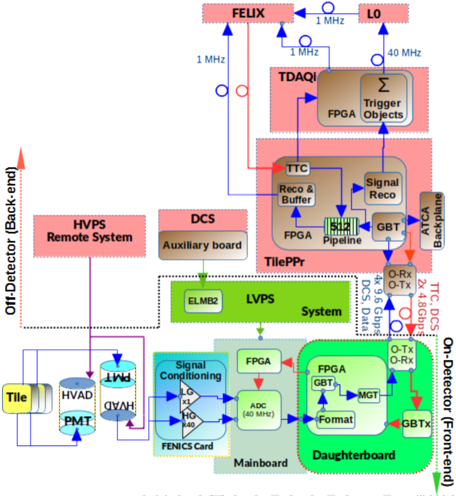
- the on-detector electronics is located inside the electronics drawers

Motivation for upgrade

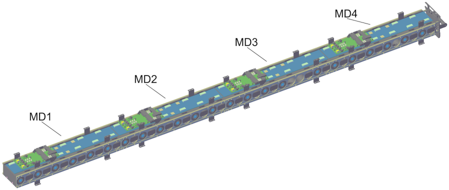
- At HL-LHC, the instantaneous luminosity will increase by a factor ~ 7, leading to around 200 simultaneous proton-proton collisions per bunch crossing
- Increased particle flux through TileCal (2 to 24 Gy for 4 ab^{-1} integrated luminosity)
- Readout electronics is ageing due to operation time and to radiation.
- Current readout architecture is not compatible with the new fully digital TDAQ system of ATLAS and with the timing requirements for trigger and data flow.
- Detector components (steel absorbers, scintillating tiles, fibres and almost all the PMTs) will not be replaced, but detector optics performance has to match the physics requirements.

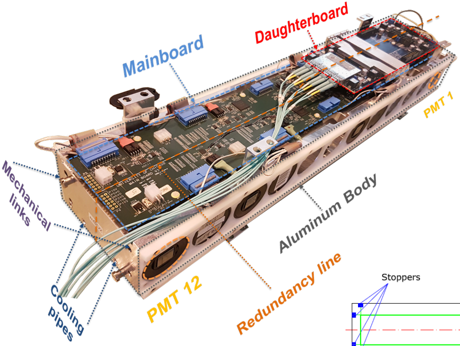
Upgrade strategy

- use electronics parts tolerant to the expected radiation level
- Improve reliability through redundancy ⇒ reduces impact of component failures
- readout electronics architecture must sustain the higher trigger rate ($\sim$1 MHz) and allow for larger event buffer ($> 10\mu$s) ⇒ move buffers and pipelines off detector and read out at the LHC crossings rate 40 MHz
- Replace PMTs that are reading-out the most exposed detector cells (high response losses)

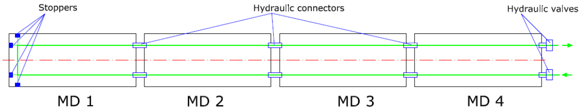


The drawer and mini-drawer concept in mechanics



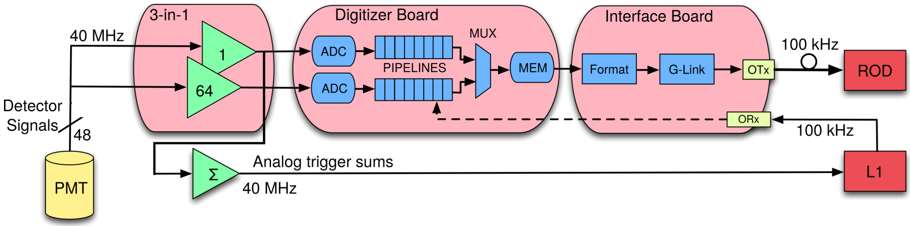


- Each drawer consists of four mini-drawers each hosting 12 PMT
  - independent readout electronics
  - independent low-voltage and high-voltage power distribution
  - Easier maintenance
  - Robustness through granularity



TileCal readout architecture

Current read-out



HL-LHC read-out

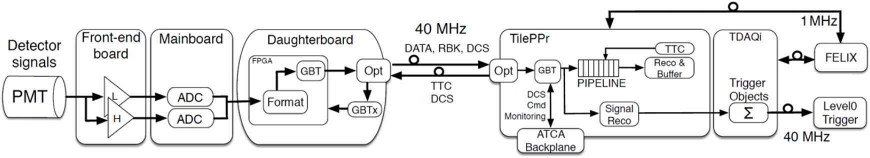
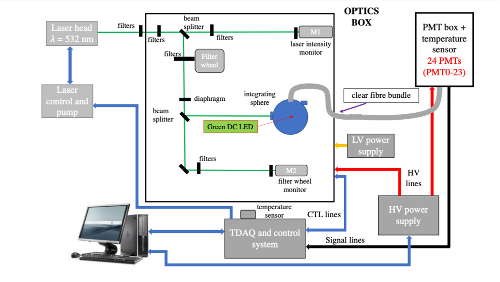
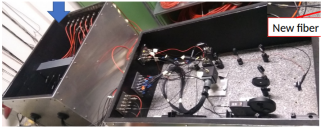


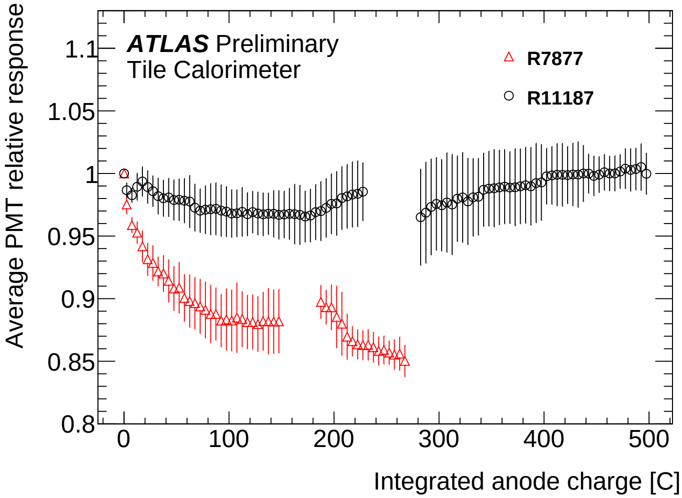
Photo-multipliers





- 1024 PMTs of 9582 in Tilecal to be replaced due to ageing effects (response loss $>$ 25%)
- Characterization of new Hamamatsu PMTs model R11187 completed (same geometry as legacy model, better response stability)
- Three identical test-benches for PMT qualification are set-up.

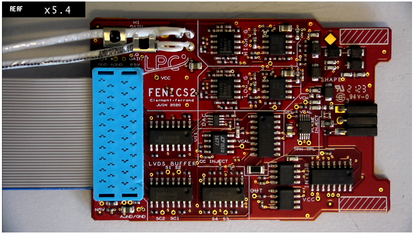
PMT vs integrated anode charge

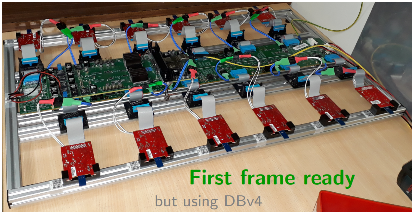


Run-4 maximum expected anode charge ∼ 600 C

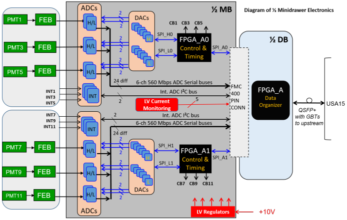
Very front-end board: FENICS

- Analog processing of the PMT pulse
- Amplification and shaping of the current delivered by the PMT
- Analog signals are sent to the next step of the readout chain: the main board
- Radiation hardness: the test of active components (same batches used for the board production) are scheduled this year

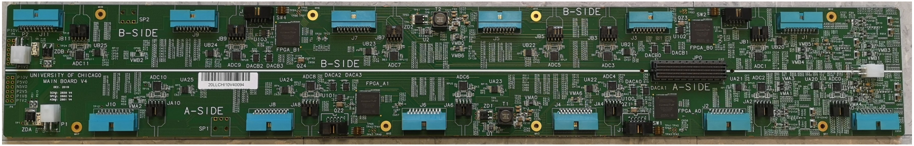




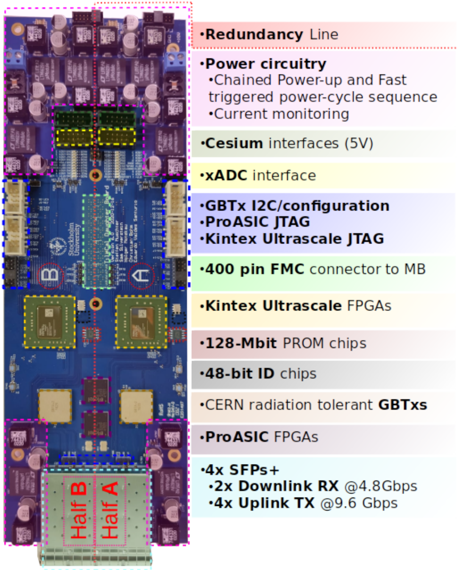
Main board



- 69cm long board, 16 layers, FPGA only for configuration
- Receives analog signals from FENICS: digitizes and sends it to Daughter Board
- Receives 10V from finger LVPS and routes it to Daghter Board and FENICS
- Controls gains and Charge Injection calibrations
- Board production is on-going
- Radiation tests of the active components are to be completed this year

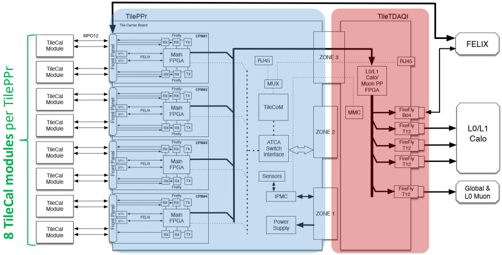


Daughter Board



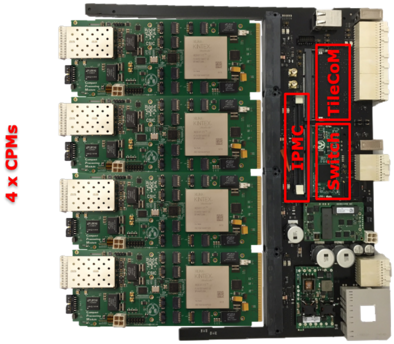
- Interface between the on-detector and off-detector electronics
- Two 4.6 Gbps downlinks and two pairs of 9.6 Gbps uplinks by four SFP+
- Downlinks receive configuration commands and LHC timing to be sent to the front-end
- Uplinks transmit continuous high-speed readout of digitized PMT signals (trigger fully digital)
- Redundant design: two functionally equal independently halves

TileCal Pre-Processor



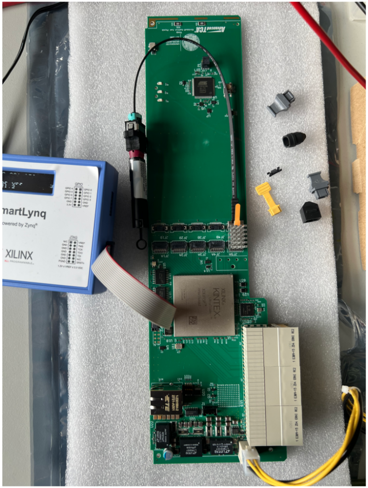
- one PPr board reads out eight super-drawers
- each PPr board consists of
  - One customized ATCA carrier board
  - Four Compact Processing Modules (CPM)
  - One TDAQi RTM (Rear Transition Module)
  - Optical transceivers with multi-mode fibres
- prototype v2 is manufactured and being tested

Processing calorimeter data

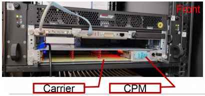


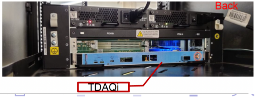
- Communication with the front-end (FE) for control, configuration and monitoring.
- LHC clock recovery and distribution to the FE
- Remote configuration of the FE electronics FPGAs
- High speed data reception from the FE and storage in pipeline memories
- Data calibration and processing (cell energy calculation) in real time every bunch crossing.
- Extraction from pipelines data of triggered events to be sent to the FELIX through the TDAQi
- Transfer data to the Trigger FPGA in the TDAQi

Interface to the trigger and data acquisition systems

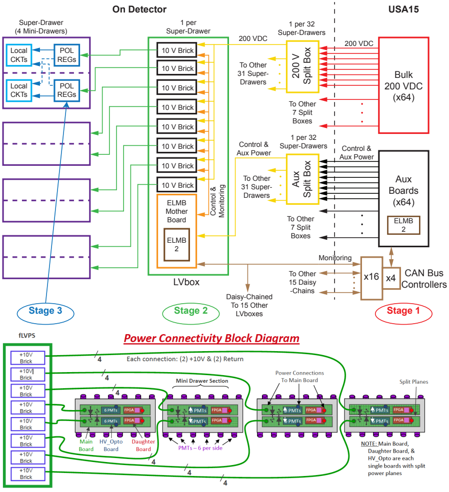


- Synchronous reception of cell energy
- Calculation of trigger objects (trigger towers or group of cells of different η/φ size)
- Making copies of the trigger objects
- Building and synchronous transmission of trigger objects to the different electron/photon, jet, muon trigger sub-systems
- Sending readout data of triggered events to the FELIX





Low-voltage power supply

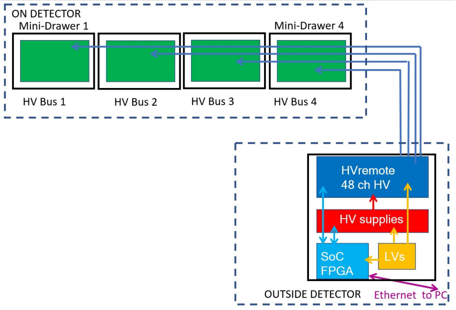


Three stage power system provides

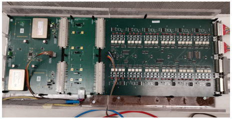
- Better reliability, lower noise
- Improved radiation tolerance
- Lower number of connections (single DC level (+10V) and POL regulators for the voltages needed by the local circuits)
- Redundant power distribution (two individual bricks per mini-drawer and redundancy control with diode on the mainboard)

High-voltage

- High-voltage bulk power supplies and regulators installed in the Atlas service cavern (USA15)
- 100 m long High-voltage wires for each individual PMT.
- High-voltage bus board brings high-voltage to individual PMTs
- Easy maintenance, no radiation hardness issues

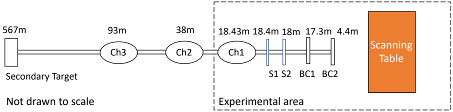


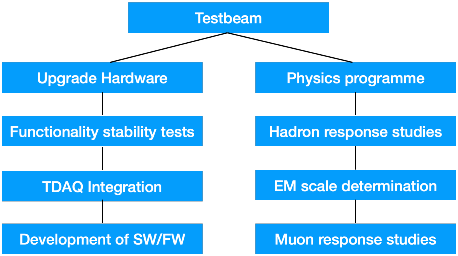
- Prototypes were produced and validated during the test-beam data-taking in Prevessin



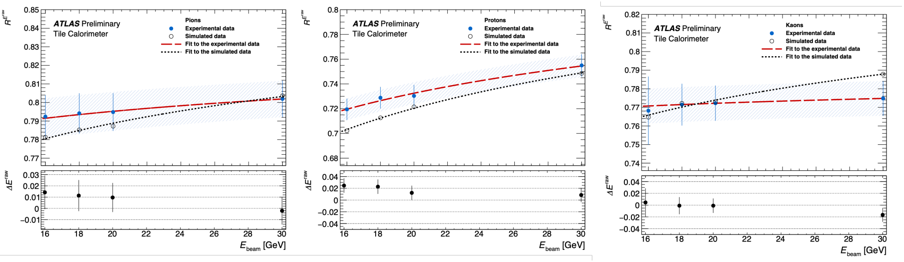
Test-beam

- An environment to validate hardware with real beam data and perform physics studies in parallel
  - 3 modules from the calorimeter (two Long-Barrel and one Extended-Barrel)
- Exposed to electron, muon and hadron beams at various energy ranges
- Hadron beams at 16, 18, 20 and 30 GeV





Test-beam results: hadron response



- Kaon content is smaller in the beam - dominated by statistical errors
- Protons have high statistics - low systematic and statistical uncertainties
- More results in the last year publication : EPJ C81 (2021) 549

Summary

- Hadronic Tile Calorimeter will continue to play crucial role for ATLAS physics program during the HL-LHC data-taking
- Full readout chain (on-detector, and off-detector electronics) and power supplies (low-voltage and high-voltage) will be replaced for Run-4
  - Ageing of the current system, new requirements on data transmission rates and latency
  - HL-LHC radiation levels are too high for the current electronics
- The R&D program is completed. All prototypes are manufactured and validated. We are finalising the design and switching to the pre-production and production phases.
- Regular test-beam campaigns allow to validate and integrate different components of the upgraded detector and provide interesting physics results