The overall electronics chain of the CMS HGCAL

Including readout and powering

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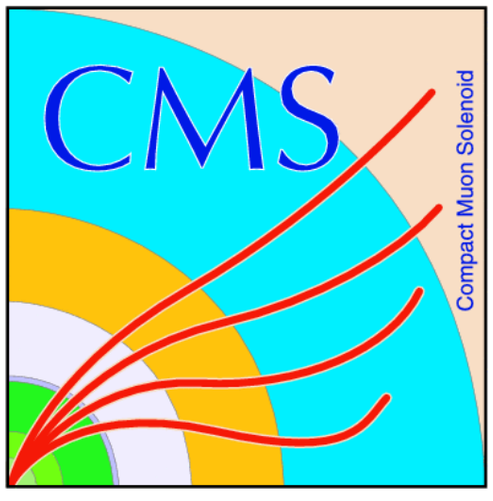
On behalf of the CMS Collaboration

CALOR 2022

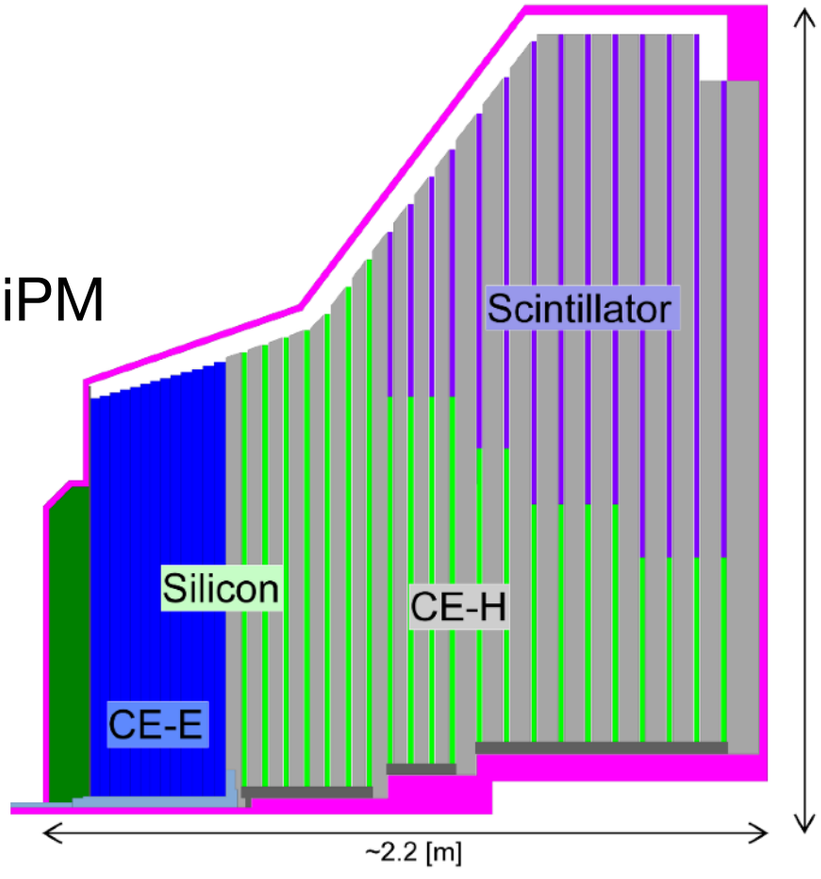


More in talk by Z. Gecse

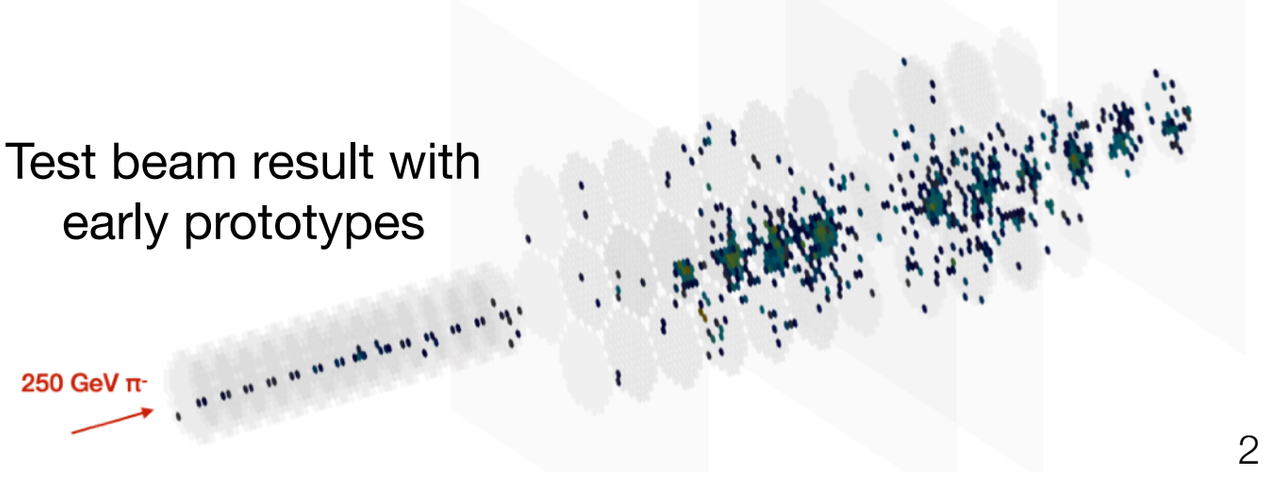
CMS Phase-II Endcap Calorimeter, a.k.a. HGCAL

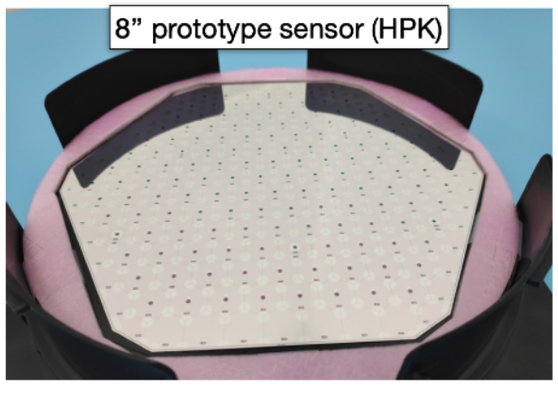
Full replacement of existing CMS endcap ECAL and HCAL with integrated 47-layer sampling calorimeter

- Absorber: Pb, CuW, Cu in CE-E; steel, Cu in CE-H
- Active material:
  - High radiation area: 8” hexagonal silicon sensors
  - Lower radiation area: scintillator tiles with on-tile SiPM
- 5D imaging calorimeter:
  - Highly granular spatial information (0.5 & 1cm^2 Si cell size, 23x23mm^2 — 55x55mm^2 Sc tile sizes)
  - Large energy dynamic range down to single MIP
  - Timing information to tens of picoseconds



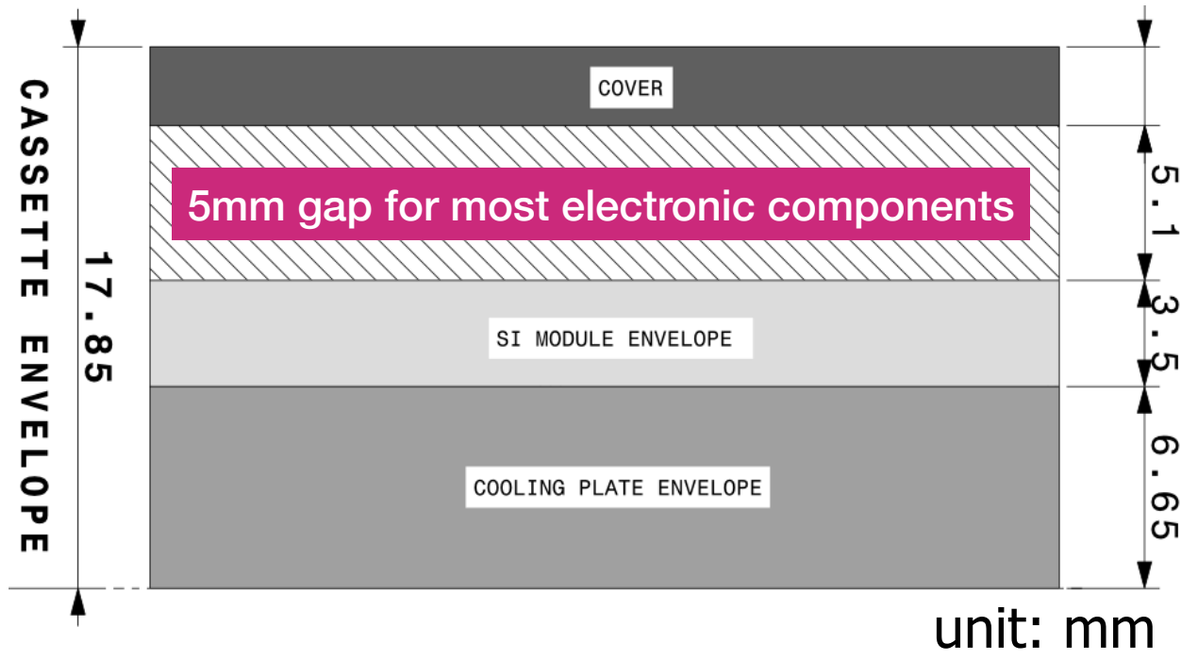
Test beam result with early prototypes





Frontend electronics for the Silicon region

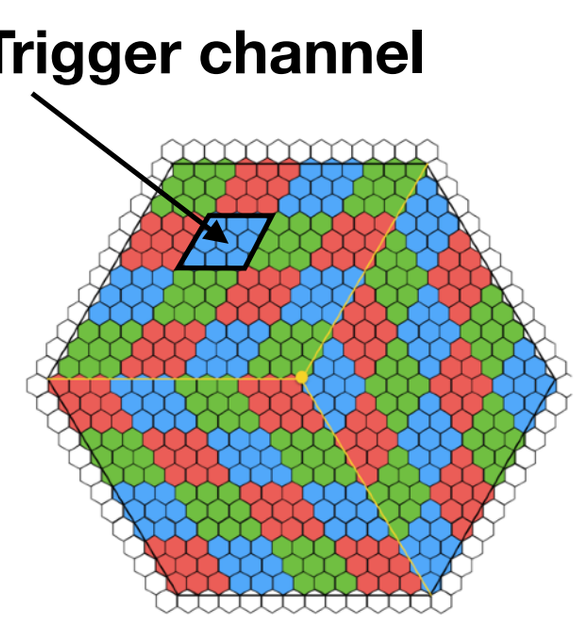
- **Purpose:**
  - Digitize, concentrate, and transmit detector data to the off-detector trigger and data acquisition electronics
  - Distribute clock and control signals (both “fast” and “slow”)
  - Provide monitoring of e.g. temperature, currents, voltages, etc
- **Requirements:**
  - Radiation tolerant (up to 1.5×10^{16} n_{eq}/cm^2 in the inner detector region)
  - Fit in limited physical space
  - Low power
  - Allow transfer of data volumes required for good trigger and physics performance



See talk by T. Kolberg for details on the Scintillator region

Frontend electronics designed around custom ASICs

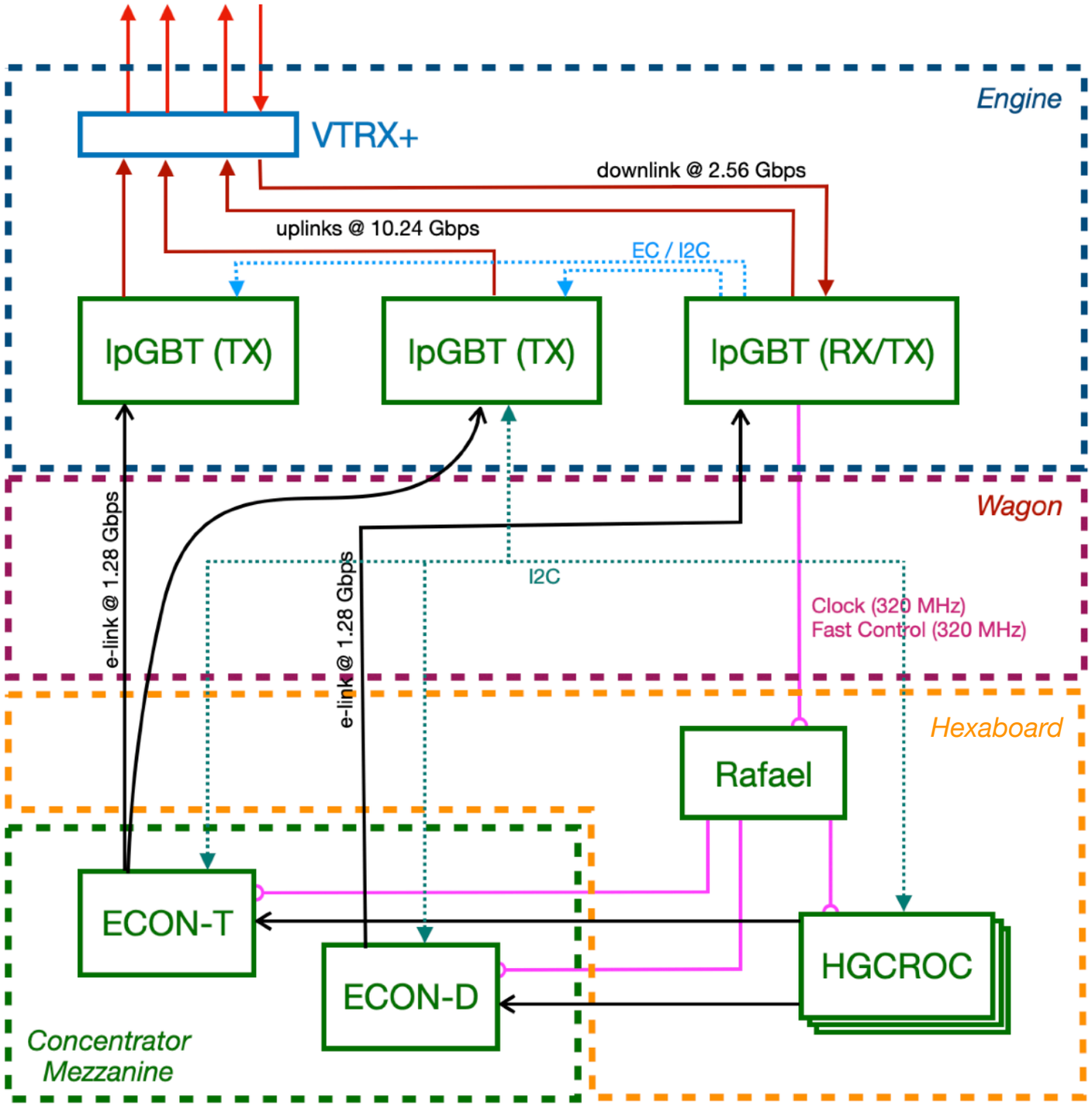
- **HGCROC-Si**: frontend readout chip, receives and digitizes signals from the Si sensors (providing ADC, TOT, TDC)
- **ECON-T**: frontend concentrator chip for trigger path, concentrates trigger channel data via one of 4 trigger algorithms
- **ECON-D**: frontend concentrator chip for DAQ path, performs channel alignment and zero suppression after L1Accept
- **Rafael** chip for clock and fast control fanout
- CERN **lpGBT** for sending/receiving data/clock/control signals via optical link (and **VTRX+**)



HGCAL-specific
CMS-specific
LHC-wide

Frontend architecture

"Low Density" region



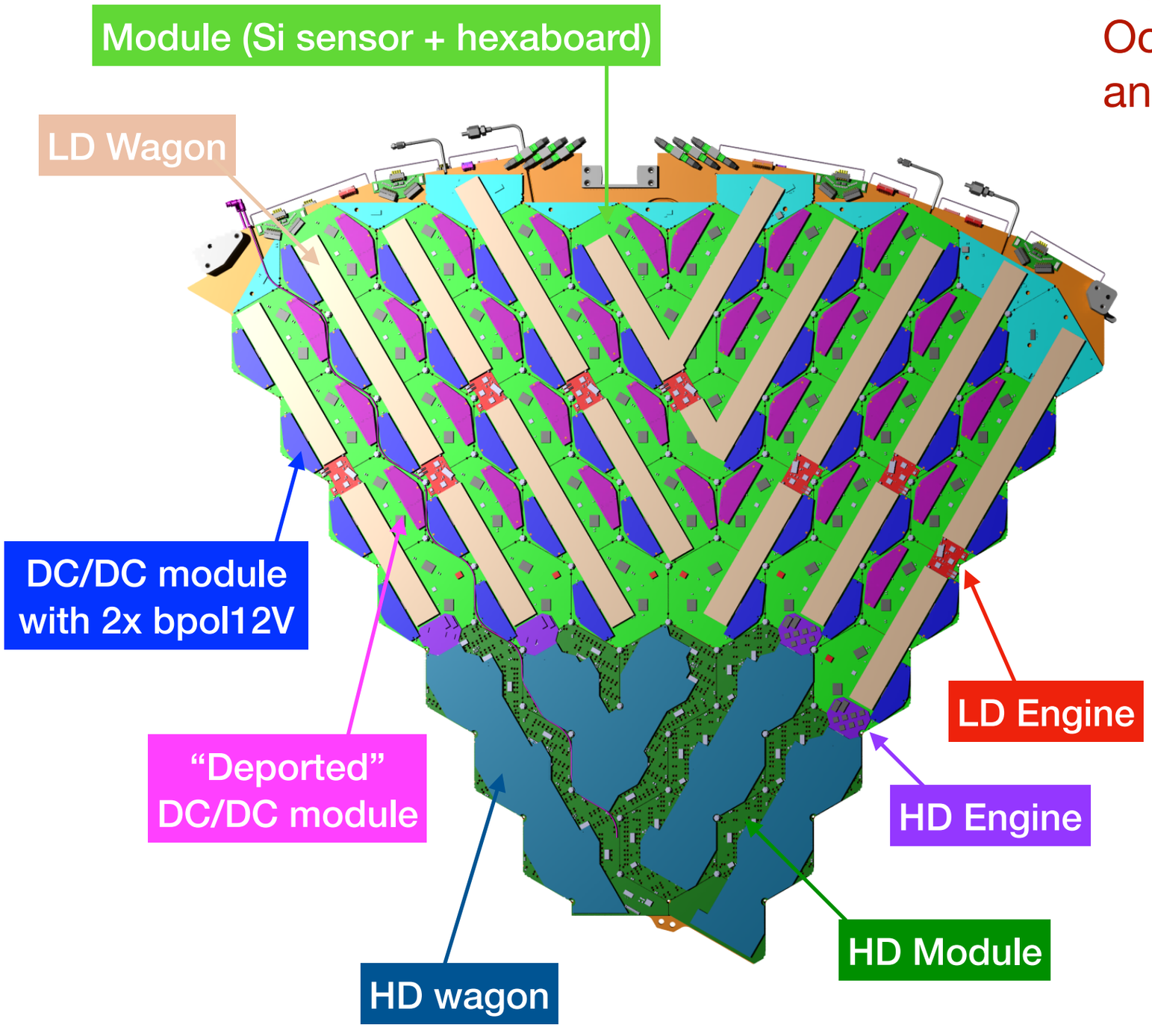
Engine board is connected to 2 Wagon boards

Passive Wagon board is connected to 1—4 Modules

Module is composed of the Si sensor and hexaboard PCB

HGCROC and ECONs are custom for this project, all other chips and components are common developments!

Modular implementation



Note: each layer is different!
Occupancies vary greatly within and between layers

Low density region

- Si sensor 200 or 300 µm thickness
- 192 channels (3 HGCROC) per 8" hexagonal module

High density region

- Si sensor 120 µm active thickness
- 432 channels (6 HGCROC) per 8" hexagonal module

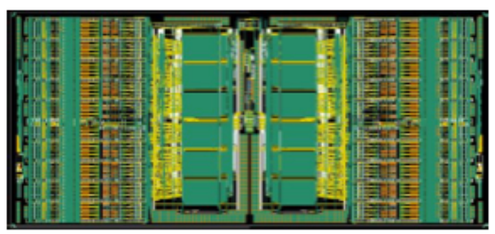
HGCROC3

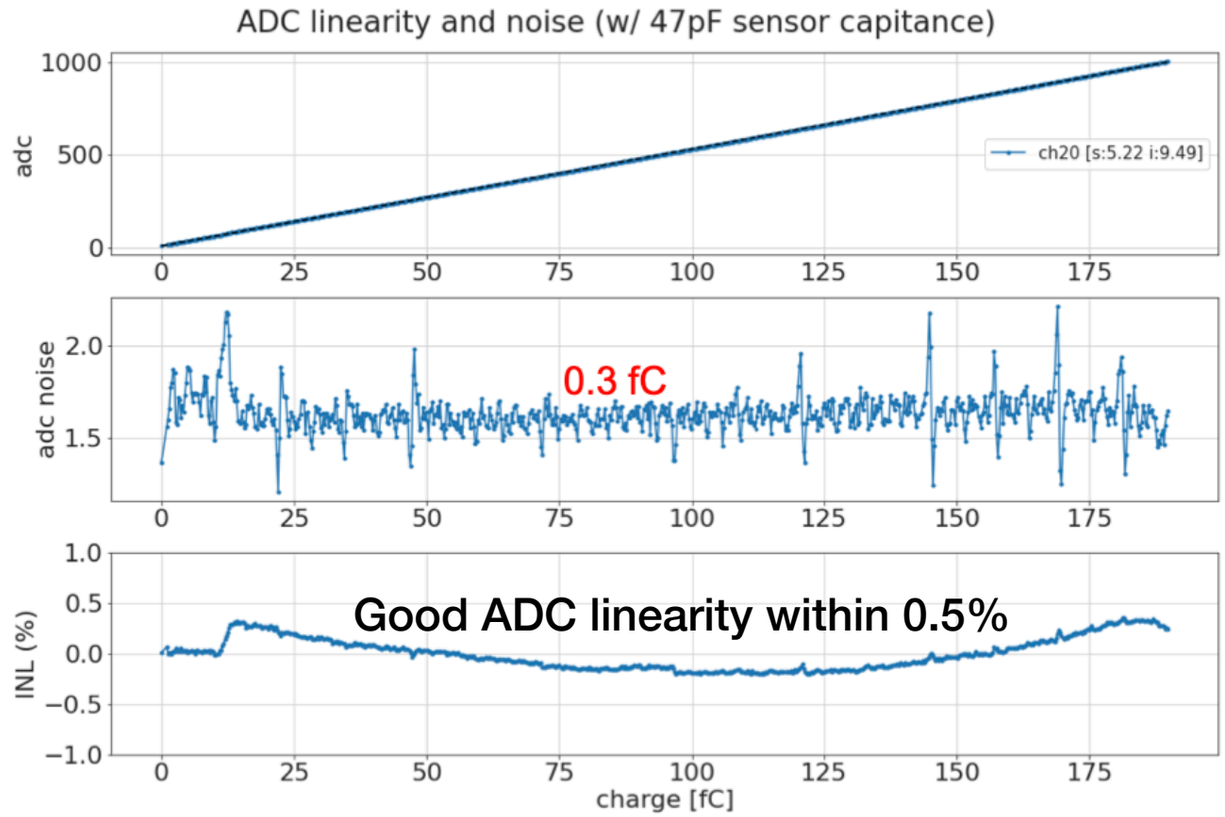
Low power, radiation tolerant readout chip

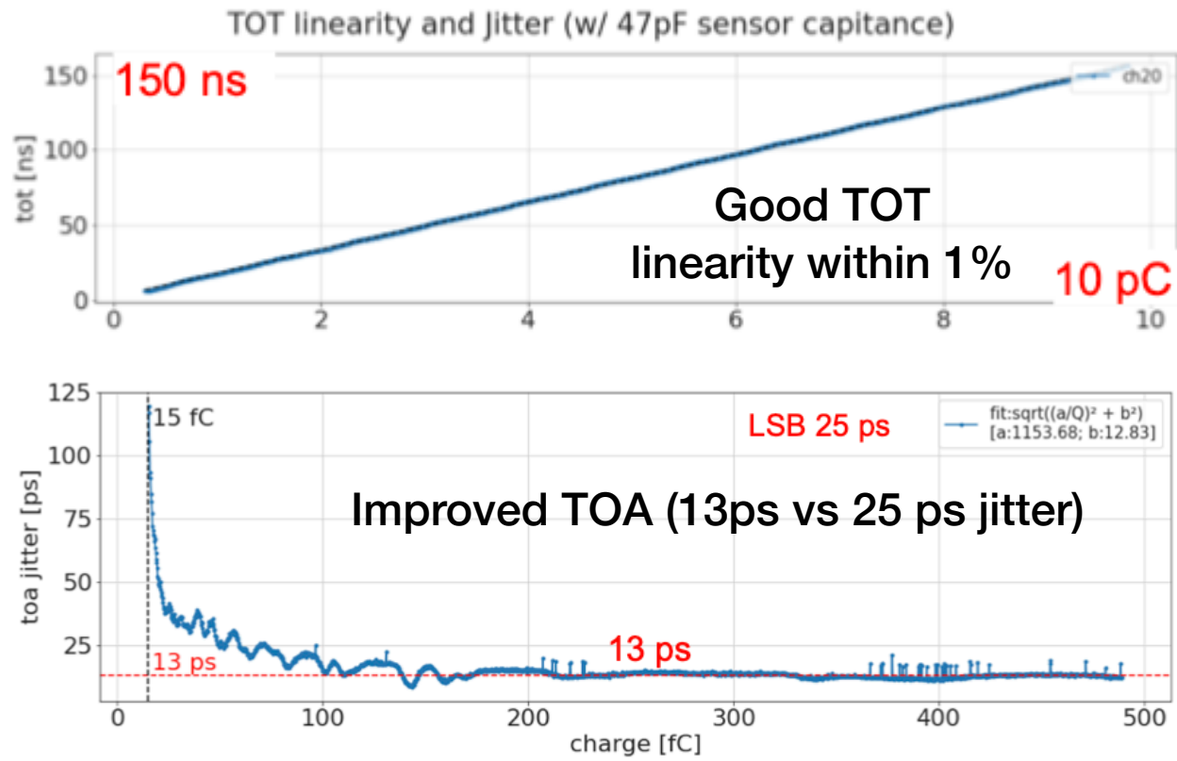
- 15mW/channel
- 200 Mrad, 1×10^{16} neq/cm^2

Measurements:

- 2x36 readout channels, 4 common mode channels, 2 calibration channels
- **Charge (0.2 fC — 10 pC)**
  - **ADC** (peak measurement, 10 bits @ 40 MHz)
  - **TOT** (12 bits, LSB = 50ps)
- **Time via TOA** (10 bits, LSB = **25ps**), jitter floor of 13 ps







HGCROC3

Two data paths:

DAQ path

- 512 depth DRAM, circular buffer, storing full event info (ADC, TOT and TOA) for 12.5μs
- 2 DAQ 1.28 Gbps CLPS output links

Trigger path

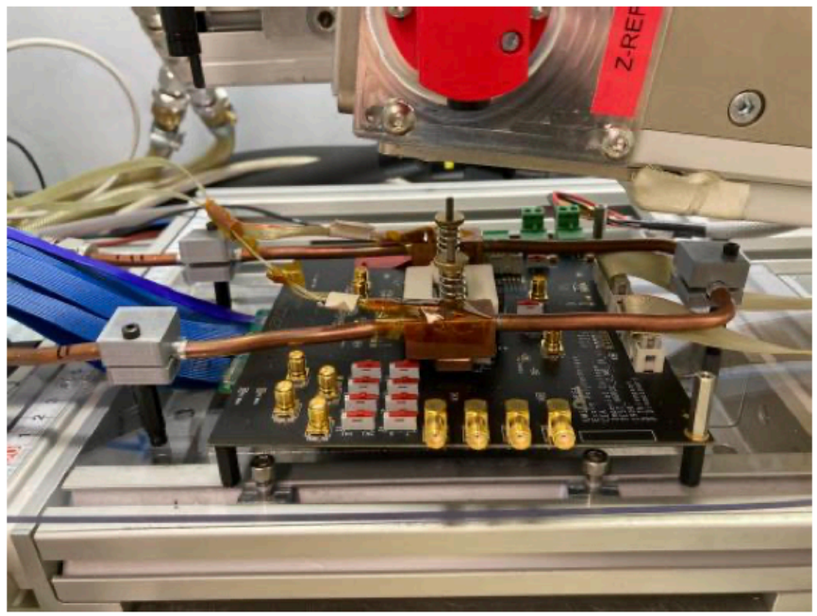
- Sum of 4 (9) channels, linearization, 7-bit floating point output
- 4 Trigger 1.28 Gbps CLPS output links

Control: I^2C protocol for slow control, 320 MHz clock and fast commands

Characterization well advanced, no showstoppers.

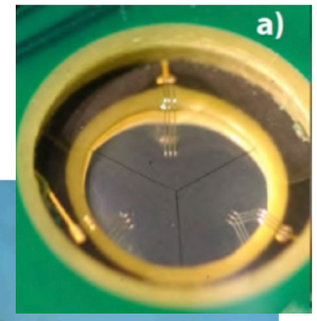
Radiation campaigns, module & system tests ongoing

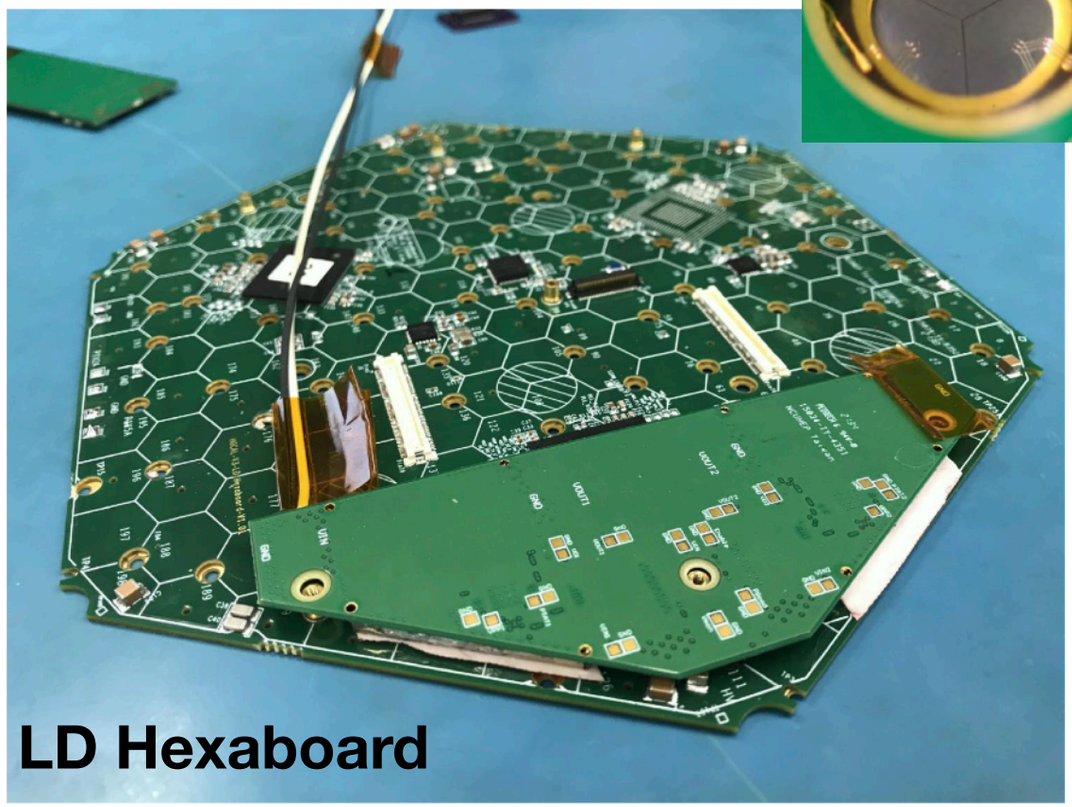
- TID results: at 5°C, up to 350 Mrad, chip behavior very stable, almost no change on ADC, TDC, PLL
- SEE results coming soon

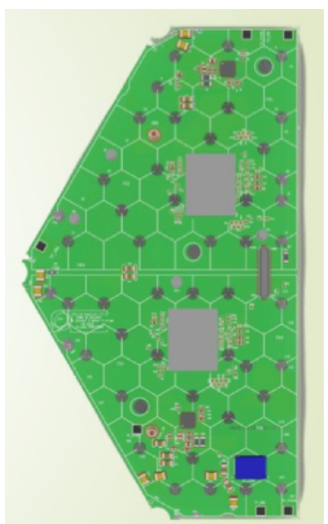


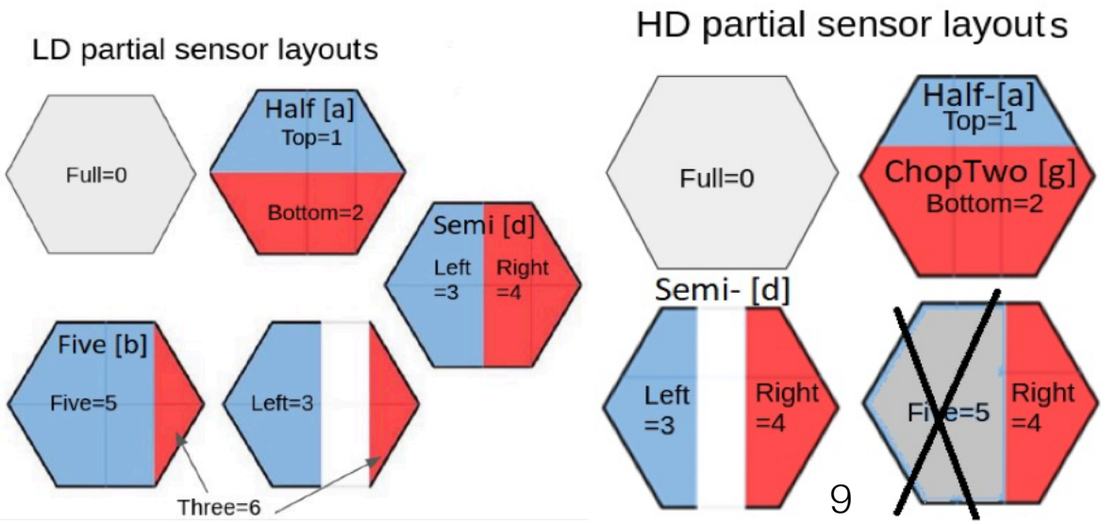
Hexaboards

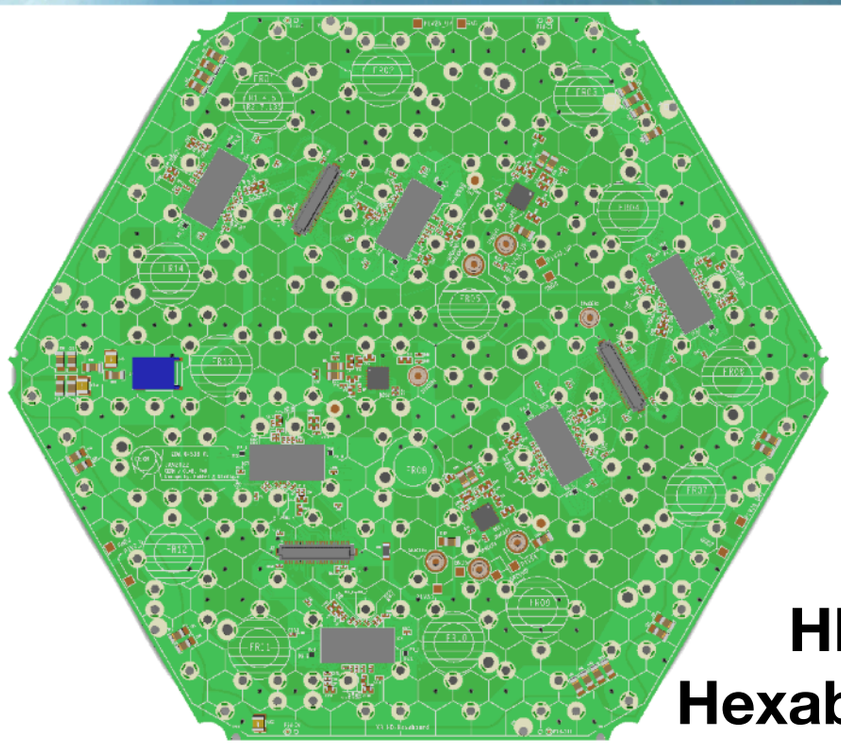
- Si sensor cells are connected to the HGCROC via wirebonds through stepped holes in the PCB
- Most of the detector tiled with Full size hexagonal sensors
  - 3 HGCROCs per LD hexaboard
  - 6 HGCROCs per HD hexaboard
- Partial hexagons used for the outer edges of the layers — these use dedicated hexaboards



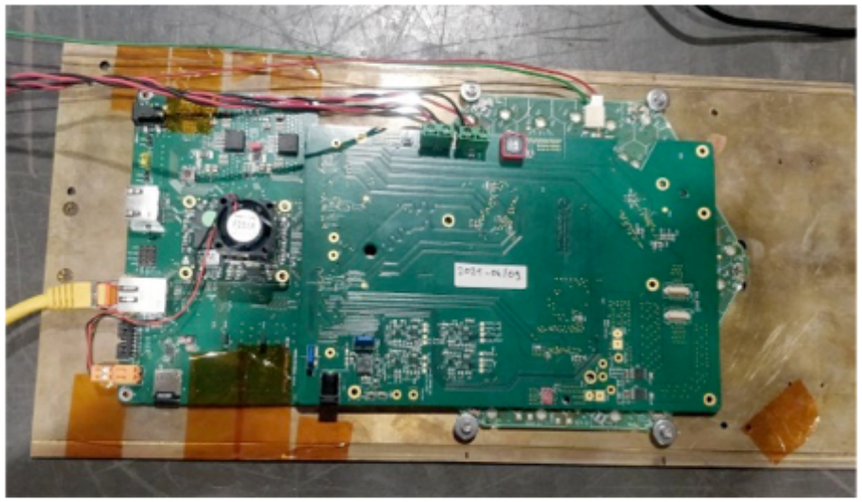

LD Hexaboard



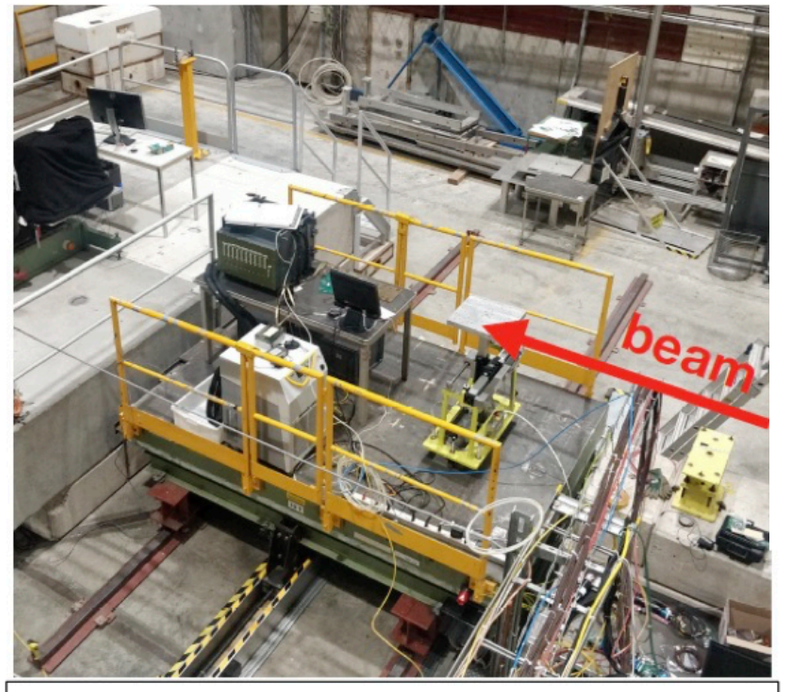



HD Hexaboard

HGCROC3 results from test at CERN SPS H2 beamline



Module and trophy card plus controller on cooling plate

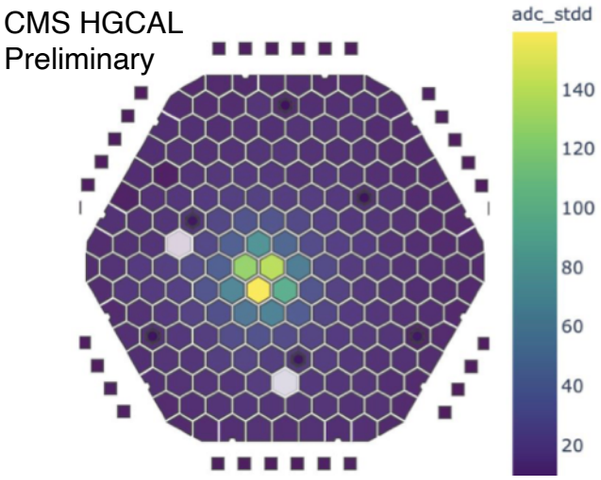


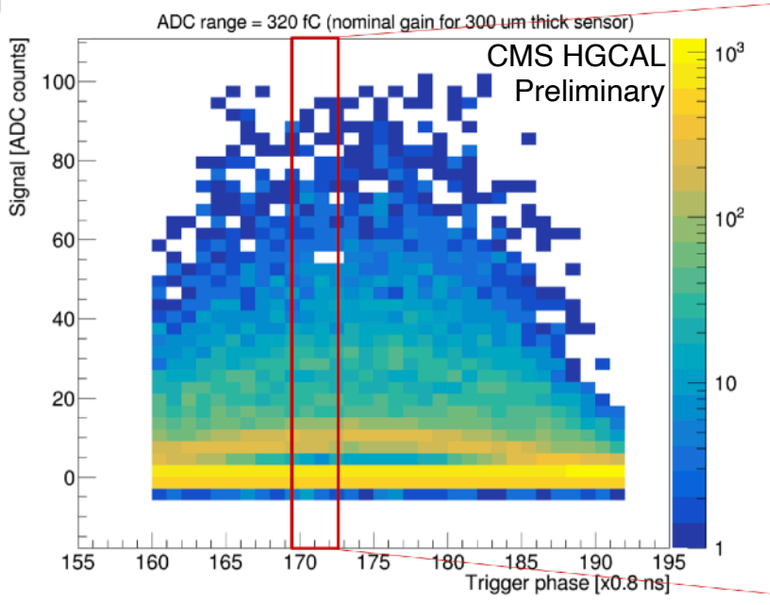
SPS H2 beam area. Device under test mounted in Vienna (cold) Box on a large controllable platform

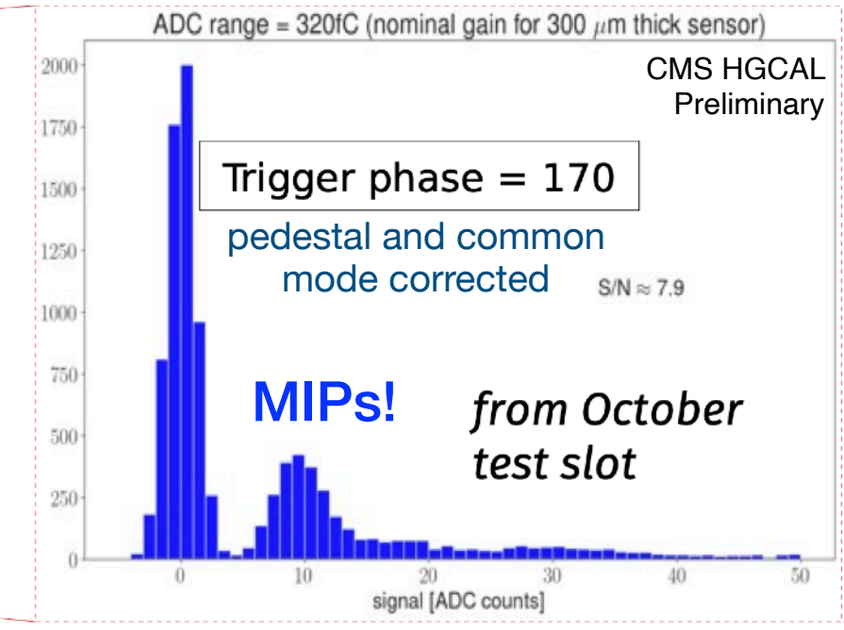
3x HGCROCv3 on module with 300µm Si in 100 GeV electron beam (without absorber)

- MIP signals observed
- S/N as expected

We see the beam!







SPS spill and our DAQ were asynchronous. Phase of the external trigger with respect to the 40MHz was recorded with our data.

ECON = Endcap Concentrator ASIC

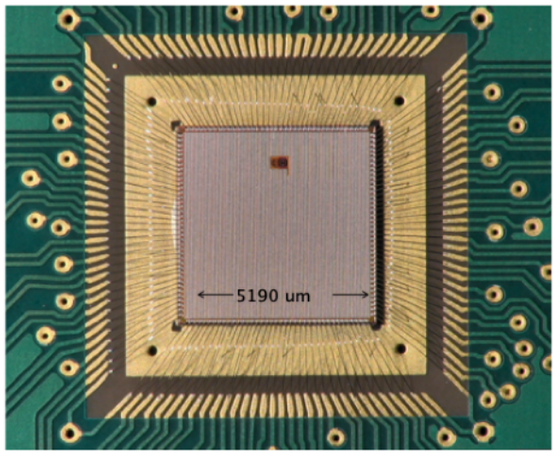
ECONs concentrate data to reduce # links to backend

ECON-D : performs most digital processing of sensor data for events passing L1 trigger at 750 kHz

- zero suppression with programmable corrections
- time-analysis of error conditions to generate reset requests

ECON-T : select or compress HGCROC trigger data for transmission off detector at 40 MHz

Threshold-Sum	Best-Choice	Super-Trigger-Cell	Encoder
Variable-latency Chooses TC above threshold	Fixed-latency Sorts TC by charge Q, sends N with largest Q	Fixed-latency Groups TC and forms larger STCs	Fixed-latency Fully reconfigurable Encodes with CNN

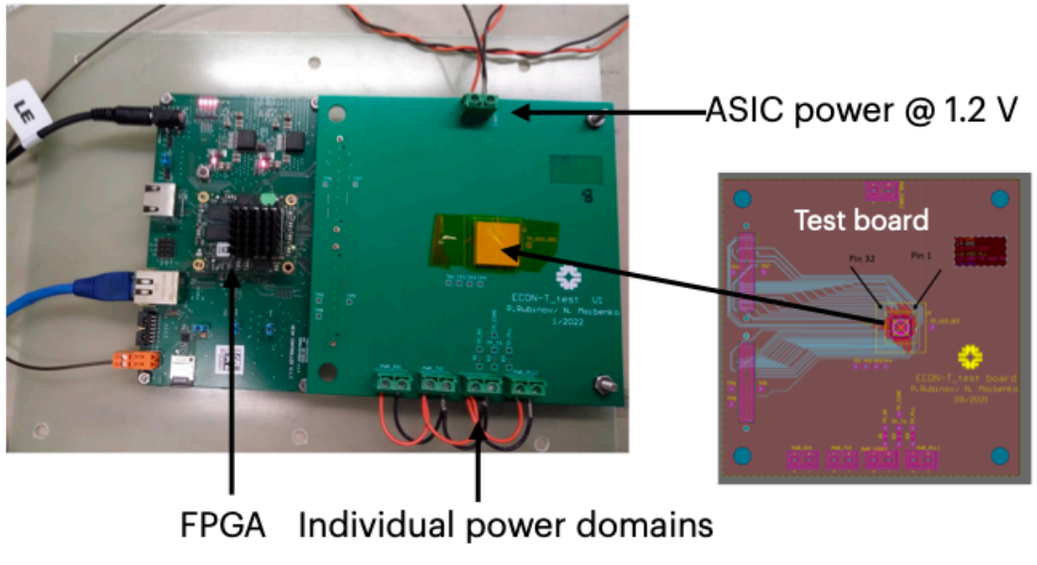


ECON-T-P1 die mounted directly on PCB and wirebonded

First ECON-T-P1 chips received, ~80% functionality tested, no major issues found

First SEE test campaigns completed: Preliminary results indicate excellent performance of configuration registers, no issues requiring human intervention

Chip-on-board @ bench

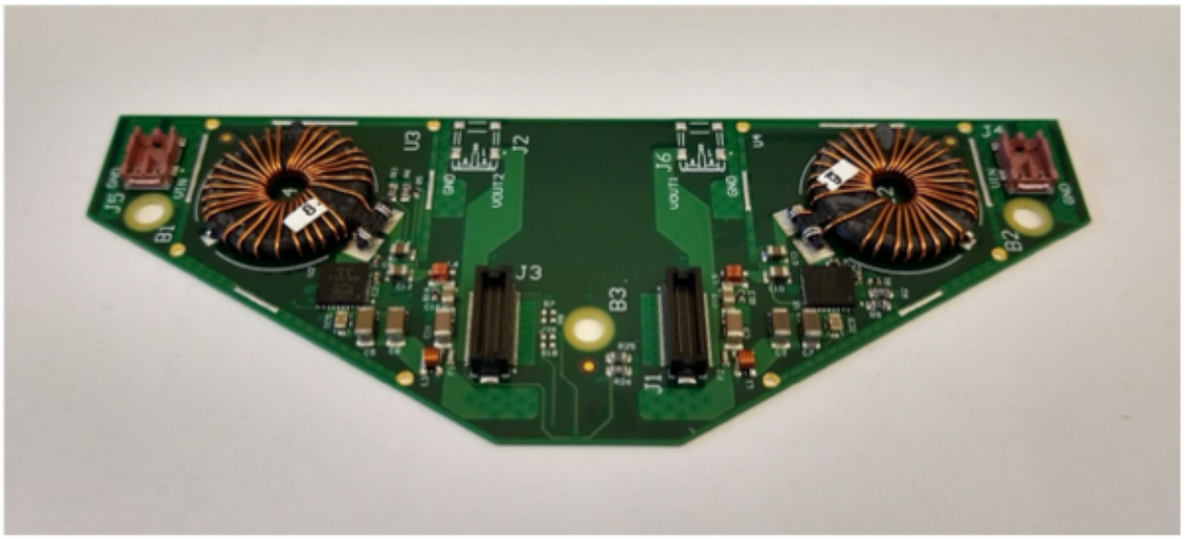


Powering the frontend

Power is delivered in 2 steps via CERN **bpol12V** and HGCAL **LDO**

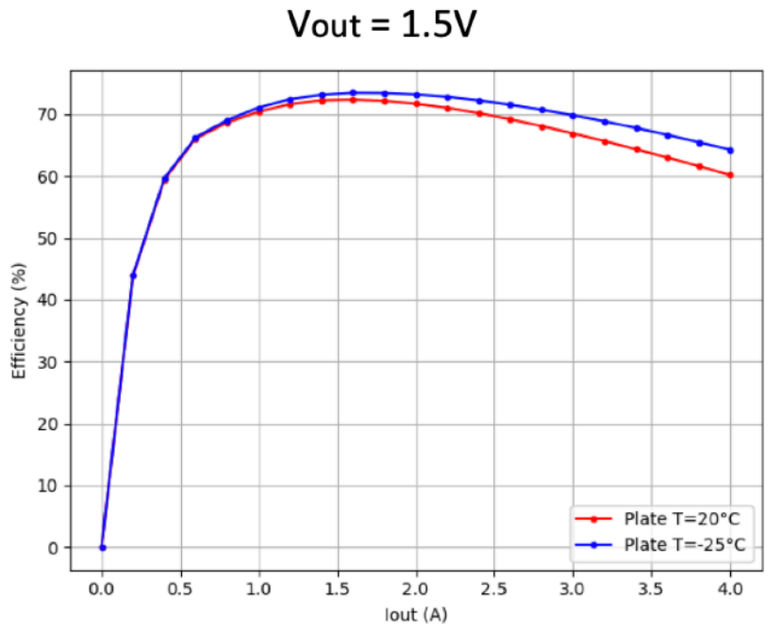
- LD modules: on-board DC/DC mezzanine with bpol12V; LDOs on the hexaboard;
- HD modules: radiation levels too high for bpol12V, they are located on a “deported” module physically in the LD region
- **Custom coil** needed for DC/DC module to fit within tight space constraints
- Point of load regulation; 4 adjustment values of 50mV increments possible as the system ages for LDO

VTRX+ optical power at 2.5V is regulated via CERN **linpol12V**

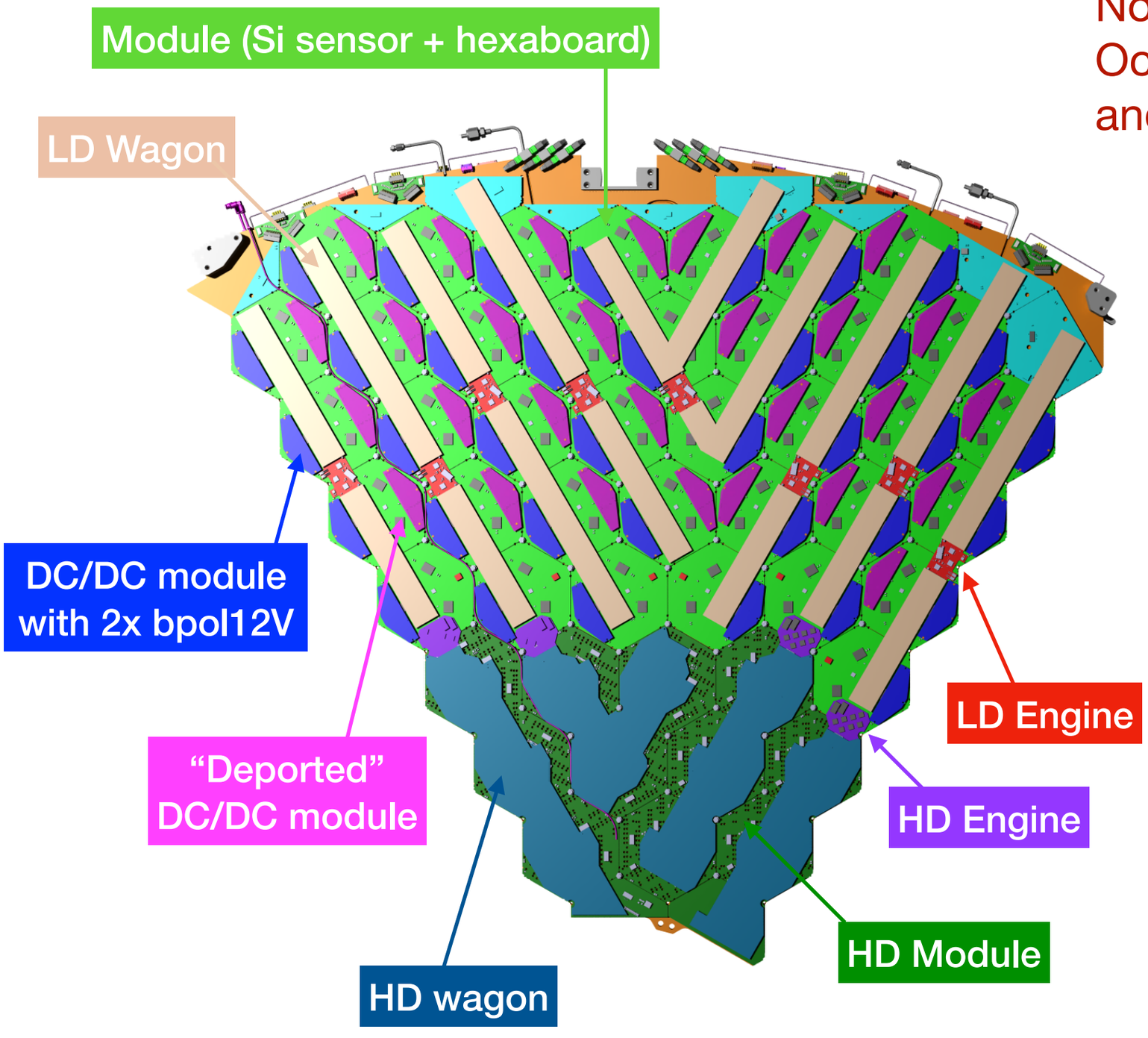


LD bPOL12V module prototype with custom coils

Custom shield with CuNi18Zn20 foil



Modular implementation



Note: each layer is different!
Occupancies vary greatly within and between layers

Readout train = engine + wagon(s)

Engine:
- complex components
- few varieties

Wagons:
- "rigid wires" absorb the geometrical complexities
- many varieties

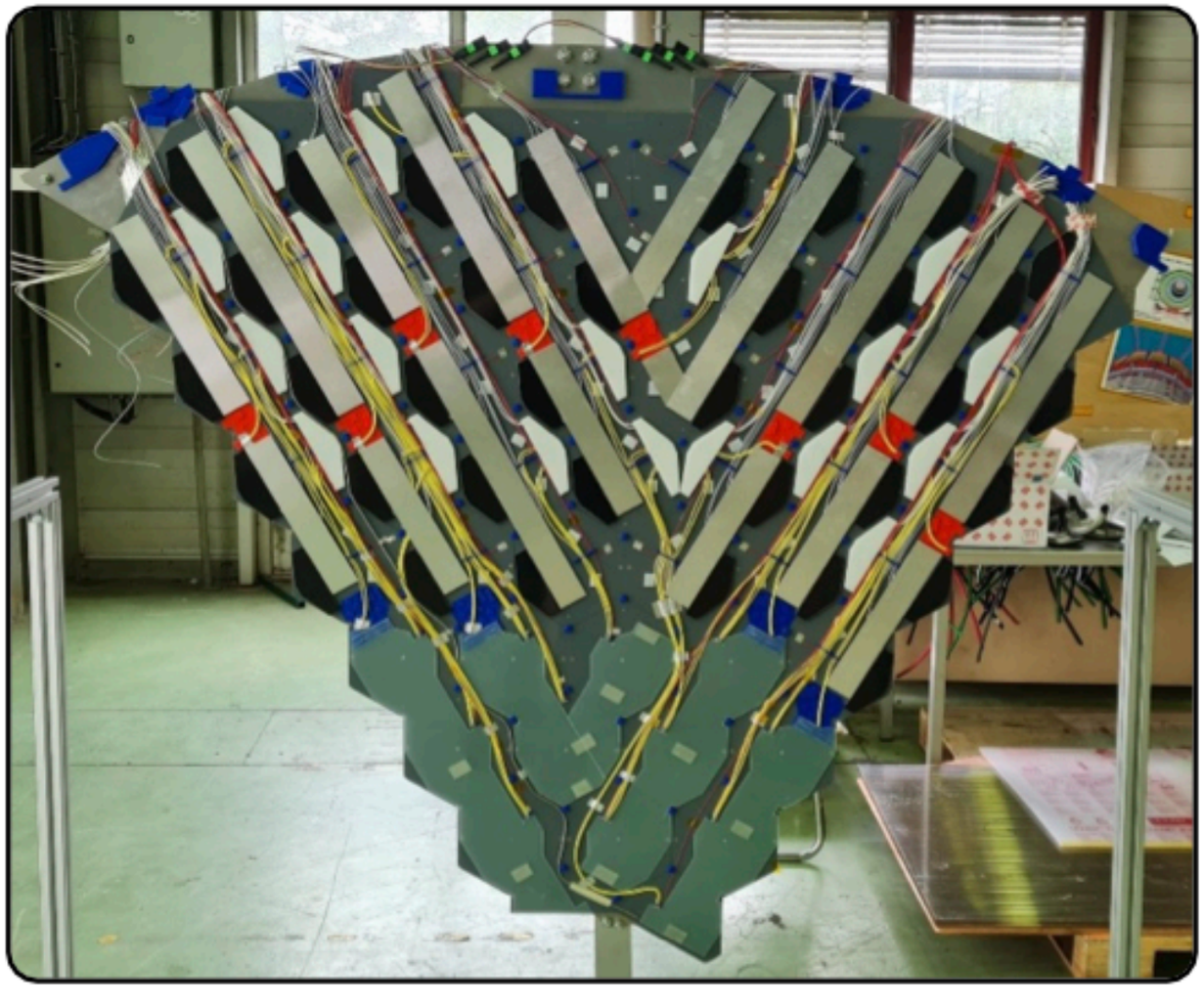
Additional design constraints from need to route services

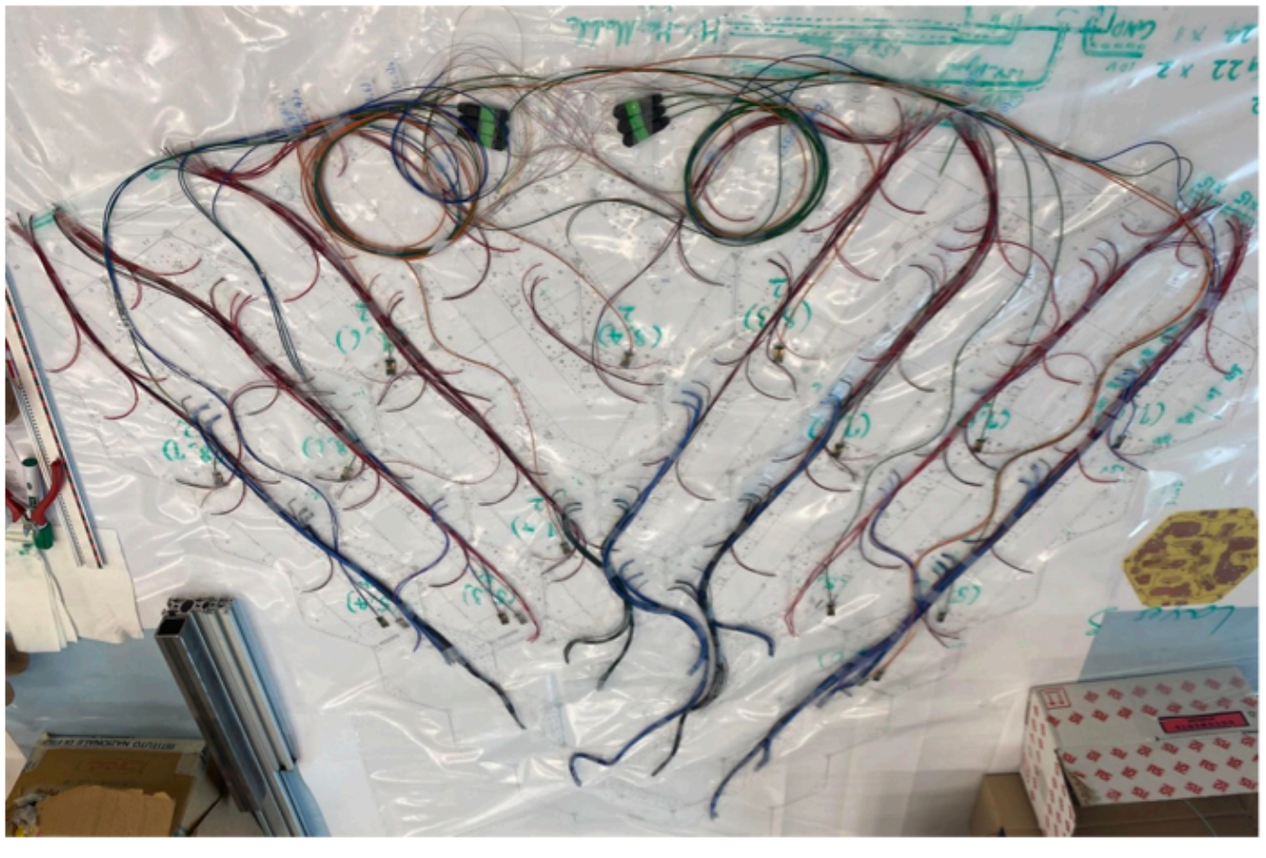
Services challenge

Space is very constrained in the HGCAL detector.

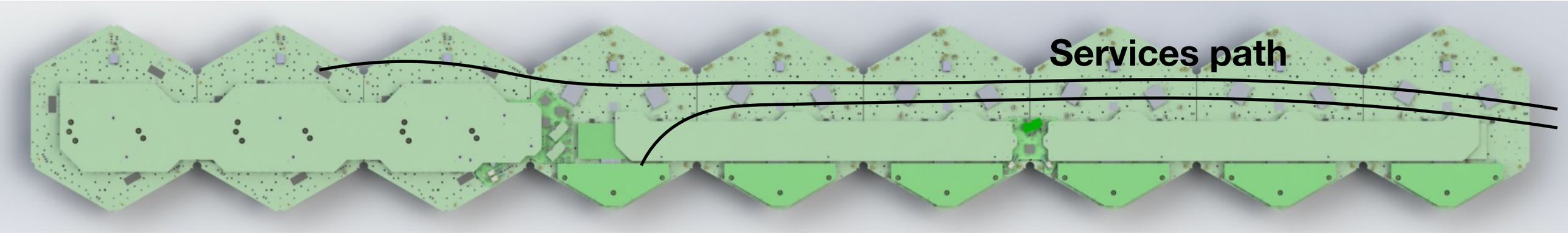
This manifests itself particularly for the services: low voltage wires, bias voltage wires, optical fibers, dry gas tube, …

Wires are hard to model in 3D CAD, so detailed mock-ups are critical

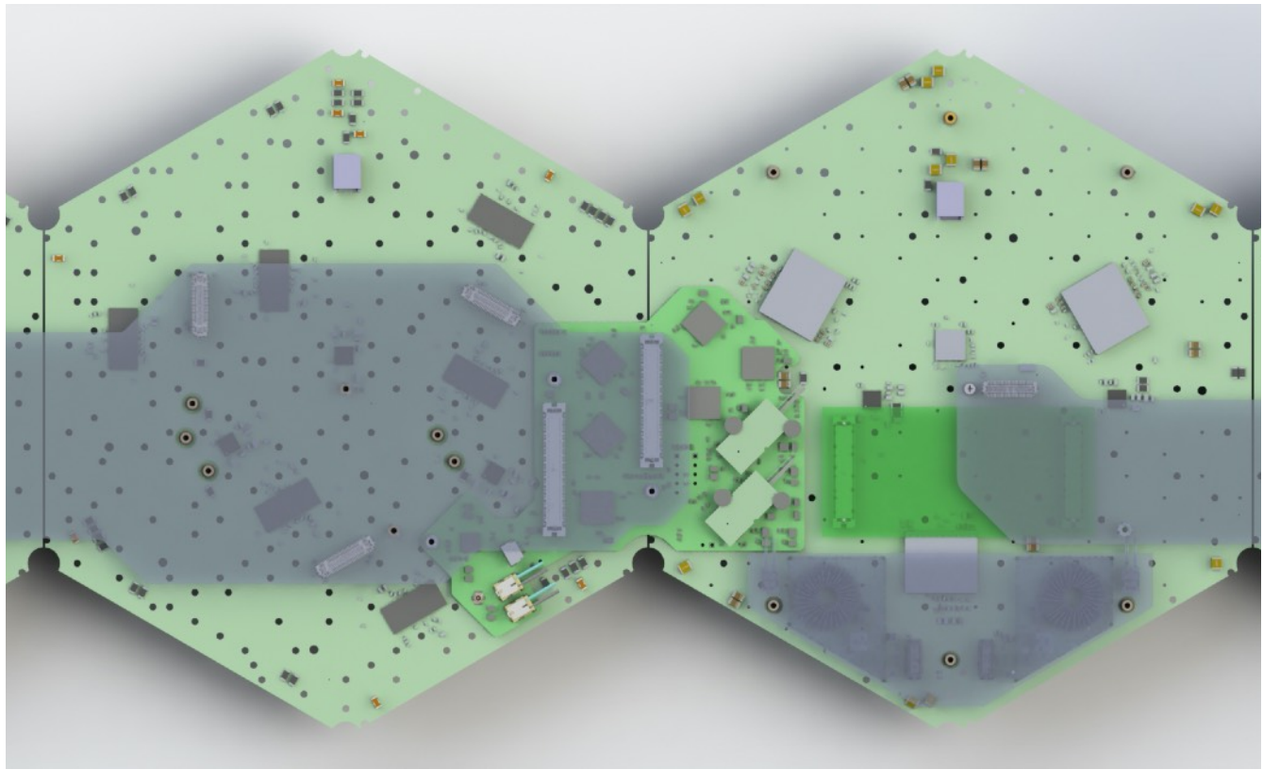




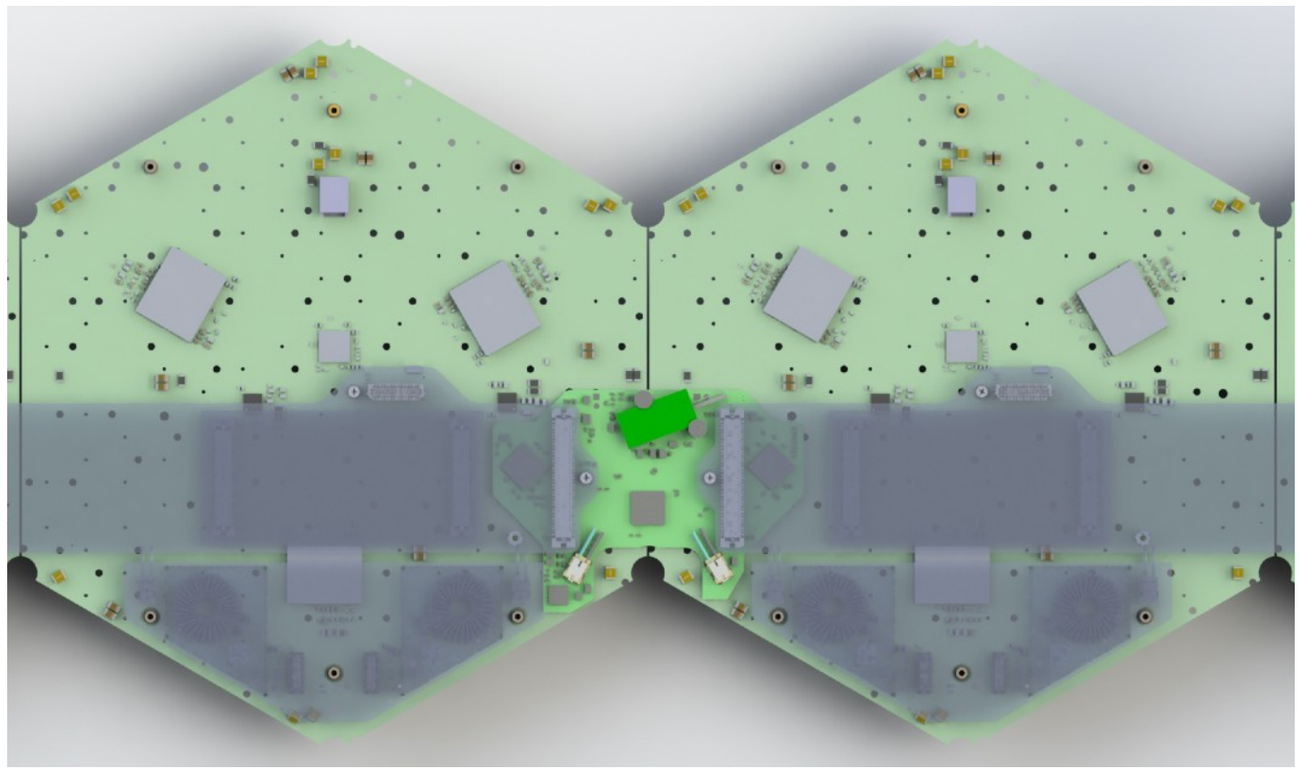
A closer look at the “readout train”



HD region

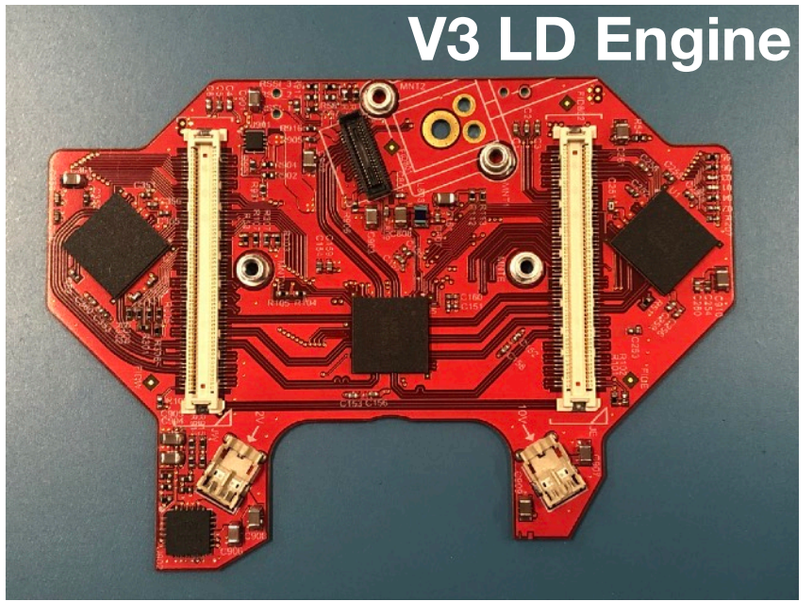


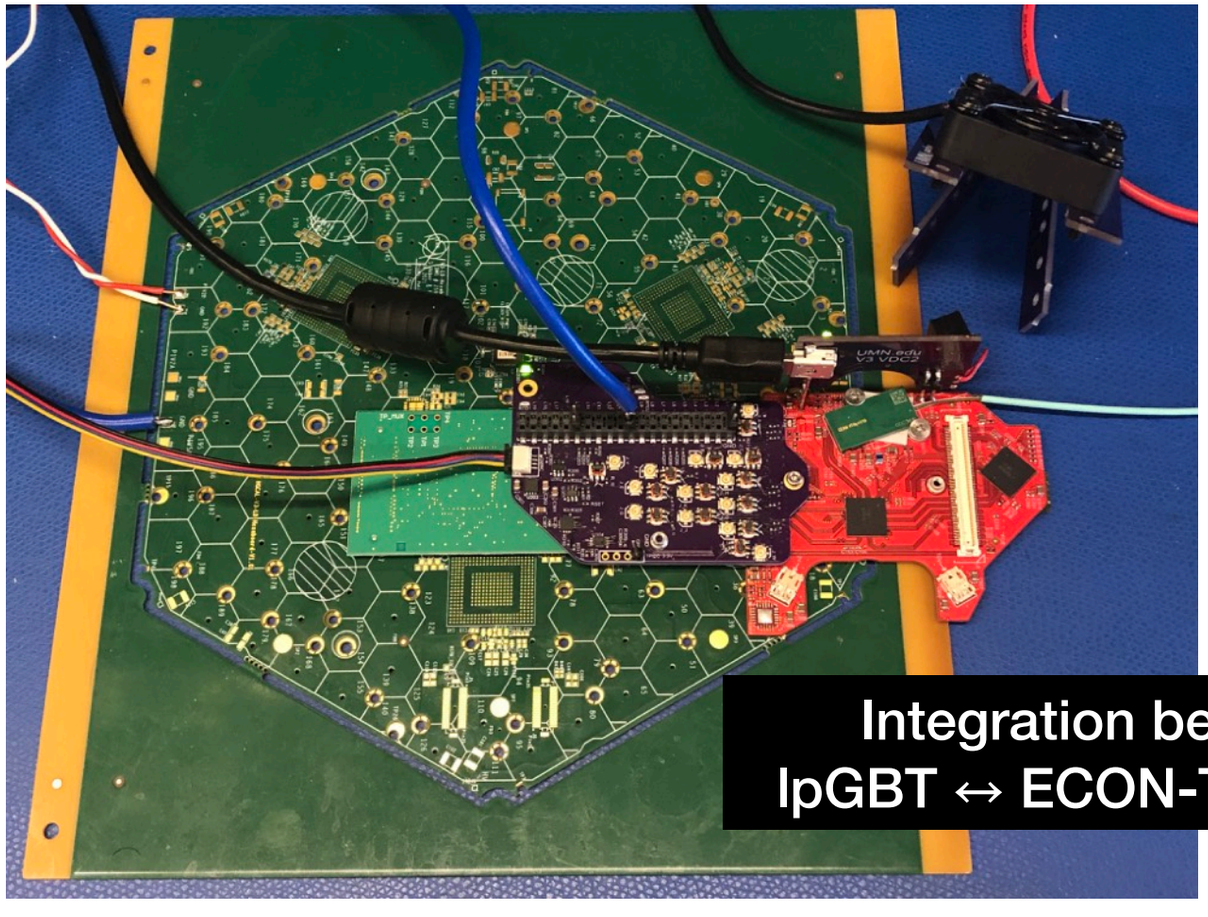
LD region

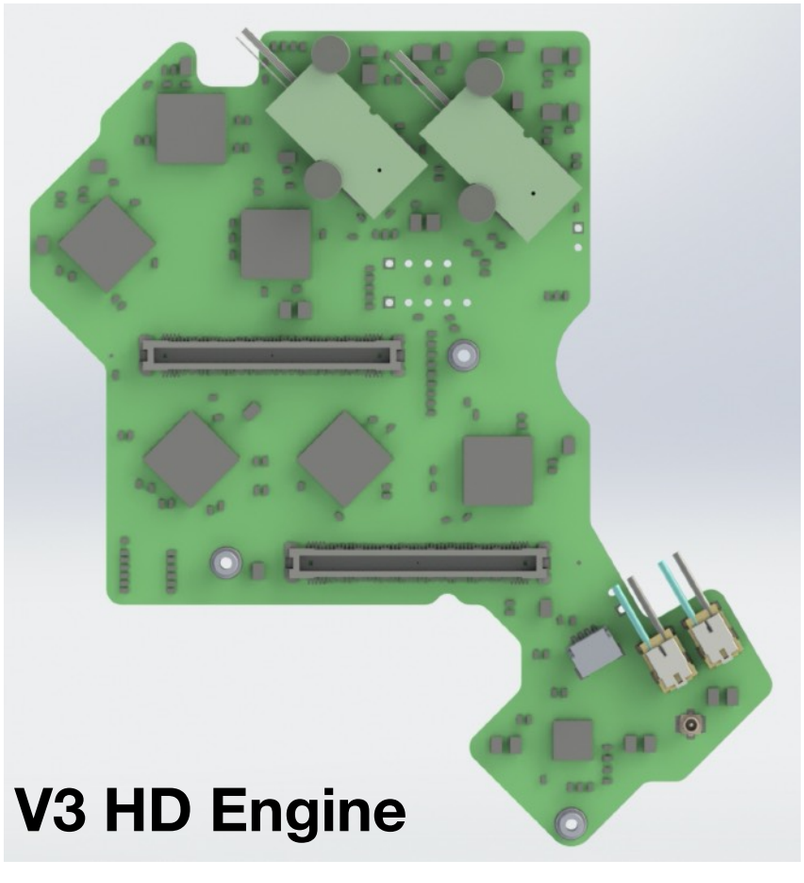


Engine boards

- One LD (HD) engine supports up to 6 LD (3 HD) Full modules
- Uplinks at 10.24 Gb/s, each uplink (i.e. lpGBT) sending DAQ or trigger data from up to 7 elinks from the ECONs at 1.28 Gb/s
- Small, complex board with fine-pitch (0.4-0.5mm) components and dense routing

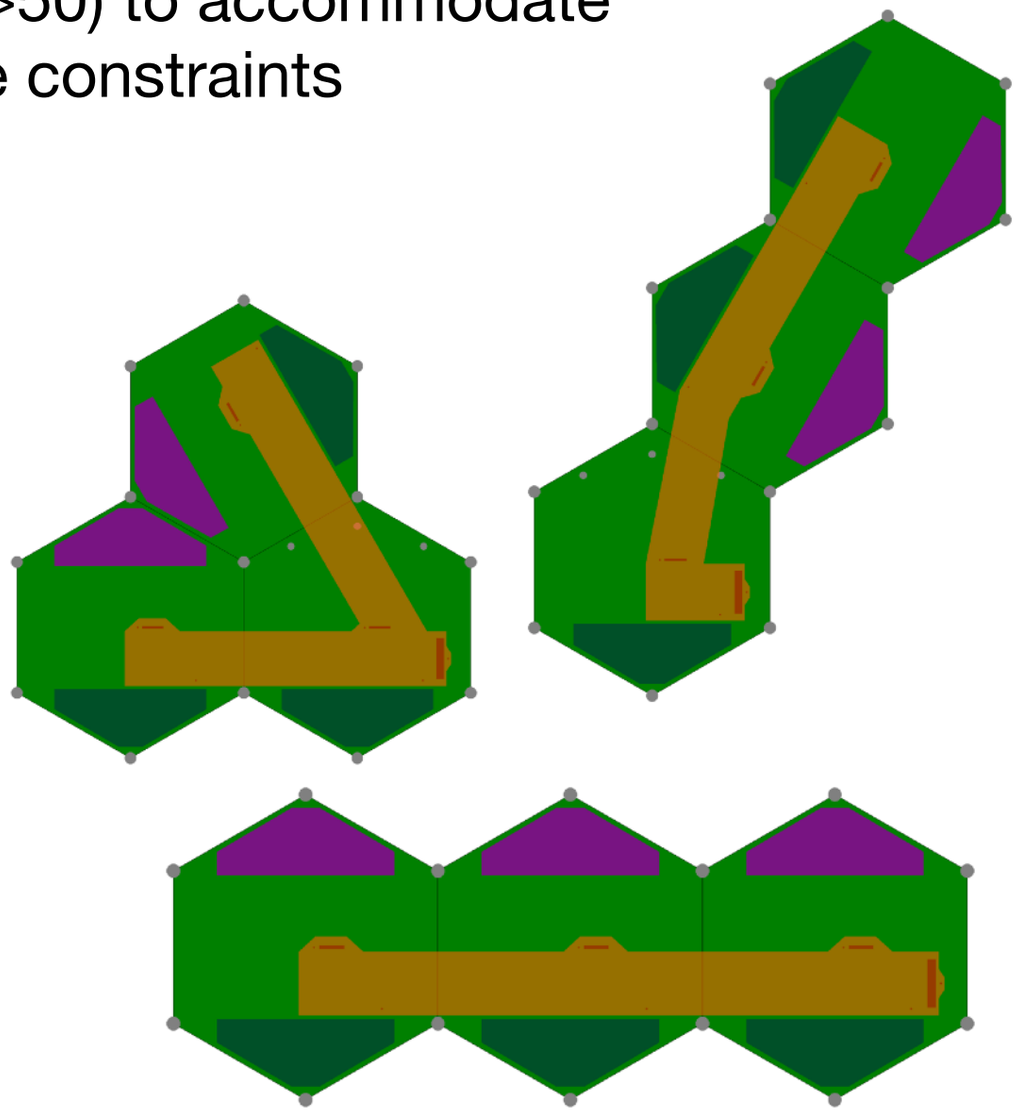




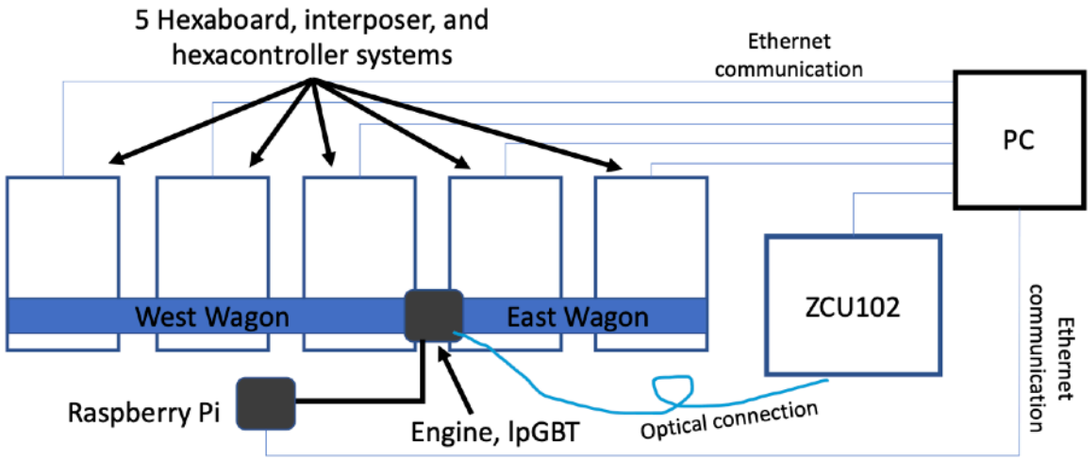


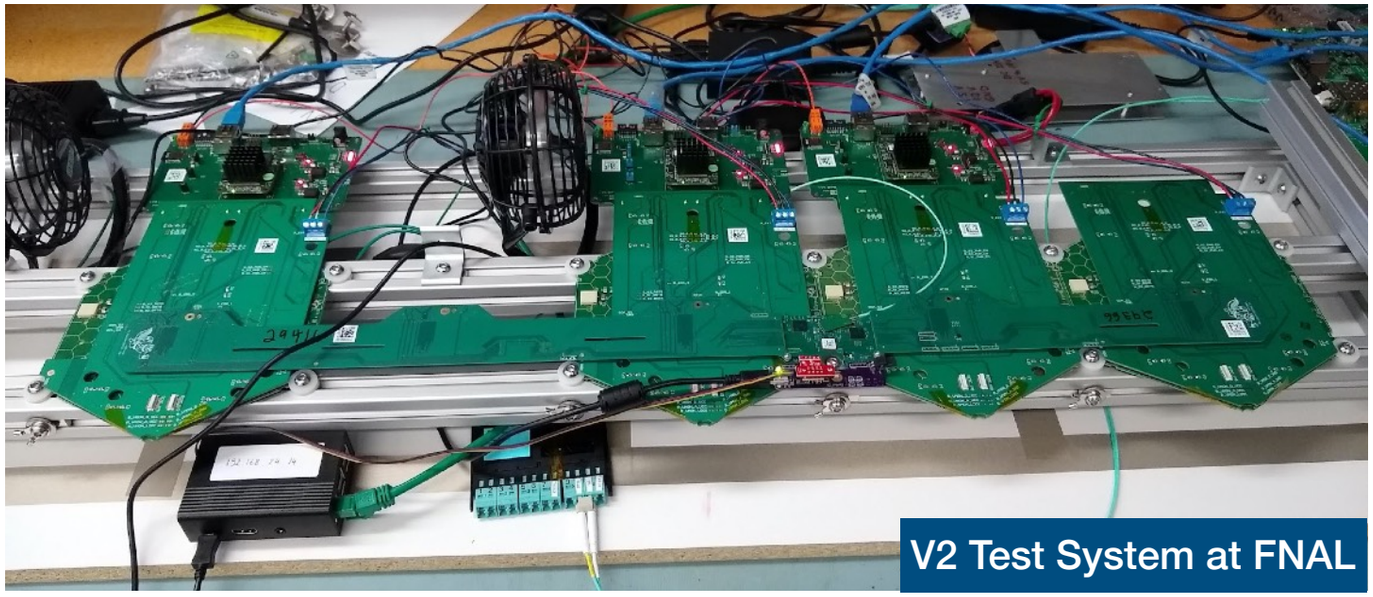
Wagons

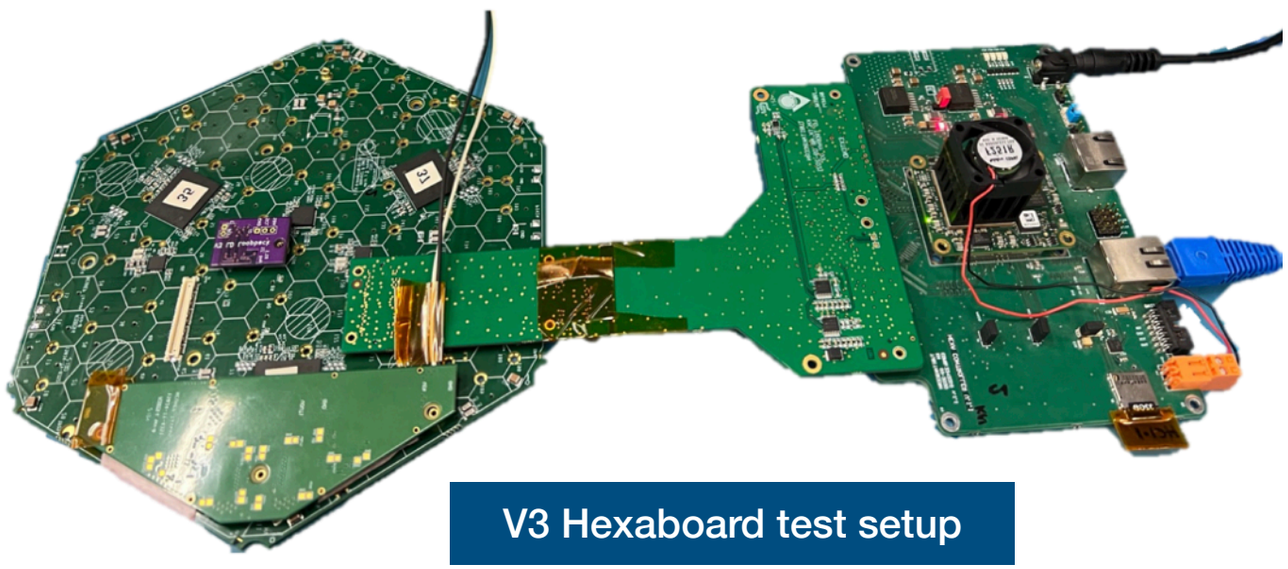
- **Fully passive boards**, connection between modules and engine
  - Main components are the connectors
  - Transfers fast and slow signals, includes AC decoupling between engine and module grounds
- Large boards that come in **many variants** (>50) to accommodate geometrical, bandwidth, and services space constraints
  - Different length
  - Different allocation of e-links per module
  - Straight shape or more irregular
- Developing a **script-assisted design** flow to reduce design time and avoid mistakes
  - Automatically places components
  - Includes “keep-out” areas
  - Interfaces with Altium design tool via text file

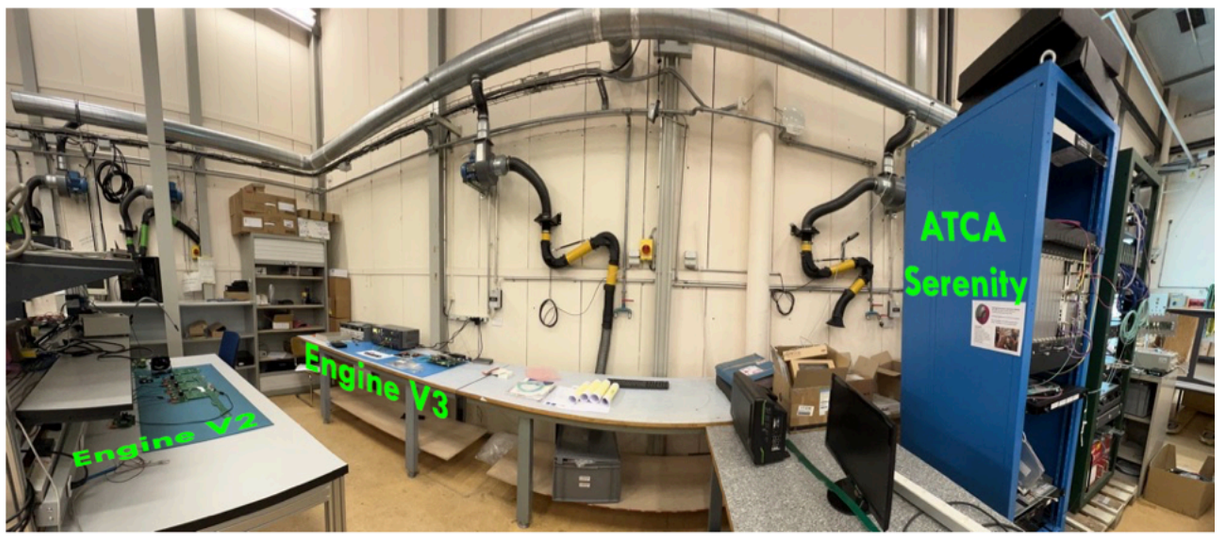


A suite of test systems









HGCAL integration lab at CERN

Backend electronics

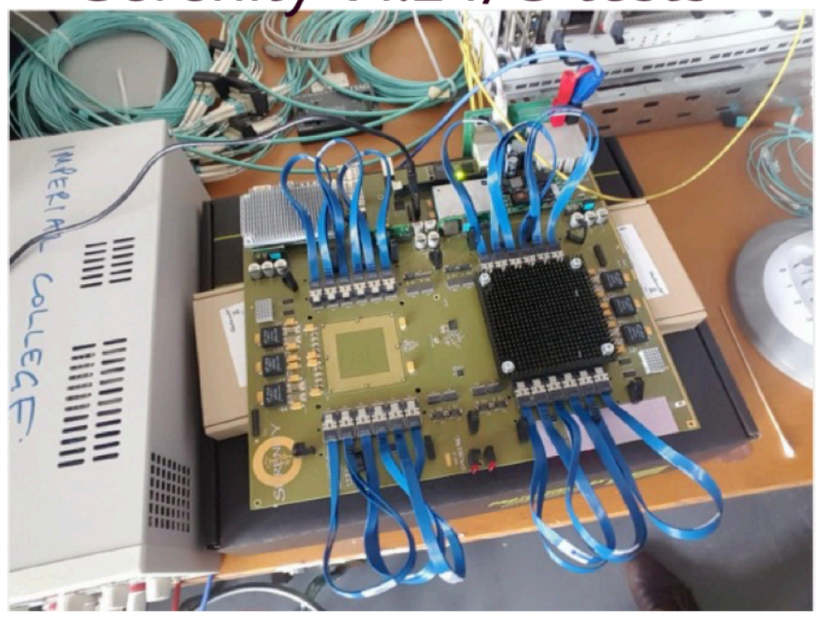
ATCA-based system, using “Serenity” boards

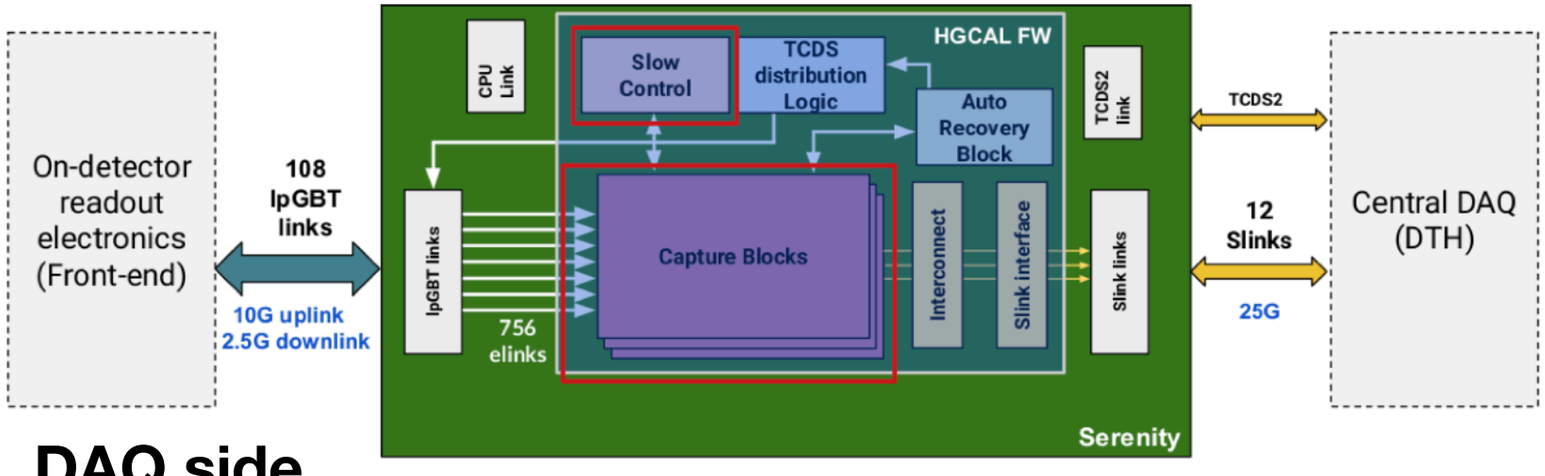
- FPGA of choice is now the larger VU13P to ensure sufficient firmware resources
- DAQ: Bidirectional: send fast command data and control signals to frontend; receive DAQ data from frontend
- TRIG: Receive trigger data from frontend

First FE+BE DAQ truncation and throttling studies under way

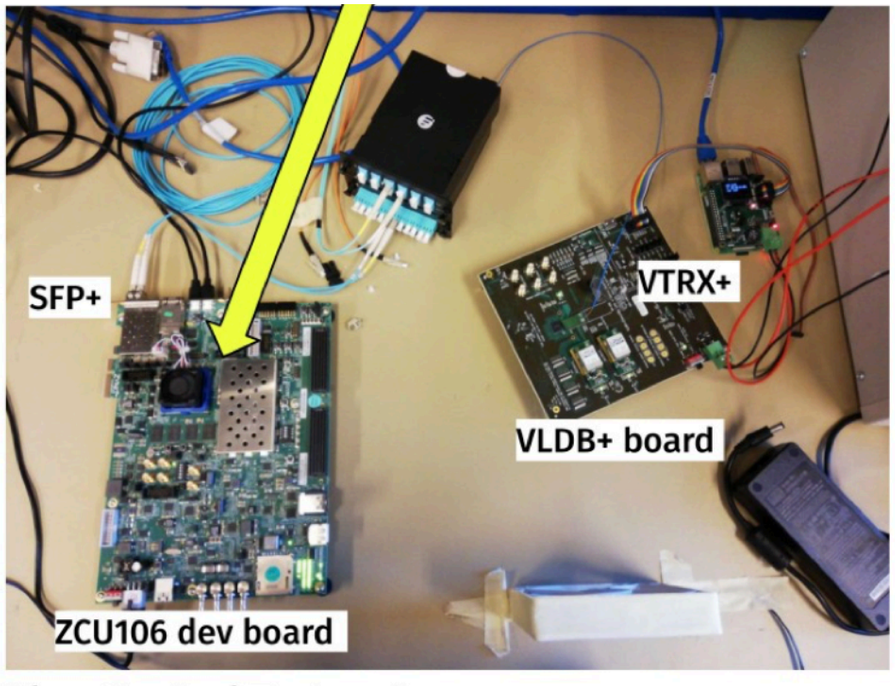
Integration with frontend hardware ongoing

Serenity V1.2 I/O tests





DAQ side



Slow Control Test system

Summary and outlook

- The HGCAL electronics are complex but we are well advanced
- No show-stoppers found in any part of the system, including the challenging custom ASICs, integration of the various boards and services, and the radiation resistance
- **Looking forward to a productive year!**
  - Complete V3 system test with successful data readout from HGCROC, via ECON-T, lpGBT to the backend electronics
  - Do a full-scale cassette integration test with realistic components and cooling plates
  - Produce more varieties of hexaboards, wagons, engines
  - Develop detailed quality control procedures