Status of Timing-SDHCAL Development

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On behalf of SDHCAL Group

CALOR2022 Meeting

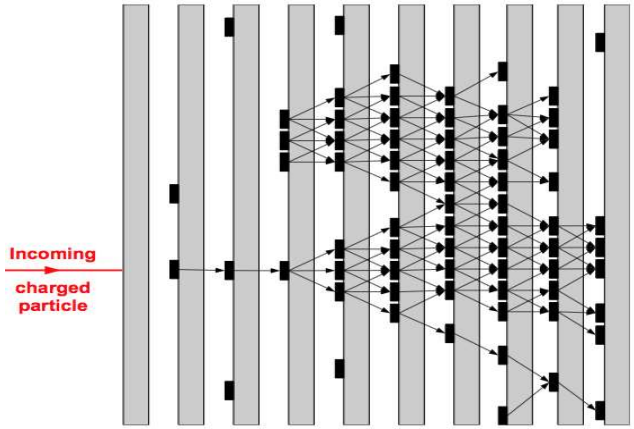
2022/05/20

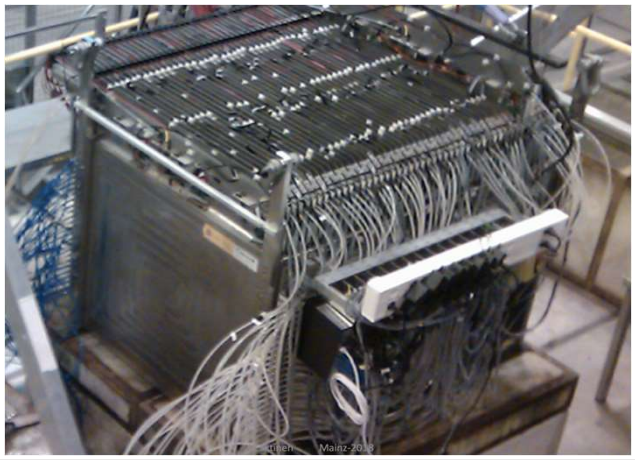
Outline

- Purpose of using timing in SDHCAL
- Detector and electronics upgrade
- Front-end readout ASIC of PETIROC2B
- The front-end Electronics and DAQ Development
- Summary

Semi-Digital Hadronic CALorimeter

- SDHCAL is one of high granularity PFA (Particle Flow Algorithm) calorimeter
  - Connect first hits and then their clusters using distance and orientation information
  - The energy information helps to optimize the connections of hits belongs to the same shower.
- A SDHCAL prototype based on Glass RPC
- Semi-digital readout: hits associated to three different thresholds
  - 1st threshold = 110fC
  - 2nd threshold = 5pC
  - 3rd threshold = 15pC
- 48 layers with GRPC as sensitive medium
- Dimensions: 1m×1m×1.3m

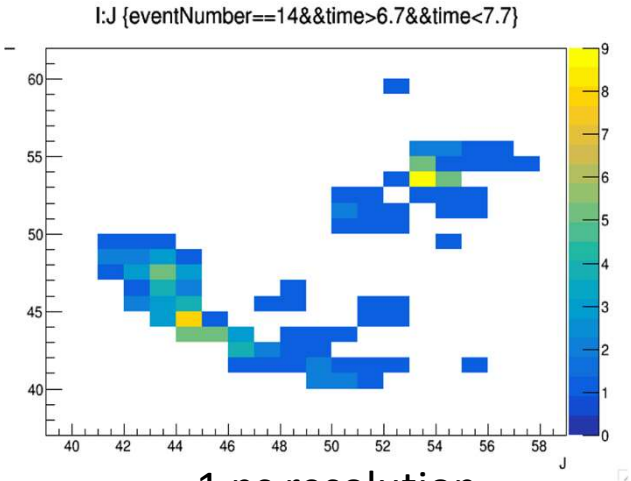




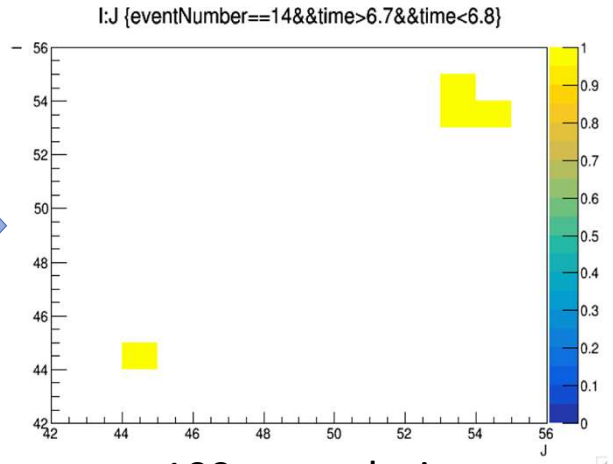
SDHCAL prototype at testbeam in 2015

Motivation of using Timing Information

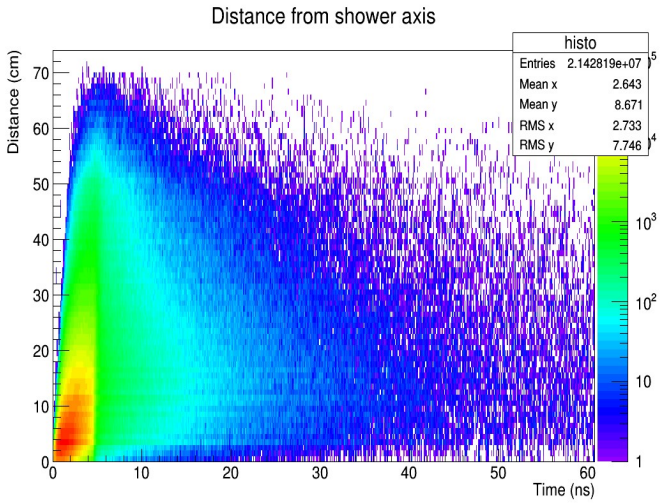
- Timing could be an important factor to identify delayed neutrons.
- Time information can be very helpful to separate close-by showers and reduce the confusion for a better PFA application.

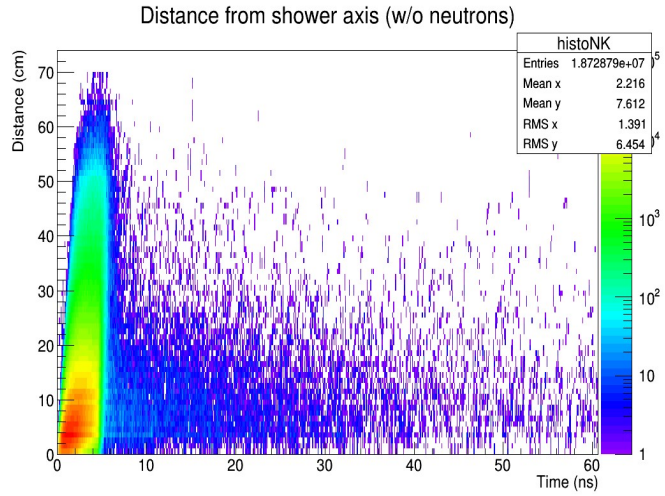


1 ns resolution



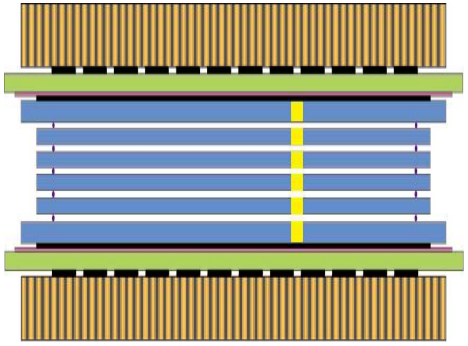
100ps resolution





SDHCAL with Timing Measurement

- Goal: Extending the SDHCAL to include timing information for a **5D-calorimeter (Position, Energy and Timing)**
- Implementation: Building **multi-gap RPC (MRPC)** detectors equipped with a **new version of readout electronics** with high timing performance
  - Timing resolution < 100ps
- The use of MRPC will improve the intrinsic timing of the detector
  - MRPC > 4 gaps



First functionality tests looks promising

Timing Electronics for SDHCAL

HARDROC3B

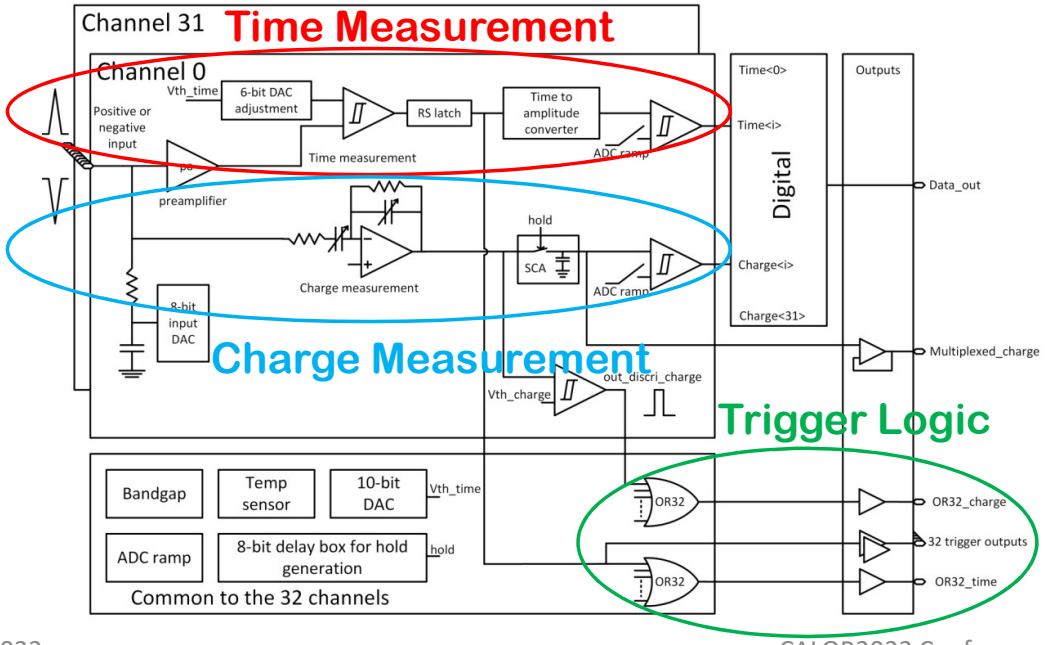
PETIROC2A

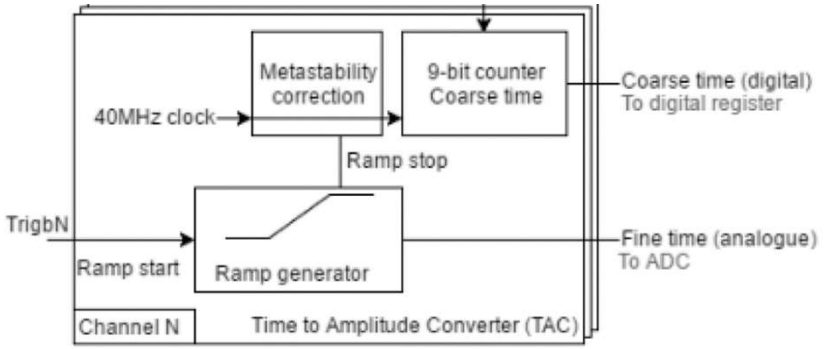
- SDHCAL: electronics based on HARDROC
  - Size: 1m x 1m; cell size: 1cm x 1cm
  - No of channels: 440K
- HARDROC2
  - 64 input channels
  - 3-threshold: 110fC, 5pC, 15pC
  - Not for timing measurement
  - Power consumption: 1mW/chan @ continuous mode; 10 µW/chan @ pulsing mode

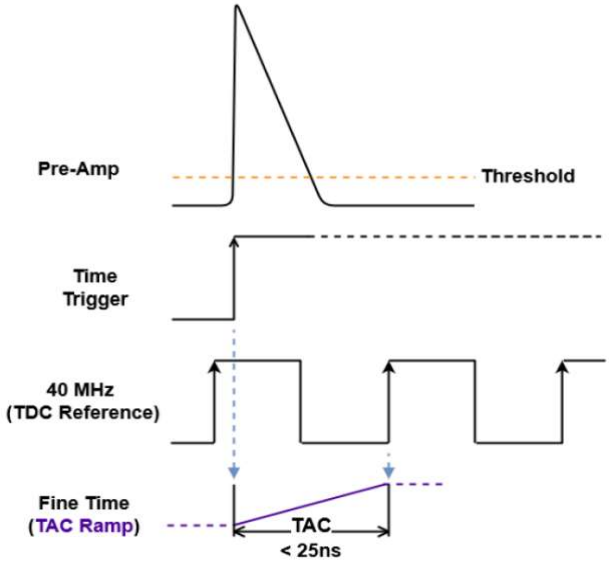
- Time measurement with 10 bits TDC interpolating 40MHz clock
- Timing resolution below 40 ps
- 32 input channels
- charge and time measurement
- Power consumption: ~6mW/channel

FE Readout ASIC: PETIROC

- Timing measurement:
  - fast pre-amplifier + discriminator + TAC + ADC ramp
- 10-bit TDC interpolates 40MHz clock, resolution of ~40ps
- Trigger output for 32-channel
- iRPC detector readout of CMS experiment

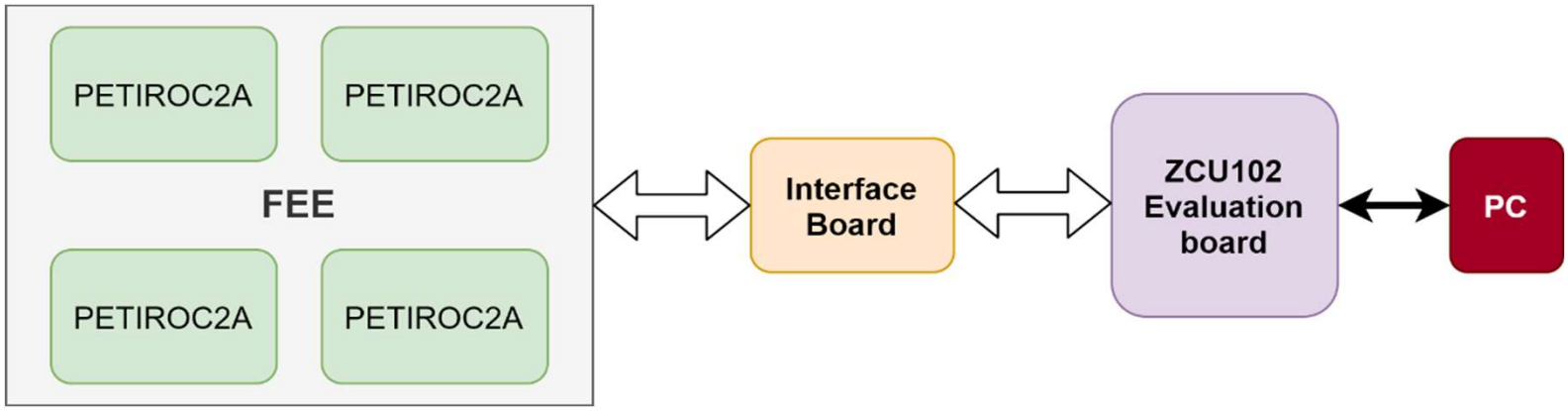






FEE Prototype

- The FEE prototype includes four PETIROC chips, 128 readout pads on the PCB bottom side for MRPC induction signals.
- Detector Interface(DIF) card was designed to connect FEE and FPGA board
  - Data transmission, power rail and clock source.
- The DAQ system should be developed to transfer data between FEE and PC.



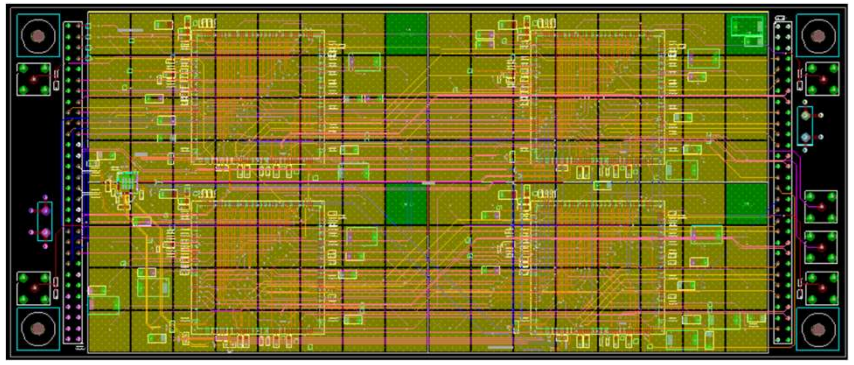
Design of Front-end Board

1		SURFACE	AIR
2	TOP	CONDUCTOR	COPPER
3		DIELECTRIC	FR-4
4	GND1	CONDUCTOR	COPPER
5		DIELECTRIC	FR-4
6	SIG1	CONDUCTOR	COPPER
7		DIELECTRIC	FR-4
8	SIG2	CONDUCTOR	COPPER
9		DIELECTRIC	FR-4
10	GND2	PLANE	COPPER
11		DIELECTRIC	FR-4
12	VDDA	PLANE	COPPER
13		DIELECTRIC	FR-4
14	VDDD	PLANE	COPPER
15		DIELECTRIC	FR-4
16	GND3	PLANE	COPPER
17		DIELECTRIC	FR-4
18	SIG3	CONDUCTOR	COPPER
19		DIELECTRIC	FR-4
20	SIG4	CONDUCTOR	COPPER
21		DIELECTRIC	FR-4
22	GND4	CONDUCTOR	COPPER
23		DIELECTRIC	FR-4
24	BOTTOM	CONDUCTOR	COPPER
25		SURFACE	AIR

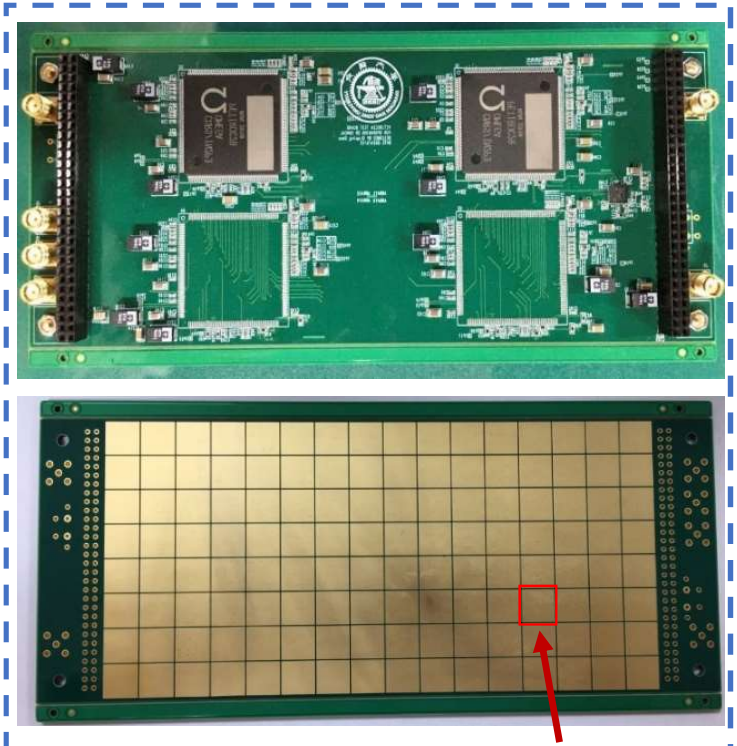
Stack-up and via design

- 12 layers PCB
- Many induction units are at the bottom

- Laser-drilled Via Technology (small size: ~0.1mm) between outside two layers
- Buried Vias with the size 0.3mm

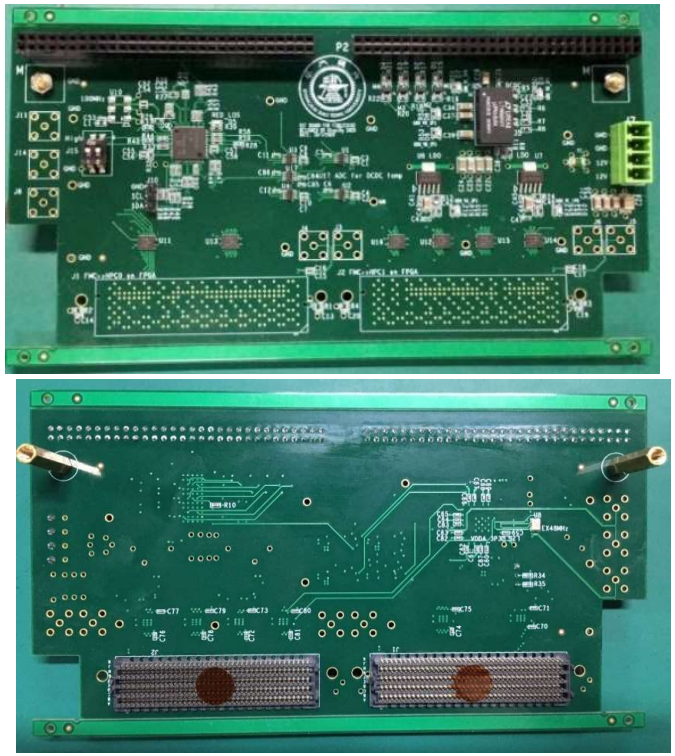


Hardware of Timing Electronics Prototype

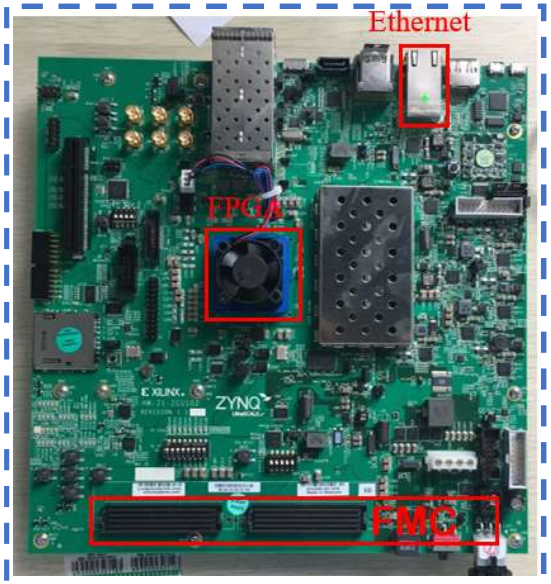


FE Board

128 pads with the cell size 1cm × 1cm

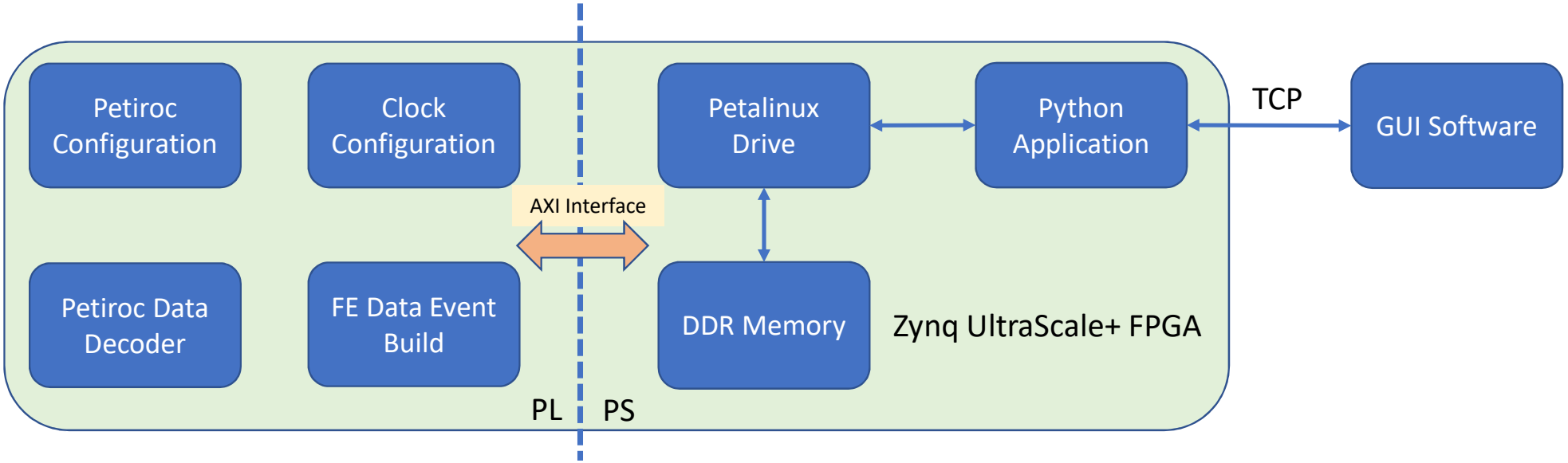


DIF Card



ZCU102

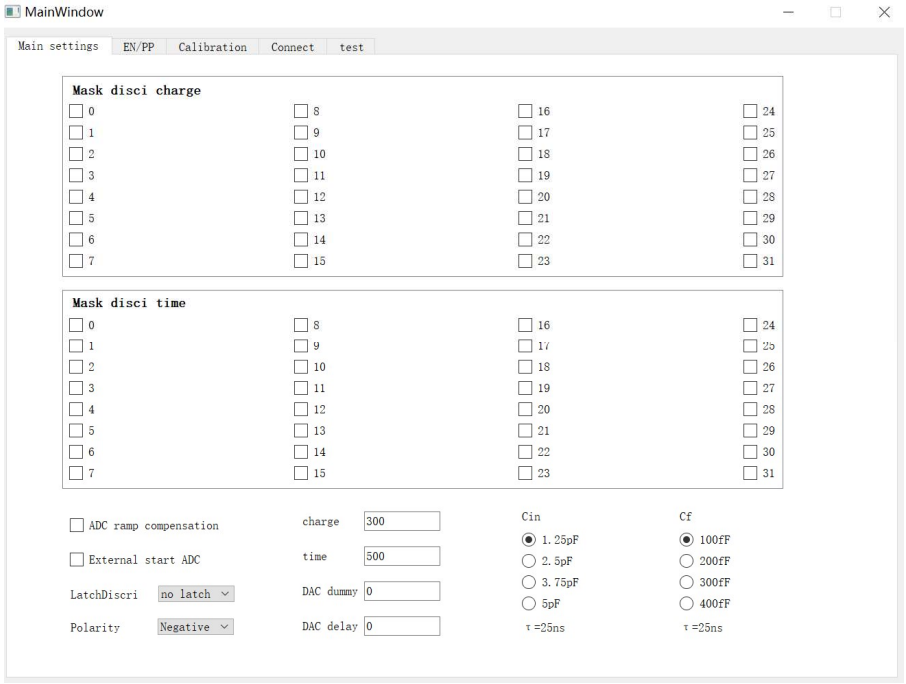
DAQ System



- Front-end interface: Petiroc configuration and data output decoder
- AXI interface between PL and PS, through DDR memory
- The PetaLinux tools allows to customize embedded Linux solutions on Xilinx processing systems.
- Python application access PS memory via linux driver, and communicates with PC via ethernet

DAQ Software

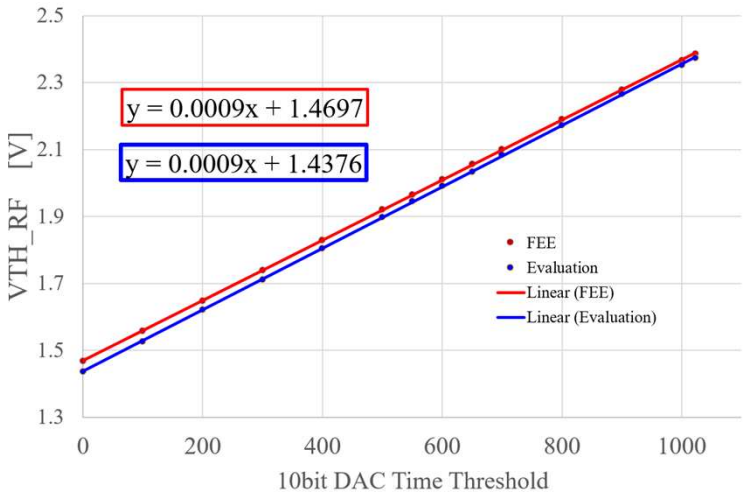
- The DAQ software is a Python GUI application.
  - The GUI is designed via QT designer, which is set of cross-platform C++ libraries that implement high-level APIs.
  - PyQt5 modules binding with QT v5.

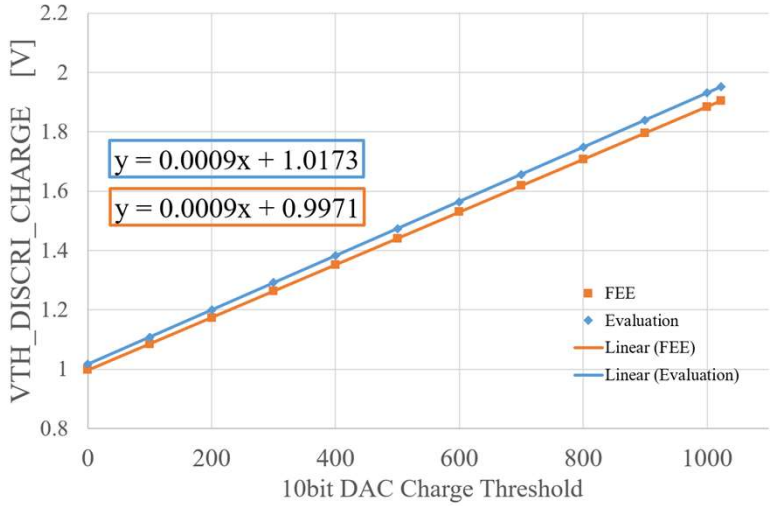


Time and Charge Threshold Voltage Te

Bias Voltage	Value(V)
vref_inpdac	0.989
vref_time	1.664
vref_charge	0.976
vref_tdc	0.133
vref_adc	0.961
vref_time_pad	1.658

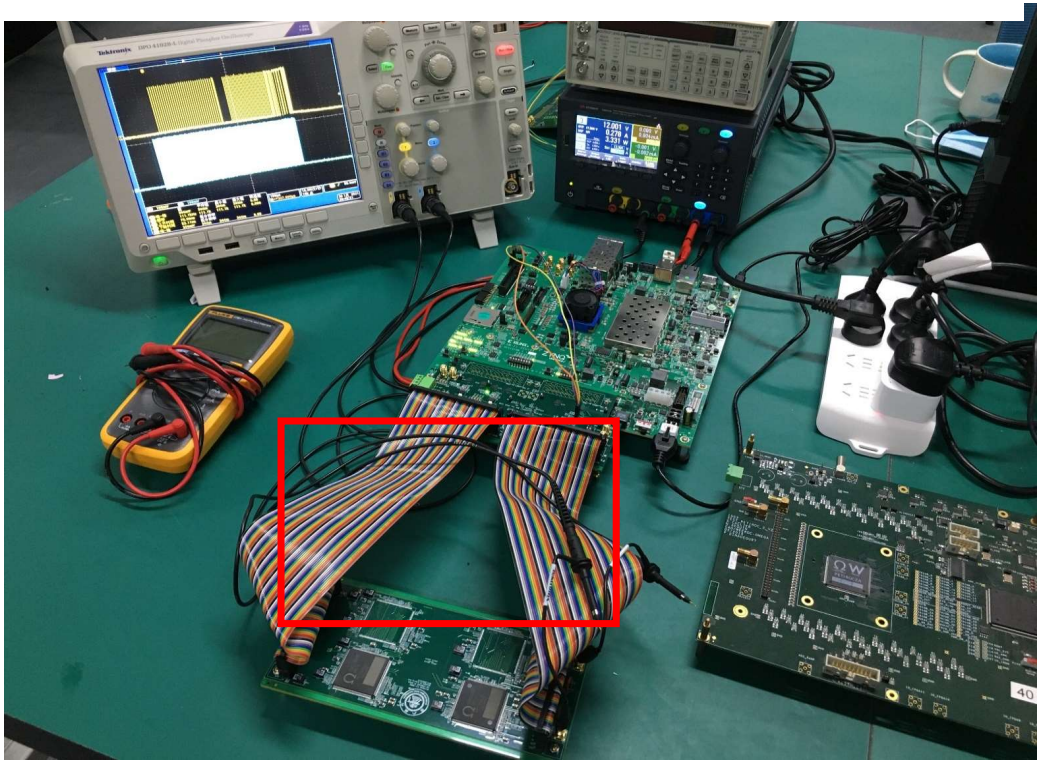
- All of bias voltage values are correct.
- Output data has been checked, after sending trigger signals.
- Time threshold is correct according to the voltage value with 10bit DAC.
- Time and Charge threshold can be well controlled.





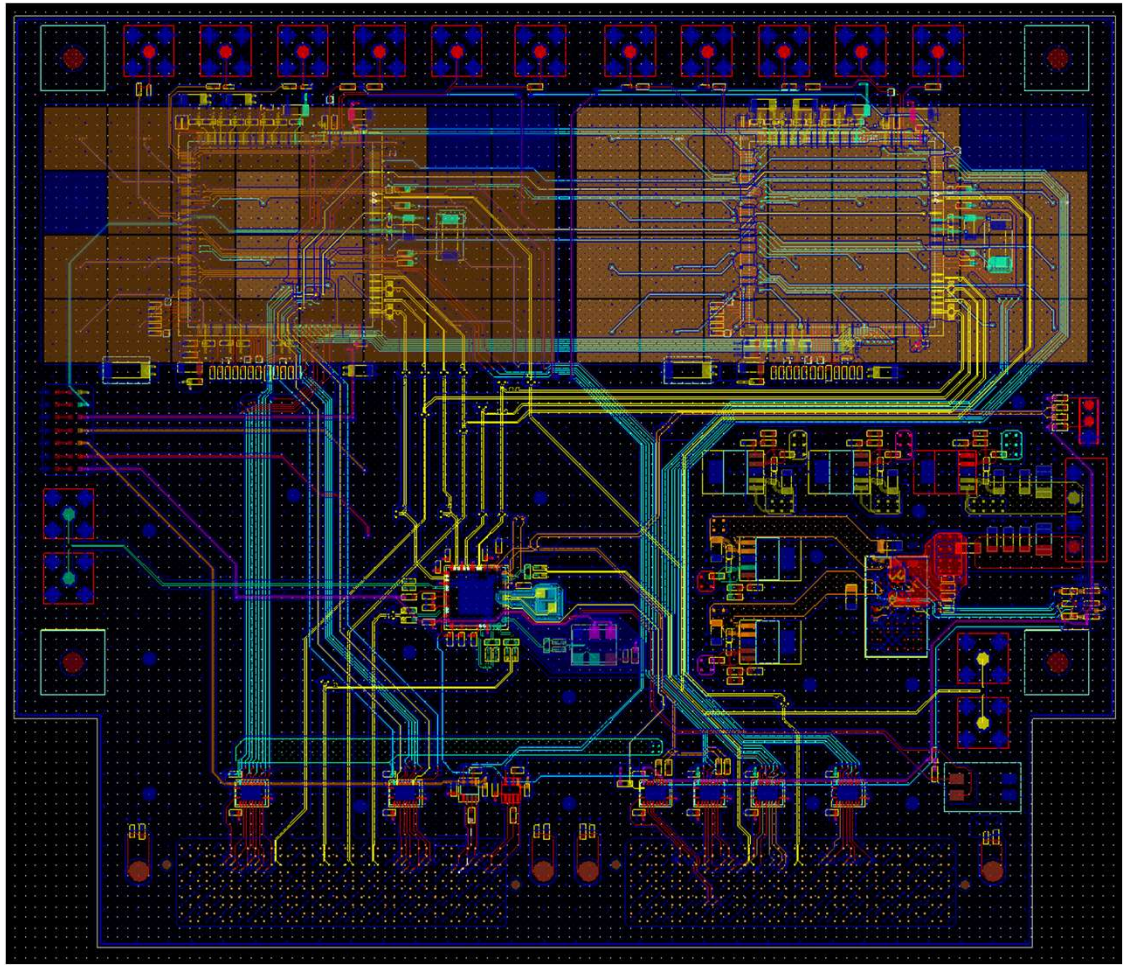
Status of System Test

```
=========================10 bit step============================
Ch0 : 64 Coarsetime: 1100011101, Decode: 100001011 ==> Counter: 267, Hit: 1
Ch1 : 65 Coarsetime: 1000010110, Decode: 111110010 ==> Counter: 498, Hit: 0
Ch2 : 66 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch3 : 67 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch4 : 68 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch5 : 69 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch6 : 70 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch7 : 71 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch8 : 72 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch9 : 73 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch10: 74 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch11: 75 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch12: 76 Coarsetime: 1111100010, Decode: 101011110 ==> Counter: 350, Hit: 0
Ch13: 77 Coarsetime: 1001011110, Decode: 111001010 ==> Counter: 458, Hit: 0
Ch14: 78 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch15: 79 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch16: 80 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch17: 81 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch18: 82 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch19: 83 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch20: 84 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch21: 85 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch22: 86 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch23: 87 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch24: 88 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch25: 89 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch26: 90 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch27: 91 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch28: 92 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch29: 93 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch30: 94 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
Ch31: 95 Coarsetime: 1100010101, Decode: 100001100 ==> Counter: 268, Hit: 1
```



- Crossstalk exists in the injection test!

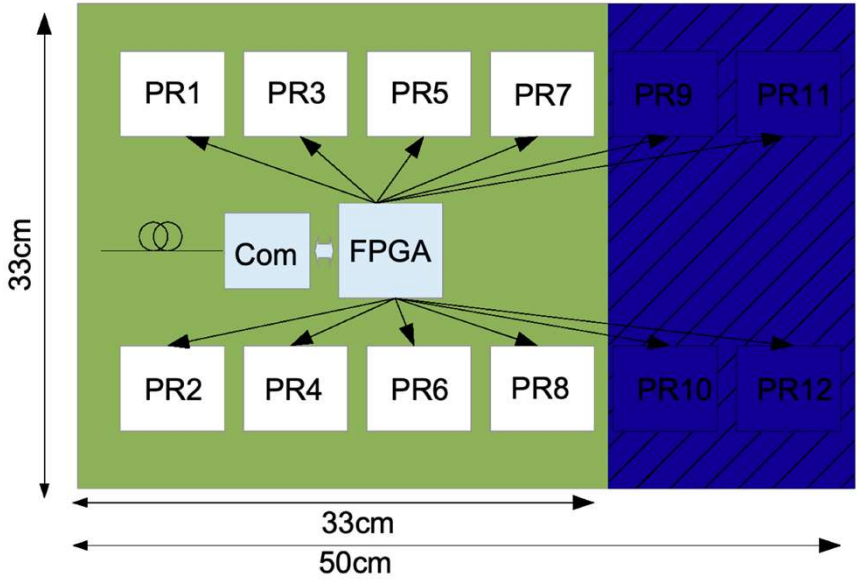
New version of FE Hardware

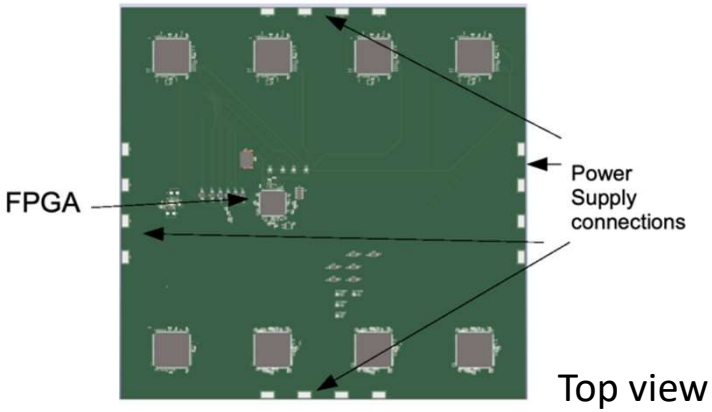


- Scheme: two Petiroc chips + clock chips + power chips + FMC connector
- Purpose: test Petiroc timing measurement performance
- Remove jump cables to reduce noise and crosstalk.
- Schematic and layout design has been finished, will be fabricated soon.

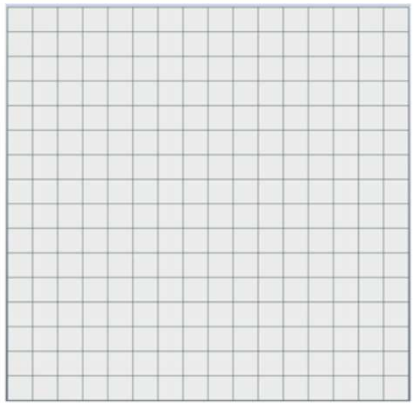
Toward Larger prototypes

- Board with 8 (could be extended to 12) Petircoc2B ASICs
- Pads 2cm x 2cm, 256 channels
- Local FPGA (Xilinx Spartan-6 TQFP) embedded on board





Top view



Bottom view

Summary

- Timing information helps to identify neutrons and separate close-by showers.
- MRPC detector is being built, which has an improved timing performance.
- A front-end prototype and a interface card has been designed and tested.
- The Xilinx ZCU102 board is used as the DAQ system.
  - The firmware and software of DAQ system has been developed.
- A new version of hardware has been designed, and will be fabricated soon.
- A larger prototype is being developed simultaneously.

Introduction of PETIROC chip

- Time measurement with 10bits TDC interpolating 40MHz coarse time
- Charge measurement (Q>50fC) with 10bits DAC
- Voltage input amplifier, 200Ohm matching
- High bandwidth preamp (GBWP> 1.2 GHz)
- PETIROC parameters:
  - One chip with 32-channels and mixed analog/digital
  - The 32chs input connected with PAD (detector unit)
  - One channel split into two parts, respectively for charge and time
  - Internal DAC for each channel to adjust the amplitude of the input signal
  - Lower power consumption (~6mW/channel)
  - Jitter ~18 ps RMS on trigger output (4 photoelectrons injected)

Embedded design based on FPGA -- UART

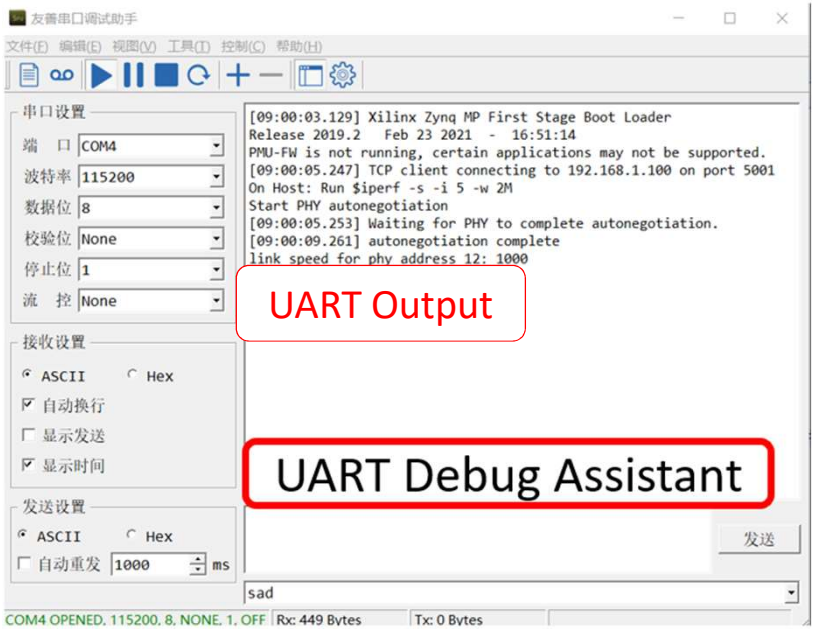
- The embedded design in ZCU102(PS side) mainly contains serial port communication(UART), ethernet communication(TCP/IP) and PETIROC configuration(Slow Control).

- UART test in PS side:
  - Hardware only needs Processing System part on ZCU102.
  - Write the C/C++ code and run on the hardware platform.
  - Information is printed on the tool window through UART port.

```c
#include <stdio.h>
#include <string.h>

#include "lwip/err.h"
#include "lwip/tcp.h"
#include "lwipopts.h"
#include "xil_cache.h"
#include "xil_printf.h"
#include "sleep.h"

#define TX_SIZE 102

static struct tcp_pcb*connected_pcb = NULL;
unsigned client_connected = 0;
//Static Global Function, blind for external file
uint tcp_trans_done = 0;

//u_char data[TX_SIZE] = {0, 1, 2, 3, 4, 5, 6, 7, 8, 9};
u_char data[TX_SIZE] = "Hello World! Successfully Send Word From PS Client";

int send_data()
{
    err_t err;
    struct tcp_pcb *tpcb = connected_pcb;

    if (!tpcb)
        return -1;

    //判断发送数据长度是否小于发送缓冲区剩余可用长度
    if (TX_SIZE < tcp_sndbuf(tpcb)) {
        //Write data for sending (but does not send it immediately).
        err = tcp_write(tpcb, data, TX_SIZE, 1);
        if (err != ERR_OK) {
            xil_printf("txperf: Error on tcp_write: %d\r\n", err);
            connected_pcb = NULL;
            return -1;
        }

        //Find out what we can send and send it
        err = tcp_output(tpcb);
        if (err != ERR_OK) {
            xil_printf("txperf: Error on tcp_output: %d\r\n",err);
            return -1;
        }
```

PS code

1



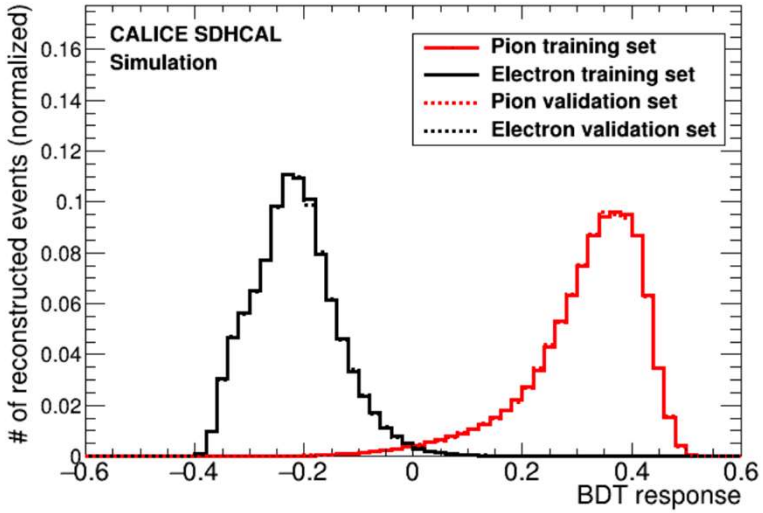
UART communication test

Particle Identification using BDT

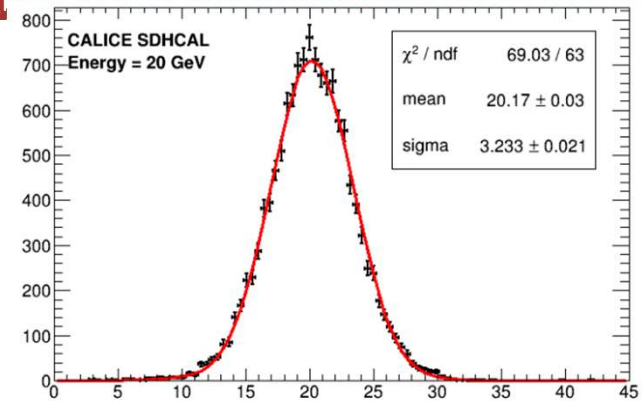
- PS and SPS testbeam at CERN in 2015
  - PS beamline: 3, 4, 5, 6, 7, 8, 9, 10, 11 GeV
  - SPS beamline: 10, 20, 30, 40, 50, 60, 70, 80 GeV
  - Contamination particles: eletrons and muons

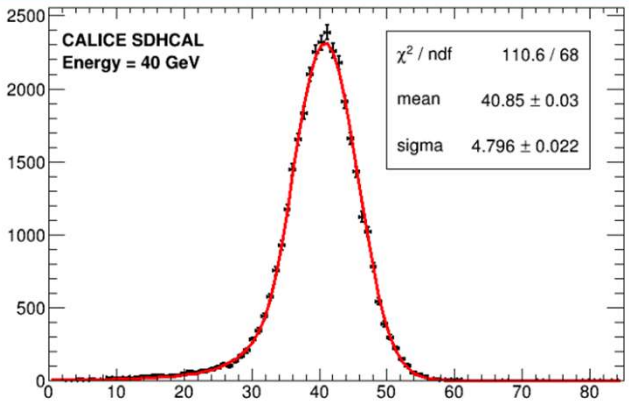
https://arxiv.org/pdf/2202.09684.pdf

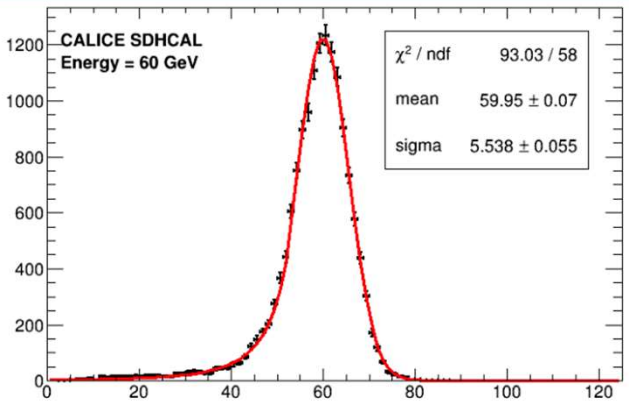
- A testbeam data analysis draft recently has been submitted to Jinst.
  - Use BDT to reject electron background from pion samples in the energy range of 10 to 80 GeV

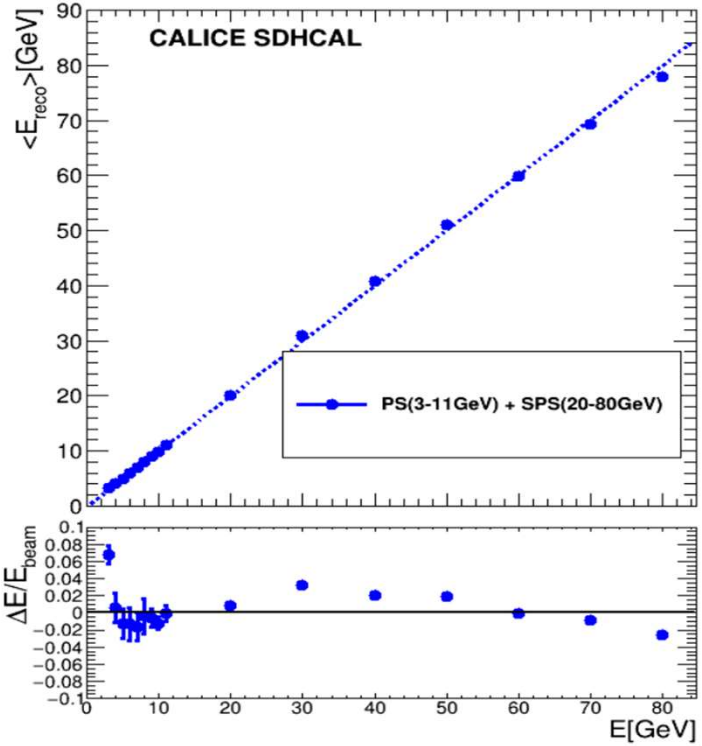


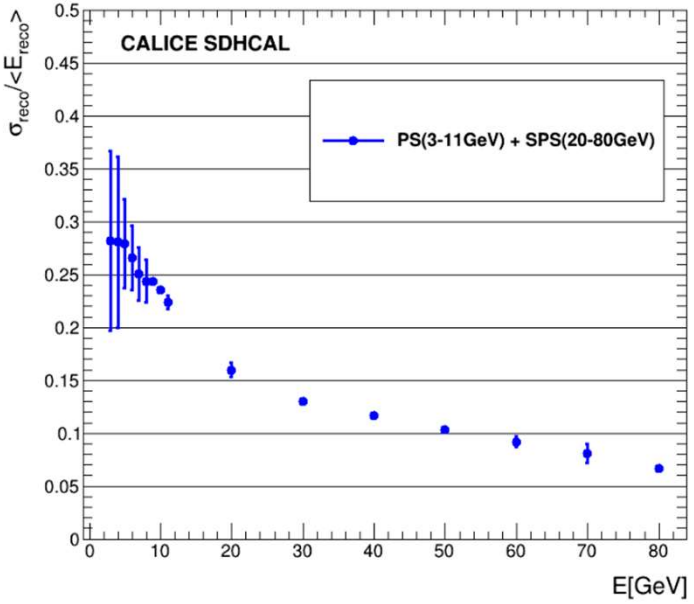
Distribution of the BDT output of training and validation set using the simulated electron (black) and pion (red) events from 1 GeV to 80 GeV.











excellent linearity and energy resolution from 3 to 80 GeV