

LHCb CO2 cooling meeting 7/10/2019

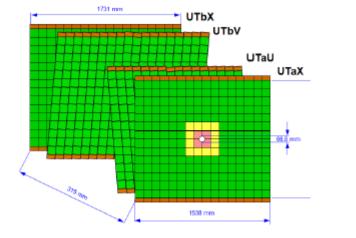


Updates from UT detector

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SUMMARY:

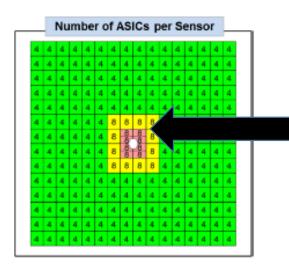
- $\Delta T CO_2 Sensor$
- Power and flow
- P&ID



UT detector 4 planes

Dissipated power coming mainly from the ASICs read-out

Requirement: max sensor T < -5°C

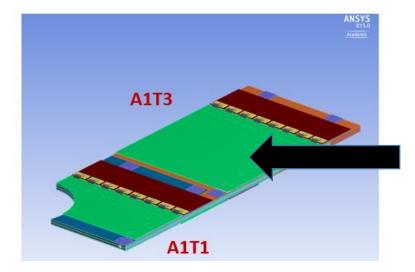


Staves in a plane have modules with 4 ASICs or 8 ASICs read-out

The thermal flow is bigger for modules with 8 ASICs

For these modules the sensor/cooling pipe temperature difference is bigger

These modules drive the coolant T set-point



<i>LHCb</i>	LHCb UT DETECTOR UPGRADE EDR June 2015			
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LHCb UT DETECTOR UPGRADE

SUMMARY OF THE THERMAL AND MECHANICAL FINITE ELEMENT ANALYSIS (F.E.A.) FOR THE DESIGN AND THE OPTIMIZATION OF THE DETECTOR STAVE The sensors in the «worst thermal condition» Are in the Central staves

position A1T3

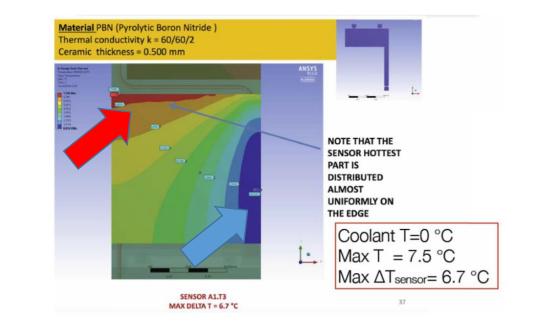
- 8 ASICs read-out
- Sensors placed over the data-cable

In the design phase FEA studies have been done to estimate the temperature field on the sensors

A sum-up of the studies could be find in the report made for the EDR:

SUMMARY OF THE THERMAL AND MECHANICAL FINITE ELEMENT ANALYSIS (F.E.A.) FOR THE DESIGN AND THE OPTIMIZATION OF THE DETECTOR STAVE https://edms.cern.ch/document/1517621/1

• PBN STIFFENER NO SLITS:



The sensors operating at nominal power have a temperature field:

A1T3 sensor thermal results

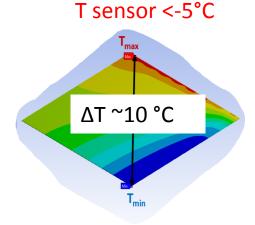
Basic assumption for the FEAs

8 ASICs read-out

Power: 0.768 W/ASIC

- Cold part of the sensor is at a temperature very near to the cooling pipe (negligible thermal flux in this region)
- Hot spot in the silicon located near the sensor edge facing the read-out chips
- The FEA worst case indicated ~7.5°C T difference from the pipe inner surface to the hot spot
- ΔT CO₂ to pipe has to be added (internal convection) estimated in ~2°C, in the region under the ASICs, where the hot spot is located

=> The $\Delta T CO_2$ - Sensor (max silicon T) was rounded to ~10 °C for these sensors



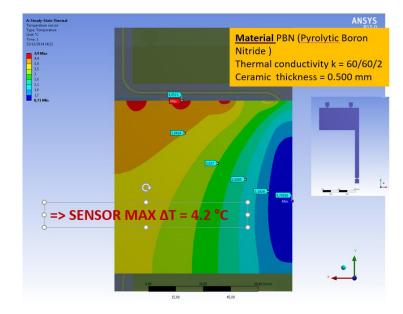
=> T CO2 < -15°C

NOTES:

• The majority of sensors have **4 ASICs read-out** Having half-power read-out the T differences are a factor 2 lower

Basic assumption for the FEA
 Power: 0.768 W/ASIC
 but real one could be as lo as 0,6 W/ASIC
 ΔT in this case will be proportionally lower (~80%)

 The ASIC chips temperature is generally higher than that of the Silicon sensor
 with a max ΔT CO₂ – ASIC estimated around ~25 °C
 Acceptable in all working conditions.



EXPERIMENTAL MEASUREMENT using a stave prototype were made in 2018

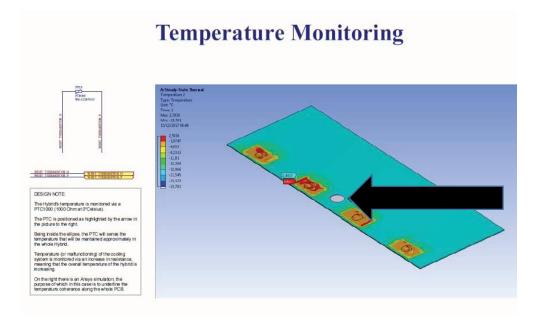


A validation of the FEA models was performed:

the conclusion was that for the 8 ASICs configuration (worst case) the expected ΔT calculated from FEA models had to be taken with a **3 °C error bar**

measured 13 °C instead of 10.3 °C

FEA RESULT 6.5 W TEMPERATURE OVER THE CERAMIC STIFFENER



All the UT hybrids have a temperature monitoring => Useful indication of the detector thermal field

Power and flow

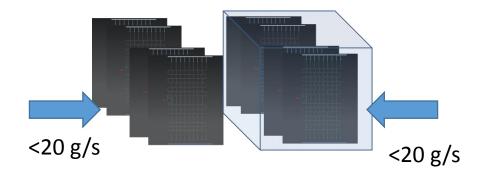
The ASIC power dissipation data from the 2018 SALT3 chip documentation states:

Table 1: Summary of the specifications of the SALT ASIC.

Variable	Specification
Technology	TSMC CMOS $130 \mathrm{nm}$
Channels per ASIC	128
Input / Output pitch	<u>80 µm / 140 µ</u> m
Total power dissipation	$< 768 m { m W}$
I	

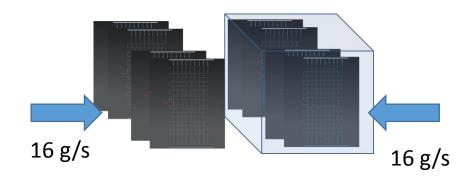
The relevant CO_2 flow calcutation, based on the assumption 1 g/s for 100 W:

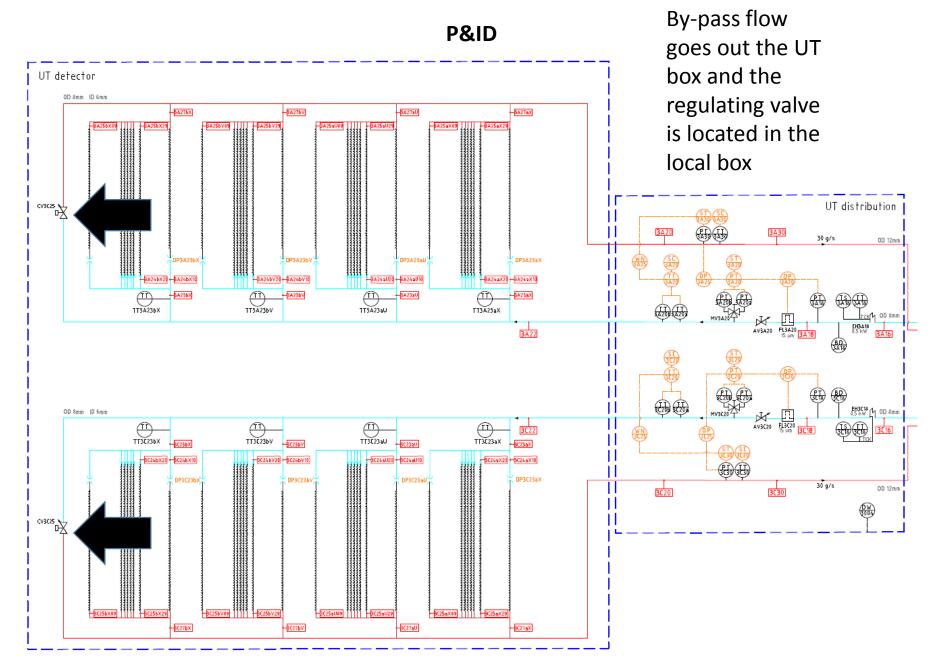
1 ASIC DISSIPATION	W	< 0,768
4192 ASICS DISSIPATION	W	3219,456
INCREMENT +10% FOR CABLES	W	3541,4016
HEAT PICK-UP	W	500
TOTAL COOLING POWER	W	4041,4016
TOTAL CO2 FLOW-RATE	g/s	40,41
tot co2 flow-rate one half box	g/s	20,21
flow-rate single stave (1/34)	g/s	0,59

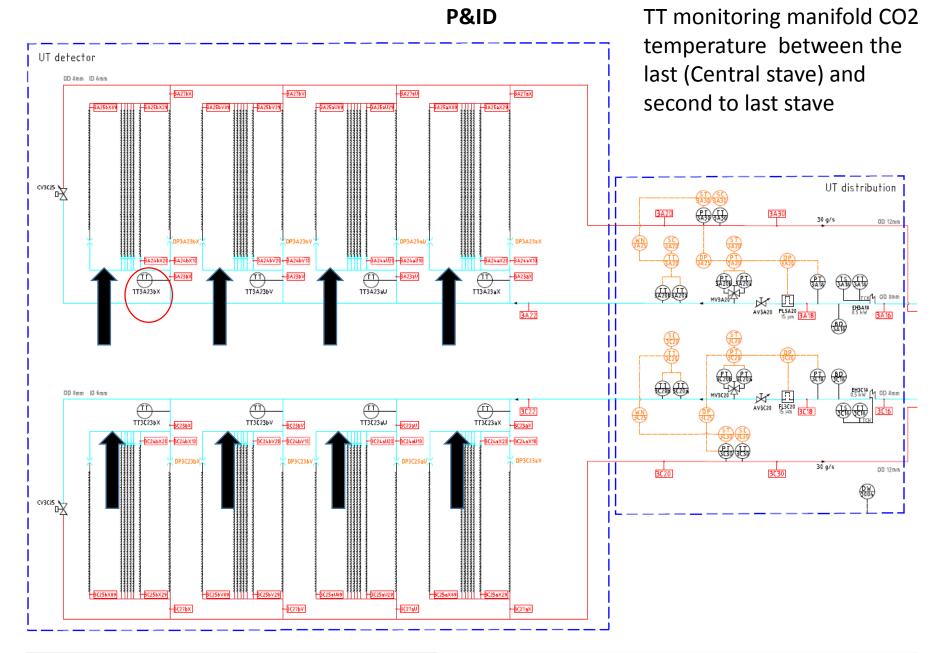


BEST GUESS FROM THE LAST INFORMAL COMMUNICATION

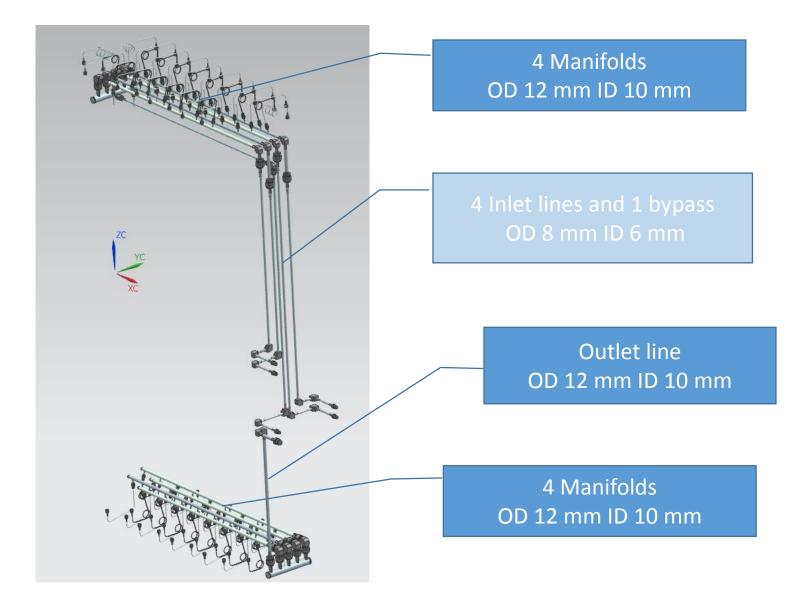
1 ASIC DISSIPATION	W	0,6
4192 ASICS DISSIPATION	W	2515,2
INCREMENT +10% FOR CABLES	W	2766,72
HEAT PICK-UP	W	500
TOTAL COOLING POWER	W	3266,72
TOTAL CO2 FLOW-RATE	g/s	32,67
tot co2 flow-rate one half box	g/s	16,33
flow-rate single stave (1/34)	g/s	0,48







Cooling distribution system: piping dimensions inside the UT detector



BACK-UP

