Risk Management
Readout Electronics

Risk Overview

WBS		Risk ID			Expires	Title	Rank
6.2.2 Readout Electronics	Threat	RD-06-02-02-001	Active	17-Oct-17	1-May-19	HV Mux does not converge' need to resort to making choices based on available cabling.	40
6.2.2 Readout Electronics	Threat	RD-06-02-02-002	Active	17-Oct-17	27-May-20	Chip run fails or radiation effects cause concern for readout at high rate and we need to do another run.	210
6.2.2 Readout Electronics	Threat	RD-06-02-02-003	Active	17-Oct-17	27-May-20	Chip set not compatible with lpGBT which won't be ready until just before or after production wafer orders for HCC are placed.	140
6.2.2 Readout Electronics	Threat	RD-06-02-02-004	Active	27-Feb-19	1-Sep-20	bPOL12V regulator is delayed	90
6.2.2 Readout Electronics	Threat	RD-06-02-02-005	Active	27-Feb-19	1-Sep-20	Loss of key personnel	60

Highest risk

WBS	6.2.2	Type	Threat	Risk ID	RD-06-02-02-002
Status	Active				
Expires	27-May-20				
Title	Chip run fails or radiation effects cause concern for readout at high rate and we need to do another run.				
Summary	Everything else is dependent on chip fabrication and performance both electrical and radiation. Chip iterations can take nearly 1 year so any failure of technical issues propagates a delay				
Owner	C. Haber				
Probability	Pre	40%	Post	25%	
Cost	Lo	550k	Hi	705k	
Schedule	Lo	9 months	Hi	15 months	
Tech Impact	3 (H)				
Post Mitg Prob	5 (M)				
Impact Score	Cost	3 (H)	Sched	3 (H)	Rank= 210
Mitigation	A thorough program of chip performance simulation during design phase, ASIC design review, and post-fabrication testing, including irradiations.				
Response	Determine cause of the problem through chip testing and its performance simulations, revise design, review with panel of experienced ASIC experts, resubmit for fabrication.				
Comments*	The schedule assumes that the preproduction chips and production chips have no problems or failures from radiation effects. There are many scenarios where the chip may need to be refabricated even though it is mostly functional. Schedule impact of 9-15 months includes the following: detect unexpected problem 2 - 4 months; determine cause 1 month; revise circuit, layout, compiler issue 1-4 months; review by experts 1 month; revised fabrication 3-4 months; wafer testing 1 month. The cost impact would be extra labor to fix the problem ($200k design) and extra cost of refabrications ($325k for a new mask, and variable cost depending on number of wafers needed, at $2.852k per wafer). This problem also propagates into the other production activities causing project wide delays. We estimate that, due to time scales associated with the root cause determination and assembly sequence in the project, we could lose up to half a year worth of labor time. Therefore cost impact could range from $550k (for design labor and fabrication only) for preproduction to around $700k for the production run of HCC/AMAC . First tasks affected are release of pre-production wafers for ABC and HCC/AMAC, since these chips are required by the rest of the project.				
Tasks Effected*	RE310335M, RE320650M				

2nd Highest risk

WBS	6.2.2	Type	Threat	Risk ID	RD-06-02-02-003
Status	Active				
Expires	27-May-20				
Title	Chip set not compatible with lpGBT which won't be ready until just before or after production wafer orders for HCC are placed.				
Summary	The lpGBT sites on the end-of-stave and communicates with the outside world. HCC ties directly to lpGBT				
Owner	C. Haber				
Probability	Pre	20%	Post	10%	
Cost	Lo	510k	Hi	635k	
Schedule	Lo	6 months	Hi	15 months	
Tech Impact	3 (H)				
Post Mitg Prob	3 (L)				
Impact Score	Cost	3 (H)	Sched	3 (H)	Rank= 140
Mitigation	lpGBT will need to be tested with HCC in a realistic physical prototype. Point to point 640 Mbps and multi-drop conditions should be fully explored to determine the level of communication robustness. It may be that EOS components are able to mitigate the problem or that a new submission of an HCC is required. It is unlikely that stave or endcap prototyping will be halted due to partially reliable communications. The HCC will retain a 320Mbps data rate in addition to the default of 640Mbps.				
Response	Move to fall back data transmission rates to allow continued testing of prototypes. Determine lowest cost mitigation that provides low or no bandwidth compromises. Implement correction on EOS or Hybrid or on HCC ASIC.				
Comments*	Prototypes of the HCC LVDS transmitters and receivers have been fabricated and work at their design frequency. The lpGBT is being designed by CERN Microelectronics and in collaboration with other institutions with proven communications circuit design ability. The risk of total failure is low, but there may be some reliability issues that need work. This would cause downstream effects on the stave building, Schedule delay is estimated from a working solution being found within 6-15 months of the production order release for HCCStar. If a resubmission of the production HCC is required, the cost is $460k for mask set and wafers and extra labor on the LVDS section design and testing is estimated at $50k-$150k. This problem also propagates into the other production activities causing project wide delays. We estimate that, due to time scales associated with the root cause determination and assembly sequence in the project, we could lose up to half a year worth of labor time. First task affected is the release of the production order for the HCC, since the production chips are what are required by the rest of the project.				
Tasks Effected*	RE321030M				

3rd Highest risk

WBS	6.2.2	Type	Threat	Risk ID	RD-06-02-02-004		
Status	Active						
Expires	1-Sep-20						
Title	bPOL12V regulator is delayed						
Summary	This chip is a CERN deliverable so is an external dependency. It is due in Spring of 2020 but still has some uncertainties related to the final supply voltage. Design studies to resolve this could, in principle, delay it.						
Owner	C. Haber						
Probability	Pre	25%	Post	25%			
Cost	Lo	4k	Hi	18k			
Schedule	Lo	1 month	Hi	6 month			
Tech Impact	2 (M)						
Post Mitg Prob	5 (M)						
Impact Score	Cost	1 (L)	Sched	2 (M)	Rank=	90	
Mitigation	There is no mitigation						
Response	This would delay the assembly and distribution of power boards which would in turn delay module assembly. Hopefully we could avoid the standing army problem since it is due to be delivered well in advance.						
Comments*	This would delay the assembly and distribution of power boards which would in turn delay module assembly. Cost impact is low since chips should be delivered at least 6 months ahead of start of production. First task affected is loading of production boards Batch 1.						
Tasks Effected	RE261410						

4th Highest risk

WBS	6.2.2	Type	Threat	Risk ID	RD-06-02-02-005		
Status	Active						
Expires	1-Sep-20						
Title	Loss of key personnel						
Summary	The readout electronics project depends upon a core engineering team at Penn for the ASICs and a team of physicicsts/engineer at LBNL for the power board						
Owner	C. Haber						
Probability	Pre	10%	Post	10%			
Cost	Lo	4k	Hi	32k			
Schedule	Lo	1 month	Hi	9 months			
Tech Impact	3 (H)						
Post Mitg Prob	3 (L)						
Impact Score	Cost	1 (L)	Sched	2 (M)	Rank=	60	
Mitigation	There is no mitigation						
Response	A position would be posted and a new hire made. In the interim the existing staff would assume additional responsibility						
Comments*	These are long term employees of the institutions with a strong commitment to the project. First tasks affected are design revisions after Jan 2019 in ABC, HCC, AMAC design, and powerboard and HV-Mux.						
Tasks Effected*	RE140360, RE260820, RE310260, RE320470,RE350510						

Retired Risk

WBS	6.2.2	Type	Threat	Risk ID	RD-06-02-02-001
Status	Active				
Expires	1-May-19				
Title	HV Mux does not converge and we need to resort to making choices based on available cabling.				
Summary	We plan an HV mux on the powerboard, per module. We are still doing a technology selectiion and the parts are boutique. While promising we could end up with no solution				
Owner	C. Haber				
Probability	Pre	40%	Post	10%	
Cost	Lo	2k	Hi	150k	
Schedule	Lo	0.5 month	Hi	3 months	
Tech Impact	1 (L)				
Post Mitg Prob	3 (L)				
Impact Score	Cost	1 (L)	Sched	1 (L)	Rank= 40
Mitigation	One of two alternative technologies was chosen in FY17 to focus the resources on the most promising solution and maximize the chances of making it work. A program of testing and irradiation is being pursued to validate the technical performance.				
Response	If the technology fails we can use extra lines on the stave bus tape to supply the additional HV lines.				
Comments	The technology is novel and may not be commercially available in the un-packaged form we need in the experiment. If it fails this will impact the tape design and granularity of HV control on the strip modules. As a last ditch solution, to preserve the schedule, we might build some staves w/o HV Mux while continuing to work on the HV Mux solution. Maximum cost is due to a 1 year engineering delay. First task affected is long term reliability tests.				
Tasks Effected	RE140180				

HV Mux review in March 2019: works and plan to use on detector.