WBS 6.2.2
Readout Electronics

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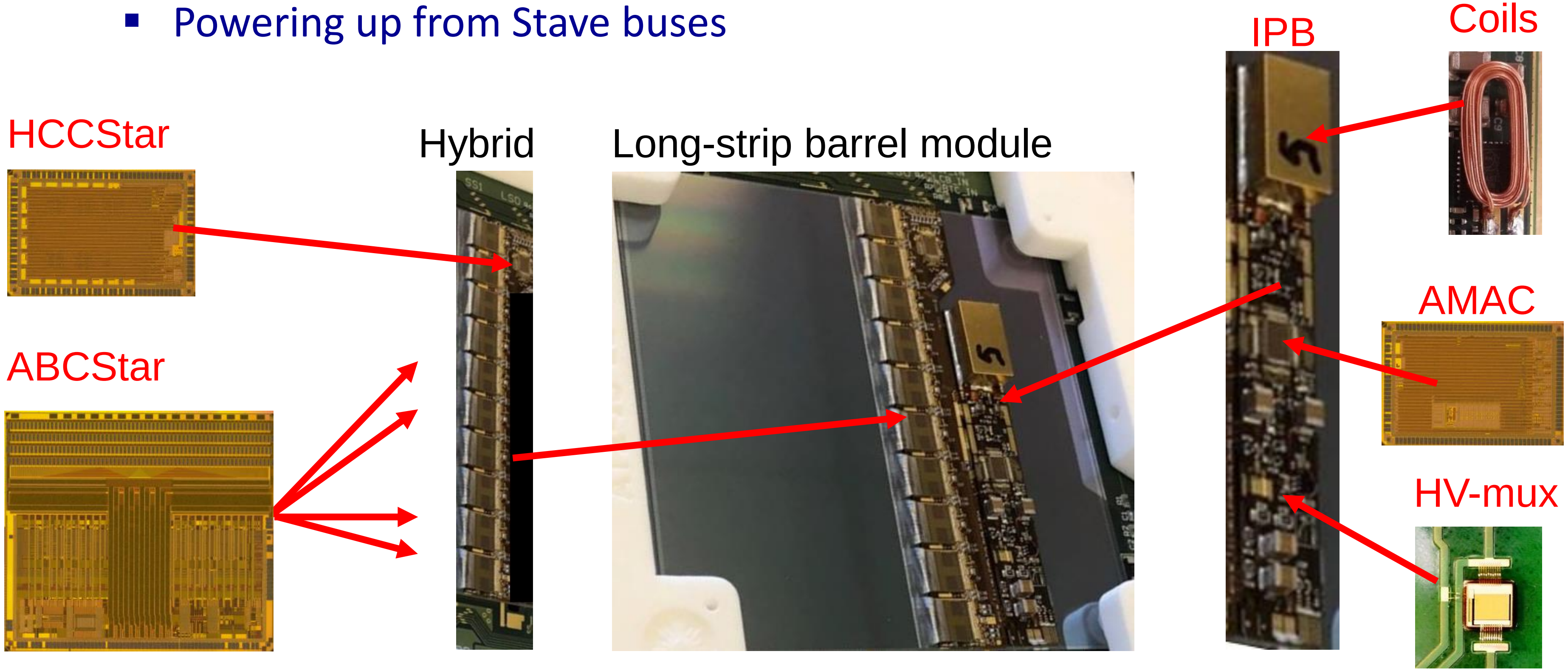
Outline

- Technical Details
  - Deliverable Overview, institutional responsibilities
  - R&D Status and Plans
  - Technical Progress in FY19
  - Pending Issues
  - Plans for pre-production
  - Plans for production
- Schedule and Cost
  - How has the schedule changed since CD-3a?
  - How has cost changed since CD-3a
- Risk and Uncertainty
- Closing Remarks

Technical Details

Deliverable Overview

- Front-end readout ASICs (ABCStar, HCCStar)
- Integrated Powerboard (IPB) with ASIC AMAC, HV-mux, Coils
- Fairly self-contained set, except for interfaces with stave side:
  - Multi-drop communication with EOS
  - Powering up from Stave buses



Deliverable Overview

This WBS covers front-end readout ASICs, and powering electronics for the silicon strip tracker.
Basic unit of tracker is a silicon strip sensor, one or two readout hybrids, and one integrated powering board (IPB).

Star chips: each barrel readout hybrid has 10 ABCStar (front-end) and 1 HCCStar (controller)

- Penn & UCSC → ABCStar design with CERN, US will pay for 88,631 chips (37.9% of entire tracker).
- Penn & UCSC → HCCStar design, Penn probes wafers, supply 25,536 chips for entire tracker.

Powerboard: IPB implements all LV, HV, monitoring, & power control functions in a single PCB.

- LBNL → design of barrel IPB, test, burn-in, supply 10,976 boards for entire barrel.
- *CERN provides bPOL12V circuit design and supplies chips,* US will pay for entire barrel.
- Penn → AMAC design, probe wafers, supply 17,888 chips for sensors in entire tracker.
- BNL → HV-mux design, prototyping, production 17,888 pieces for sensors in entire tracker.
- Yale → design, testing of coils, US will pay for 10,976 coils for entire barrel.

(NB: numbers to install on this slide, yield factors and numbers to fabricate on next slide).

Deliverable Overview

Total number of components larger than number required to install

- System yield factor includes losses in downstream assembly
  - Failure of installation of components on hybrid is 97% (rounded to 1.031)
  - Failure of module assembly of 91% (rounded to 1.095)
  - Failure of stave substructures of 95% (rounded to 1.053)
- Component yield factor accounts for losses in fabrication of components
- Planned order includes QA/QC for IPBs and HV-mux

Deliverable	Number to install	System yield factor	Component yield factor	Production number to fabricate	Production QA/QC	Pre-production number (circa 5%)	Total with pre-production
ABCStar (37.9%)	88,631	1.1890	1.1340	119,504	-	5,975	125,479
HCCStar	25,536	1.1890	1.1340	34,431	-	1,722	36,152
AMAC	17,888	1.1890	1.1340	24,119	305	1,206	25,630
HV Mux	17,888	1.1890	1.0730	22,821	685+305	-	23,811
Coils	*10,976*	*1.1890*	*1.0500*	*13,703*	*305*	*1,021*	*16,000*
IPBs (barrel)	10,976	1.1530	1.0740	13,592	508	1,000	15,100

Progress in FY19

- HV-Mux
  - Production order being organized through RAL.
  - Future BCP: Reduction in cost per device.
- Readout Electronics
  - Preproduction significant delay due to critical additional design effort for SEE protection
  - Preproduction order of ABCStar via CERN, investigating HCCStar/AMAC order via Penn
  - Future BCP: Change in ASIC costs from new CERN contract with foundry
- Powerboard
  - V3 series: 130 provided to modules, 15 for testing development, 50 more in assembly
  - Preproduction design in progress.
- Coils
  - Production order in progress through Yale.
  - Future BCP: Additional cost from China tariff, but US only needs to pay for coils for barrel.

Pending Technical Issues

- HCCStar design effort increased due to critical radiation issue.
  - Risk: Corrupted data from a module until HCCStar reset.
  - Irradiation results: high upset rate in physics mode operation.
  - **Additional design effort**: Triplicate control logic to protect against SEE. Complicated on densely packed chip. Multiple spins of place and route. Detailed simulation of SEE including transients.
  - **Design completion? Estimate end of April 2020 (range: 1 April – 30 June 2020)**
  - **Preproduction chips available? Estimate end of September 2020**
    - SEE issues discovered in irradiation during summer 2019 have led to a 7 month delay.
- AMAC design effort increased to lower risk of SEU.
  - Risk: Permanent irreplaceable loss of power to a module.
  - Irradiation results: AMAC worked successfully but SEU rate higher than desired.
  - FDR recommendation on Nov 8 2019: lowest failure risk achievable.
  - **Additional design effort:** Triplicate clock net to protect against SEE. Requires simplification of monitoring checks to free space (two-sided to one-sided interlocks), and respins of place and route.

Reviews

- Production Readiness Review (PRR) will release production orders
  - Requires irradiation tests of preproduction chips for SEE
  - Requires tests of modules and staves built with preproduction chips (system test FDR)

Deliverable	Past prototypes	Current prototype	PDR	FDR	PRR	Future path
ABCStar	ABCN250, ABC130	ABCStar	Jan 2018	July/Nov 2019	FY2021	Preproduction Production
HCCStar	HCC130	HCCStar	Jan 2018	July /Nov 2019 May 2020	FY2021	Preproduction Production
AMAC	AMAC v1, v1a, v2	AMAC v2a	Nov 2017	July/Nov 2019 May 2020	FY2021	Preproduction Production
HV-mux	GaN-FET, 3D-FET	GaN-FET	As part of IPB			Production
IPB	V1, V2	V3	Feb 2018 (module)	Sept 2019 (module)	FY2021	Preproduction Production
Coils	Planar, Toroidal	Planar 3 layers	As part of IPB			Production

Schedule and Cost

Schedule

Prototyping phase (ends FY19 *) dates range for sub-projects

- ✓ Design and testing of prototype ABCStar, HCCStar, AMAC by Penn & UCSC
- ✓ Radiation hardness, reliability evaluation of GaN-FET based circuit HV-mux by BNL
- ✓ Coil and shield tests by Yale, order 1000 coil sets by Yale
- ✓ Design, fabrication, and testing of V2 and V3 of the IPB by LBNL

Pre-production phase (FY19 to FY20 *)

- Preproduction design of ABCStar, HCCStar, AMAC Critical Path. 7 month delay since CD-3a
- Testing of Preproduction HCCStar and AMAC by Penn (wafer and irradiations)
- Preproduction IPB design revision, fabrication of 250+750 boards

Production phase (FY20 to FY22 *)

- Financial contribution to ABCStar production
- Production HCCStar and AMAC: fabrication, then wafer testing at Penn, and distribution
- PreProduction+Production order for 24,000 GaN-FET devices, QC tests including irradiations by BNL
- PreProduction+Production order for fabrication and testing of 16,000 coil sets by Yale
- Production IPB fabrication and testing of the IPB, including burn-in, by LBNL

External dependencies

Powerboard external dependencies

- bPOL12V – from CERN. In Risk Register.
  - Have 1000 V4 chips for preproduction powerboards, but V4 is not radiation hard.
  - Need V5 for production. Expect to have 100 for testing in summer, more by end of 2020, well ahead of production.
- LinPOL12V – from CERN. Parts in hand.

Milestones

- Readout electronics must supply the following
  - HCCStar to 3 hybrid sites in US (BNL, UCSC, LBNL) and international sites
  - AMAC to Barrel IPB site (LBNL) and international sites for Endcap IPB
  - Barrel IPB to 3 hybrid sites (BNL, UCSC, LBNL) and international sites

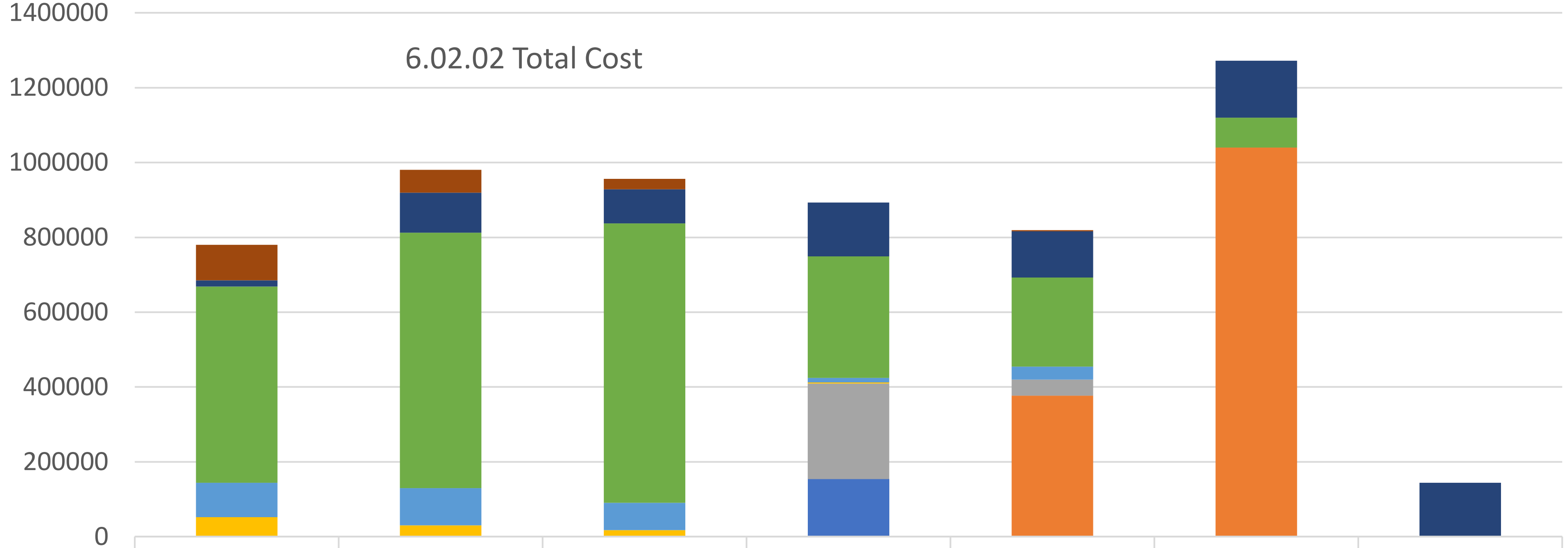
Milestone	Finish	Float
AVAIL: Pre-Production of ABC Chips for PP3 Hybrids	~~04-10-20~~ 07-31-20	134
AVAIL: HCC Chips at BNL Hybrid Assembly Test Site	09-29-20	100
AVAIL: 1st Production HCC Chips to BNL Hybrid Assembly Site	10-14-21	13
AVAIL: Pre-Production AMAC to 6.2.2.2 - LBNL	09-29-20	0
AVAIL: Prod Batch 1 - AMAC Chips at 6.2.2.2 - LBNL	11-18-21	50
AVAIL: Devices for LBNL *HV Mux*	12-24-20 To be updated	198
AVAIL: Pre-Pro PP3a Power Boards for Module Sites *(using prototype AMAC)*	05-28-20	135
AVAIL: PrePro PP3b Power Boards for Module Sites *(using pre-pro AMAC)*	11-30-20	67
AVAIL: Power Boards Available for Modules Batch 1	10-22-21	16
AVAIL: Coils at LBNL IPB (6.2.2.2.6)	~~04-22-20~~ 07-31-20	369
RECEIVE: Prod BPOL12V from CERN	~~06-01-20~~ 12-31-20	342

Cost

Engineering effort for ASIC design & testing

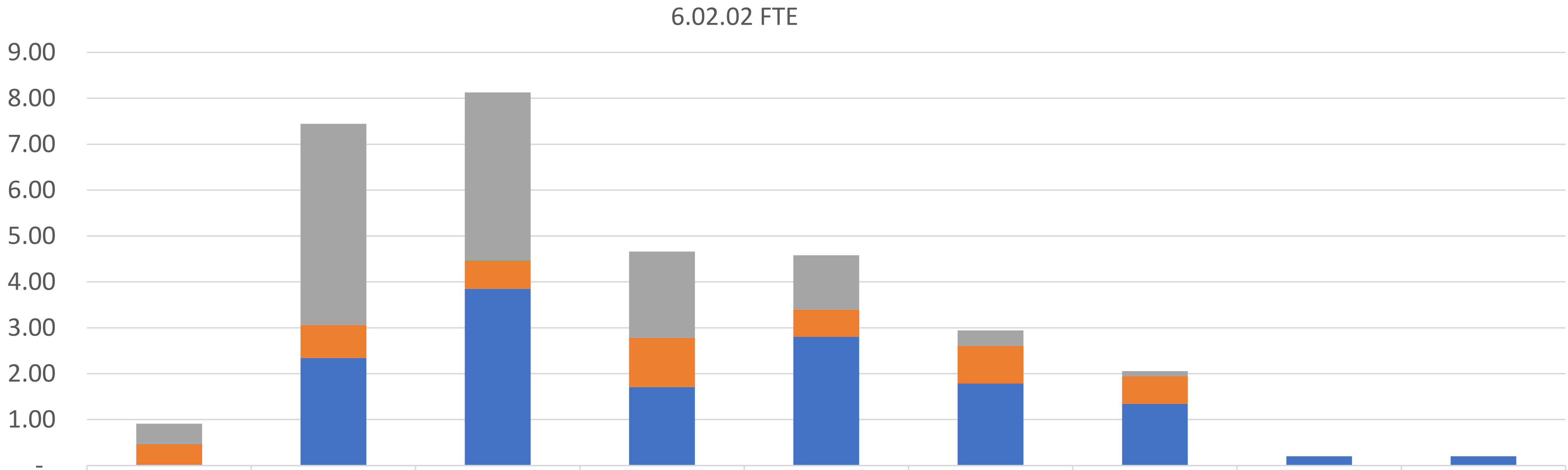
CD-3a HVMux QC & Irradiation

CD-3a Powerboards



	2017	2018	2019	2020	2021	2022	2023
6.02.02.01 Readout Electronics-BNL	95,192	60,706	27,453		3,508		
6.02.02.02 Readout Electronics-LBNL	17,005	107,352	91,719	143,750	123,574	152,827	144,466
6.02.02.03 Readout Electronics-Penn	523,872	682,457	746,605	325,012	238,027	79,659	
6.02.02.04 Readout Electronics-UCSC	91,679	98,954	72,532	12,120	34,706		
6.02.02.05 Readout Electronics-Yale	52,638	30,777	17,845	2,481			
6.02.02.31 Readout Electronics-BNL - CD-3a				255,492	42,688		
6.02.02.32 Readout Electronics-LBNL - CD-3a					376,981	1,039,769	
6.02.02.35 Readout Electronics-Yale - CD-3a				154,098			

FTE



	2017	2018	2019	2020	2021	2022	2023	2024	2025
ENG	0.45	4.38	3.67	1.87	1.19	0.34	0.11		
TECH	0.45	0.72	0.62	1.08	0.59	0.81	0.60		
UNCOST	0.02	2.35	3.85	1.71	2.81	1.79	1.34	0.20	0.20

Readout Electronics Cost Variance

WBS	CD-3a cost	BCP-19 change	BCP-22 change	BCP-24 change	BCP-25 change	BCP-27 change	BCP-28 change	BCP-31 change	March 2020 cost	Total change	Change (%)
		(24 Jul)	(28 Aug)	(Nov 5)	(Dec 17)	(Nov 28)	(Jan 21)	(Feb 25)			
	July '19	Merge WBS	ASIC sched	SQ equip ASICs	HCC complx	ASIC irrad	SQ and sched	Delay cores			
6.02 Strips	38,419	-19	196	194	405	42	246	113	39,596	1,177	3.1%
6.02.02 Readout	**5,587**	**0**	**16**	**26**	**220**	**0**	**0**	**-4**	**5,846**	**258**	**4.6%**
6.02.02.01 BNL*	485	0	0	-298	0	0	0	0	187	0	0.0%
6.02.02.02 LBNL*	2,159	0	9	-1,386	6	0	0	-7	781	39	1.8%
6.02.02.03 Penn	2,377	0	7	26	186	0	0	0	2,596	218	9.2%
6.02.02.04 UCSC	309	0	0	0	1	0	0	0	310	1	0.4%
6.02.02.05 Yale*	258	0	0	-154	0	0	0	0	104	0	0.0%
6.02.02 CD-3a items	**1,834**	**0**	**8**	**0**	**27**	**0**	**0**	**3**	**1,871**	**38**	**2.1%**
6.02.02.31 CD-3a BNL†				298	0	0	0	0	298	0	0.0%
6.02.02.32 CD-3a LBNL†				1,386	27	0	0	3	1,417	30	2.2%
6.02.02.35 CD-3a Yale†				154	0	0	0	0	154	0	0.0%
6.02.07 CERN Procure	**4,225**	**0**	**5**	**0**	**0**	**42**	**13**	**0**	**4,285**	**60**	**1.4%**
6.02.07.31 CD-3a CERN	0	0	0	2,432	0	0	0	0	2,431	0	0.0%

*Change relative to CD-3a when including CD-3a procurements (BCP-24 created separate accounts)

†Change relative to BCP-24

Note that changes for BCP-25 and BCP-27 computed with respect to BCP-24

Future BCP

- ASIC costs will increase due to new contract with foundry
  - Dicing cost is an estimate of $1000 per wafer
  - Attachment 10A and updates to attachments 9,11,12
- HV Mux cost decrease due to lower cost per device for large production order
  - Attachment 2A
- Coils cost decrease due to US paying for barrel only, but 15% China tariff
  - Attachment 13A

Item	P6 task	P6	New quote	Change	Change (%)
ABCStar production	RE310390M CD-3a	$833,800	$1,083,404	$249,604	29.9%
ABCStar preproduction	RE310335M	$152,876	$190,577	$37,701	24.7%
HCCStar production	RE321030M CD-3a	$462,176	$570,874	$108,698	23.5%
HCCStar preproduction	RE320650M	$325,200	$421,630	$96,430	29.7%
Sum of ASICs		**$1,774,052**	**$2,266,486**	**$492,434**	**27.8%**
HV-Mux	RE140400M CD-3a	$849,621	$552,000	-$297,621	-35.0%
Coils	RE530450M CD-3a	$105,600	$91,001	-$14,599	-13.8%
Sum of Readout Electronics		**$2,729,273**	**$2,909,486**	**$180,213**	**6.6%**

Risk and Uncertainty

Risk Register

WBS	Risk Type	Risk-ID	Status	Date Modified	Expected Expiration	Title	Probability category Pre-Mitig.	Post-Mitig.	Probability Post-Mitig.	Cost Impact (k$) Low	High	Schedule Impact (months) Low	High	Technical Impact	Post-Mitig. Prob. Score	Impact Score Cost	Schedule	Risk Rank
6.2.2	Threat	RD-06-02-02-002	Active	19-Dec-19	31-Dec-21	ABCStar chip run fails or rad	3 Mod	3 Mode	36%	170	190	9.0	15.0	3 (H)	5 (M)	2 (M)	3 (H)	210
6.2.2	Threat	RD-06-02-02-003	Active	19-Dec-19	1-May-21	Chip set not compatible with	2 Low	2 Low	18%	650	750	6.0	15.0	3 (H)	3 (L)	3 (H)	3 (H)	140
6.2.2	Threat	RD-06-02-02-004	Active	19-Dec-19	31-Dec-21	bPOL12V regulator is delaye	2 Low	2 Low	18%	4	18	1.0	6.0	2(M)	3 (L)	1 (L)	2 (M)	60
6.2.2	Threat	RD-06-02-02-005	Active	27-Feb-19	31-Dec-24	Loss of key personnel	2 Low	2 Low	18%	4	32	1.0	9.0	3(H)	3 (L)	1 (L)	2 (M)	60
6.2.2	Threat	RD-06-02-02-006	Active	19-Dec-19	31-Mar-21	ABCStar additional complexi	4 Mod	3 Mode	36%	20	40	5.0	9.0	3 (H)	5 (M)	1 (L)	3 (H)	210
6.2.2	Threat	RD-06-02-02-007	Active	19-Dec-19	31-Dec-21	HCCStar/AMAC chip run fails	3 Mod	3 Mode	36%	550	750	9.0	15.0	3 (H)	5 (M)	3 (H)	3 (H)	210
6.2.2	Threat	RD-06-02-02-008	Active	19-Dec-19	31-Jul-20	HCCStar/AMAC additional co	4 Mod	3 Mode	36%	200	600	3.0	9.0	3 (H)	5 (M)	3 (H)	3 (H)	210
6.2.2	Threat	RD-06-02-02-009	Active	19-Dec-19	31-Dec-21	Exposure due to single foun	3 Mod	3 Mode	36%	200	400	3.0	6.0	2(M)	5 (M)	3 (H)	2 (M)	210
6.2.2	Threat	RD-06-02-02-010	Active	19-Dec-19	31-Dec-20	Chip run fails for HV Mux	1 Very	1 Very	5%	600	800	9.0	12.0	2(M)	1 (VL)	3 (H)	3 (H)	70

9 active risks (006-010 added since review)

- ABCStar risks
  - Additional submission (Chip run fails)
  - Additional complexity for design
- HCCStar/AMAC risks
  - Additional submission (Chip run fails)
  - Additional complexity for design
- Single foundry risk
- bPOL12V (external dependency delay)
- HV Mux (Chip run fails)
- lpGBT risk (Additional submission)
- Loss of key personnel

Risk Checklist from PO

- Basic maintenance of all risks
  - ✓ Check if risks are still active
  - ✓ Revisit tasks affected column in RR, especially after recent RLS changes
  - ✓ Recheck comments section for each risk. Is there an explanation for how risk probabilities and impacts were estimated? Can a reviewer reconstruct the impact ranges from the information provided?
  - ✓ <u>Check that every external dependency has a risk associated with it.</u>
- Add new risks
  - ✓ Risk of loss of key personnel. One risk per deliverable.
  - ✓ Risk of needing additional labor force due to unexpected complexities that arise. Estimate as the labor cost of one prototype iteration.
- Maturity scores
  - Check that all tasks in P6 have maturity scores assigned
  - Retune if necessary the scores (for example if R&D performed to date has improved the maturity)

Closing Remarks

- Significantly more preproduction design effort than expected by Penn for HCCStar and AMAC, and by CERN for ABCStar
  - Delay of 7 months after SEE problems discovered during irradiations in summer 2019
  - Extensive SEE simulations to validate designs of ABCStar, HCCStar, AMAC
  - Irradiation tests being scheduled for as soon as preproduction chips expected available in 2020
- Future BCP
  - Updated quotes for ASICs and production orders of HV Mux and Coils
  - Irradiation tests of preproduction chips

BACKUP

Bio Sketch of L3 manager

- Evelyn Thomson, Associate Professor, University of Pennsylvania
- ATLAS: 2007-present
- ATLAS responsibilities
  - US L3 manager for readout electronics
  - Supervisor of Dr. Jeff Dandoy and graduate student James Heinlein on ITk
  - ATLAS speaker's committee, US ATLAS speaker's committee
  - ATLAS TRT
- Previous experiments
  - CDF – Top quark physics group leader
  - CDF – L1 track trigger (XFT)
  - ALEPH – PhD thesis on W boson mass

Technical Specifications

- In most cases there are advanced long ATLAS ITk specification documents :
  - **ABC**: https://edms.cern.ch/ui/#!master/navigator/document?D:1408948628:1408948628:subDocs (77 pages)
  - **HCC**: https://edms.cern.ch/ui/#!master/navigator/document?D:1854950570:1854950570:subDocs (36 pages)
  - **AMAC**: https://edms.cern.ch/ui/#!master/navigator/document?D:1176677015:1176677015:subDocs (22 pages)
  - **IPB**: https://edms.cern.ch/ui/#!master/navigator/document?D:100054839:100054839:subDocs (23 pages)
- Below are examples of key specifications (U.S. ATLAS HL-LHC Upgrade Technical Specifications , ATLAS HL-LHC Upgrade Document 216-v6)

Deliverable	Type	Spec. examples	Challenge
ABCStar: design + % of fab cost	Custom IC	Up to 4 MHz trigger rate; high-bandwidth communication with HCC. Detailed specifications exist.	Design complexity, radiation hardness
HCCStar: design + probing	Custom IC	160 Mbps input from each of up to 11 ABCStar ICs; data output at 640 Mbps to w\ EOS. Detailed specifications exist.	Design complexity, radiation hardness
AMAC: design + probing	Custom IC	Precision power monitoring, control of other ICs: HV-mux, bPOL12V, HCCs. I(sensor) of 10s nA to 10 mA. Specifications exist.	Design complexity, radiation hardness
HV-mux: devel + QC	IC	500 V bias, “off” failure rate << 1%, radiation hardness. Part of IPB specs.	Reliability of new technology
DC-DC coils: devel + QC	Coil	Air-coils low mass and footprint, L = 700 nH, low pickup noise. Part of IPB specs.	Small coil fab, Pickup noise
IPB (barrel): design + fab	Flex circuit	High-density design with 3 ICs on the small board; 11 mm x 72 mm area.	Pickup noise, reliability

Institute Capabilities

- Paul Keener (Penn) is international activity co-ordinator for ASICs with Laura Gonella (Univ. of Birmingham, UK)
- Penn (Mitch Newcomer, Paul Keener, Nandor Dressnandt, Bill Ashmanskas, Adrian Nikolica) contributing to ABCStar, HCCStar, AMAC. UC Santa Cruz (Alex Grillo) contributing to ABCStar and HCCStar. Both groups have a strong history of designing and testing custom Ics, with long and close R&D collaboration on FEE with CERN microelectronics.
- Penn has a probing station for testing of HCCStar and AMAC wafers
- HV-mux at BNL (David Lynn), led development in ITk strips while collaborating with UK colleagues.
- Yale (Satish Dhawan) established feasibility of low-profile air-coils and measurement of pickup for different coils and shields.
- LBNL (Timon Heim, Carl Haber) produced V2 and V3 of IPB, personnel with high degree of engineering expertise, delivered specialized high-density PCB boards (e.g. hybrids) for many projects (IceCube, CDF, ATLAS).