The ALPIDE telescope

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on behalf of the ALICE collaboration

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Outline

1. Introduction
2. ALPIDE telescope
3. Selected results
4. Summary and future developments
Outline

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4. Summary and future developments
1. Introduction

12.5 G-pixel camera:
- binary readout
- $\sim 10 \text{ m}^2$ total area
- $\sim 25000$ chips

Fully equipped with Monolithic Active Pixel Sensors (MAPS)

- hybrid
- monolithic
- readout chip
- sensor
- thinned down to 50$\mu$m!
1. Introduction

Features:
- Dimension: 30mm x 15mm (1024 x 512 pixels)
- Pixel pitch: 29μm x 27μm
- Thinned to 50μm (0.05% x/X₀)
- Possibility to apply reverse bias voltage
- Event-time resolution 2-4 μs (charge collection time only 1-30ns, but not exploited)
- Very low power consumption (40mW/cm²) no cooling needed in test beam setup
- Global shutter: triggered acquisition (up to 200kHz Pb-Pb or 1MHz pp <-> ~6MHz/cm² particle hit rate) or continuous (progr. integration time: 1μs – quasi ∞)
- Binary readout
- 1.2 Gbit/s serial link, can drive up to 5m of cable
- Two possible connection schemes: pads over the matrix and pads at the periphery

Key concepts:
- In-pixel amplification
- In-pixel hit discrimination
- In-pixel 3-level event memory
- In-matrix zero-suppression

• Produced in the TowerJazz 180nm CMOS Imaging Sensor (CIS) process
• 25μm epitaxial layer
• Full CMOS within pixel matrix
Outline

1. Introduction
2. ALPIDE telescope
3. Selected results
4. Summary and future developments
ALPIDE carrier card and DAQ board

2. ALPIDE telescope

ALPIDE carrier card:
- Large opening underneath ALPIDE to reduce material budget
- PCIe connector used as mechanical and electrical interface (with custom electrical protocol)
- Small pads at periphery used for bonding

DAQ board:
- USB-3.0 for connection to PC
- PCIe connector for carrier card
- Various GPIO connectors

- ALPIDE telescopes typically consist of 7 planes, plane distance ~2cm
- Central chip is typically treated as Device Under Test (DUT)
ALPIDE Telescopes

2. ALPIDE telescope

Telescope 1

Telescope 2
ALPIDE Telescopes

2. ALPIDE telescope

- ALPIDE telescopes successfully operated in various test beam facilities all over the world (CERN PS, DESY, BTF Frascati, Pohang/Korea, SLRI/Thailand)
- Simulated track resolution at DUT around 2-3μm with 6GeV/c pions
- Studied performance in terms of: detection efficiency, position resolution, cluster sizes and shapes

Both telescopes installed in EA T10 (CERN PS)
ALPIDE Telescope: Software

2. ALPIDE telescope

- DAQ using EUDAQ:

  - ALPIDE producer specialities:
    - Control of external equipment
    - Automatic reconfiguration for errors
    - Online data consistency checking (absolute and relative timestamps as well as trigger ids)

  - Automation:
    - Generation of configuration files
    - Changing configuration files after a certain number of events
    - Control of power supplies, pulser, linear and rotary stages
    - Watchdog sending texts and emails
      - Check EUDAQ control
      - Last event written
      - File size of current run
      - Out-of-sync

  - Like this about 1000 runs, each with a different setting (threshold, reverse bias, integration time, etc.), could be performed in 10 days without presence of shift crew

- Analysis using EUTelescope
Telescope Optimizer tool

2. ALPIDE telescope

Nice online tool for optimizing telescope setup

- Variable parameters:
  - Plane position
  - Material budget per plane
  - Resolution per plane
  - Particle type and momentum

- Planes can be moved by mouse, results will be automatically updated
- Tracks and measured points in planes can be simulated
- One can also construct a setup by URL, see e.g. at bottom of this slide

- Source: https://gitlab.cern.ch/mmager/telescope-optimizer

http://mmager.web.cern.ch/mmager/telescope/tracking.html#part=e&p=1&x=[-10,-6,-4,-2,0,2,4,6,10]&XX0=[0.005,0.0005,0.0005,0.001,0.0005,0.0005,0.0005,0.0005,0.0005]&sy=[0.0005,0.0005,0.0005,0.0005,0.0005,0.0005,0.0005,0.0005,0.0005]&en=[0,1,1,0,1,1,1,0]&ymc=[0,0,0,0,0,0,0,0,0]&ym=[0,0,0,0,0,0,0,0,0]&scaley=0.0005
Outline

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ALPIDE: Reverse bias dependence

3. Selected results

Detection efficiency and fake-hit rate

- Detection efficiency stays at 100% - $\epsilon$ over wide range of thresholds
  - Chip-to-chip fluctuations negligible
- Clear ordering: increasing performance with larger reverse bias
  - Most significant improvement from 0V to -1V
- Extremely low fake-hit rate (Gaussian noise only 2-6 e$^-$)
  - Below measurement limit of 10$^{-11}$/pixel/event after masking 10 pixels (1/50 000), only increased for -6V

25μm epitaxial layer -> ~1600e$^-$ produced produce by MIP (MPV)
-> then also charge sharing, Landau fluctuations to be considered.
3. Selected results

Position resolution and average cluster size

- Position resolution around desired 5μm in threshold range with detection efficiency > 99%
  - Biggest improvement from 0V to -1V
  - Little dependence on reverse bias from -2V to -6V
- Average cluster sizes vary between 1 and 3 pixels (for MIPs)
Cluster size and detection efficiency as function of the impinging point of the track within area of 2x2 pixels

- for reverse bias of -3V, threshold of \(\sim 180e^-\) (high for ALPIDE!), 6GeV/c pions

- Cluster size strongly depending on impinging point: \(\sim 1\) in pixel centers, \(\sim 4\) in pixel corners

- At higher thresholds, detection efficiency first starts to drop in pixel corners \(\leftrightarrow\) almost equal charge sharing between 4 pixels
3. Selected results

Cluster shapes as function of the impinging point of the track within area of 2x2 pixels

- for reverse bias of -3V, threshold of ~180e⁻ (high for ALPIDE!), 6GeV/c pions
1. Introduction

2. ALPIDE telescope

3. Selected results

4. Summary and future developments
4. Summary and future developments

- Successfully designed and operated a 7-plane beam telescope fully consisting of ALPIDE chips
  - With 6GeV/c pions, a track resolution at the Device Under Test (DUT) of 2-3μm was reached
  - Setup highly automated: about 1000 runs, each with a different setting (threshold, reverse substrate bias, integration time, etc.), could be performed in 10 days without presence of a shift crew

- ALPIDE is very suitable chip for beam telescopes
  - Can be thinned down to only 50μm (0.05%x/X₀), making it suitable for high-resolution beam telescopes even at low beam energies
  - 3cm x 1.5cm in size
  - Spatial resolution of ~5μm
  - Event-time resolution of <4μs (a single additional plane with better timing resolution could easily be added to improve this)
  - Global shutter architecture
Future developments

4. Summary and future developments

- **Hardware:**
  - 9-plane telescope with high-speed back plane
    - Plane distance of only 1 cm
    - Using ITS Inner Barrel module readout topology with 9 1.2 Gbit/s serial links
    - Connected via firefly cable (up to 5 m) to ITS Readout Unit (RU) prototype
    - RU connected via USB-3.0 to PC
  - Test beam with ITS modules

- **Software:**
  - Generalise EUDAQ producer to
    - our other readout systems (including the Readout Unit)
    - cover both single chips and modules
  - Update our analysis code w.r.t. general EUTelescope developments

- **High precision measurements with different angles of beam incidence**
  - First tries with summer student last summer, but desired track resolution not yet achieved
  - Setup (plane distances) to be optimized, go to SPS to reduce multiple scattering
  - Analysis software
BACKUP
ALICE ITS pixel chip requirements

2. ALPIDE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Inner Barrel</th>
<th>Outer Barrel</th>
<th>ALPIDE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon thickness</td>
<td>50μm</td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>Spatial resolution</td>
<td>5μm</td>
<td>10μm</td>
<td>~5μm</td>
</tr>
<tr>
<td>Chip dimension</td>
<td>15mm x 30mm</td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>Power density</td>
<td>&lt; 300mW/cm²</td>
<td>&lt; 100mW/cm²</td>
<td>&lt; 40mW/cm²</td>
</tr>
<tr>
<td>Event time resolution</td>
<td>&lt; 30μs</td>
<td></td>
<td>~2μs</td>
</tr>
<tr>
<td>Detection efficiency</td>
<td>&gt; 99%</td>
<td>✔</td>
<td></td>
</tr>
<tr>
<td>Fake hit rate</td>
<td>&lt; 10⁻⁵/event/pixel</td>
<td></td>
<td>&lt;&lt;&lt; 10⁻⁶/event/pixel</td>
</tr>
<tr>
<td>NIEL tolerance</td>
<td>1.7x10¹² 1MeV nₑq/cm²</td>
<td>10¹¹ 1MeV nₑq/cm²</td>
<td>&gt;1.7x10¹³ 1MeV nₑq/cm²</td>
</tr>
<tr>
<td>TID tolerance</td>
<td>270krad</td>
<td>10krad</td>
<td>&gt;500krad</td>
</tr>
</tbody>
</table>

• ALPIDE fulfills or surpasses pixel-chip requirements of the ALICE ITS upgrade
• ALPIDE development represents significant advancement of MAPS regarding power density, fake-hit rate, readout speed, and radiation hardness
ALPIDE: Process technology
1. Introduction

TowerJazz 180nm CMOS imaging sensor process:

• High-resistivity (>1kΩcm) p-type epitaxial layer (18μm-40μm) on p-type substrate (~10Ωcm)
• Deep p-well for full CMOS circuitry within the matrix
• Feature size 180nm and 6 metal layers ➔ dense circuitry

Sensor only partially depleted ➔ application of moderate reverse bias $V_{BB}$ (<6V) possible via the substrate

Signal from collection diode: $\Delta V \sim Q/C$

• particular focus put on low pixel-input capacitance C
  ➔ values as low as 2fF achieved (signal of 80mV for 1000e⁻)

Charge collection time: ~1-30ns

• depending on size of depletion zone (reverse substrate bias, collection diode geometry)
2. ALPIDE

ALPIDE in-pixel circuitry

- **Front-end**: continuously active, power consumption 40nW (9 transistors, full custom)
- **Multi-event memory**: 3 stages (62 transistors, full-custom)
- **Configuration**: masking and pulsing registers (31 transistors, full-custom)
- **Testing**: analog and digital test pulse circuitry (17 transistors, full-custom)
- **Matrix read-out**: priority encoder, asynchronous, hit-driven
Q/C ratio and sensor design parameters

2. ALPIDE

Sensor performance mainly determined by:

- Pixel pitch
- Collection n-well size
- Spacing between the collection n-well and surrounding (deep) p-well
- Epitaxial layer thickness and resistivity
- Reverse bias voltage $V_{BB}$ on the collection diode

- Sensor optimization studies mainly by small-scale prototypes with analog readout
- During design of ALPIDE, particular focus put on low pixel-input capacitance $C$
  - values as low as 2fF achieved (signal of 80mV for 1000e⁻)

Parameters selected for ALPIDE (29μm x 27μm pixel size):

- 25μm epitaxial layer
- 2μm n-well diameter, 3μm spacing
  - 88% of pixel surface can be used for circuitry
Sensor optimization – Pixel-input capacitance

2. ALPIDE

Pixel input capacitance significantly decreased with increasing $|V_{BB}|$
- $\sim 5\,\text{fF}$ for $V_{BB}=0\,\text{V}$ $\Rightarrow$ $\sim 2.5\,\text{fF}$ for $V_{BB}=-6\,\text{V}$

Epitaxial layer resistivity
- No influence in range between $1\,\text{k}\Omega\,\text{cm}$ and $7.5\,\text{k}\Omega\,\text{cm}$ with current pixel layout

Collection diode geometry
- smaller collection n-well, larger spacing $\Rightarrow$ smaller pixel input capacitance at large $V_{BB}$
Sensor optimization – Epitaxial layer thickness

2. ALPIDE

Prototypes produced on wafer with different epitaxial layer thickness and resistivity

- increasing epitaxial layer thickness:
  - generated charge (matrix signal) increases linearly
  - cluster size increases non-linearly

Optimum epitaxial layer thickness depending on achievable depletion volume

- depending on $V_{BB}$ and geometry

Parameters selected for ALPIDE: 25µm epitaxial layer, 2µm n-well diameter, 3µm spacing
ALPIDE: Floor plan

1. Introduction

Features:
- Dimension: 30mm x 15mm (1024 x 512 pixels)
- Pixel pitch: 29μm x 27μm
- Thinned to 50μm or 100μm
- Global shutter: triggered acquisition (up to 200 kHz Pb-Pb, 1MHz pp) or continuous (progr. integration time: 1μs - ∞)

Concepts:
- In-pixel amplification
- In-pixel hit discrimination
- In-pixel 3-level event memory
- In-matrix zero-suppression

26/01/2016
J.W. van Hoorne, CERN
Front-end acts as delay line

- Sensor and front-end continuously active
- Upon particle hit front-end forms a pulse with peaking time of 2-4\(\mu\)s (\(<\rightarrow\) time walk)
  - charge collection time \(< 30\text{ns}\) \(\rightarrow\) long pulse duration a choice made for ALICE ITS: functioning as delay line and reduce power consumption (40nW/pixel) \(<\rightarrow\) material budget
- Threshold is applied to form a binary pulse
  - globally set by front-end bias DACs
- Hit is latched into memory if STROBE is applied during binary pulse
  - Global shutter: triggered (up to 200 kHz Pb-Pb, 1MHz pp) or continuous (progr. integration time: 1\(\mu\)s - \(\infty\))
1. Introduction

- Threshold globally adjustable via on-chip DACs
- **Good threshold uniformity**
  - Threshold RMS 10-15% of average threshold
- **Very low noise values**
  - 5-6e- without reverse substrate bias, 2-3e- with
- **Large threshold-to-noise ratio**
  - Fake-hits due to Gaussian noise extremely rare
- **Large operational margin**
  - MIPs release in order of 1600e- (MPV) in sensitive layer (Landau fluctuations, charge sharing also to be considered.)
Performance after NIEL and TID irradiation

2. ALPIDE

Detection efficiency and fake-hit rate

- Sufficient operational margin after $1.7 \times 10^{13}$ 1MeV n/cm$^2$ (10 times life time dose of upgraded ITS)
Performance after NIEL and TID irradiation

2. ALPIDE

Position resolution and cluster size

- Cluster sizes and position resolution slightly reduced after $1.7 \times 10^{13}$ 1MeV n/cm$^2$ (10 times lifetime dose of upgraded ITS)
  - Resolution remains around desired 5μm in threshold range with detection efficiency > 99%
Matrix readout by hit-driven asynchronous circuit (priority encoder) in double-columns:

- sequentially provides addresses only of hit pixels \(\Rightarrow\) in-matrix zero suppression, fast
- no activity if not hit (no free running clock) \(\Rightarrow\) low-power matrix readout (\(~2\text{mW})

- Readout time: 1 clk cycle (20MHz) for one hit
- Minimum event size: chip header (16bit), region header (8bit), short data(16bit), trailer (8bit) \(\Rightarrow\) 48 bit
1. Introduction

- ALICE prepares major upgrade of experimental setup in LS2 of LHC in 2019/2020
- Targets:
  - Large sample of recorded events: 10 nb\(^{-1}\) Pb-Pb plus pp and p-Pb data -> gain factor 100 in statistics over originally approved program
  - Significant improvement of tracking and vertexing capabilities at low \(p_T\)

6 layers:
- 2 layers silicon pixel (SPD)
- 2 layers silicon drift (SDD)
- 2 layers silicon strips (SSD)

ALICE prepares major upgrade of experimental setup in LS2 of LHC in 2019/2020

Targets:
- Large sample of recorded events: 10 nb\(^{-1}\) Pb-Pb plus pp and p-Pb data -> gain factor 100 in statistics over originally approved program
- Significant improvement of tracking and vertexing capabilities at low \(p_T\)

also present ITS needs to be upgraded!
ITS upgrade: design objectives

1. Introduction

Improve pointing resolution by a factor \( \sim 3 \) in r-\( \phi \) and \( \sim 5 \) in z at \( p_T = 500 \text{MeV/c} \) (~40 \( \mu \text{m} \) at \( p_T = 500 \text{ MeV/c} \))

- reduce beam pipe radius: 29mm \( \rightarrow \) 19mm
- get closer to IP: 39mm \( \rightarrow \) 22mm (innermost layer)
- reduce material budget: \( \sim 1.14\% \times X_0 \rightarrow \sim 0.3\% \times X_0 \) (inner layers)
  \( \Rightarrow \) less material \( \Rightarrow \) reduce power consumption
- reduce pixel size: 50x425\( \mu \text{m}^2 \) \( \Rightarrow \) \( O(30\times30\mu\text{m}^2) \)

Improve tracking efficiency and \( p_T \)-resolution at low \( p_T \)

- increase granularity: 6 layers \( \rightarrow \) 7 layers, only pixel sensors

Fast readout

- readout of Pb-Pb at up to 100 kHz (presently 1kHz) and 400kHz for pp

Fast insertion/removal of detector modules

- possibility to replace non-functioning detector modules during yearly shutdown

\( \Rightarrow \) Decision to fully replace present ITS
7-layer geometry:

- r-coverage: 23 mm - 400 mm
- $\eta$-coverage: $|\eta| \leq 1.22$ for tracks from 90% luminous region

- 3 Inner Barrel layers: 0.3% $x/X_0$ per layer
- 4 Outer Barrel layers: 1% $x/X_0$ per layer
1. Introduction

Inner Barrel stave

Flexible PCB

9 sensors

Cold Plate

Space Frame

Inner barrel module (x48):
• 9 chips, each read out using 1.2 Gb/s link

Outer Barrel

Power Bus

Flexible PCB

2 x 7 sensors

Cold Plate

Space Frame

Half-Stave

Half-Stave

Outer barrel module (x1800)
• 2×7 chips (1 master, 6 slaves), locally interconnected, read out using 2×400 Mb/s links
Module assembly

1. Introduction

Module (HIC – hybrid integrated circuit): chips glued and wire-bonded to flexible PCB

Chip placement + gluing to flexible PCB

- Placement is handled by automated custom-made machine (distributed to 6 assembly sites worldwide)
- Flexible PCB is glued to chips

Wire bonding

- Chips are wire bonded through vias in the FPCB distributed over full chip surface
1. Introduction

Detector readout

Detector

- Readout logic fully integrated into ALPIDE
- ALPIDE can directly drive 5m cables using integrated high-speed transmitters (up to 1.2 Gb/s)
- No further electronics on detector

5m cable

- 1.2 Gb/s (data IB)
- 400 Mb/s (data OB)
- 80 Mb/s (ctrl IB/OB)
- Clock
- Power

Readout units

- Total: 192 Readout Units
- Distribute trigger and control signals
- Interface data links to ALICE DAQ
- Control power supplies of chips
ALPIDE: Power consumption

2. ALPIDE

Data: combination of available measurements and simulations
Values scaled for readout at 100 kHz rates and max occupancies
Clock gating enabled
3. Future developments

- **INVESTIGATOR**: dedicated test chip developed within ALPIDE R&D phase, designed for systematic studies on influence of design parameters on sensor characteristics

- Consists of 134 matrices of 8x8 pixels (“mini-matrices”, MM)
  - Various pixel sizes (20x20\(\mu m^2\) to 50x50\(\mu m^2\)) and collection electrode designs (n-well size, spacing)

- Each of the mini-matrices can be selected and connected to a set of 64 output buffers (~10ns rise time)
  - All 64 pixels of a mini-matrix can be read out in parallel, allowing for continuous parallel signal sampling
  - Possibility of measuring evolution of a cluster, i.e. charge collection time in each pixel
  - Dedicated 64-channel readout system developed, sampling at 65MHz

- Chips produced on different wafers with epi-layer thickness between 18\(\mu m\) and 30\(\mu m\), and in different process variants (std, mod)
  - Samples tested up to \(10^{15}\) 1MeV \(n_{eq}/cm^2\) and 1Mrad

<table>
<thead>
<tr>
<th>MM address</th>
<th>Pixel pitch [(\mu m)]</th>
<th>Number of MM (per pitch)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 - 35</td>
<td>20</td>
<td>36</td>
</tr>
<tr>
<td>36 - 57</td>
<td>22</td>
<td>22</td>
</tr>
<tr>
<td>58 - 67</td>
<td>25</td>
<td>10</td>
</tr>
<tr>
<td>68 - 103</td>
<td>28</td>
<td>36</td>
</tr>
<tr>
<td>104 - 111</td>
<td>30</td>
<td>8</td>
</tr>
<tr>
<td>112 – 123</td>
<td>40</td>
<td>12</td>
</tr>
<tr>
<td>123 - 134</td>
<td>50</td>
<td>10</td>
</tr>
</tbody>
</table>
3. Future developments

- Precise charge-collection time measurements performed using differential probe and fast scope on single pixel

- Fit of waveforms with function:
  
  \[
  \begin{align*}
  t & \leq t_0, & f &= a + m \cdot (t - t_0) \\
  t & > t_0, & f &= a + m \cdot (t - t_0) - b \cdot (e^{-\frac{t-t_0}{\tau}} - 1)
  \end{align*}
  \]

- ALPIDE-like pixel studied: 28μm pitch, 2um n-well diameter, 3μm spacing, 25μm epi
- Measurements performed with \(^{55}\text{Fe}\)
Charge-collection time measurements with X-Rays

3. Future developments

For X-Ray absorption in sensor fabricated with the std process three cases can be defined:

1. Absorption in depletion volume: charge collected by drift, no charge sharing, single pixel clusters
   - Events of this case populate the calibration (K-α) peak in signal histogram
   - Charge collection time expected to be ≈ 1ns

2. Absorption in epitaxial layer: charge partially collected by diffusion and then drift, charge sharing between pixels depending on position of X-Ray absorption
   - Charge collection time expected to be dependent on distance of the X-Ray absorption from a depletion volume, and longer than for events of case 1

3. Absorption in substrate:
   - contribution depending on depth of X-Ray absorption position within substrate, and charge carrier lifetime within substrate

---

55Fe: two X-Ray emission modes:
1. K-α: 5.9keV (1640e/h in Si), relative frequency: 89.5%
   attenuation length in Si: 29μm
2. K-β: 6.5keV (1800e/h in Si), relative frequency: 10.5%
   attenuation length in Si: 37μm
Rise time ($\tau$):

Calibration (drift) peak: no charge sharing, signal collected by drift (in $\leq 1$ns)
- Rise time about equal for all values of $V_{BB}$, moreover about equal to buffer rise time
- Drift peak clearly visible in low-$V_{BB}$ rise time histograms, for larger $V_{BB}$ it overlaps with diffusion-drift peak

Charge-collection time - Standard process

3. Future developments

MM75: 28$\mu$m pitch, 2$\mu$m n-well diameter, 3$\mu$m spacing, 25$\mu$m epi

$V_{BB} = -1$V
$V_{BB} = -3$V
$V_{BB} = -6$V
Charge-collection time - Standard process

3. Future developments

MM75: 28μm pitch, 2um n-well diameter, 3μm spacing, 25μm epi

\[ V_{BB} = -1V \] \[ V_{BB} = -3V \] \[ V_{BB} = -6V \]

Charge sharing – signal collected partly by diffusion and then drift
- Larger rise times with decreasing signal clearly visible in low-\(V_{BB}\) measurements
- Less clear in high-\(V_{BB}\) measurements (larger depletion volumes)

Rise time (\(\tau\)):