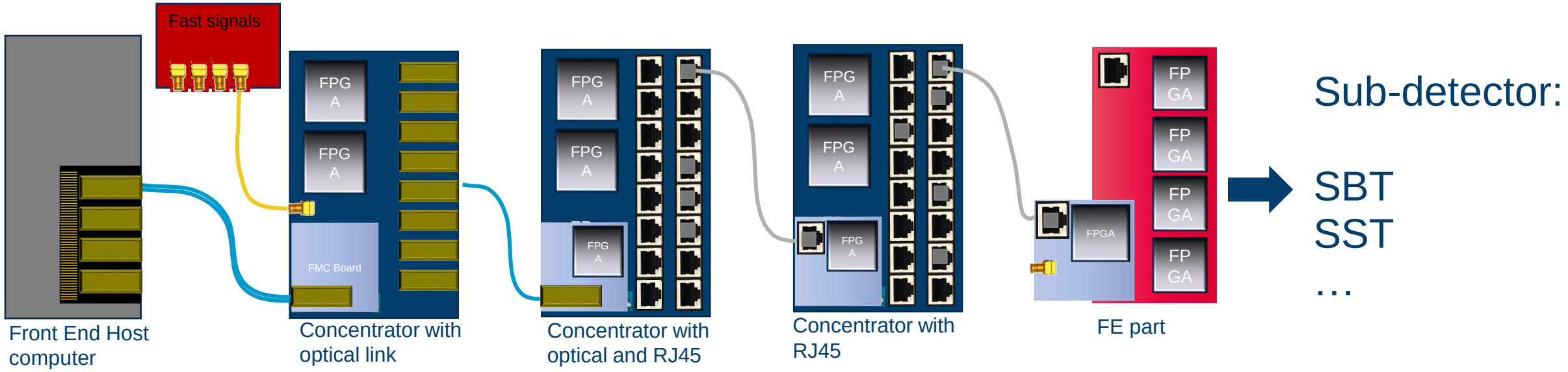
SBT/SST FRONT-END ELECTRONICS CONCEPT

27.03.2020 I C. GREWING, D.ARUTINOV

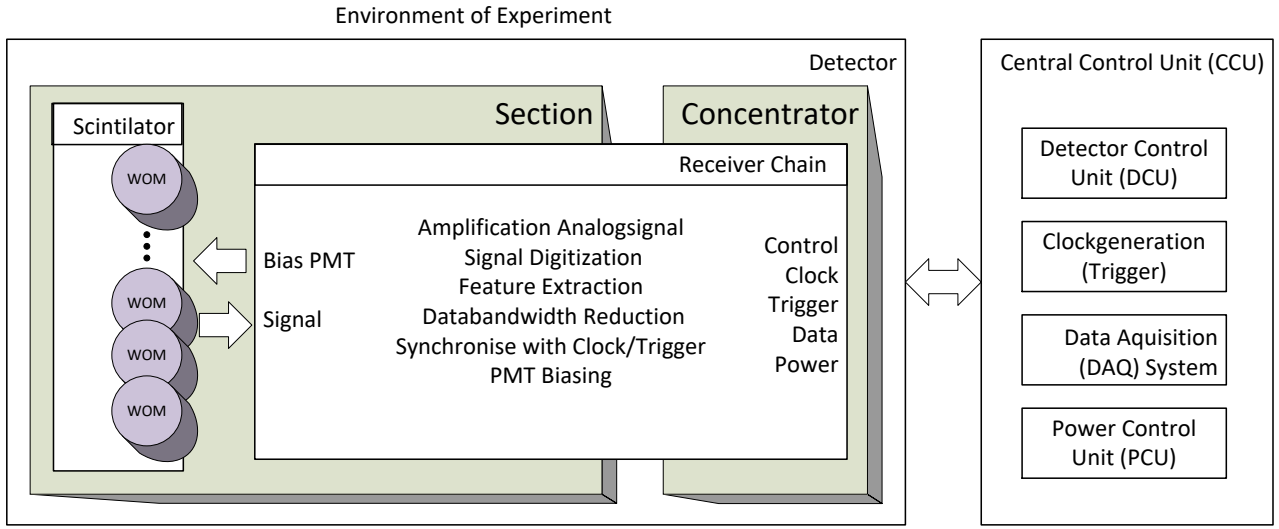
SUB DETETECTOR ELECTRONICS CONFIGURATION

ALL POSSIBLE OPTIONS

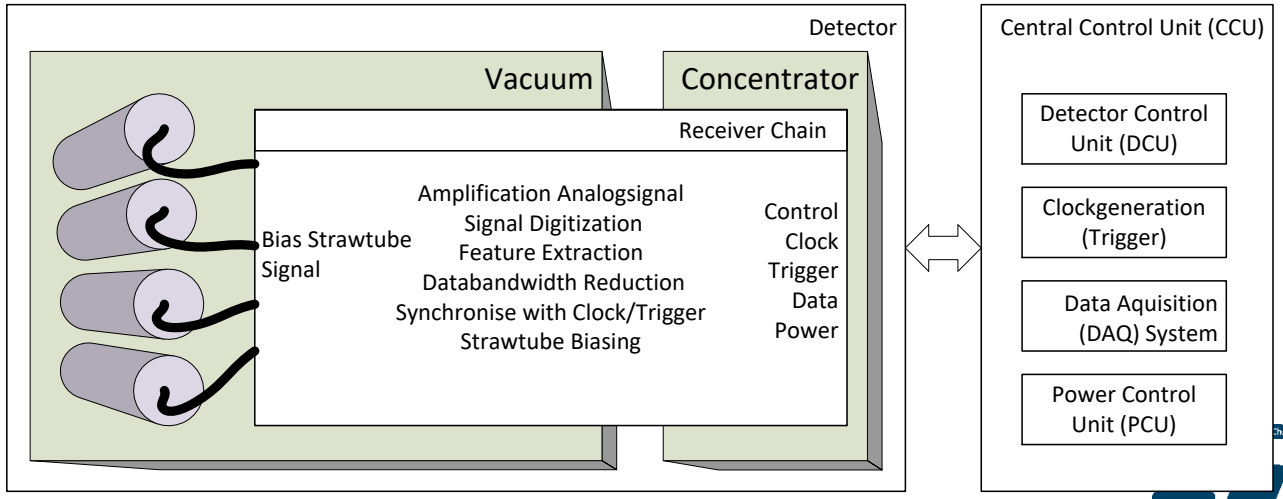


RECEIVER CHAIN (RX-CHAIN) DEFINITION

SBT:



SST:



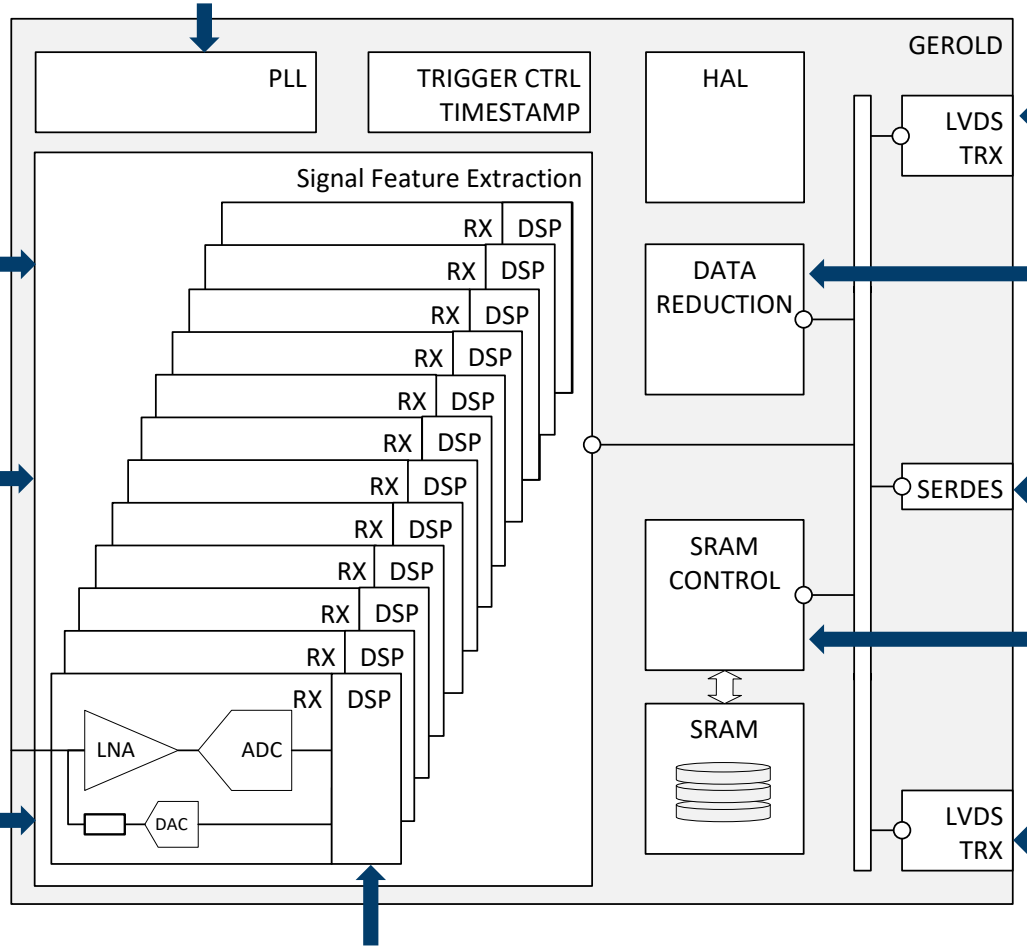
GEROLD: SIGNAL FEATURE EXTRACTION (SFE) HUB

Internal Clock Generation

12 ADC in one ASIC, variable to combine for higher clock or ENOB

Programable Input Impedance 10 – 100Ohm

Programable Bias Built in Self Test



LVDS Interface to link up with other ASIC

Data ordered by timestamp and zerosuppression, feature extraction e. g. integration

Highspeed Interface to optical converter for up to 100m Data upload

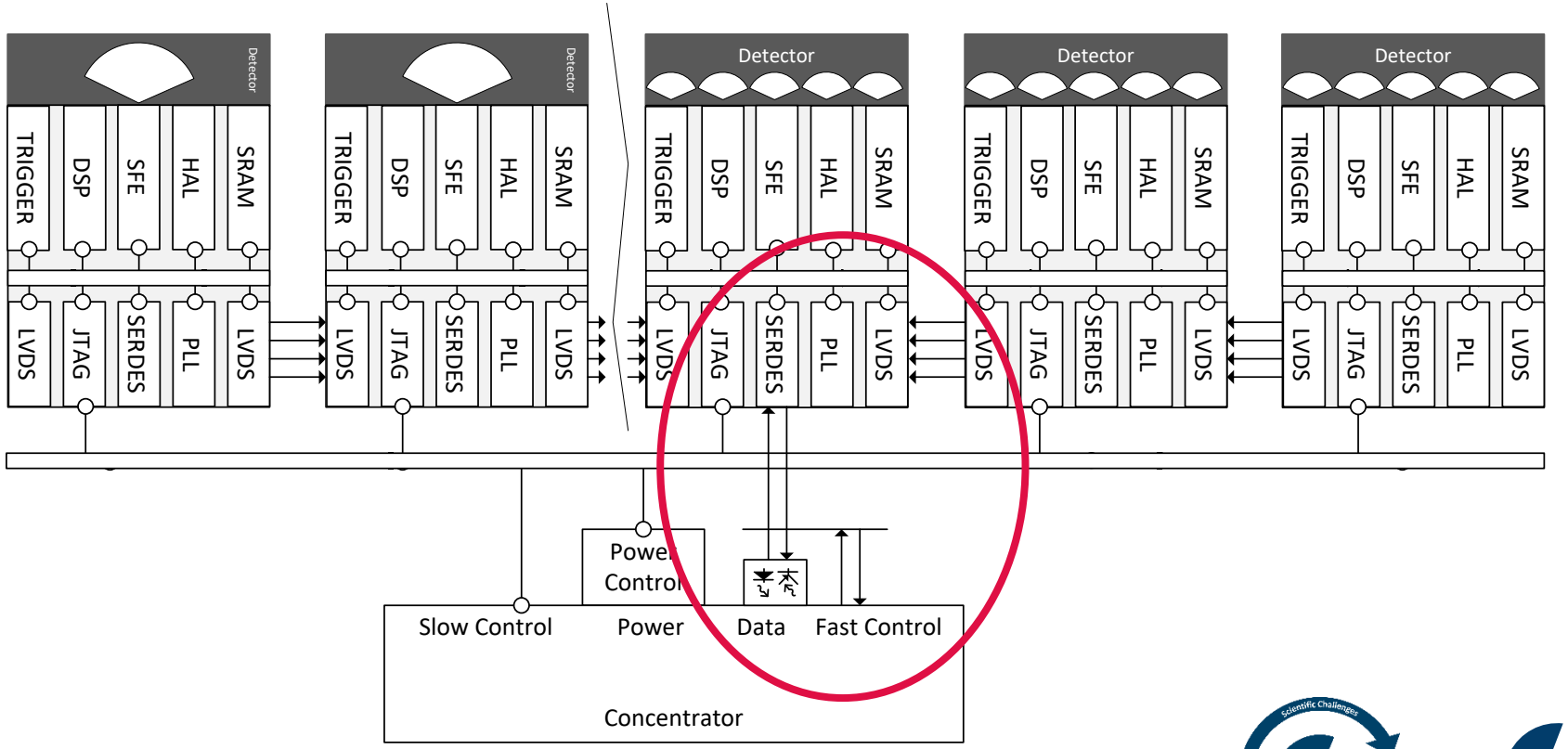
Built in SRAM Memory to lower Bandwidth requirment to average

LVDS Interface to link up with other ASIC

Calculation of TOA, Feature Extraction: Wavelet, TOT, Number of Hits,…

GEROLD: SIGNAL FEATURE EXTRACTION (SFE) HUB

- Frontends can be linked together to send information over one high speed data line
- Feature extraction like Energy Estimation for all Frontends in the link trigger data download
- Central trigger over fast control



GEROLD AS A SIGNAL CONVERTER HUB (CONT.)

SPECS:

- Analog inputs: 12
- Resolution: up to14 bits (ENOB: 6,5…12 bits)*
- Sampling rate: up to 1 GHz*
- Power: 60-100mW/Ch
- LVDS input/output: up to 1GHz (I/O)
- SERDES output: up to 2,5GHz (O)

FUNCTIONALITY:

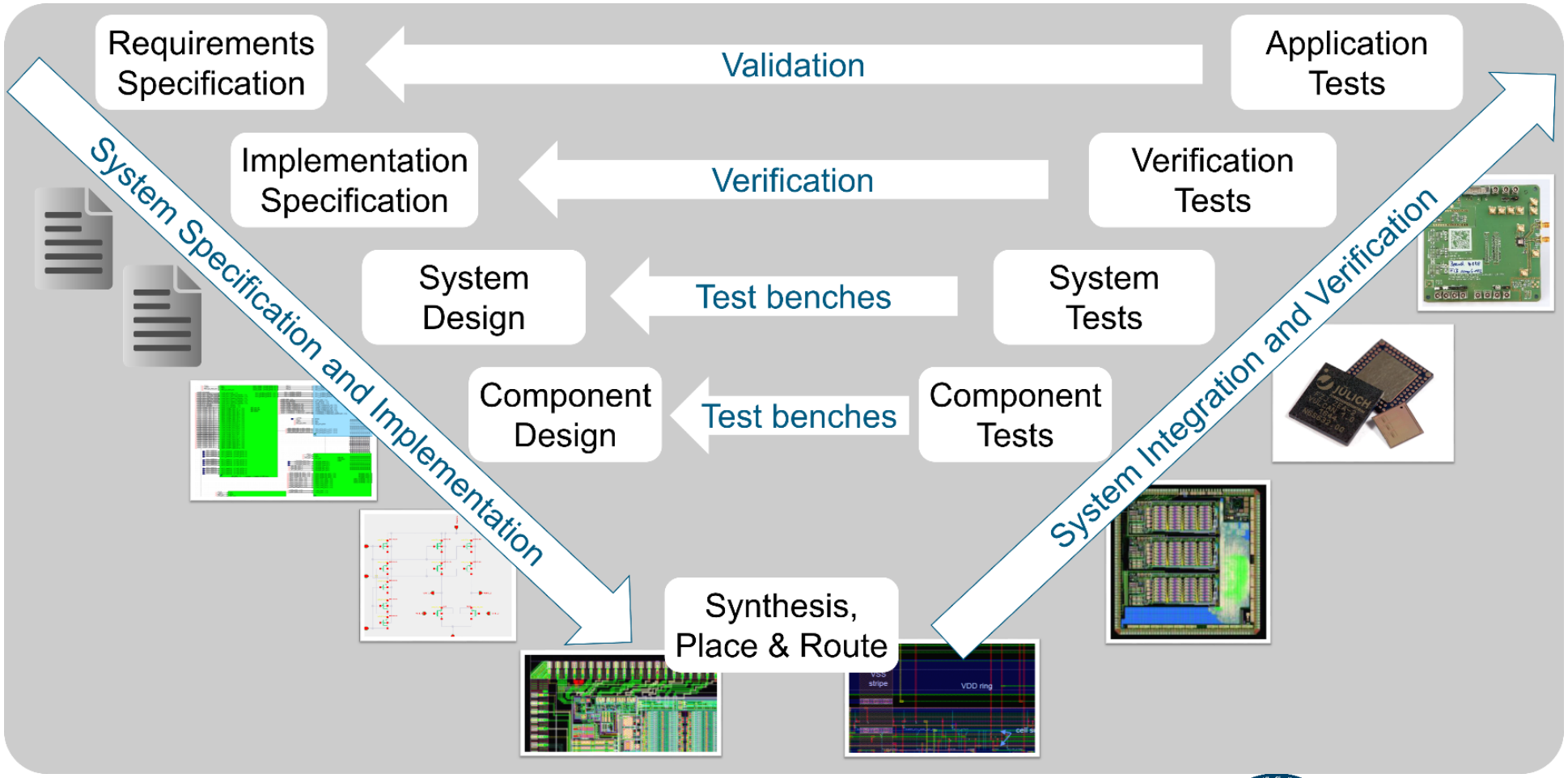
- Selectable Feature Extraction modes (ToT, Wavelets, number of hits…)
- Programmable resolution / sampling rate / # of inputs, impedance…
- ASICs can be linked

- **Specifications need to be defined early, IC design phase starts soon!!! Target: first proto – end of 2021**
- **IC architecture defines system architecture for RX Chain, after specs are defined no or few changes possible**
- **ZEA-2 responsible for IC Architecture**
- **All input is welcome**

*depends on # of inputs

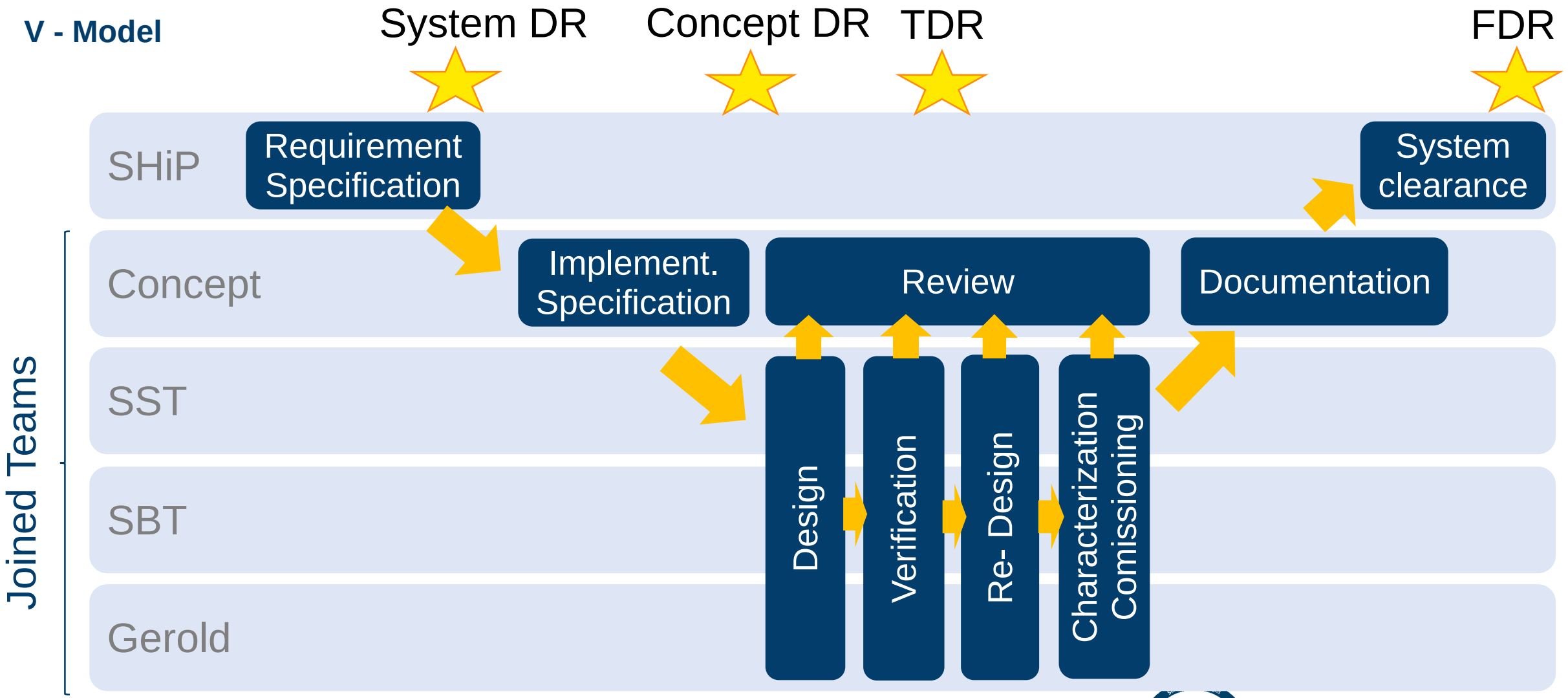
ZEA-2 – DEVELOPMENT FLOW

V - Model



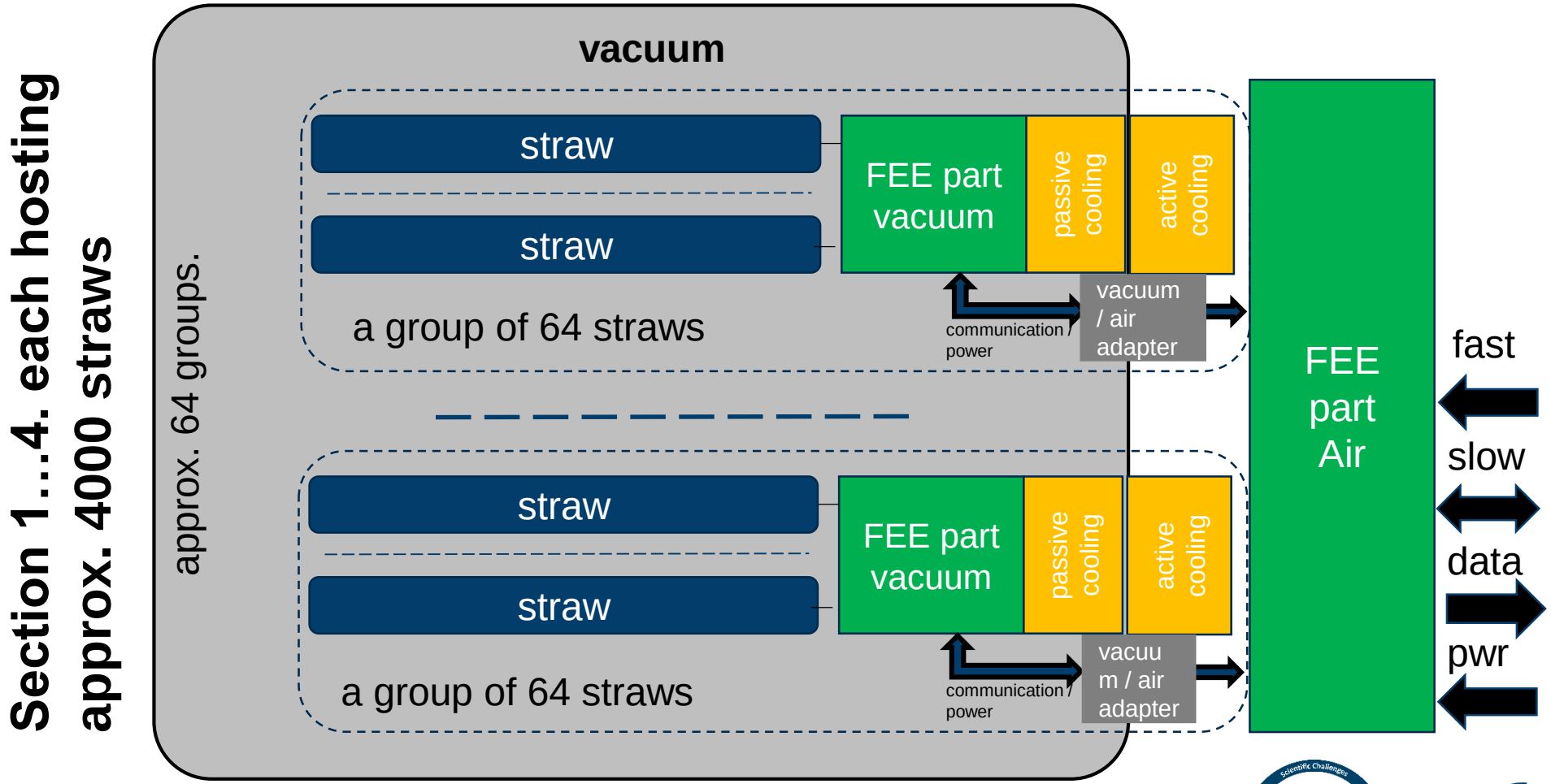
DEVELOPMENT PROCESS

V - Model



SST SECTION

Example configuration



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DATA / POWER CALCULATION FOR A SECTION 2.5Gb LINK

Section number	1 (closest to beam)	4 (outmost)
inputs/ic	12	12
hit rate / straw	3.900	1.100
data rate / straw (bit/s)	2.090.400	589.600
data rate / IC (bit/s)	25.084.800	7.075.200
data/hit (bit)	536	536

HIT-SAMPLE SIZE	
samples/event (ave) ?	70
bits/sample (bit)	7
timestamp (bit) ?	32
channel ID	14
sample size (bit)	536

less data for ToT, charge, wavelets, etc.

2.5Gb link vacuum/air		
ICs/2,5Gb LVDS	55	197
straws/2,5Gb LVDS	669	2374
data air/vacuum xing	**6**	**2**

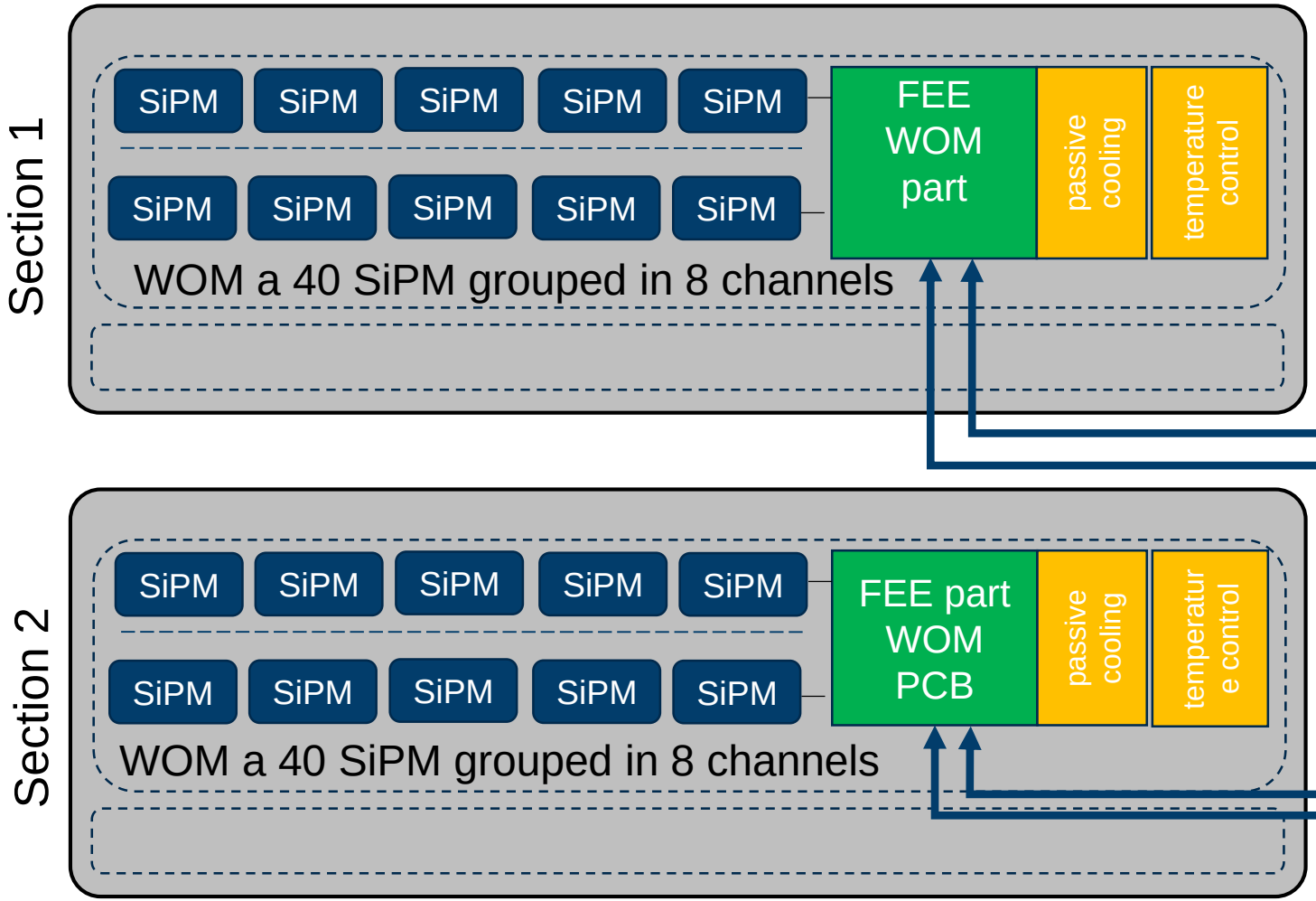
Total data rate (Gbit/s)	**6**

Total IC power (W)	400,0
N. of PoE connections (≥)	10,0

- Nr. of vacuum / air xings depends on section position
- For powering a serial solution can be used for the same reason
- 60% of payload is assumed

SBT SECTION

Example configuration 2



- total # of sections → 4000
- tradeoff between pwr. and resolution
- Several SiPMs / channel
- Material reduction, less connections to concentrators / DAQ

pwr
data

FEE Section part

- data collection from sections
- signal distribution
- data processing (e. g. clustering)

fast
slow
data
pwr

pwr
data

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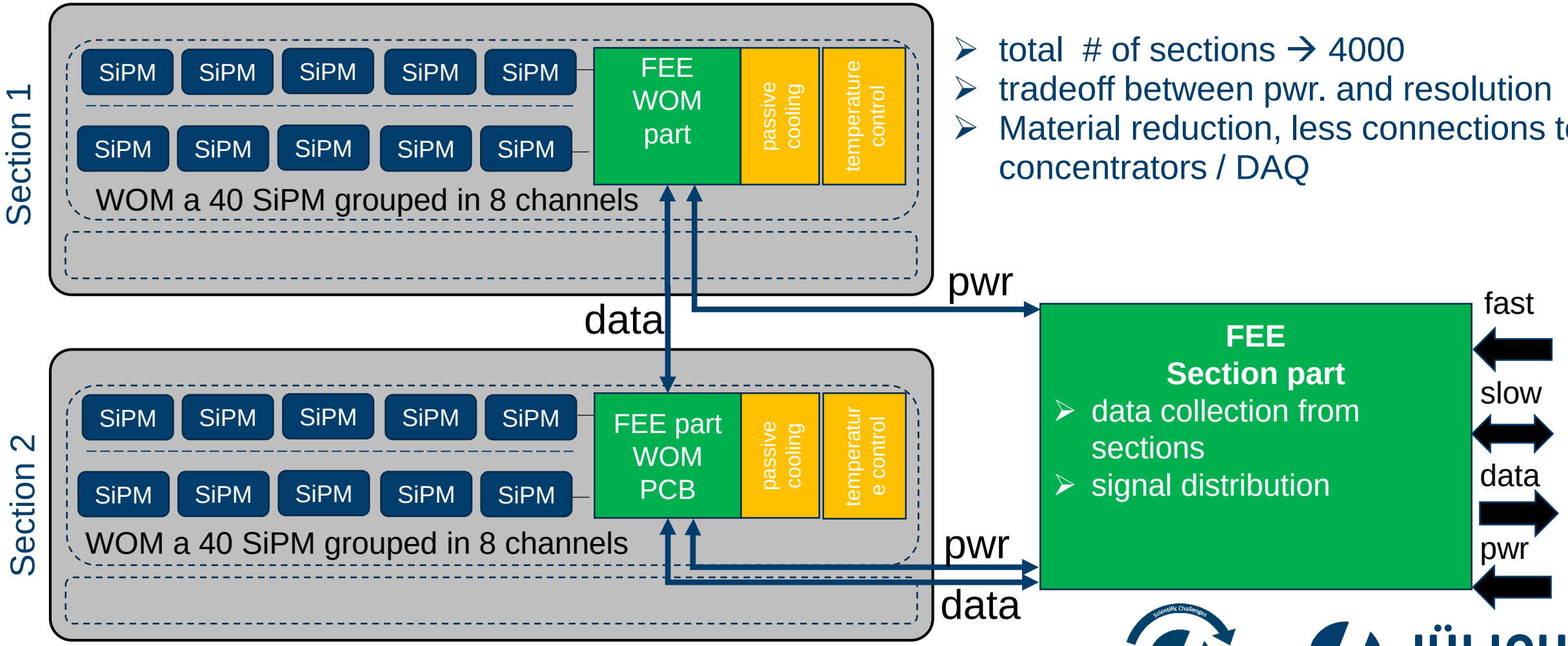
SBT SECTION

Example configuration 1



- total # of sections → 4000
- tradeoff between pwr. and resolution
- Material reduction, less connections to concentrators / DAQ

DATA / POWER CALCULATION FOR SBT:1WOM - 8CHANNEL

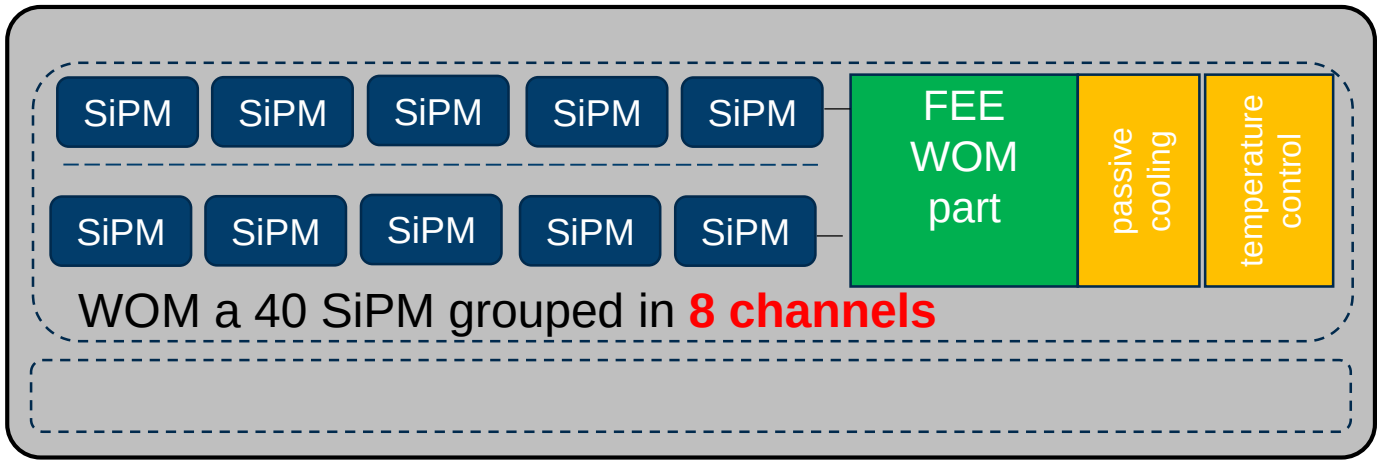
Section number	
inputs/ic	8
hit rate / input	250.000
data rate / input (bit/s)	17.750.000
data rate / IC (bit/s)	142.000.000
data/hit (bit)	71

HIT-SAMPLE SIZE	
samples/event (ave) ?	2
bits/sample (bit)	12
timestamp (bit) ?	32
channel ID	15
sample size (bit)	71

2.5Gb link	
ICs/2,5Gb LVDS	10
channels/2,5Gb LVDS	83
sections / 2,5 GB link	**6**

Total data rate (Gbit/s)	568,0

Total IC power (W)	4000,0



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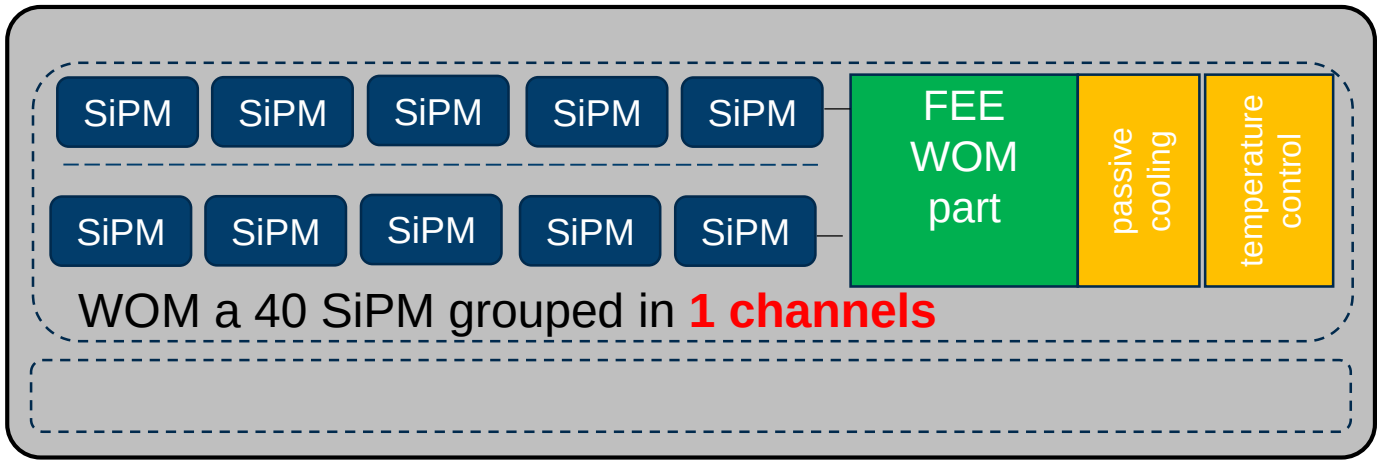
DATA / POWER CALCULATION FOR SBT:1WOM - 1CHANNEL

Section number	
inputs/ic	12
hit rate / input	250.000
data rate / input (bit/s)	17.000.000
data rate / IC (bit/s)	204.000.000
data/hit (bit)	68

HIT-SAMPLE SIZE	
samples/event (ave) ?	2
bits/sample (bit)	12
timestamp (bit) ?	32
channel ID	12
sample size (bit)	68

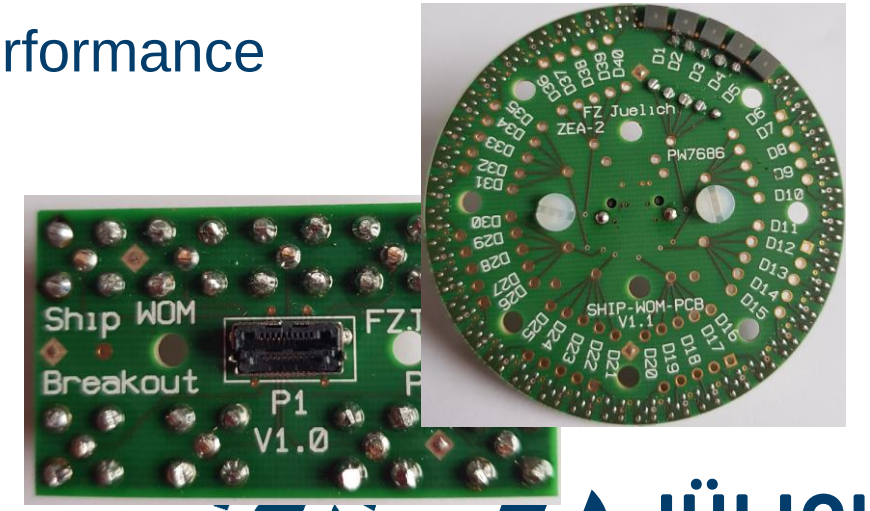
2.5Gb link	
ICs/2,5Gb LVDS	7
channels/2,5Gb LVDS	89
sections / 2,5 GB link	**45**
Total data rate (Gbit/s)	68,0
Total IC power (W)	666,0



Data rate and power decrease dramatically

STATUS ZEA-2 WORK AS OF YET

- Define realistic hit distribution in the detector
  - Tune data transfer rate accordingly and
  - Update the concept of the FE electronics
- Define FE functionality for both detectors
- Investigate the impact of power dissipation on straw performance
- Rough cooling concepts
- Straw-tube received from Hamburg, testing will follow
- New version of WOM PCB available, testing ongoing



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SUMMARY

- **Precondition because of to the ASIC design process:**
  - Top Down Approach (Requirement Specification with project clearance)
  - Early setting of all implementation details (Implementation Specification with project clearance)
- **Joined effort in the concept work of the RX chains**
  - Team up to get all requirements and optimal solutions
  - Various parts of the electronics (interfaces to concentrators, high voltage network, data protocols, FPGA programming for concentrators, etc.) are not defined yet, any help will be appreciated, join the development
  - Go for an early agreement and clearance on:
    - Requirement Specification for the RX Chain Q2/2020
    - Implementation Specification for all parts Q3/2020
  - No Architecture Decision in RX Chain or Responsibilities before specifications are cleared

Thank u!

We will appreciate any help in our work.

Please join !