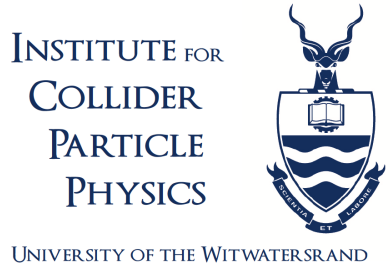

DAQ software implementation in the TileCal ALTI Module

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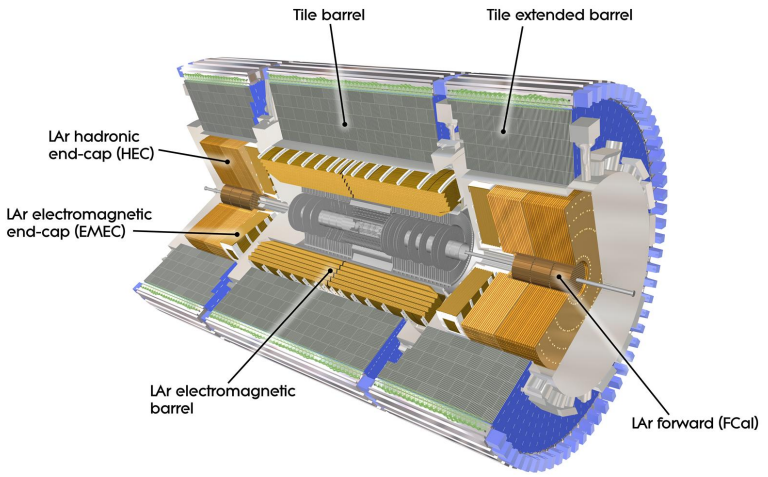
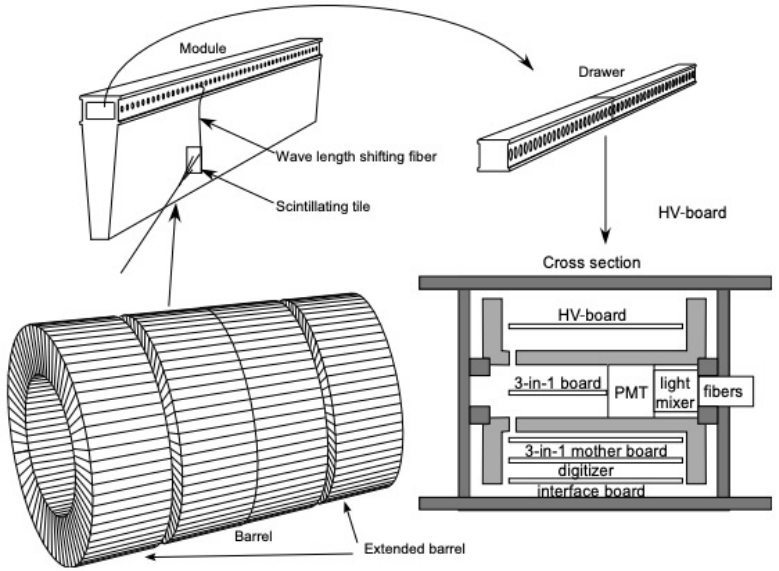
Overview

1. The Tile Calorimeter
2. Back-End read-out electronics
3. ALTI Module
4. ALTI Schematics
5. Tile Online software
6. Dependence graph
7. TileALTI GitLab project
8. Summary

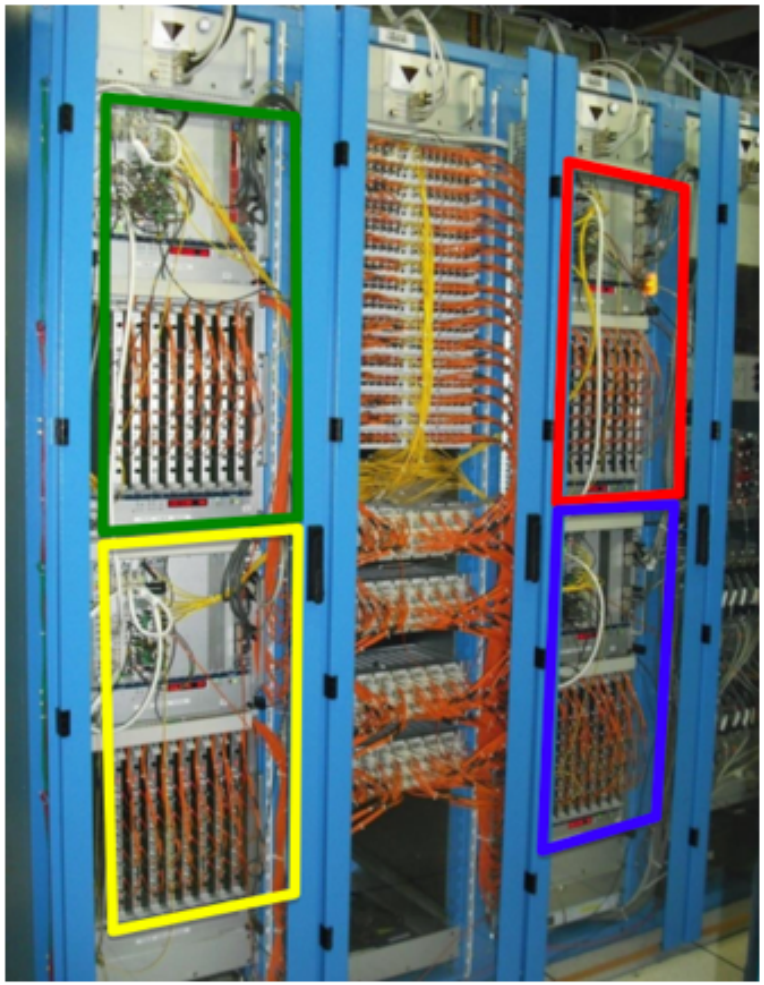
The Tile Calorimeter





- Central hadronic calorimeter ($|\eta| < 1.7$) in ATLAS detector
- Mechanically partitioned into 3 barrels, 2 extended barrels and 1 central long barrel
- Split into 4 partitions, 2 in long barrel and 1 for each extended barrel
- Each barrel is assembled out of 64 wedge-shaped modules staggered in the ϕ direction
- Each module is made up of steel and scintillating plastic tiles
- Double photomultiplier readout using wave length shifting fibers

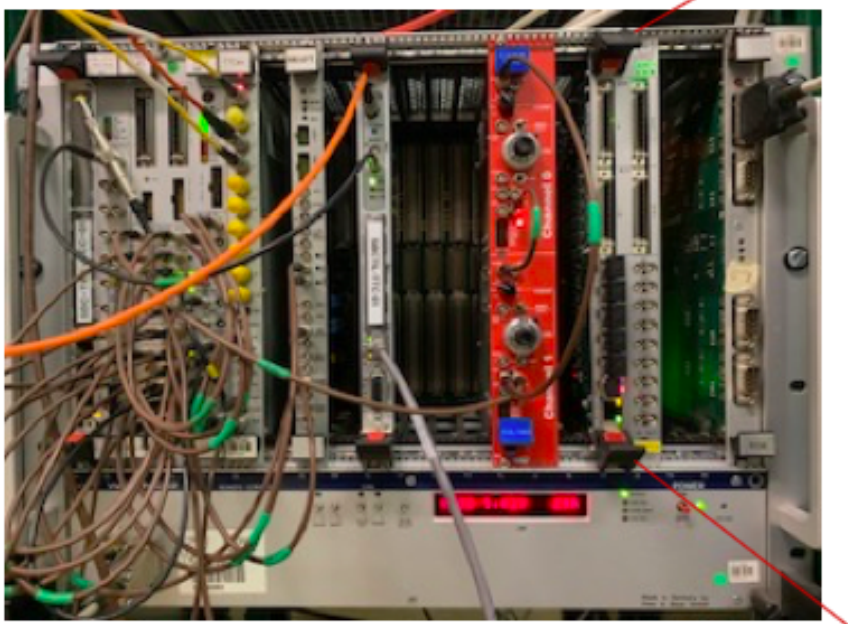
Back-End read-out electronics



- The TileCal BE read-out electronics in the ATLAS USA15 counting room consist of four partitions, while B175 test bench consists of one partition.

ALTI Module

TTC crate in the test bench



- ATLAS is replacing the ageing Timing Trigger and Control (TTC) hardware with newer electronics

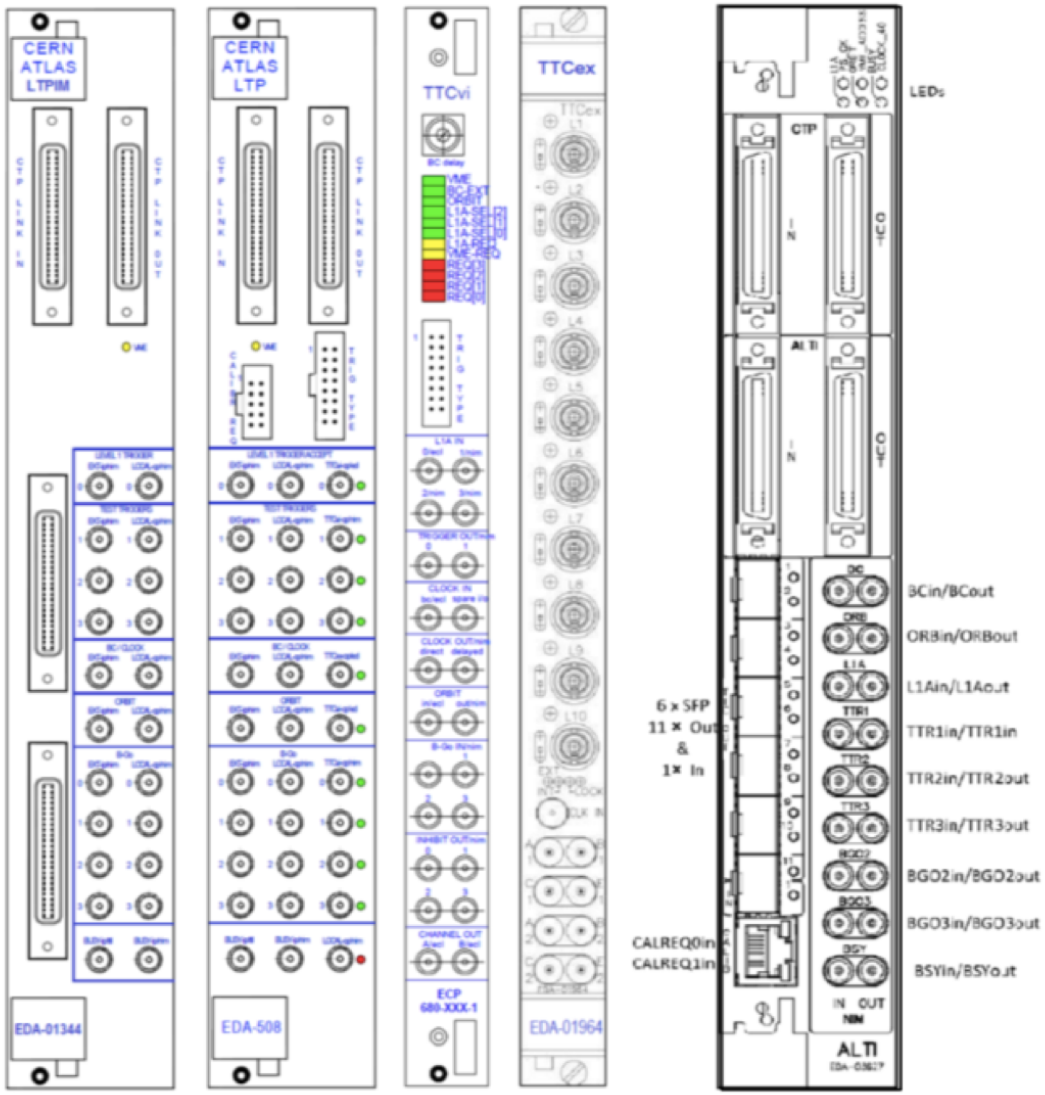
Main issues:

- new sub-detectors for the Phase-1 upgrade require TTC modules
- low on spares, just barely reaching the 10% per module type
- the TTC modules are now very old ($>$15 years) with obsolete components
- not possible to re-produce modules for new sub-detectors and for stocking-up spares cupboard
- ALTI (ATLAS Local Trigger Interface) module replaces the 4 legacy modules in the TTC crate (LTP, LTPi, TTCvi, TTCex)

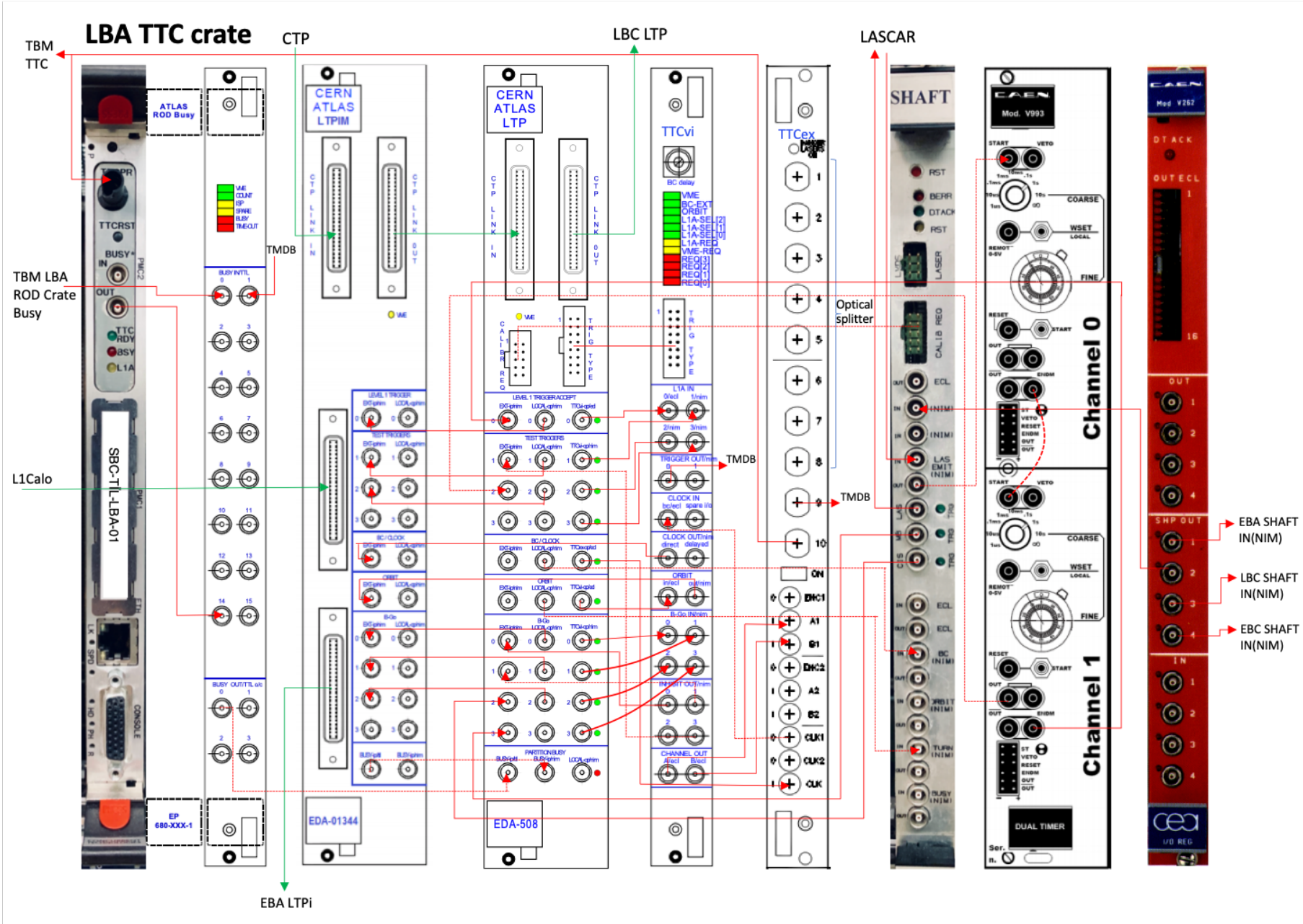
Main task:

- update the Tile Online software in order to make use of the ALTI board for the TTC and drawer configuration
- Run tests in B175 test bench and later in the USA15 counting room

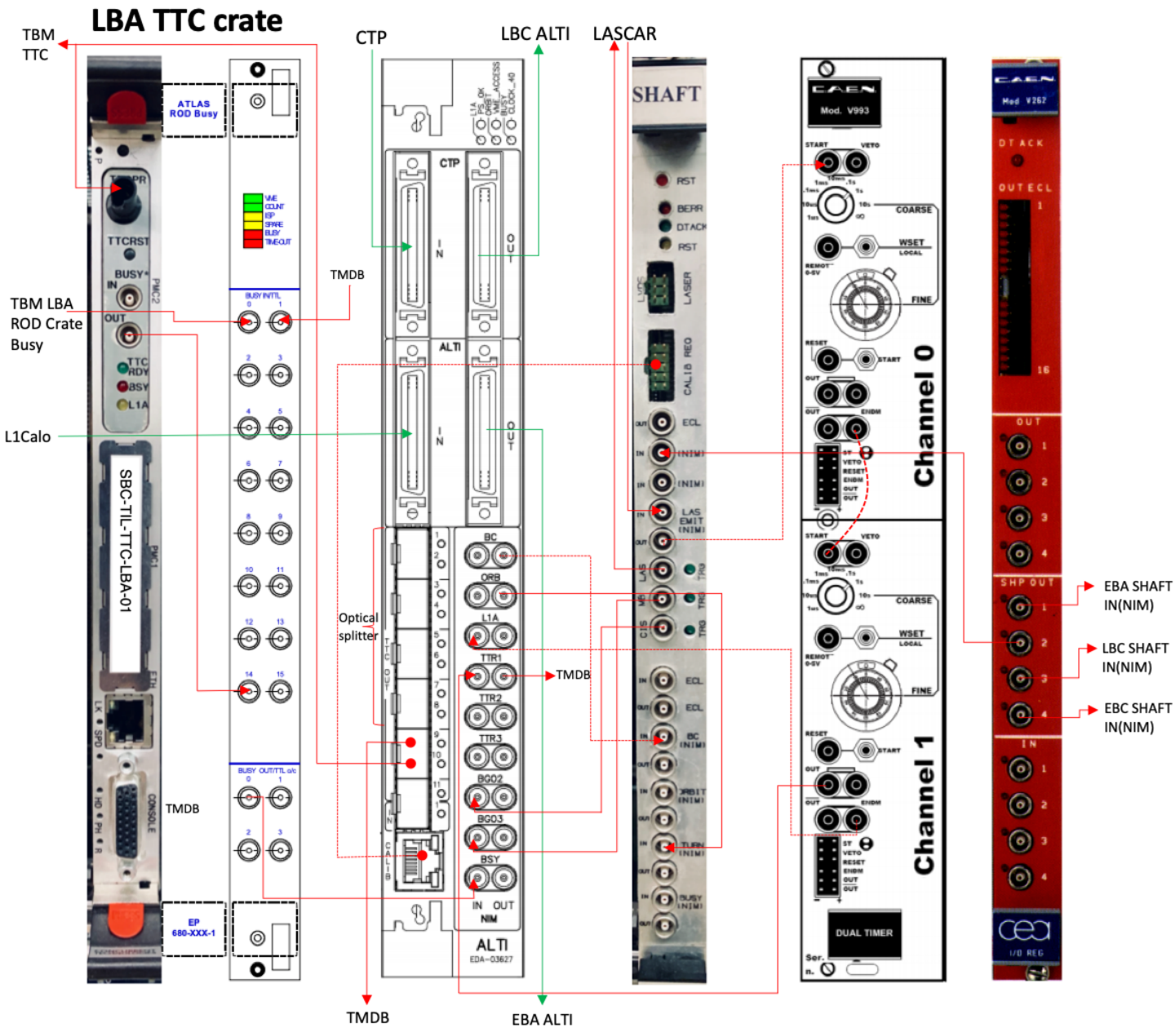
ALTI Schematics



- LTPi, LTP, TTCvi, TTCex and the ALTI module



- 4 of the TTC legacy modules, to be replaced with the ALTI module



- Functionalities of the 4 modules, integrated into the ALTI module

Tile Online software

A set of TDAQ software used for the operation of the Tile Calorimeter. It is built up of CMake packages which are stored in Gitlab (atlas-tile-online)
Tile Online Release projects are built on the TDAQ release

tile-07-01-02 on tdaq-07-01-00 [x86_64-slc6-gcc62-opt]

- Used in 2017/2018 data taking, HLT based on off-line 21.1.*
- To continue using it during LS2
- /afs/cern.ch/user/t/tiledaq/public/tilercd/tile-7.1.0.2

tile-8.2.0.0 [x86_64-slc6-gcc8-opt]

- LCG 95, HLT 22.0.1/2
- Includes ALTI package
- /afs/cern.ch/user/t/tiledaq/public/tilercd/tile-8.2.0.0
- /afs/cern.ch/atlas/project/TicalOnline/tilercd/tile-8.2.0.0 (B175 test bench)

tile-8.3.1.0 [x86_64-centos7-gcc8-opt] $\longrightarrow$ B175 test bench

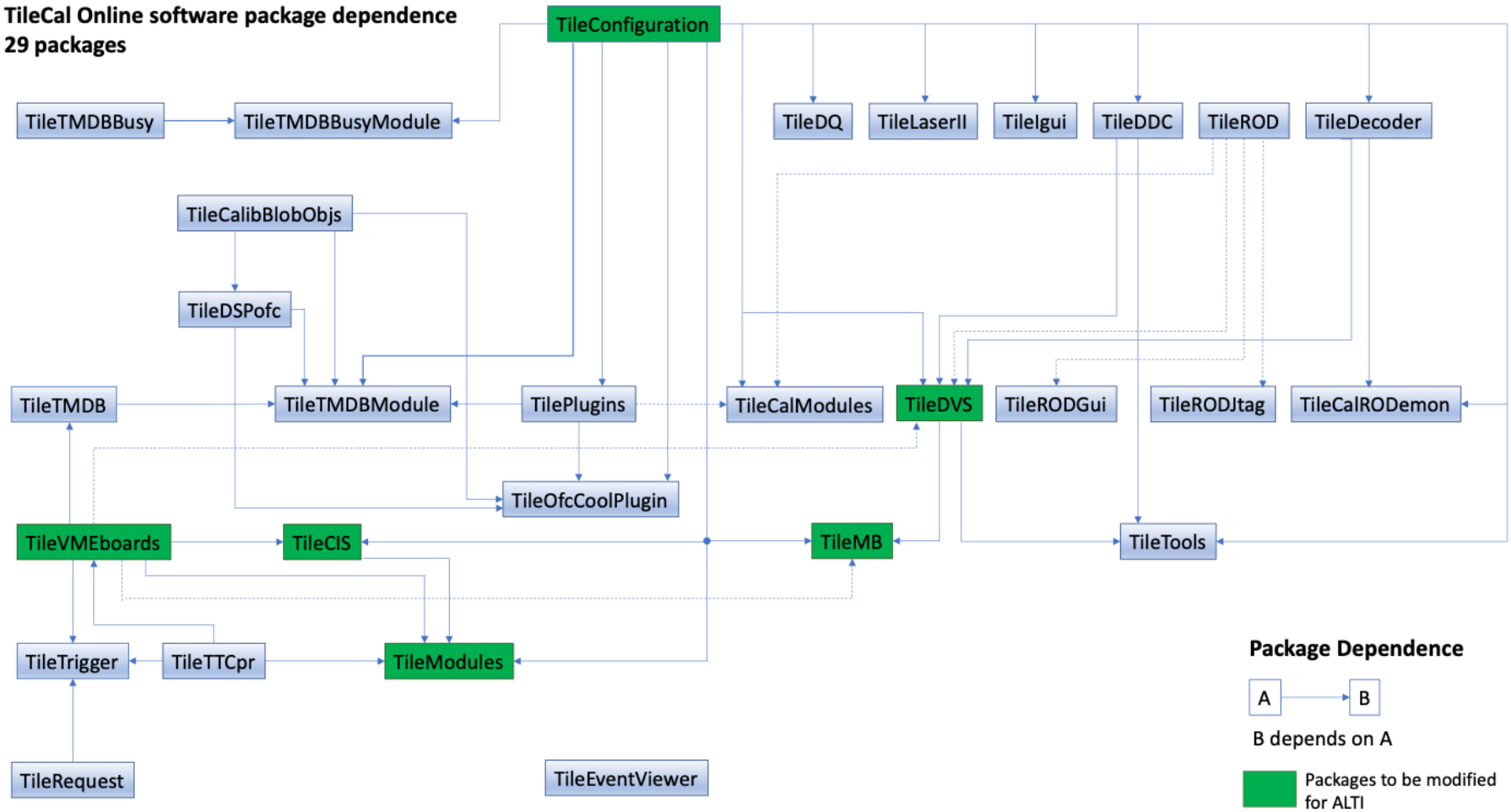
- LCG 96, HLT 22.0.3
- Includes ALTI package
- /afs/cern.ch/atlas/project/TicalOnline/tilercd/tile-8.3.1.0

Next after **tdaq-08-03-01 is tdaq-09-*** in 2020
B175 ROD lab machines migrated from SLC 6 to CentOS 7
Plan to migrate all TileCal machines to CentOS 7
The ALTI software is organised into two levels:

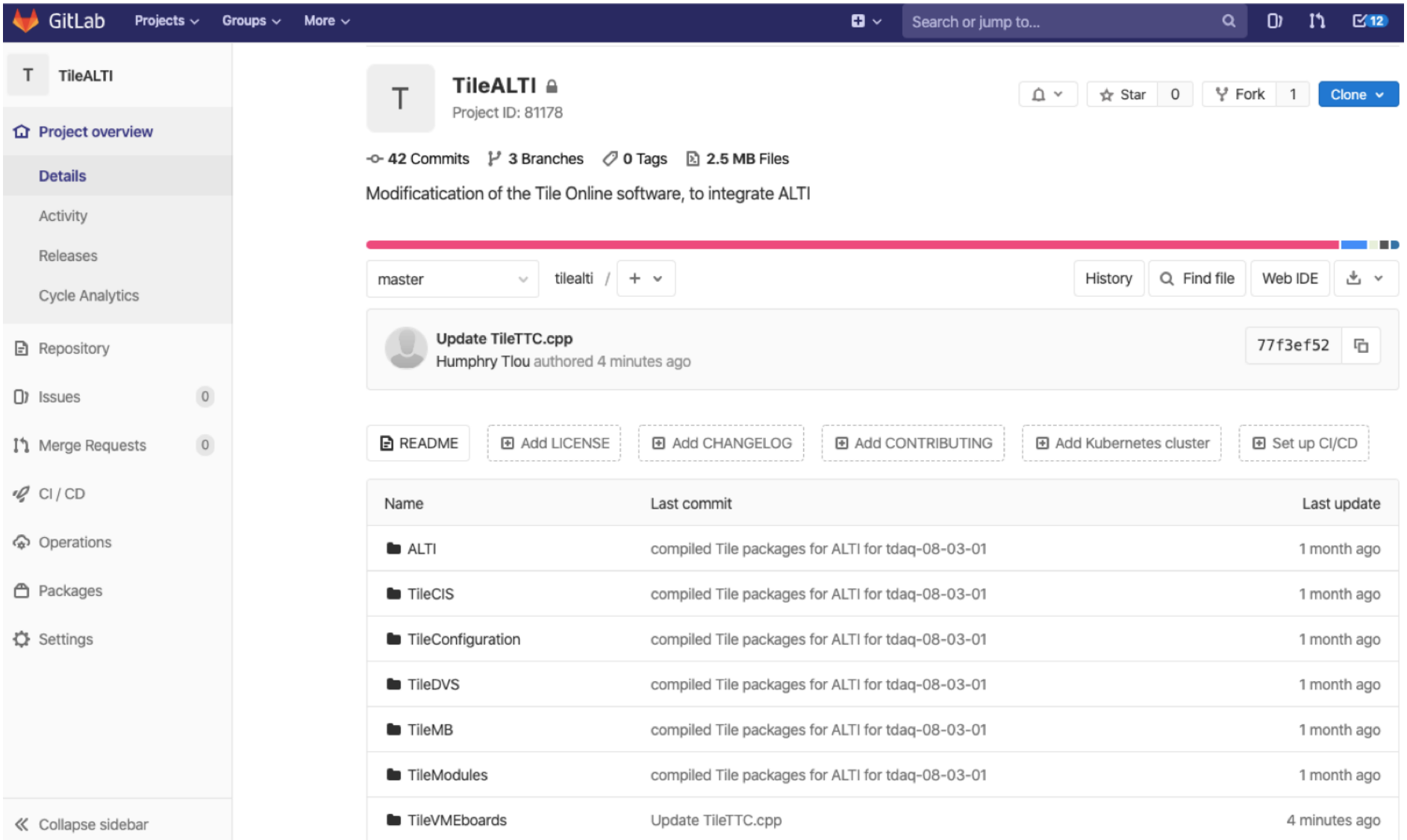
- low-level software, including test and menu programs: https://gitlab.cern.ch/atlas-tdaq-software/ALTI
- high-level software: DAQ controller: https://gitlab.cern.ch/atlas-tdaq-software/AltiController

Tools: C++ and OKS (Object Kernel Support) -an object oriented database with storage based on XML

Dependence graph



TileALTI GitLab project



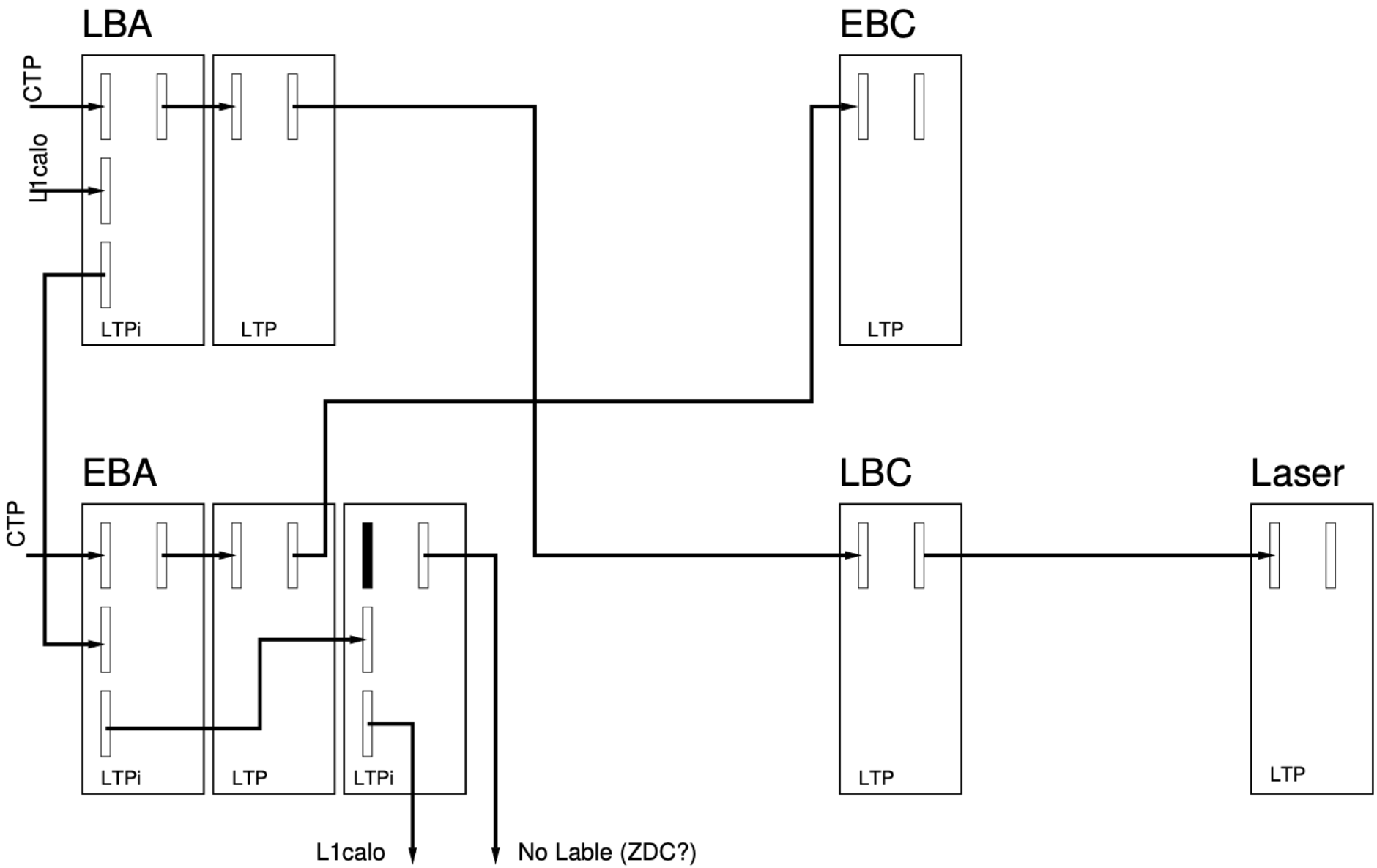
In general ALTI replaces the functionality of TTCvi and LTP boards. Hence 'TileTTC' class compatible with TTCvi and ALTI modules has been added.
'TileTTC' includes constructor with next arguments:
TileTTC(int ttcBoardType, int ch, unsigned long addr, unsigned int slot, bool useDVS = false, unsigned int tm=10000);
where:

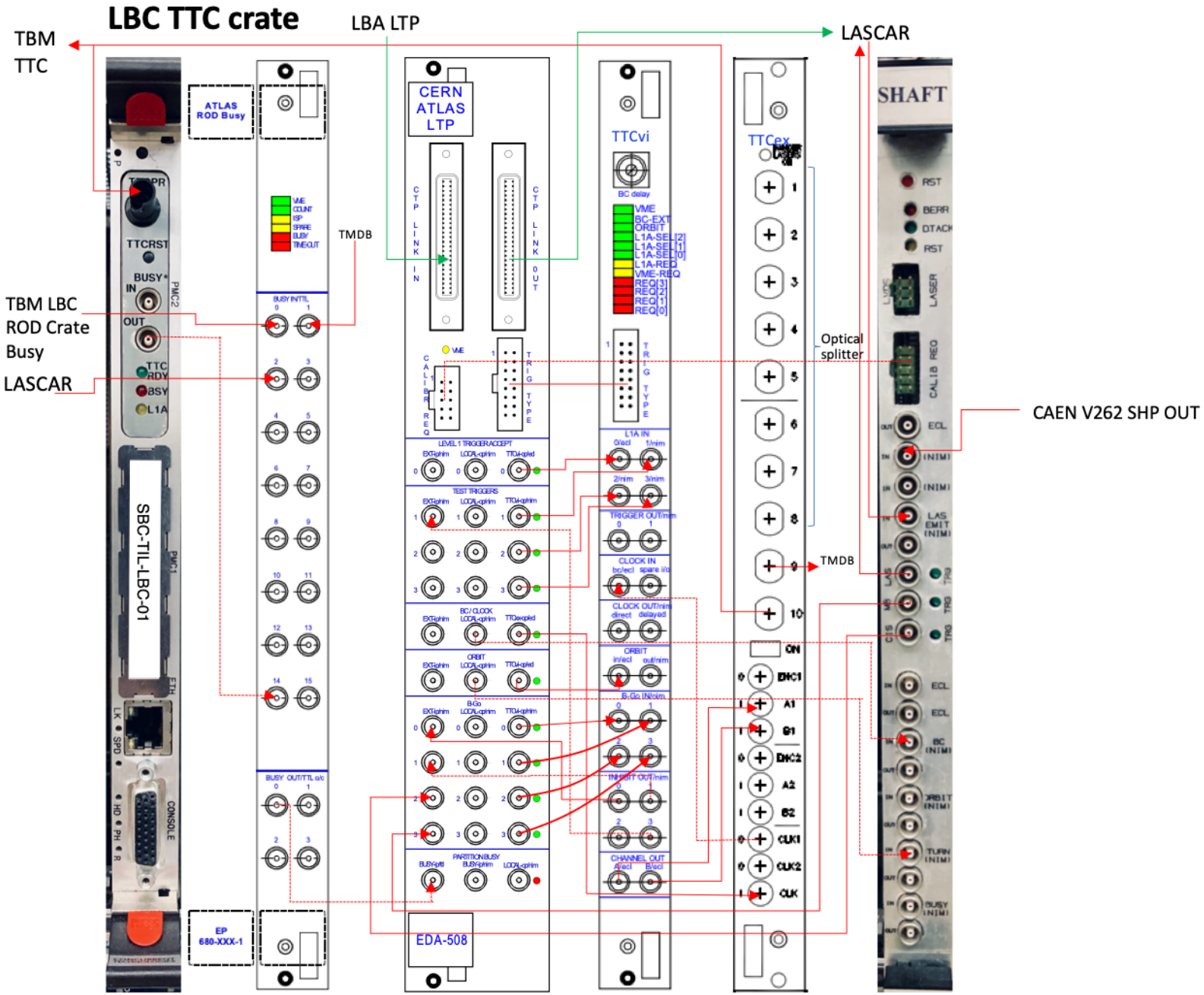
- 'ttcBoardType = 0' - ttcvi functionality, '1' - ALTI
- ch - channel as in ttcvi class, but for ALTI could be only: 0 - L1A, 1 - TTR1, 2 - TTR2, 3 - TTR3
- addr - VME address only for ttcvi, if 'ttcBoardType = 1' addr is not used at all
- slot - slot number only for ALTI, if 'ttcBoardType = 0' slot is not used at all
- 'useDVS = true' - standalone configuration of ALTI for all tests during reset() function. Implemented in the same way as in AltiController for AltiModeAltiMaster. During normal run 'useDVS = false' we will use AltiController to configure and control all other functionality as LTP, BCR etc.

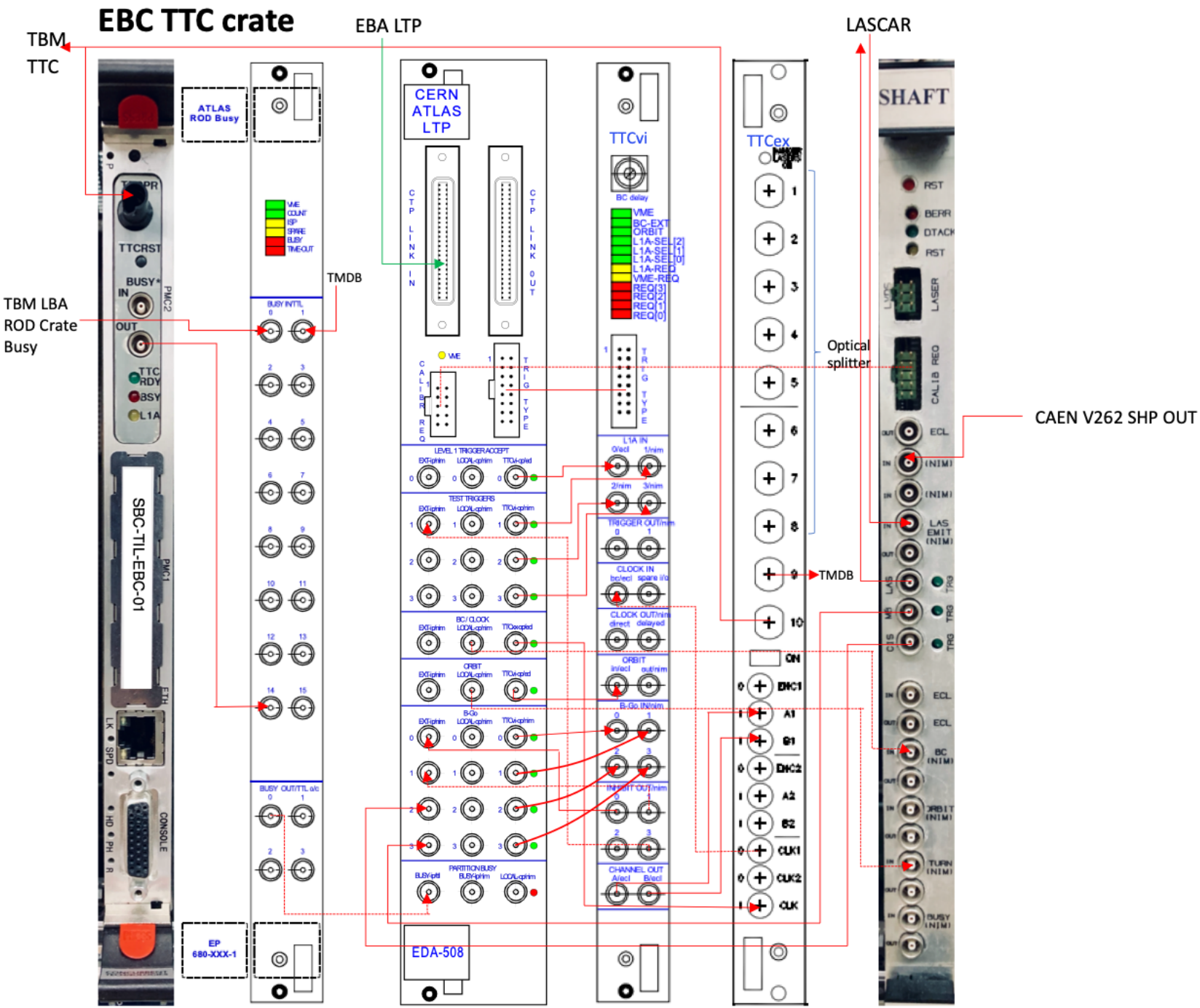
Summary

- ALTI module to replace the 4 legacy TTC modules
- Schematics for the connections within the TTC crates are now available for anyone who wants to make use of them
- ALTI software package included Tile release tile-8.2.0.0 and tile-8.3.1.0
- B175 ROD lab machines migrated from SLC 6 to CentOS 7
- Modifications of the packages, stored in the TileCal GitLab project
- To perform tests and assess the performance of the ALTI module in 2020

Backup


LBA
EBC
CTP
L1calo
LTPi
LTP
LTP
EBA
LBC
Laser
CTP
LTPi
LTP
LTPi
LTP
LTP
L1calo
No Lable (ZDC?)


LBC TTC crate
TBM
TTC
LBA LTP
LASCAR
TBM LBC
ROD Crate
Busy
LASCAR
TMDB
Optical
splitter
CAEN V262 SHP OUT
TMDB
ATLAS
ROD Busy
CERN
ATLAS
LTP
TTCvi
TTCex
SHAFT
SBC-TIL-LBC-01
EDA-508
EP
680-XXX-1


EBC TTC crate
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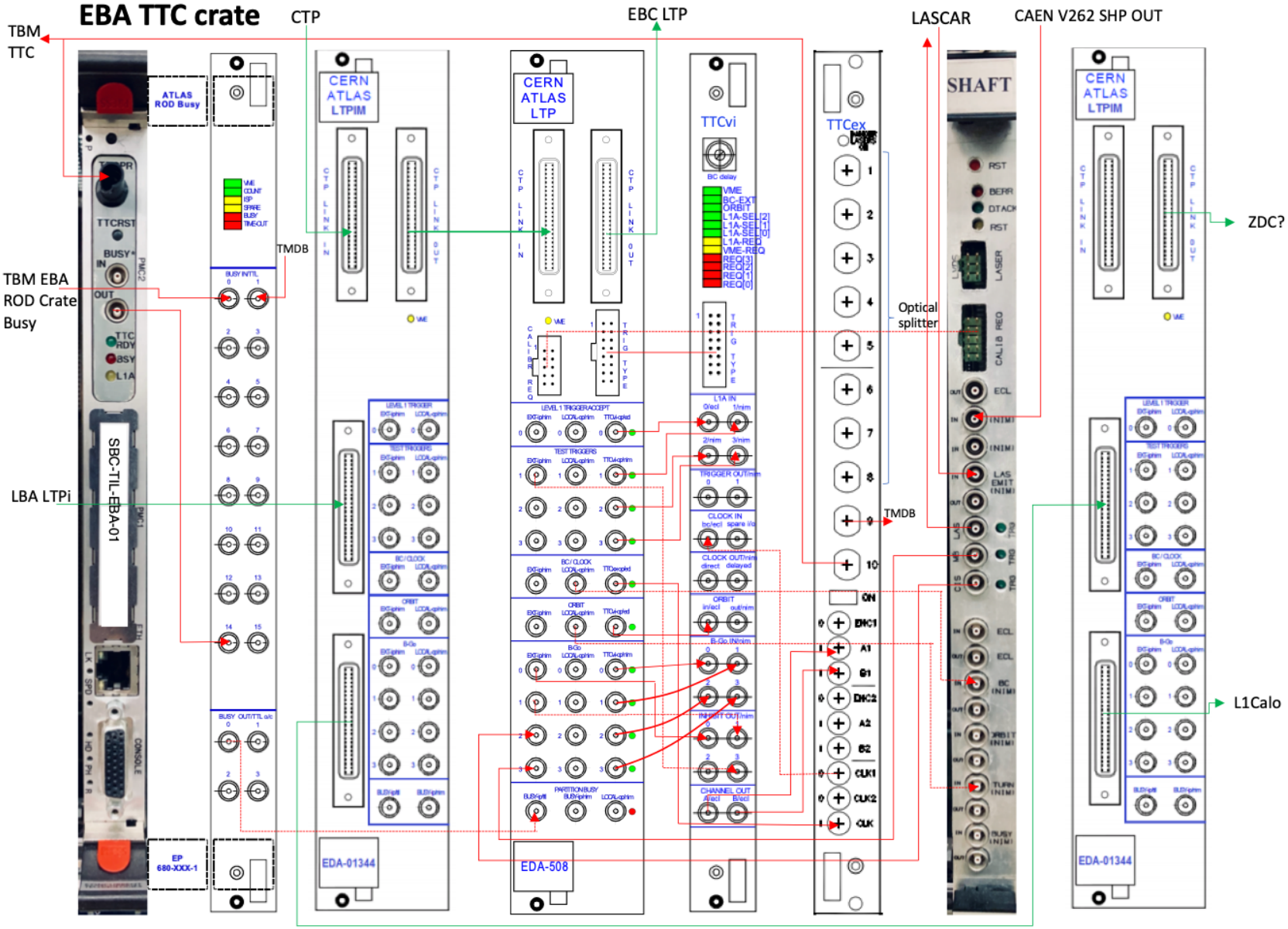
EBA TTC crate
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CERN
ATLAS
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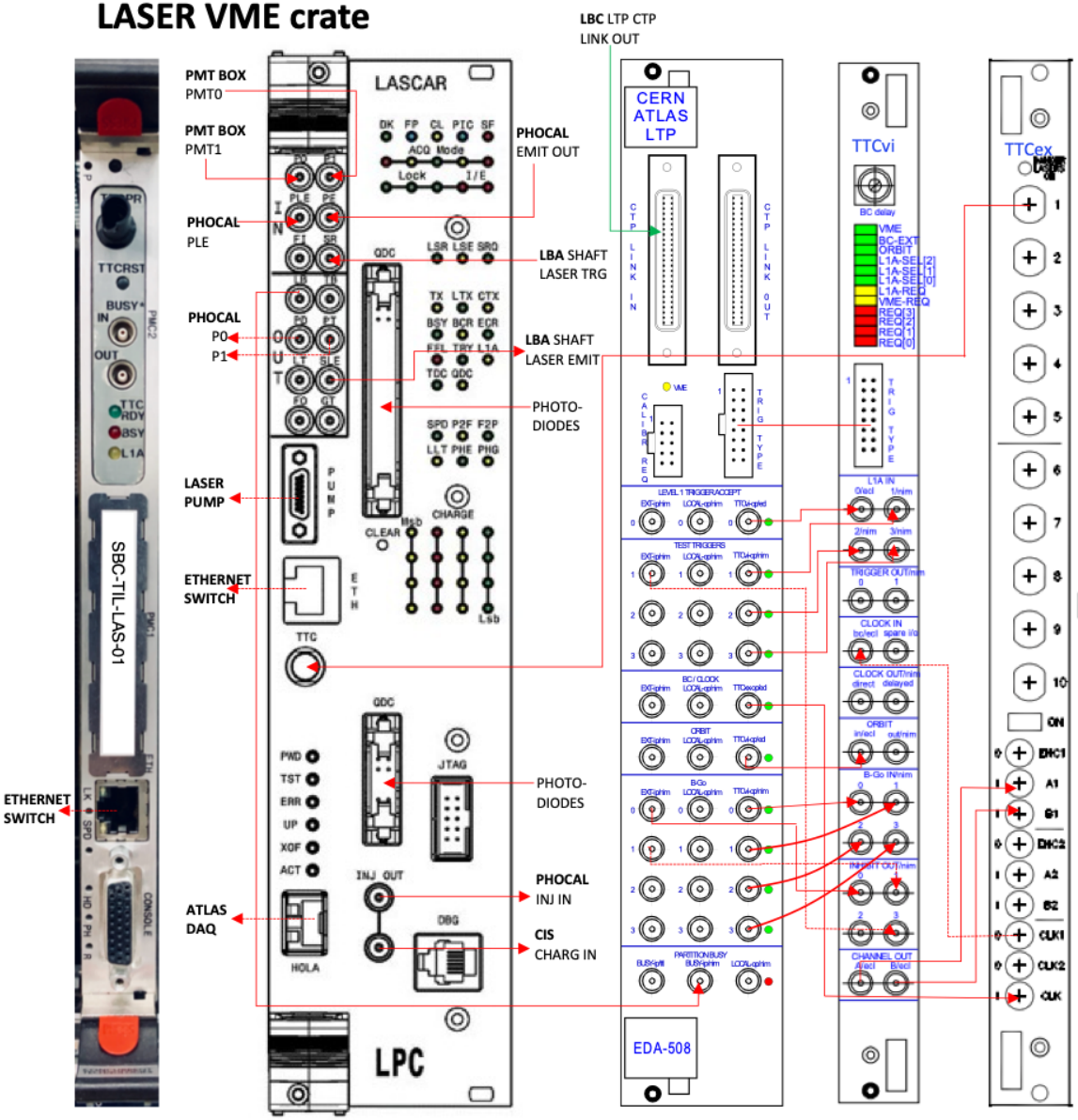
TTCex
SHAFT
EDA-01344
EDA-508
EDA-01344

LASER VME crate



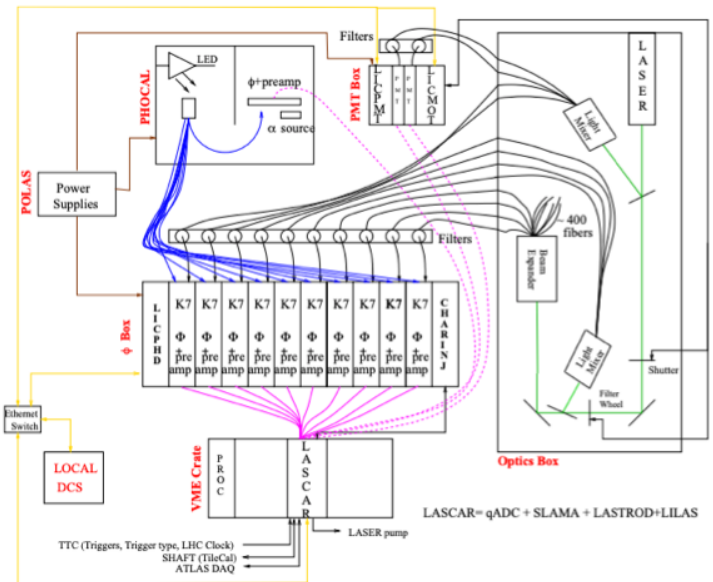


Figure 1: Scheme of the LASERII system

Lemo Connectors

P0: Pmt 0 input
P1: Pmt 1 input
PLE: Phocal Led Emit input
PE: Phocal input
FI: Free input
SR: Shaft Request input
LB: Link Busy Output
TB: TTL Busy Output
PD: Phocal Oscillator Disable Output
PT: Phocal Trigger Output
LT: Lilas Trigger Output
SLE: Shaft Laser Emit Output
FO: Free Output
GT: Gate Output