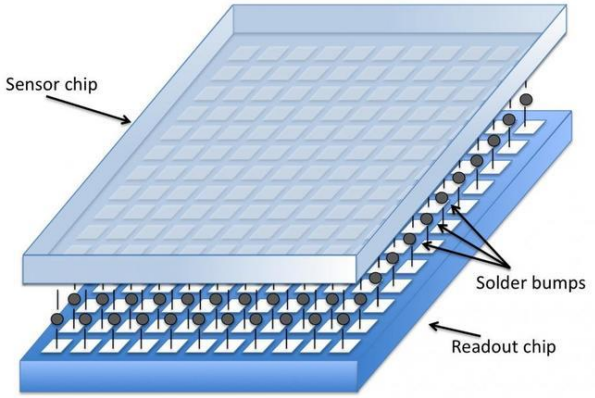
Lab session on
RD53 Pixel Front-End Characterization

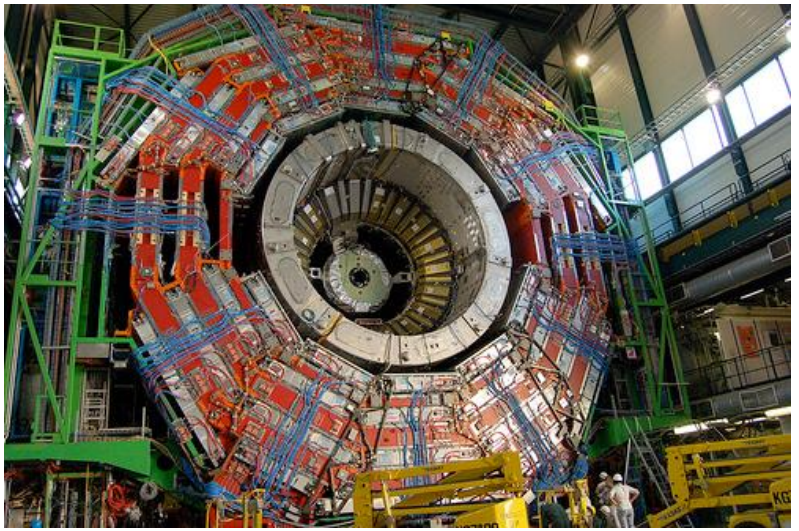
Valerio Re, Luigi Gaioni
(valerio.re@unibg.it, luigi.gaioni@unibg.it)

Università di Bergamo and INFN Pavia, Italy

Focus of the lab

- Pixel front-end ASICs are located at the very beginning of the **signal processing chain** in pixel based detectors used in many fundamental and applied research fields
- **Experimental characterization** of front-end circuits in advanced microelectronic technologies is an **integral part of the implementation** of modern radiation detection systems
- The focus of the lab will be the **characterization of front-end channels for pixel detectors in a 65 nm CMOS technology**
- The circuit under test is a prototype chip for the **CMS phase 2 upgrade** designed in the framework of the international **RD53 collaboration**

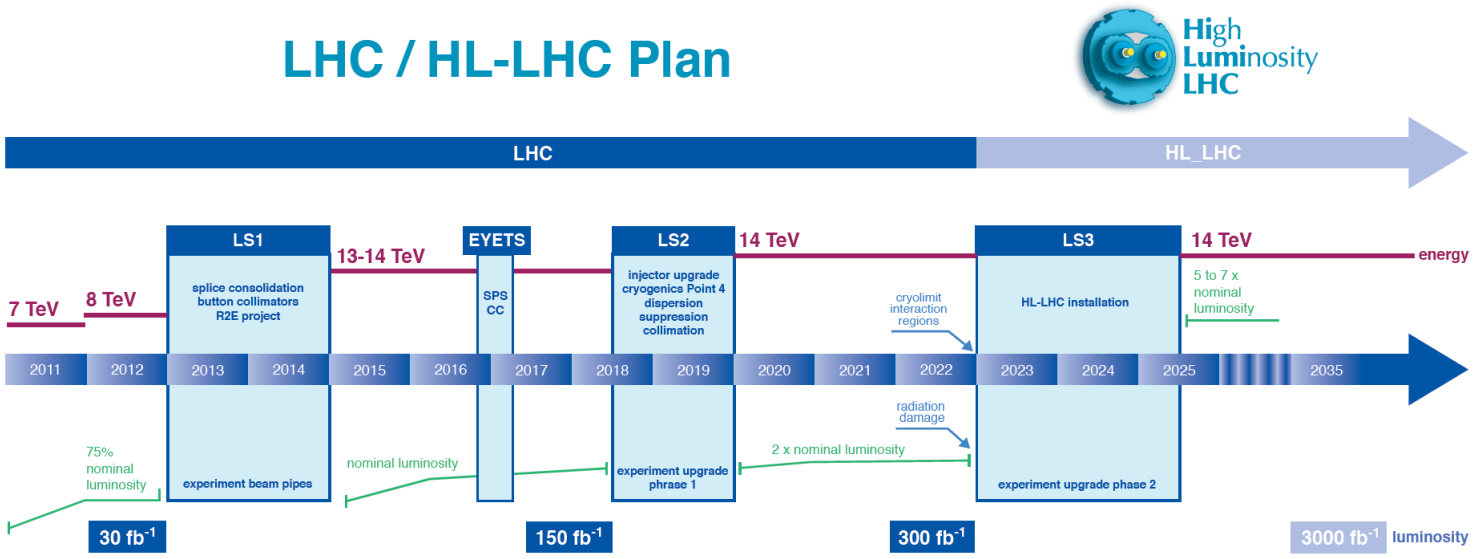




Pixel Detector Requirements at HL LHC

Very **challenging requirements** for the innermost layers of the pixel detectors in ATLAS and CMS @ the HL LHC

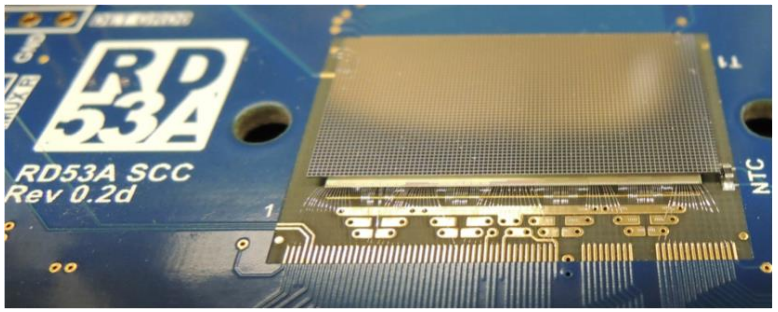
- Very **high particle rate** → pixel hit rates up to 3 GHz/cm^2
- **Small pixels**: 50x50um^2 → increased resolution, improved track separation
- **Large chips**: ~2cm x 2cm (1 billion transistors)
- **Low mass, low power systems**: ~10 uW per cell (including analog and digital sections)
- **Low threshold**: ~1000 e- → severe requirements on noise and dispersion
- **Harsh radiation environment**: 1 Grad(SiO_2) TID; 10^{16} eq. n/cm^2 fluence



RD53 – An overview

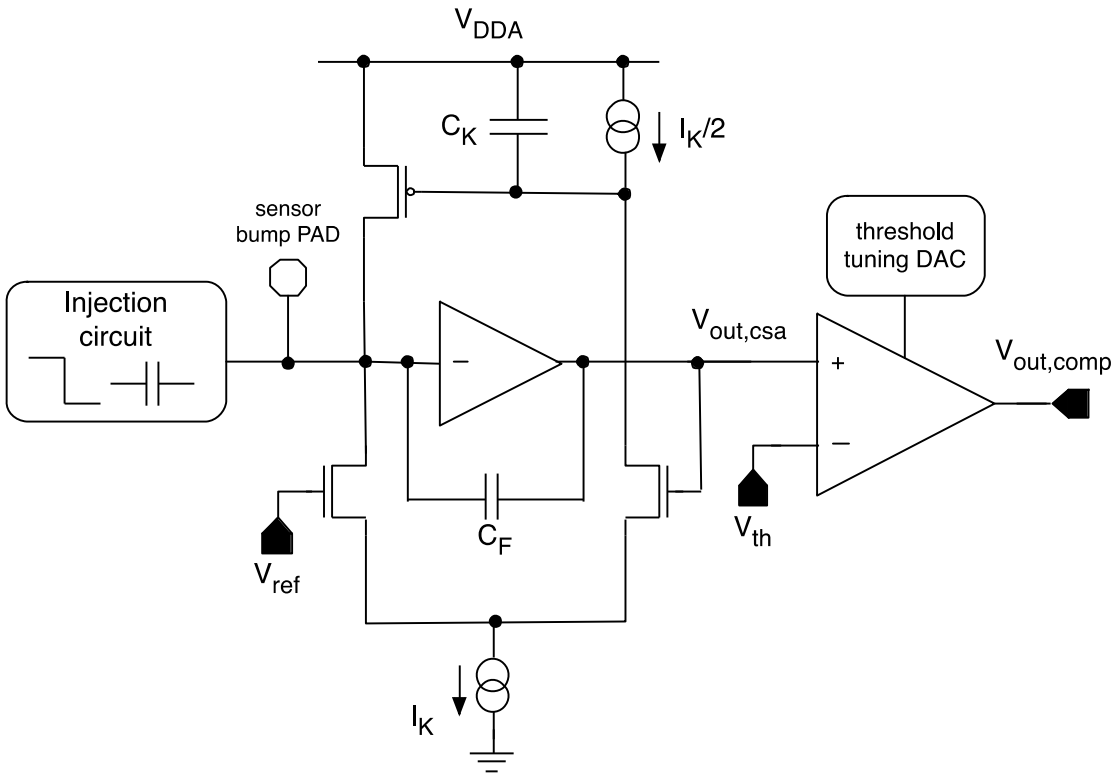
- Collaboration among **ATLAS** & **CMS** communities aiming at the development of large scale pixel chips for LHC phase-2 upgrades
- **65 nm CMOS** is the common technology platform

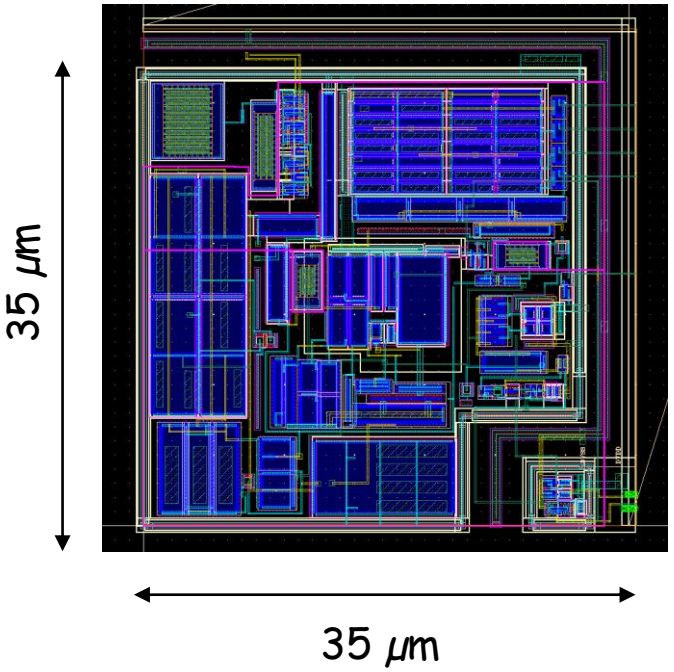
- **RD53 Goals**
  - Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
  - Design and characterization of **full size pixel array chip**



- The efforts of the RD53 collaboration led to the submission (2017) of the **RD53A chip including three different front-end flavors: Synchronous, Linear and Differential**
- Linear front-end has been adopted in the **RD53B CMS** chip (submitted in June 2021), including a matrix of 336x432 pixels (50x50 μm^2 each)
- A small prototype chip including **RD53A** and **RD53B** Linear front-end has been submitted and **will be characterized during lab activities**

RD53 Linear front-end

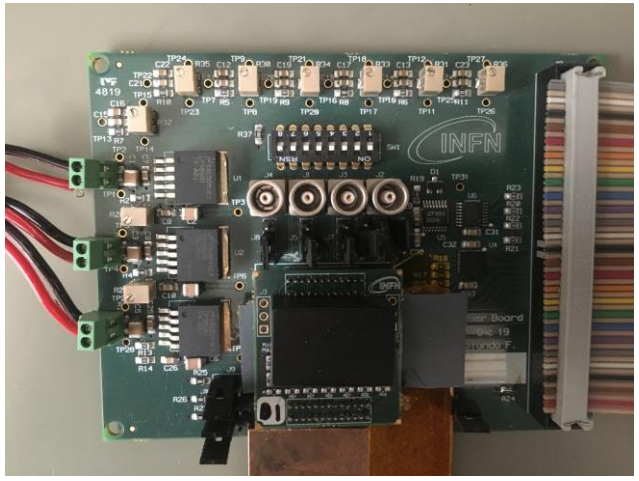


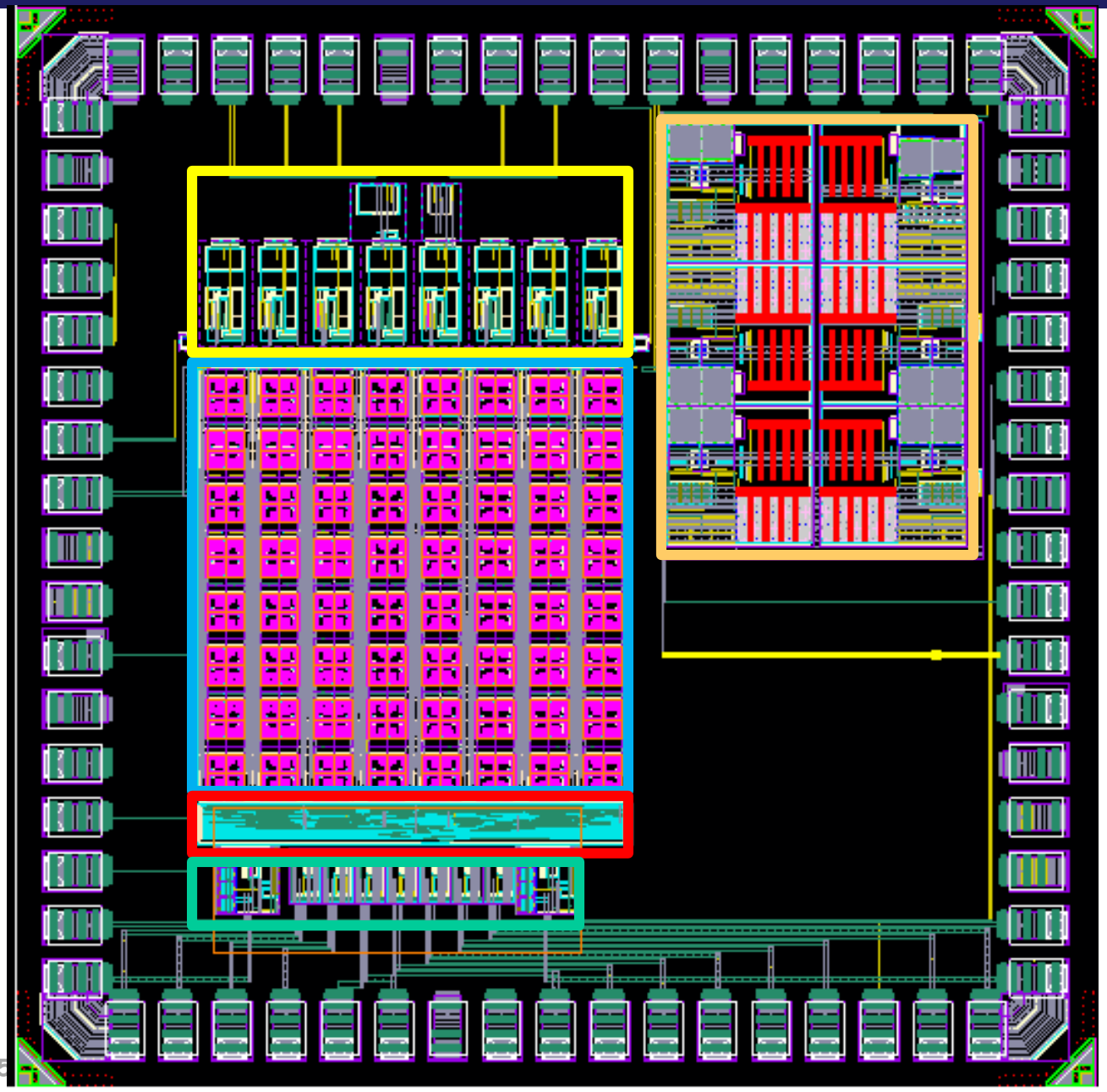


- **Single stage front-end** with **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- Low power asynchronous **current comparator** combined with a **40 MHz Time-over-Threshold (ToT) counter** for digitization of the signal
- 4 bit (RD53A) and 5 bit (RD53B) local DAC for **threshold tuning**

Device under test (DUT)

- 16x16 pixel matrix
  - Two regions: RD53A – RD53B
- Analog bias
- Configuration block
  - SPI-based
- Custom LVDS TX/RX

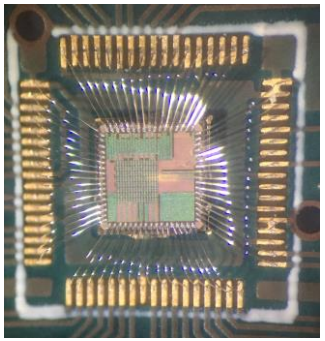




Test setup

Agilent 3631A power supply

Power cables



DUT

Ribbon cable

Kintex7 board

Ethernet + USB

Laptop

- Simple LavVIEW-based test setup is used for measuring **the main analog performance parameters** (noise, threshold dispersion, time-walk, Time-over-Threshold) of the front-end channels
- **No previous experience** in pixel front-end characterization is required
- **Basic knowledge** on electronic circuit operation is a prerequisite