

# Lab session on RD53 Pixel Front-End Characterization

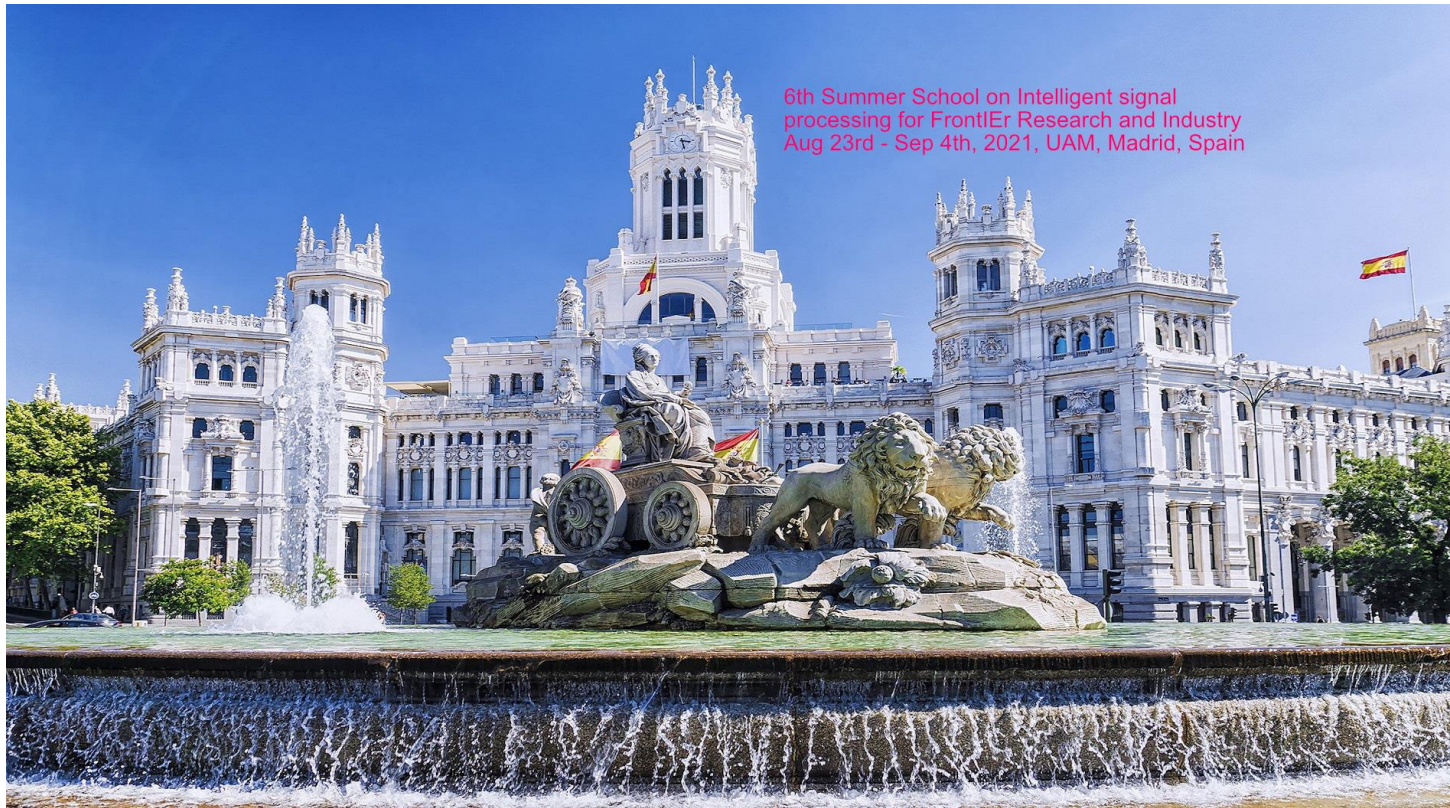


**Valerio Re, Luigi Gaioni**  
([valerio.re@unibg.it](mailto:valerio.re@unibg.it), [luigi.gaioni@unibg.it](mailto:luigi.gaioni@unibg.it))

Università di Bergamo and INFN Pavia, Italy

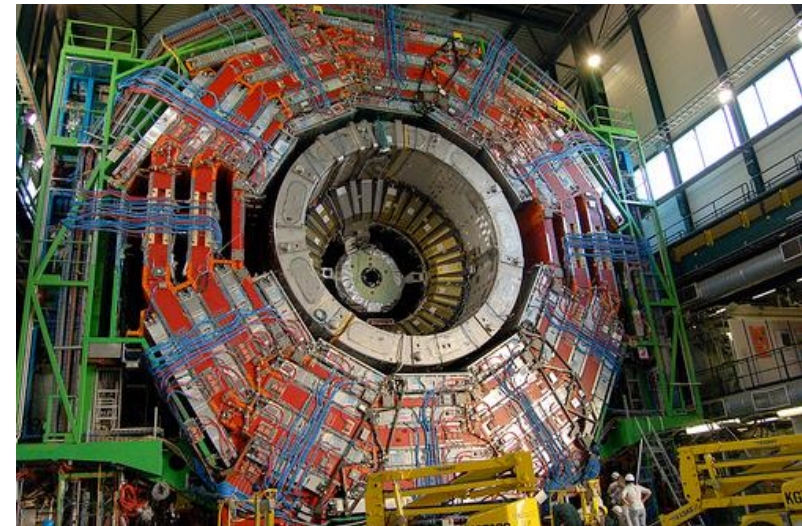
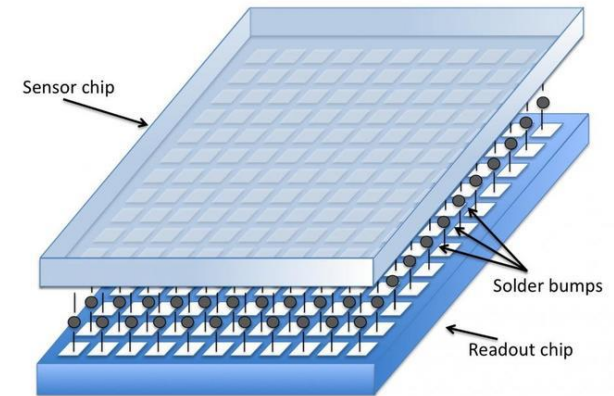


**UNIVERSITÀ  
DEGLI STUDI  
DI BERGAMO**



# Focus of the lab

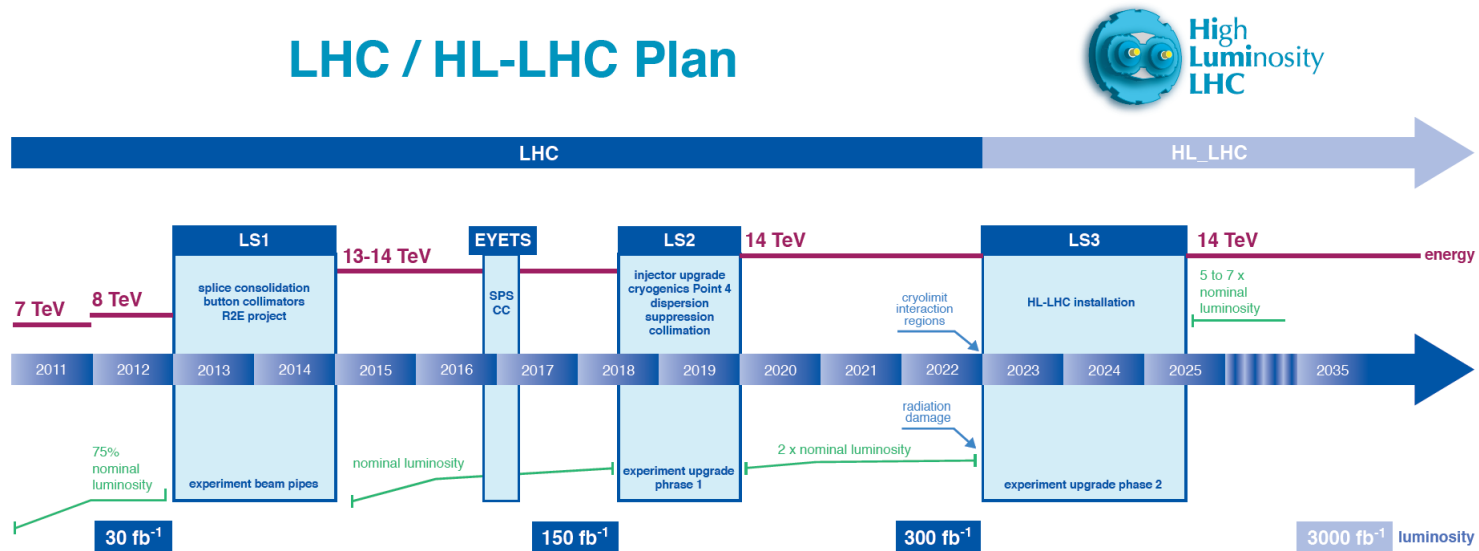
- Pixel front-end ASICs are located at the very beginning of the **signal processing chain** in pixel based detectors used in many fundamental and applied research fields
- **Experimental characterization** of front-end circuits in advanced microelectronic technologies is an **integral part of the implementation** of modern radiation detection systems
- The focus of the lab will be the **characterization of front-end channels for pixel detectors in a 65 nm CMOS technology**
- The circuit under test is a prototype chip for the **CMS phase 2 upgrade** designed in the framework of the international **RD53 collaboration**



# Pixel Detector Requirements at HL LHC

Very **challenging requirements** for the innermost layers of the pixel detectors in ATLAS and CMS @ the HL LHC

- **Very high particle rate** → pixel hit rates up to 3 GHz/cm<sup>2</sup>
- **Small pixels:** 50x50um<sup>2</sup> → increased resolution, improved track separation
- **Large chips:** ~2cm x 2cm (1 billion transistors)
- **Low mass, low power systems:** ~10 uW per cell (including analog and digital sections)
- **Low threshold:** ~1000 e<sup>-</sup> → severe requirements on noise and dispersion
- **Harsh radiation environment:** 1 Grad(SiO<sub>2</sub>) TID; 10<sup>16</sup> eq. n/cm<sup>2</sup> fluence

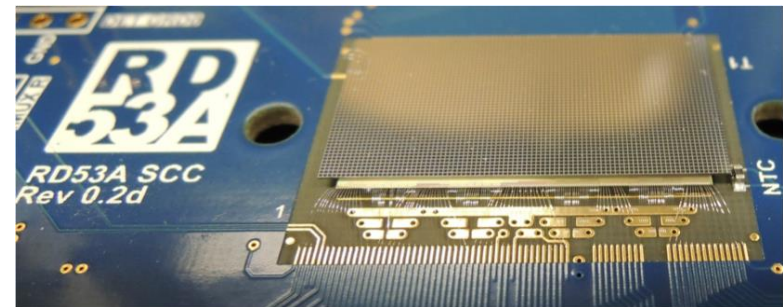


# RD53 - An overview

- Collaboration among **ATLAS & CMS** communities aiming at the development of large scale pixel chips for LHC phase-2 upgrades
- **65 nm CMOS** is the common technology platform

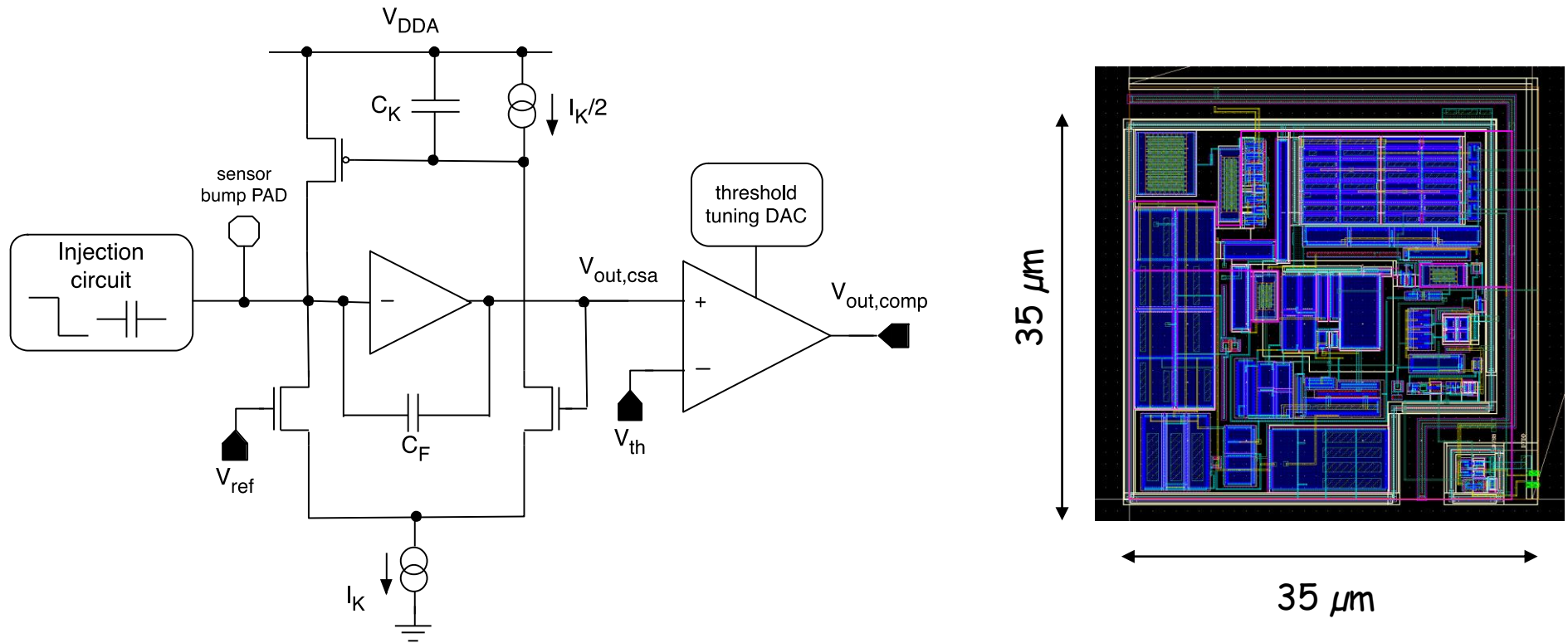
- **RD53 Goals**

- Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
- Design and characterization of **full size pixel array chip**



- The efforts of the RD53 collaboration led to the submission (2017) of the **RD53A chip including three different front-end flavors: Synchronous, Linear and Differential**
- Linear front-end has been adopted in the **RD53B CMS** chip (submitted in June 2021), including a matrix of 336x432 pixels (50x50  $\mu\text{m}^2$  each)
- A small prototype chip including **RD53A and RD53B Linear** front-end has been submitted and **will be characterized during lab activities**

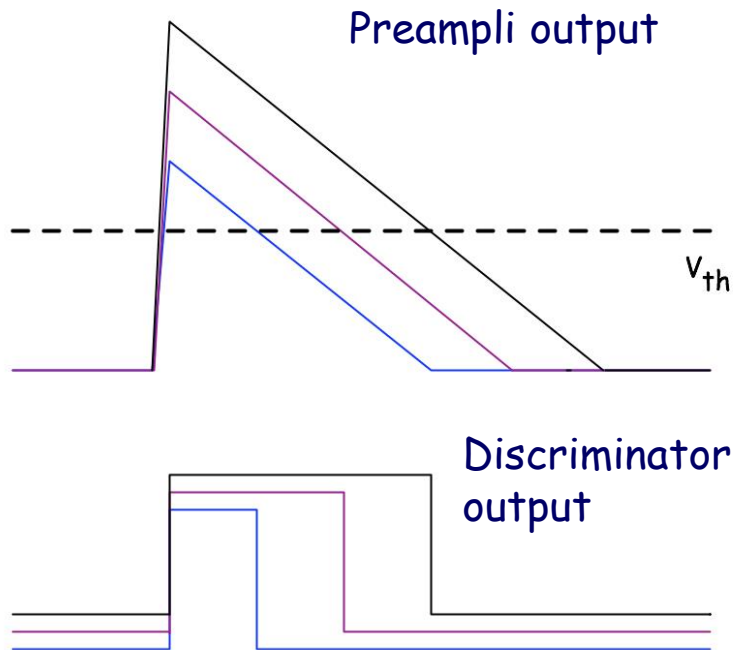
# RD53 Linear front-end



- **Single stage front-end with Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- Low power asynchronous **current comparator** combined with a **40 MHz Time-over-Threshold (ToT) counter** for digitization of the signal
- 4 bit (RD53A) and 5 bit (RD53B) local DAC for **threshold tuning**

# Time over threshold (ToT)

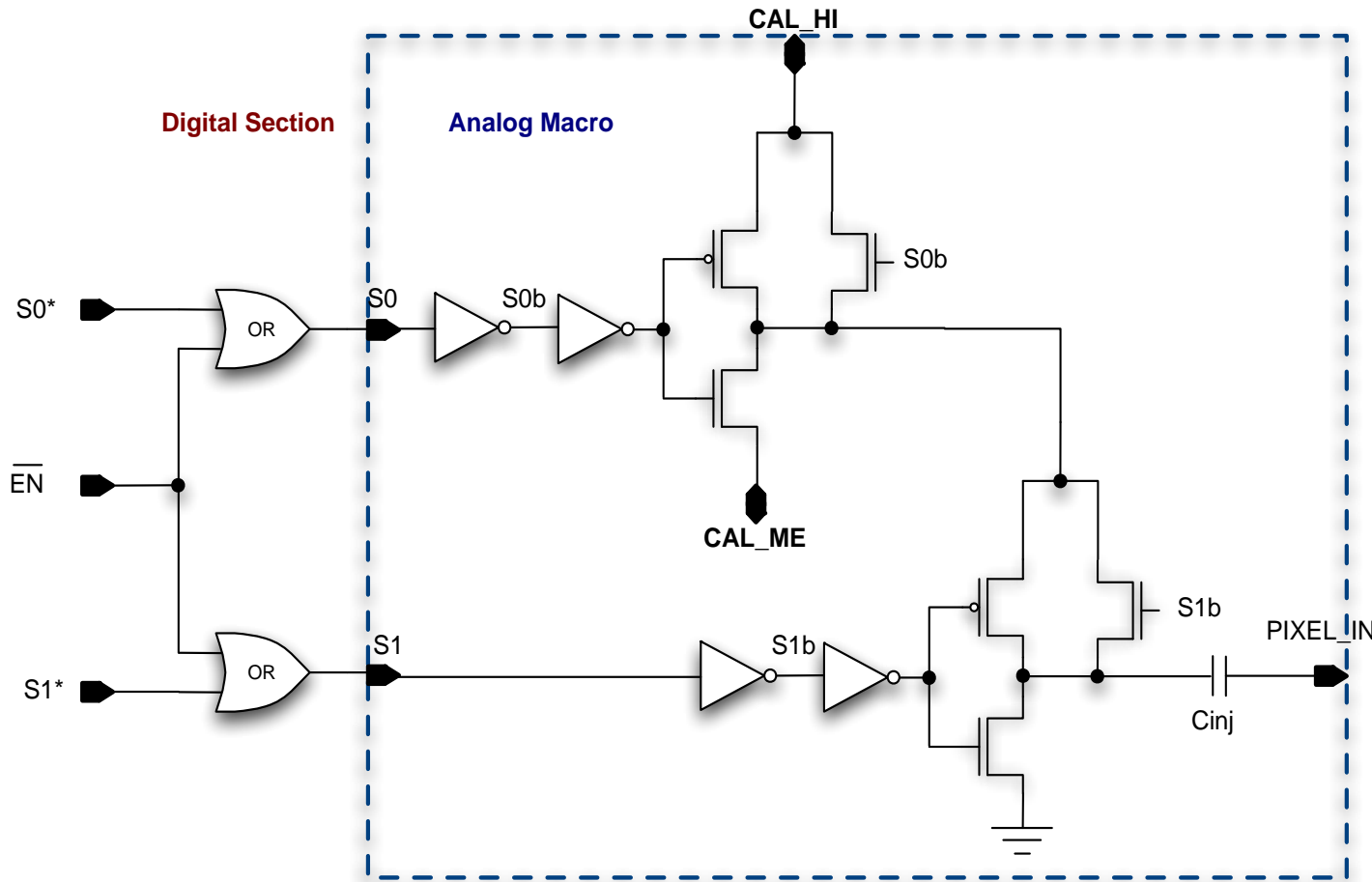
- The **Time over Threshold (ToT)** technique provides a direct **amplitude-to-time** conversion; the signal at the preamp output is compared to a fixed voltage at the input of a threshold discriminator; the signal at the output of the discriminator is a digital pulse, whose duration is equal to the time during which the signal at the preamp output exceeds the threshold; digitization is easily achieved by computing the logic AND between the discriminator pulse and a reference clock and by counting the number of clock pulses



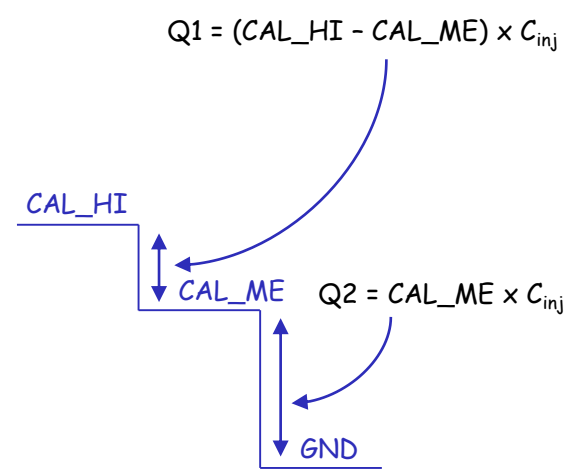
- If the signal at the preamp output returns to the baseline with a constant slope, then a linear relationship exists between the peak amplitude at the preamp output and the ToT duration (the rise time of the preamp output signal is assumed to be negligible)

$$ToT = \frac{V_{peak} - V_{th}}{\left| \frac{dV_{shaper}}{dt} \right|}$$

# Analog scan



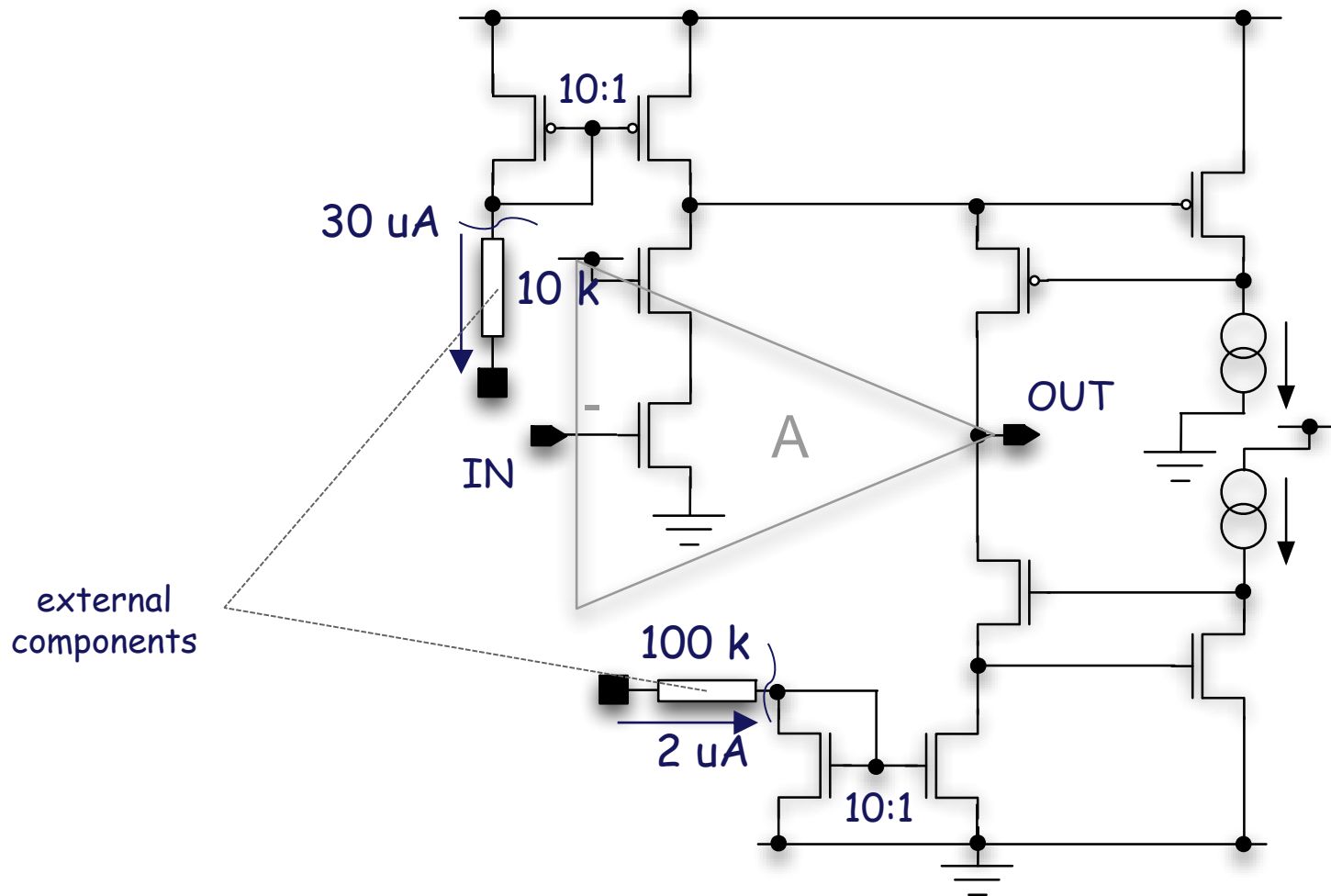
Q-V conversion factor →  
~50 e-/mV



- Local generation of the analog test pulse starting from 2 defined DC voltages CAL\_HI and CAL\_MI distributed to all pixels and a 3rd level (local GND)
- It is possible to generate two consecutive signals of the same polarity

# Amplifier schematic

- Gain stage based on a **folded cascode** configuration



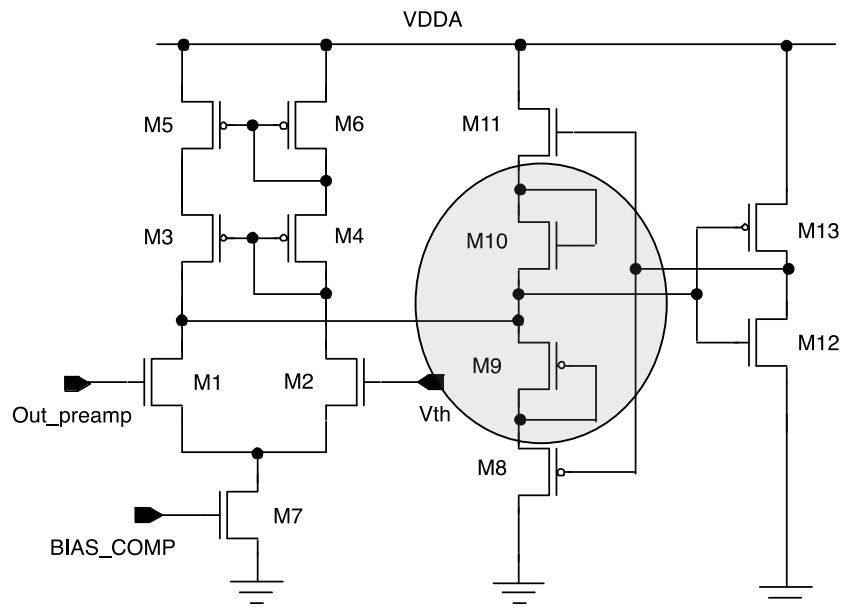
total power dissipation is about 3.8  $\mu\text{W}$  (not considering power in the reference branch of the mirror - the same reference branch can be used for all the pixels in an array)



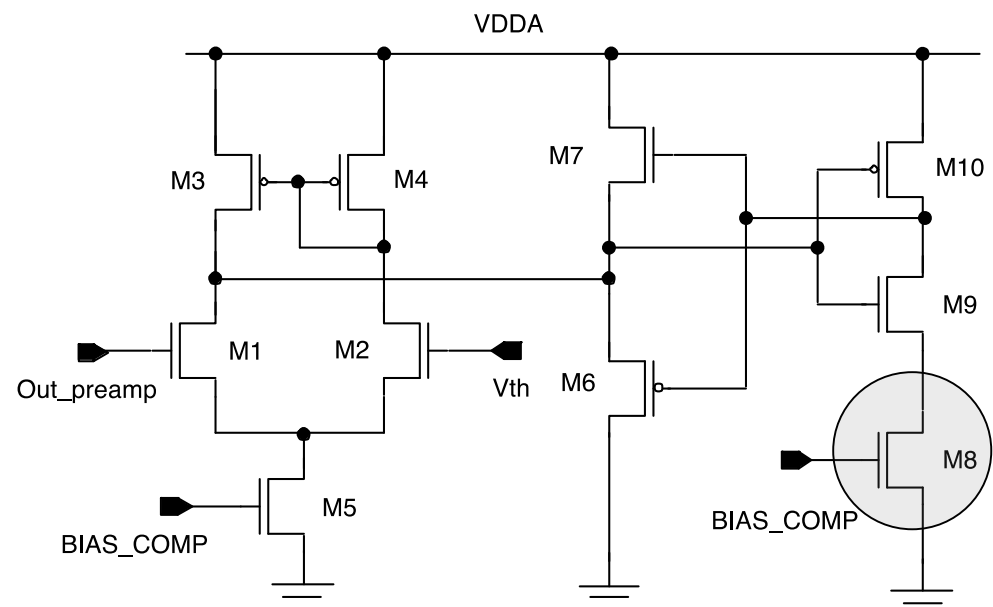
# Boosting time-walk performance

- Partial re-design of the **comparator** led to improvement in front-end **time-walk performance**

RD53A

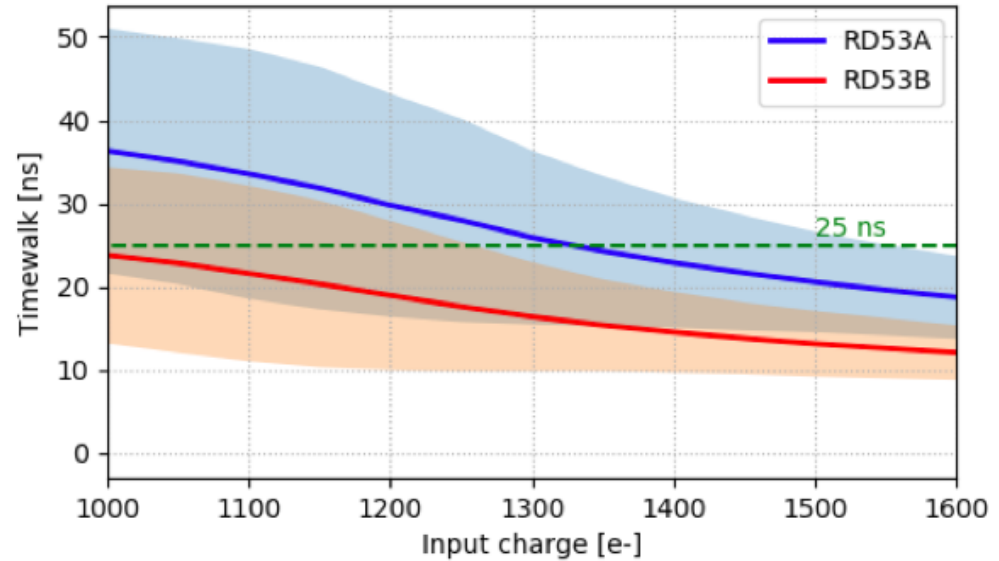
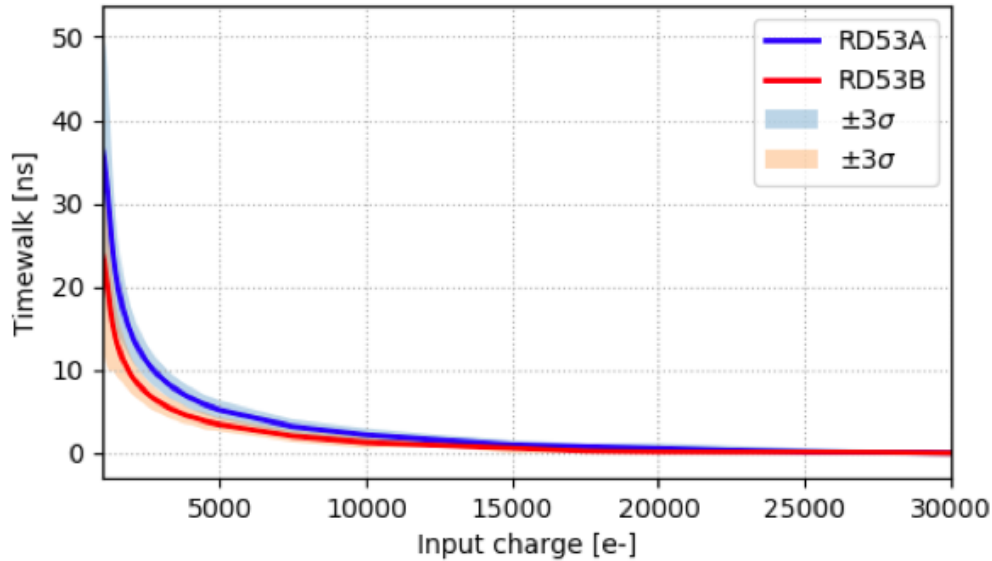


RD53B



- Fast turn-on time of M6 and M7 (RD53B) thanks to removal of M9 and M10 (RD53A)
- Current starving M8 (RD53B)

# Time-walk test results

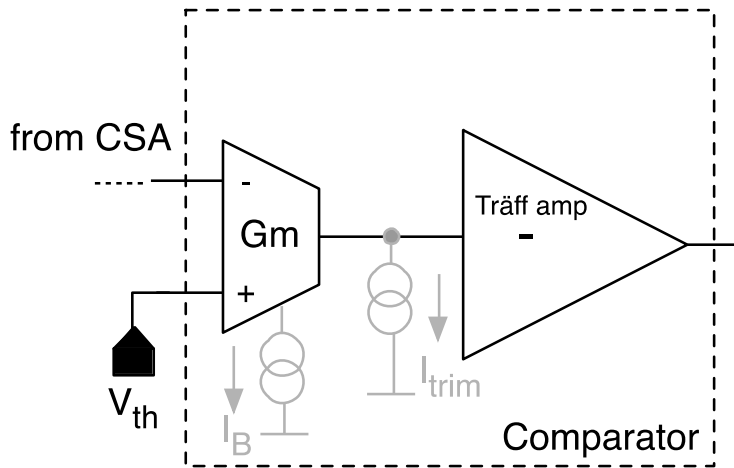
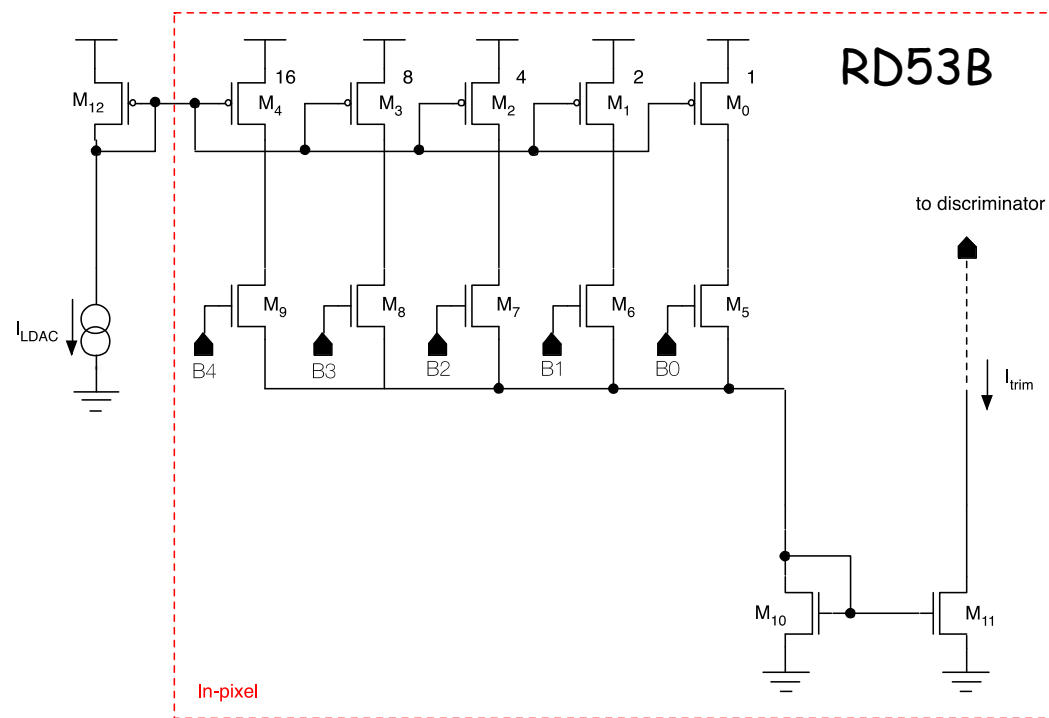
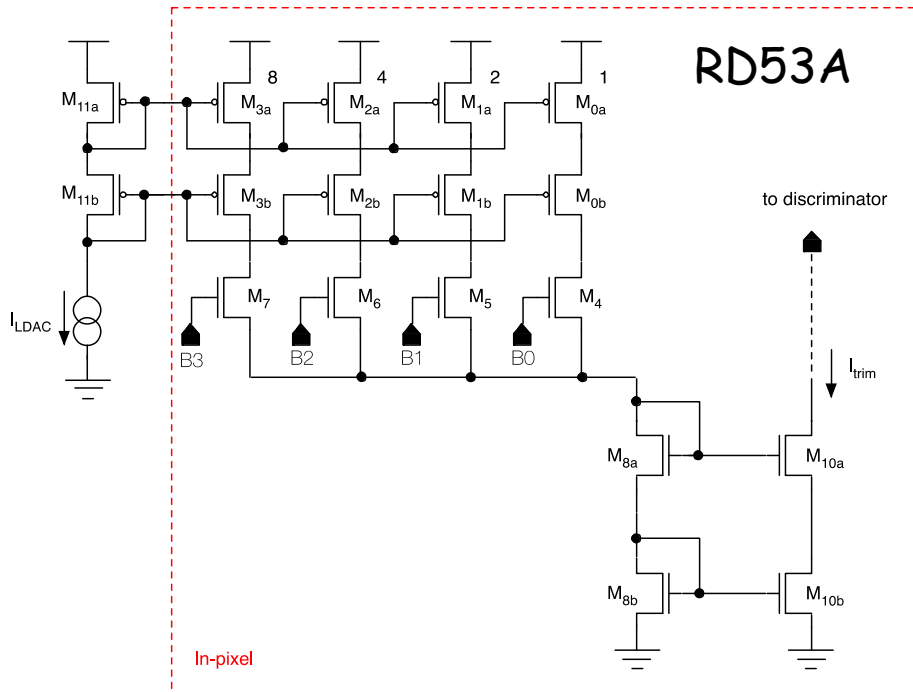


- Results on a sample chip at  $T = -20^\circ \text{C}$
- Threshold  $\sim 1000 \text{ e-}$ ,  $5 \mu\text{A}$  per-pixel current consumption,  $133 \text{ ns ToT}$  @  $Q_{\text{in}} = 6 \text{ ke-}$ ,  $C_{\text{D}} = 50 \text{ fF}$

Significant improvement in time-walk at the cost of a marginal increase ( $\sim 4\%$ ) in static current consumption

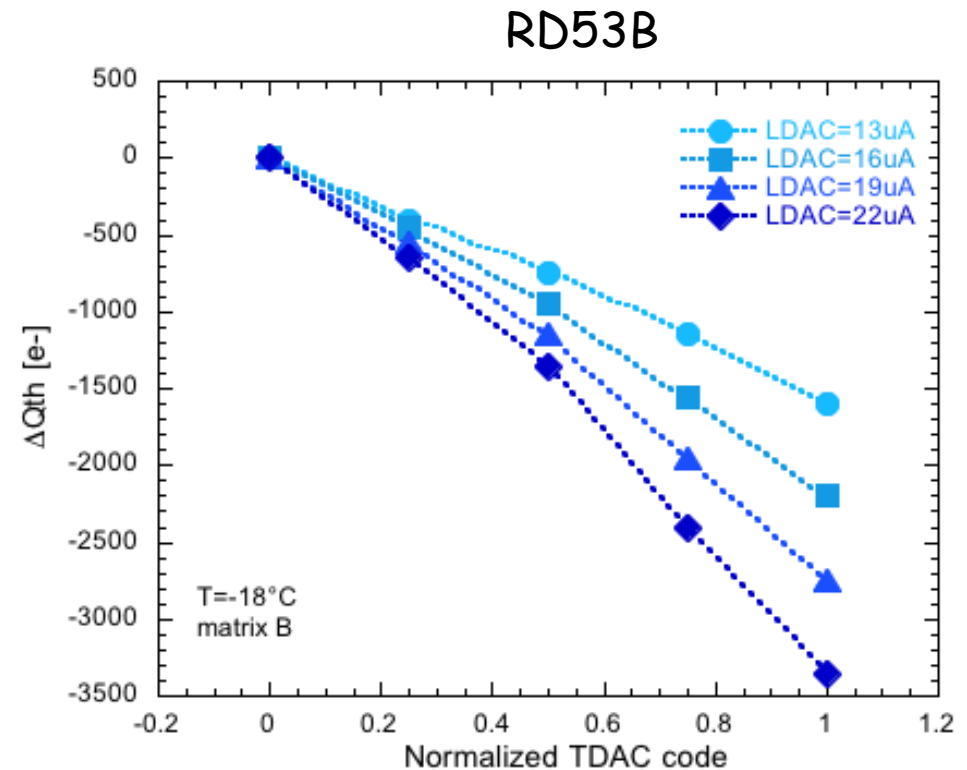
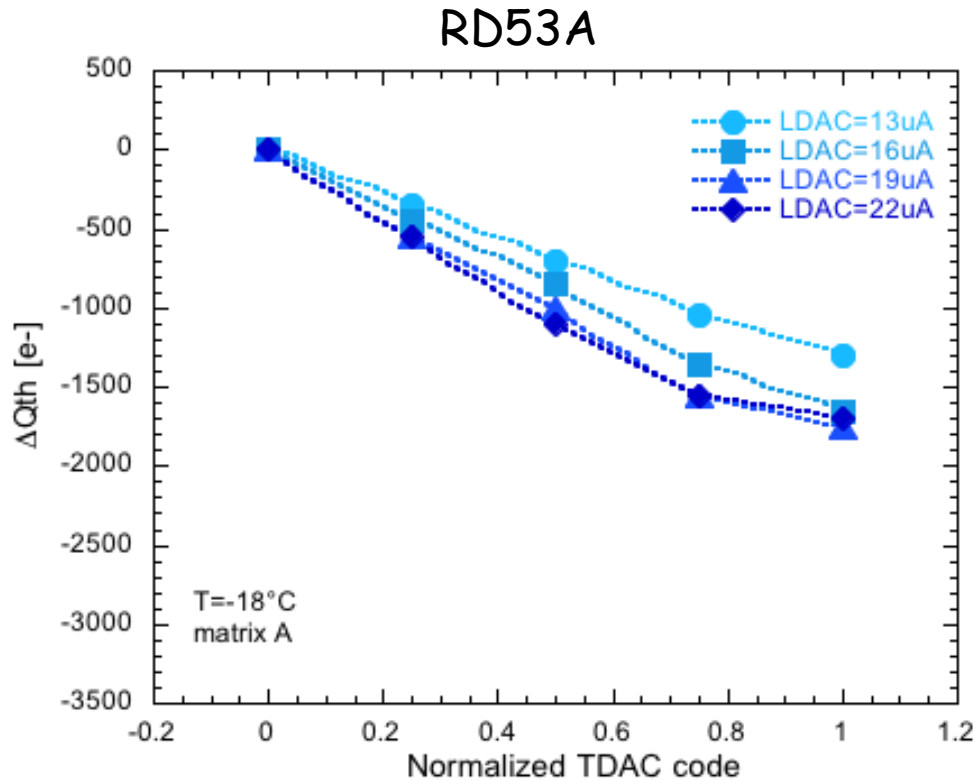


# Threshold tuning DACs



- Current-mode threshold tuning DACs
  - RD53A → 4 bits, **cascoded** current mirrors
  - RD53B → 5 bits, **regular** current mirrors
- **NMOS** switches

# TDAC input-output characteristics

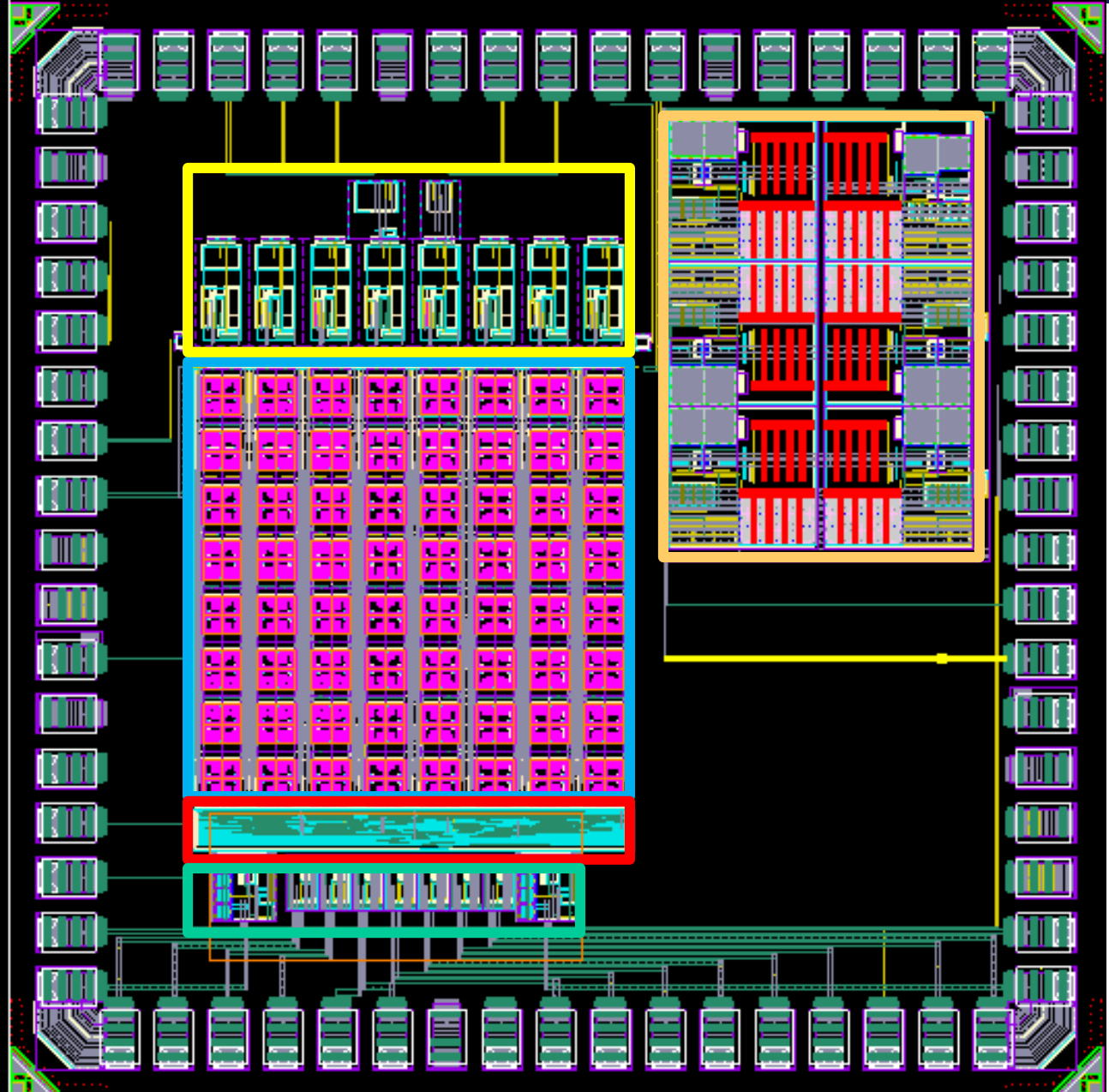


- TDAC **dynamic range** controlled by "LDAC" current (matrix periphery)
- **Saturation effect** taking place for RD53A at cold (for large  $I_{LDAC}$ )
- The effect is **fixed** in the RD53B version

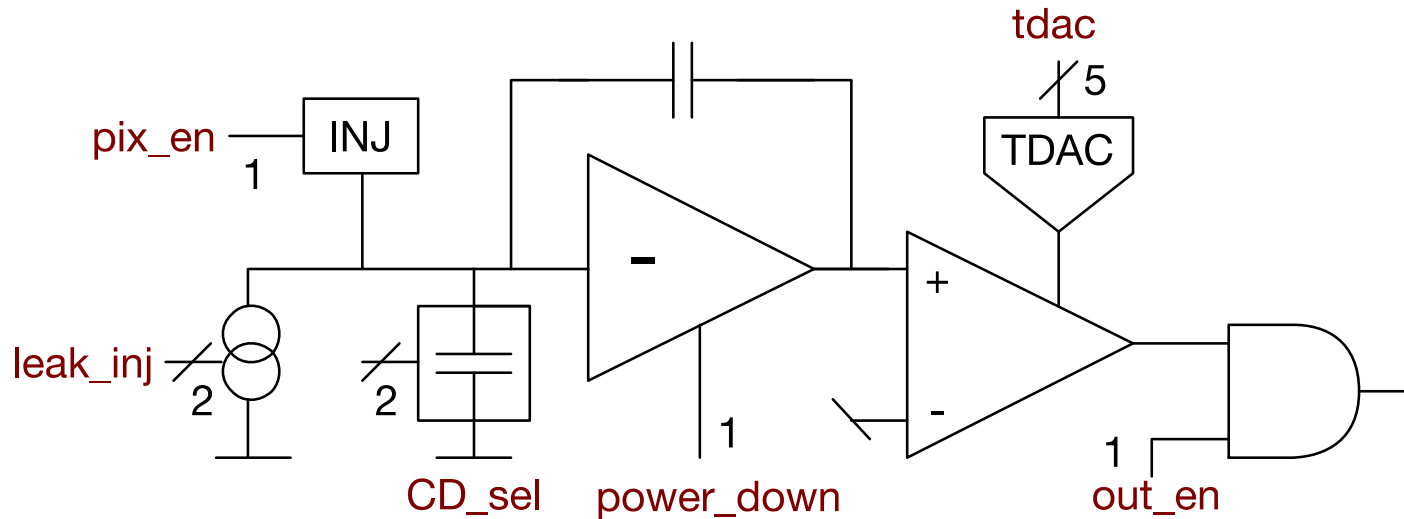
# Device under test (DUT)

- 16x16 pixel matrix
  - Two regions: RD53A - RD53B
- Analog bias
- Configuration block
  - SPI-based
- Custom LVDS TX/RX
- Bandgap test structures

Top metal layers not shown



# Pixel block diagram



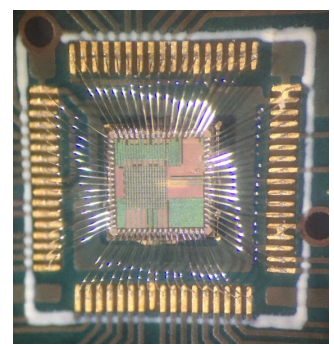
- **2 detector emulating capacitors:** 50 fF and 100 fF  
→ CD = 0, 50 fF, 100 fF, 150 fF
- **Leakage injection circuit** (possibility to inject "positive" or "negative" currents)

# Test setup

Agilent 3631A power supply



Power cables



DUT



Ribbon cable



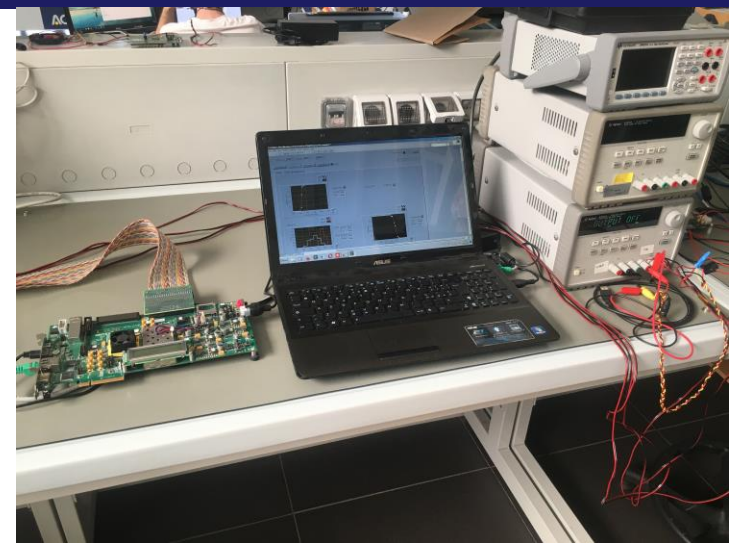
Kintex7 board



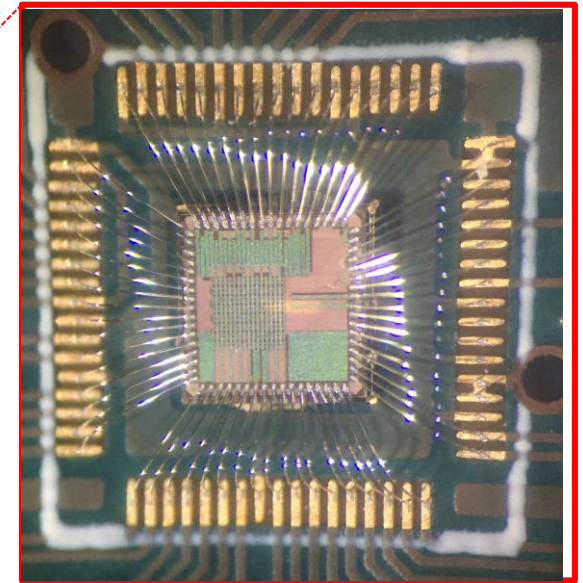
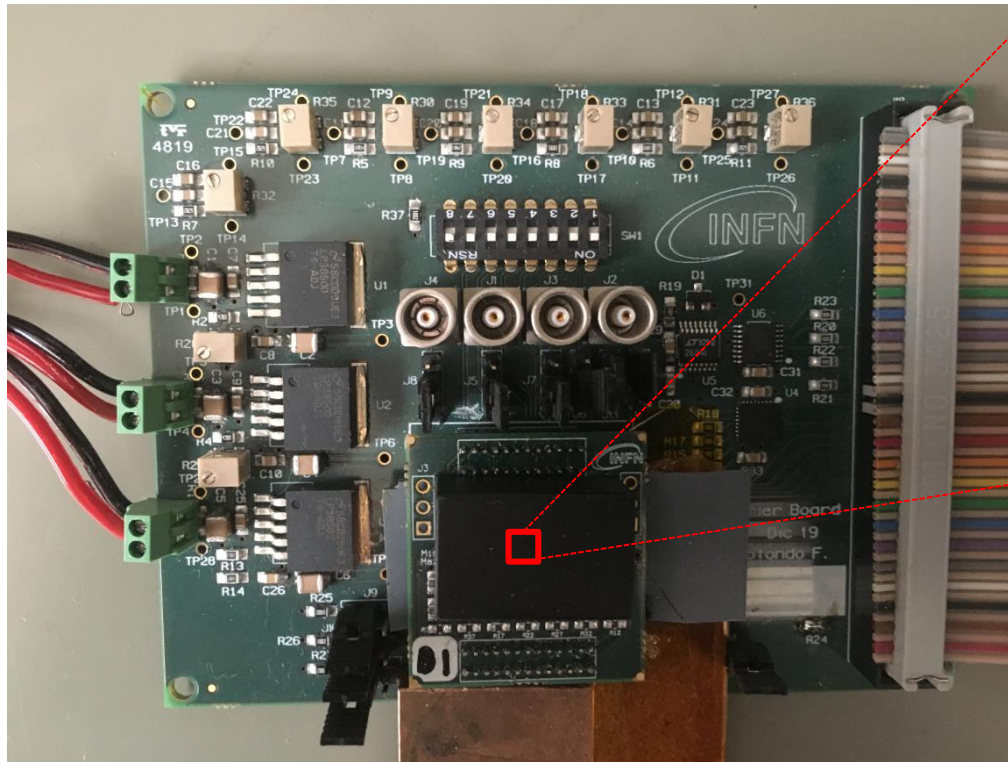
Ethernet + USB



Laptop



- 2 mm x 2 mm chip including a 16x16 matrix featuring the RD53A and RD53B version of the Linear Front-end



- Chip on a small daughter board mounted on a test PCB, including potentiometers for front-end bias setting

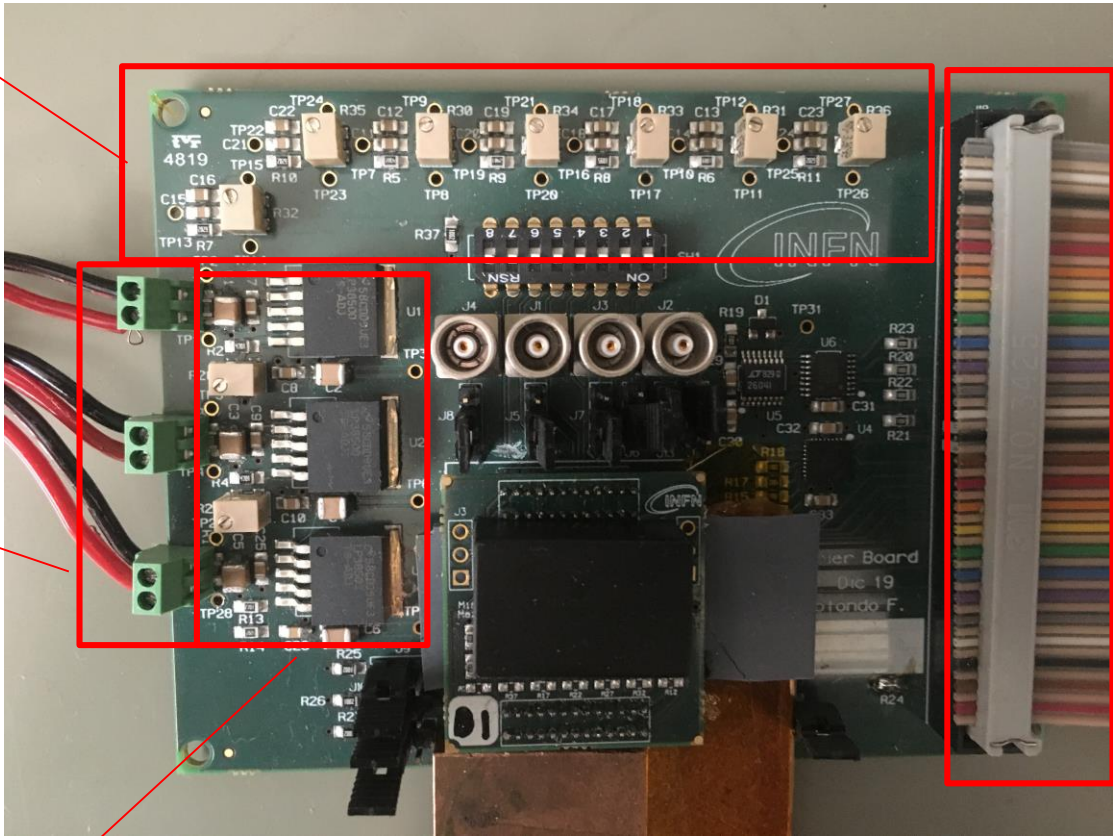


# Test board

Potentiometers for front-end bias setting

Power connectors (from top: analog, digital, aux)

Power supply regulators



FPGA connector

# Main analog performance parameters

- Equivalent noise charge (ENC)
- Threshold dispersion
- Charge sensitivity
- Time-walk
- Time-over-threshold

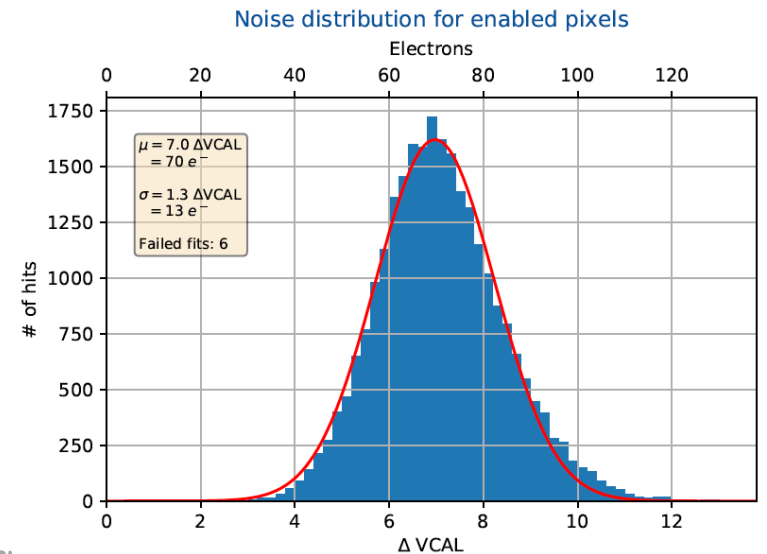
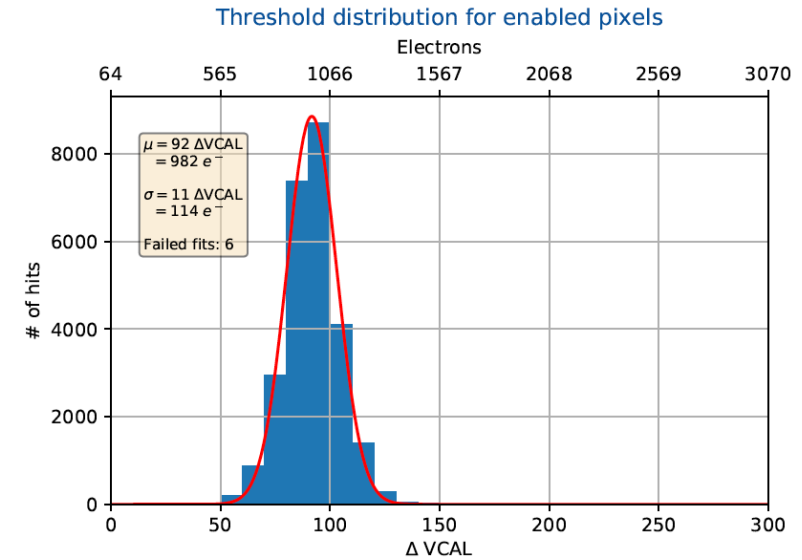
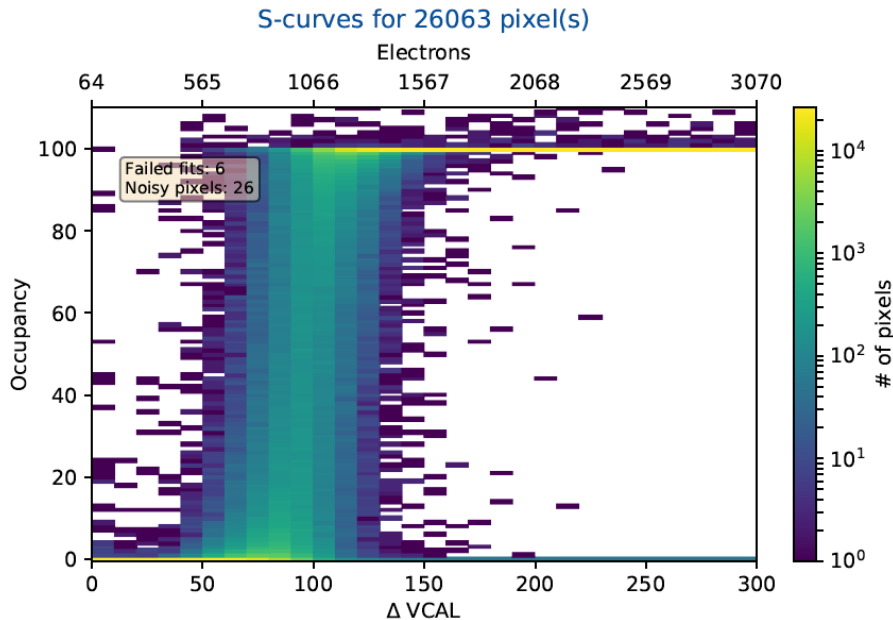


Only the **comparator digital output** is available: how can we measure all these parameters?

# Charge scans

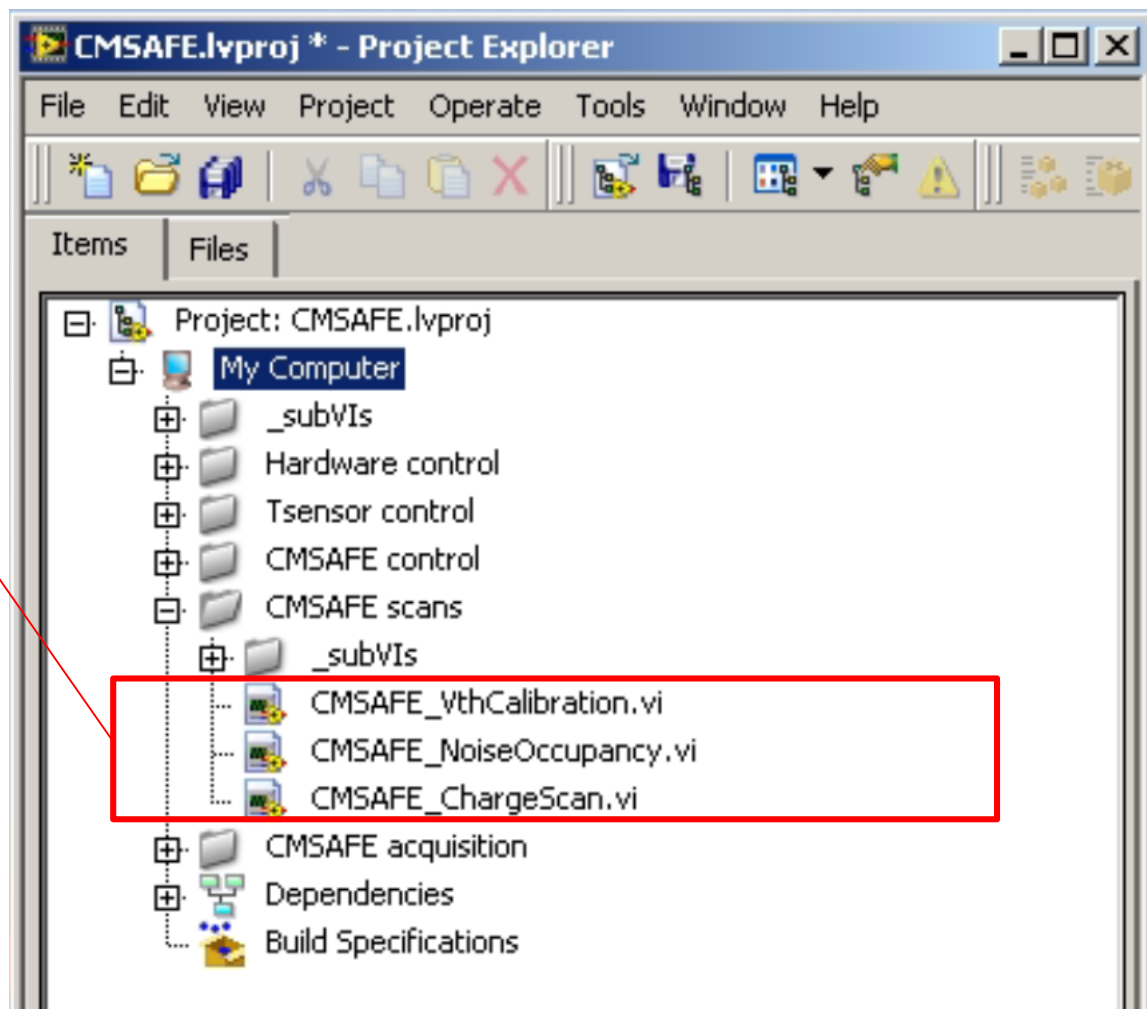
- Measures probability of discriminator to fire vs input charge
- Fitting S-Curve provides measurement of threshold and noise

$$\eta_{hit} = \frac{1}{2} \left[ 1 + \operatorname{erf} \left( \frac{Q_{in} - p_1}{\sqrt{2}p_2} \right) \right]$$



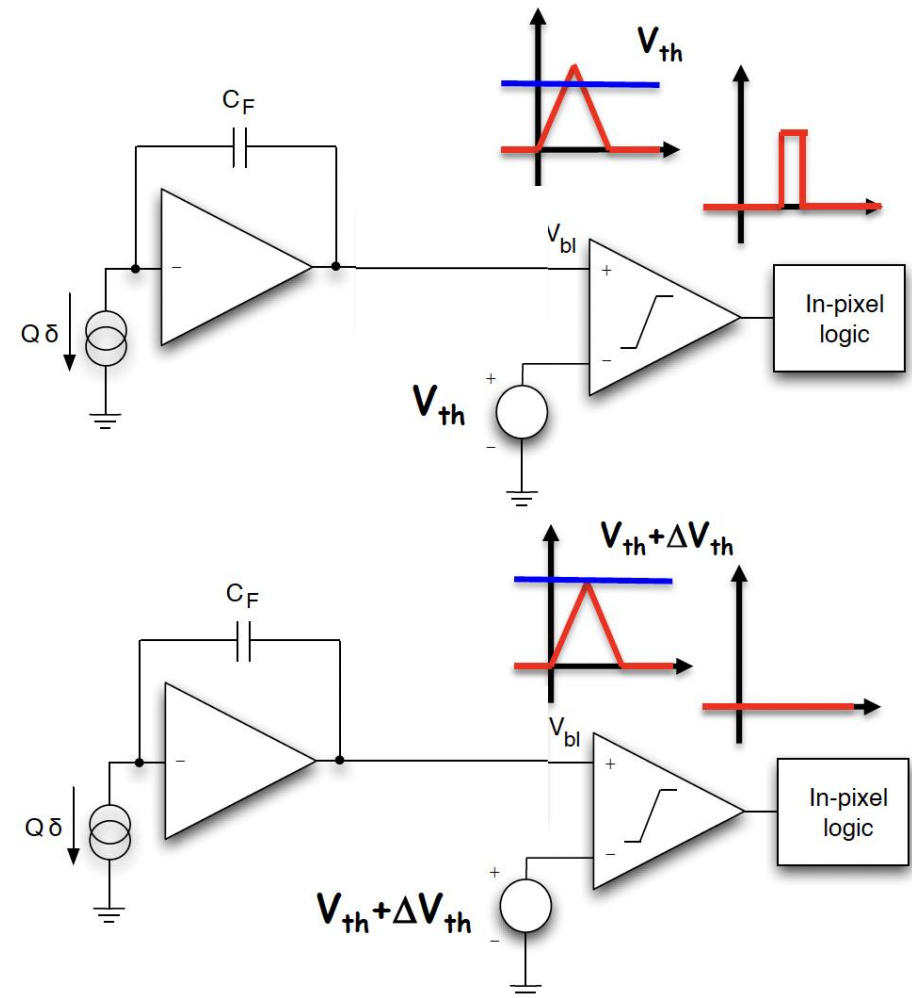
- DAQ system based on LabVIEW
- Main virtual instruments (VIs):
  - Threshold calibration
  - Charge scan
  - Noise occupancy

DAQ control panel



# Threshold tuning

- In a multichannel binary readout circuit, random and systematic variations of process (doping) and geometrical (device dimensions, thickness of the various involved layers) parameters may be responsible for introducing non uniformities in the parallel path followed by the signals
- Two channels, nominally identical to each other and featuring a common threshold at the inverting input of the discriminator, may provide different responses to the same charge pulse at the preamplifier input



# Threshold tuning (VthCalibration.vi)

run timeout (ms) 1000 Firmware xAA00 Board 0 Command error Quit

Start scan Stop scan Save data Load data Load Ok End

Settings Results Temperature

calibration input file

Vth Calibration

Channel range Start 1 Stop 239

threshold

Krummenacher ref voltage

VTH\_GBL A (mV) 500.000

VTH\_GBL B (mV) 560.000

VRIF\_KRUM A (mV) 300

VRIF\_KRUM B (mV) 360

CAL\_MI\_GBL (mV) 500

CAL\_HI\_GBL min (mV) 500 max (mV) 900 Increment 5

TP period 60 us

TP width 20 us

Number of TPs 100

PIXELS 0-127 → RD53A

PIXELS 128-255 → RD53B

CAL\_MI (test pulse setting)

CAL\_HI (test pulse setting)

Middle Th DAC A x8

Middle Th DAC B x10

TDAC codes before tuning (set to mid range)

Check data

PCR A configuration

Output enable 0

Leakage P enable 0

Leakage N enable 0

C\_det = 50 fF enable 0

C\_det = 100 fF enable 0

TP inject enable 0

Gain selector 0

Threshold DAC x0

Power down 0

Configuration bits for RD53A

PCR B configuration

Output enable 0

Leakage P enable 0

Leakage N enable 0

C\_det = 50 fF enable 0

C\_det = 100 fF enable 0

TP inject enable 0

Threshold DAC x00

Power down 0

Configuration bits for RD53B

# Threshold tuning

timeout (ms) 1000 Firmware AA00 Board 0 Command error Quit

Start scan Stop scan Save data Load data Load Ok

Settings Results Temperature

**Q/V conversion factor  $\rightarrow \sim 50 \text{ e-/mV}$**

End

Data Fit

Invalid events

532.762	Mean
1.44	Sigma

Channel 239 CMSAFE SPI

**Hit efficiency curve for a single pixel (ch 239)**

- Threshold (CAL\_HI): 533 mV
- CAL\_MI set to 500 mV
- Effective threshold  $\rightarrow (533 \text{ mV} - 500 \text{ mV}) \times 50 \text{ e-/mV} = 1650 \text{ e-}$
- Noise:  $1.44 \text{ mV} \times 50 \text{ e-/mV} = 72 \text{ e-}$

**Threshold dispersion:**

- $1.47 \text{ mV} \times 50 \text{ e-/mV} = 73 \text{ e-}$  (RD53A)
- $0.98 \text{ mV} \times 50 \text{ e-/mV} = 49 \text{ e-}$  (RD53B)

**Threshold distributions**

Binning 1

Type A Type B

Type A

533.949	Mean
1.47	Sigma

Type B

532.052	Mean
0.979	Sigma

**TDAC search**

Invalid events

13.2	Mean
0.49	Sigma

CMSAFE.lvproj/My Computer

# EXE1: threshold tuning



- Set detector capacitance to 50 fF and tune the matrix to 1000 e-
- What is the threshold dispersion for RD53A and RD53B?
- Why there is a significant difference between the two values?
  
- Hints → start tuning the matrix to higher threshold, than decrease the threshold down to 1000 e-



# Charge scan (ChargeScan.vi)

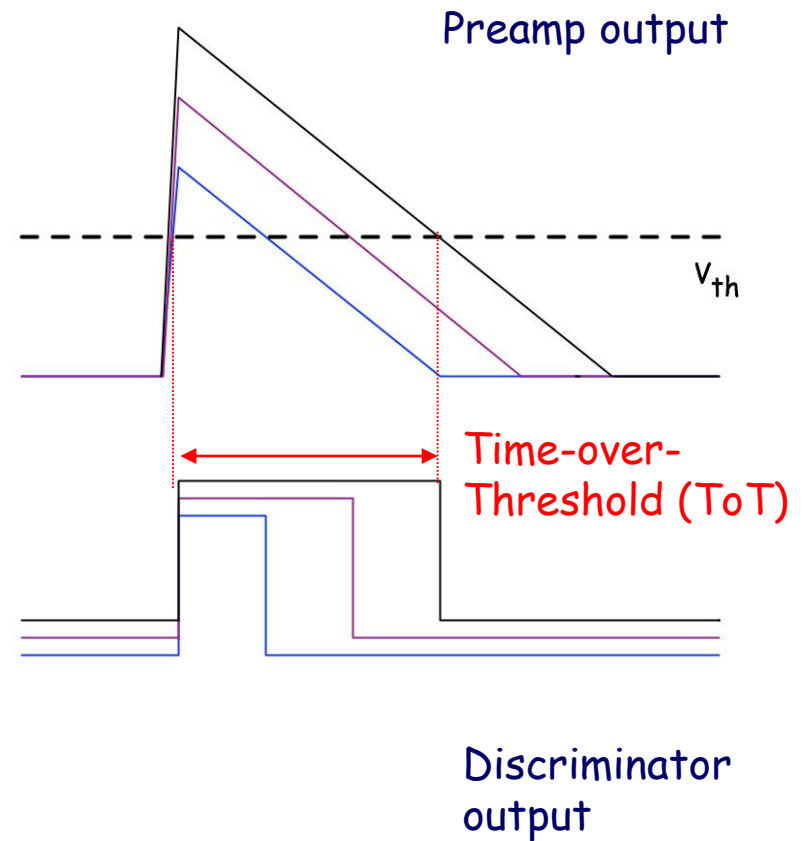
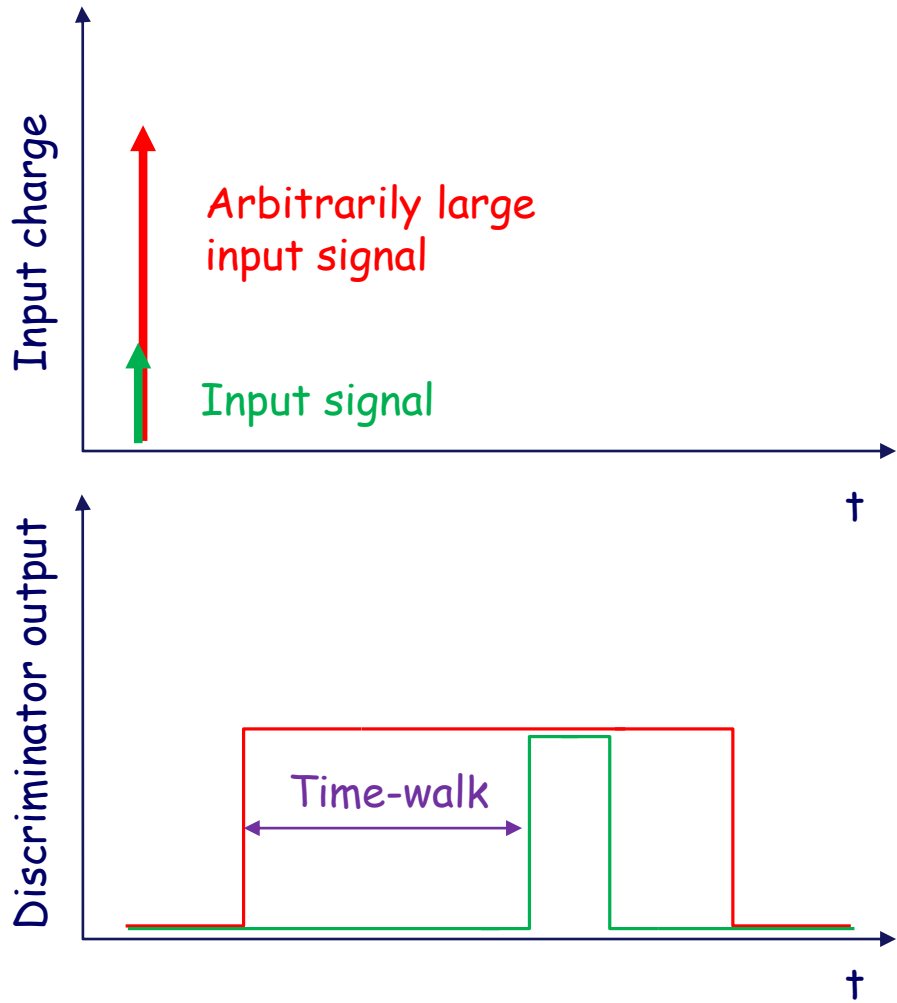
The screenshot shows the CMSAFE\_ChargeScan.vi software interface. The window title is "CMSAFE\_ChargeScan.vi" and it has a menu bar with "File", "Edit", "View", "Project", "Operate", "Tools", "Window", and "Help". Below the menu bar are icons for running, refreshing, and pausing. A toolbar contains buttons for "Start scan", "Stop scan", "Save data", "Load data", "Load Ok", and "End".

There are several tabs: "Settings", "Channel measurements", "S curve histograms", "TW histograms", "TOT histograms", and "Temperature". The "Settings" tab is active.

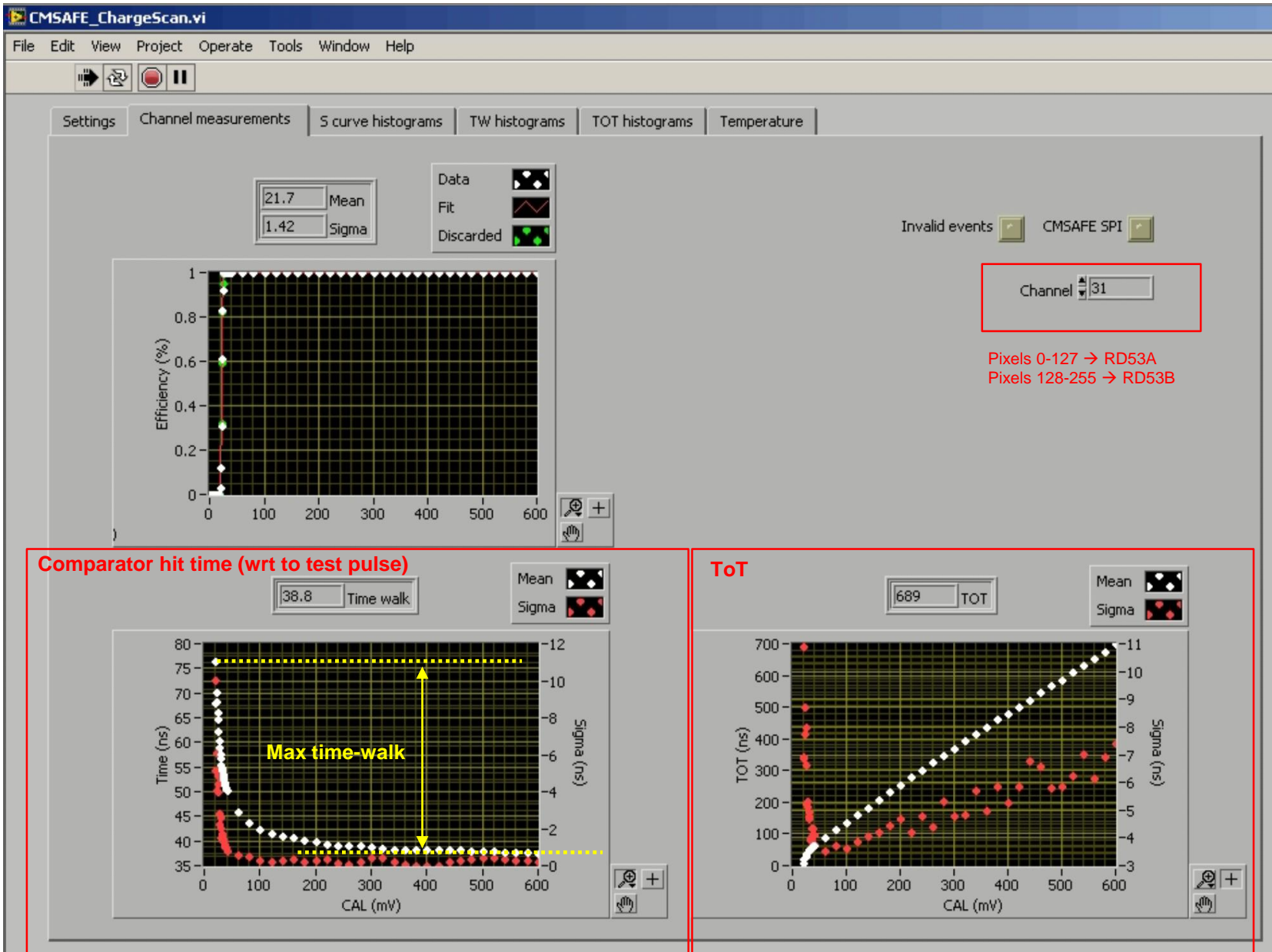
Key settings and annotations:

- Calibration:** "Vth Calibration" is set to "C:\Users\...\calib\_PREAMP\_30\_CD\_50\_LDAC\_14\_soglia\_1000.txt".
- Channel range:** Start is 1, Stop is 239. An annotation indicates "Pixels 0-127 → RD53A" and "Pixels 128-255 → RD53B".
- Charge scan settings:** CAL\_MI\_GBL is 500. CAL\_HI\_GBL is a range from 500.000 to 1100.000 with an increment of 1.000. The "Double range" checkbox is checked. An annotation points to this section: "Charge scan settings" with a list:
  - Min-max value for CAL\_HI
  - Fixed CAL\_MI
  - Possibility to enable double range scan for faster measurements
- TP parameters:** TP period is 60 us, TP width is 20 us, and Number of TPs is 100.
- Time threshold:** Set to -1 ns.
- PCR configurations:** PCR A and PCR B configurations are shown. PCR A has C\_det = 50 fF enable set to 1. PCR B has C\_det = 50 fF enable set to 1. An annotation indicates "Configuration read from calibration file".

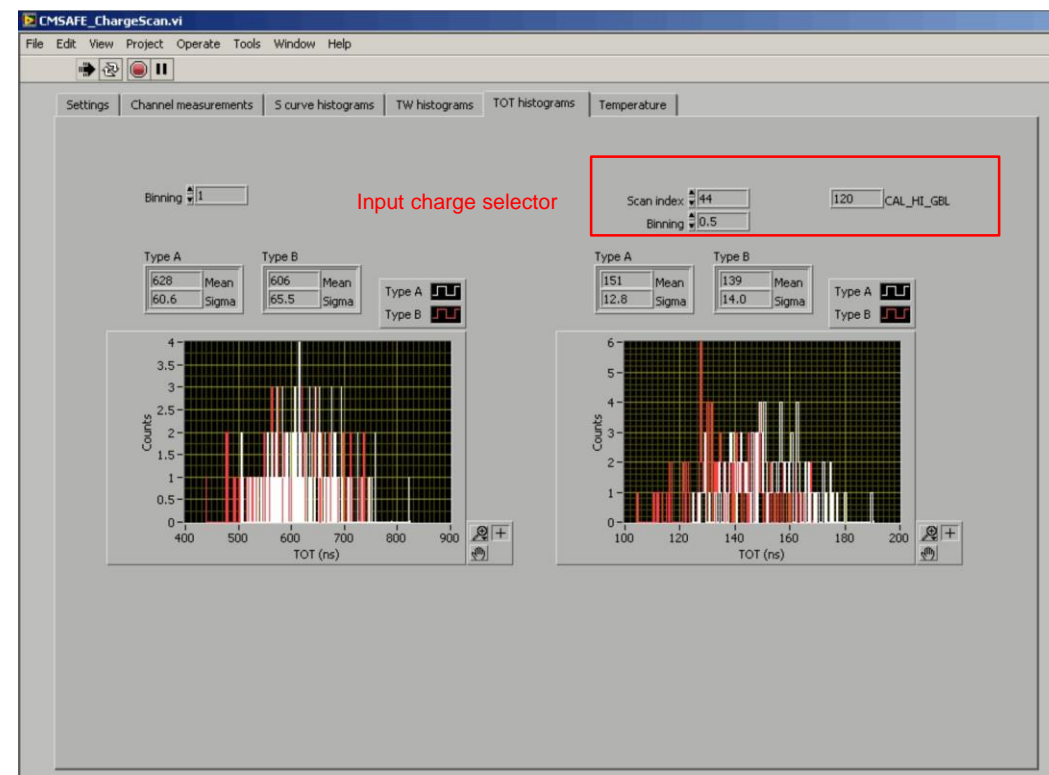
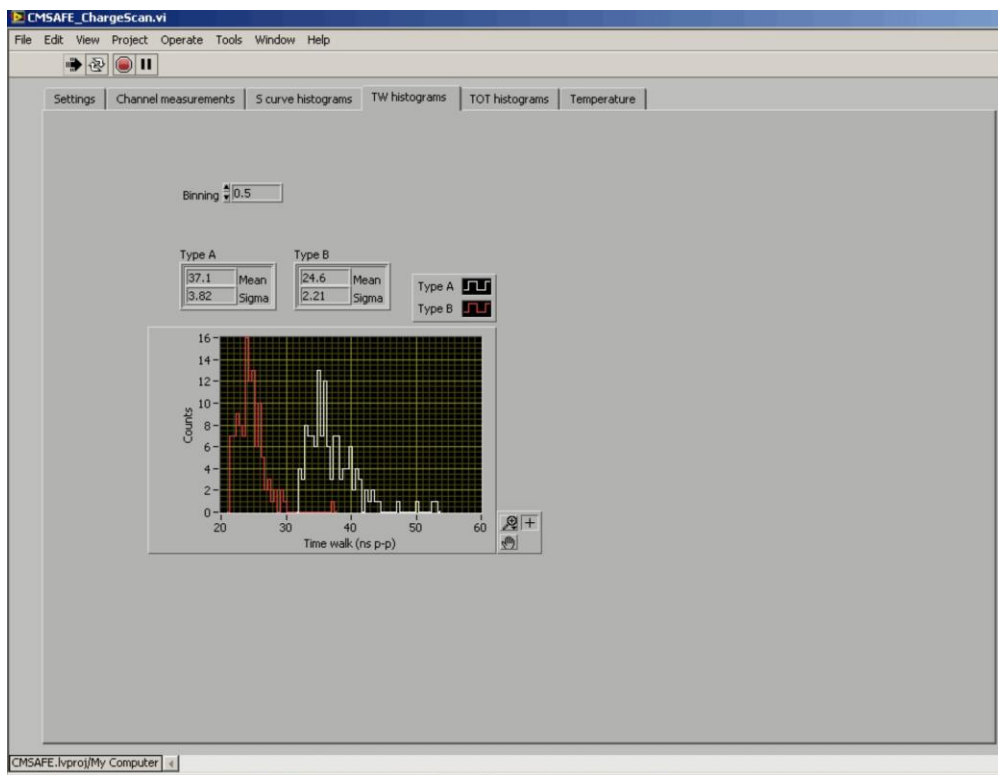
# Time-walk and Time-Over-Threshold (ToT)



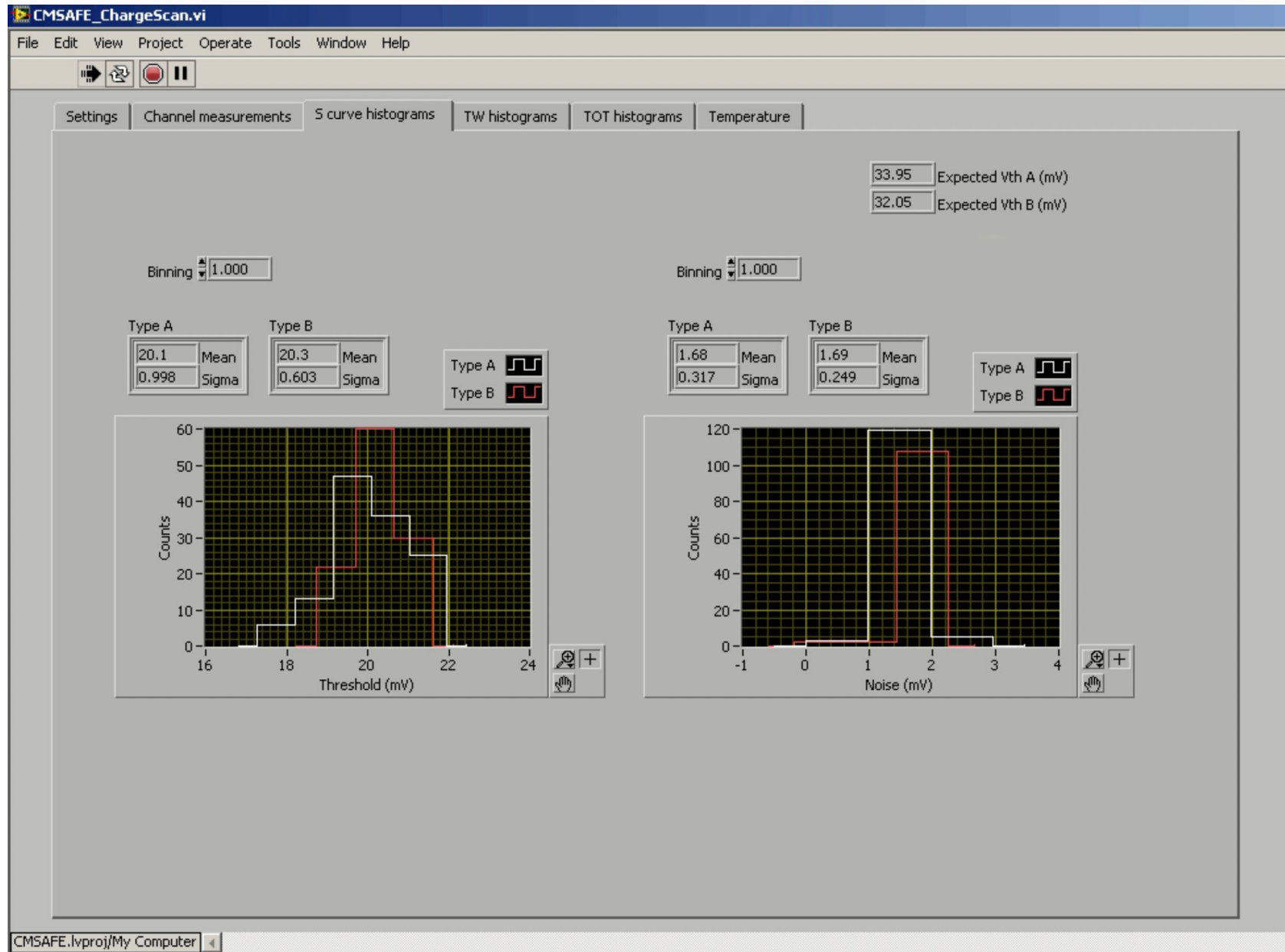
# Time-walk and ToT



# Time-walk and ToT histograms



# Threshold and noise histograms



# Noise and equivalent noise charge (ENC)

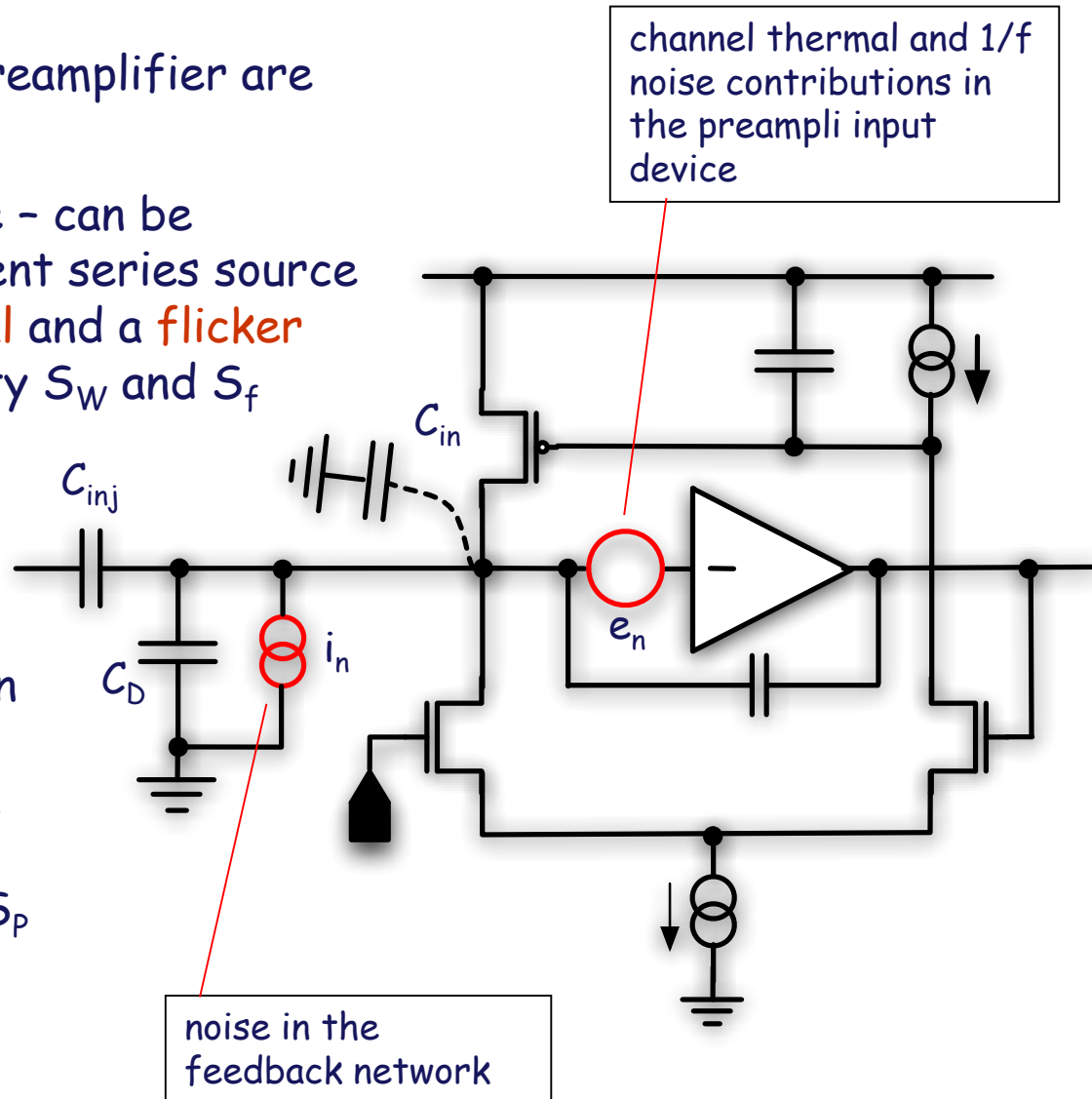
- The main noise sources in the preamplifier are located

- in the preamplifier input device - can be represented through an equivalent series source ( $e_n$ ) and includes a **white thermal** and a **flicker** term with power spectral density  $S_W$  and  $S_f$  respectively

$$\overline{\frac{de_n^2}{df}} = S_W + \frac{S_f}{f}$$

- in the feedback network - can be represented through an equivalent parallel source ( $i_n$ ), mostly with a white spectrum with power spectral density  $S_p$

$$\overline{\frac{di_n^2}{df}} = S_p$$



# ENC and detector capacitance

- A quite general expression for the ENC is the following, accounting for the different noise contribution

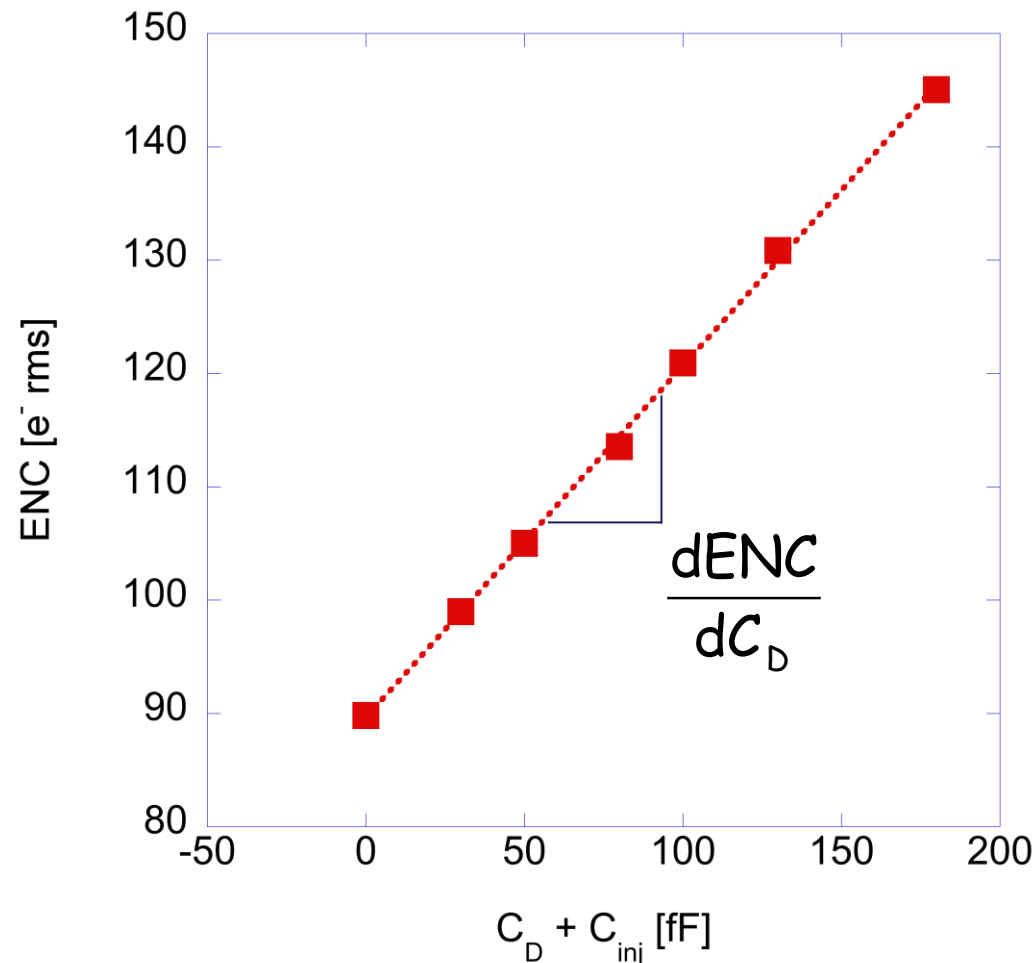
$$\text{ENC}^2 = C_T^2 A_1 S_W \frac{1}{t} + C_T^2 A_2 S_f + A_3 S_p t$$

$$C_T = C_D + C_{in} + C_F + C_{inj}$$

$A_1, A_2, A_3$  = shaping coefficient

$\tau$  = shaping time (has some relationship with  $t_p$ )

- The effect of the series noise source on the overall noise performance gets more pronounced as  $C_T$  (the capacitance shunting the circuit input terminal) increases
- The slope of the ENC vs  $C_D$  is a figure of merit telling us how the noise performance of the circuit degrades as the detector capacitance increases



# EXE2: charge scan

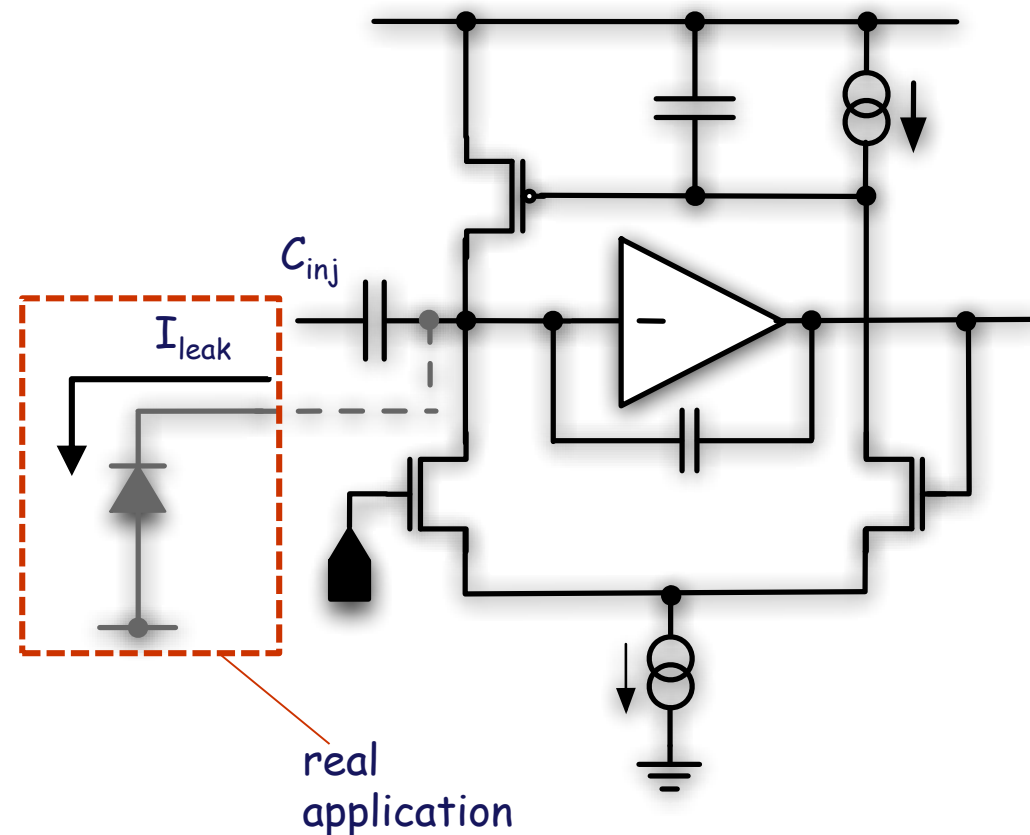


- Set the detector capacitance to 50 fF and tune the matrix to 1000 e<sup>-</sup>
- Measure the maximum time-walk for RD53A and RD53B
- Measure the ToT for an input charge of 6000 e<sup>-</sup>
- Set the threshold to around 2000 e<sup>-</sup> and evaluate the ENC for CD=0, 50, 100 and 150 fF. What is the dENC/dCD slope for the front-end channels?



# Measurements in the presence of a leakage current

- The readout channel has to work correctly also in the presence of a leakage current at the input terminal
- In the real application, this leakage current comes from the detector and may exceed 10 nA when the detector is exposed to very high ionizing radiation doses - ~1 Grad for 10 year operation is expected for the inner layers of the CMS detector at the HL-LHC
- In the DUT, a leakage emulator circuit can be enabled, providing a DC current  $I_{leak}$  at the preamp input



# EXE3: detector leakage current



- Set the threshold to around 2000 e- and the detector capacitance to 50 fF.
- Measure the ENC.
- Enable the leakage current emulator (default values is around 20nA/pixel). How does the ENC vary?

# Noise hit rate

- An important figure of merit for a front-end chip is the **noise hit rate** at a given threshold.
- Ideally, we would like to have a low threshold for better efficiency. This actually translates in larger number of hits due to noise.
- **Optimum efficiency** is generally constrained by the maximum rate of noise induced transitions at the discriminator output, or maximum noise hit rate, due to the signal at the preamplifier output randomly crossing the discriminator threshold. Such a noise hit rate limit is strongly dependent on the readout architecture and on the target readout efficiency. Under some very general assumptions, in a binary channel the noise hit rate  $f_n$ , whose analysis represents a specific aspect of the more general level crossing problem, can be written as

$$f_n = f_{n0} \cdot e^{-\frac{Q_{t0}^2}{2ENC_{sl}^2}}$$

where  $Q_{t0}$  is the mean value of the threshold, and  $f_{n0}$  is the noise hit rate at zero threshold.

L. Ratti et al. "Design of Time Invariant Analog Front-End Circuits for Deep N-Well CMOS MAPS" DOI: [10.1109/TNS.2009.2024536](https://doi.org/10.1109/TNS.2009.2024536)

# Noise hit rate (NoiseOccupancy.vi)

timeout (ms) 1000 Firmware x0000 Board 0 Command error   Quit

Start scan Stop scan Save data Load data Load Ok Init comms

Settings Results

Vth Calibration

Channel range Start 0 Stop 255

VTH\_GBL A (mV) 360  
VTH\_GBL B (mV) 360  
VRIF\_KRUM A (mV) 1000  
VRIF\_KRUM B (mV) 1000  
CAL\_MI\_GBL (mV) 500  
CAL\_HI\_GBL A (mV) 600  
CAL\_HI\_GBL B (mV) 600

TP T Cycles 1000  
TP period 90 us

PCR A configuration  
Output enable 0  
Leakage P enable 0  
Leakage N enable 0  
C\_det = 50 fF enable 0  
C\_det = 100 fF enable 0  
TP inject enable 0  
Gain selector 0  
Threshold DAC x0  
Power down 0

PCR B configuration  
Output enable 0  
Leakage P enable 0  
Leakage N enable 0  
C\_det = 50 fF enable 0  
C\_det = 100 fF enable 0  
TP inject enable 0  
Threshold DAC x00  
Power down 0

**The system records the noise hits in a time frame lasting  $1000 \times 90\mu\text{s} = 90\text{ms}$**   
Pixel noise hit rate = total\_counts/90ms/num\_pixels

# EXE4: noise hit rate



- Tune the matrix threshold to  $1000e^-$ .
- Measure the noise hit rate.
- Repeat the measure for smaller thresholds (900, 800, 700, 600, 500).
- Plot the noise hit rate as a function of the threshold.