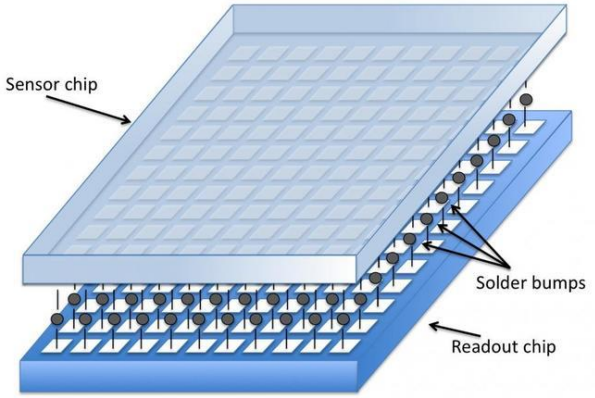
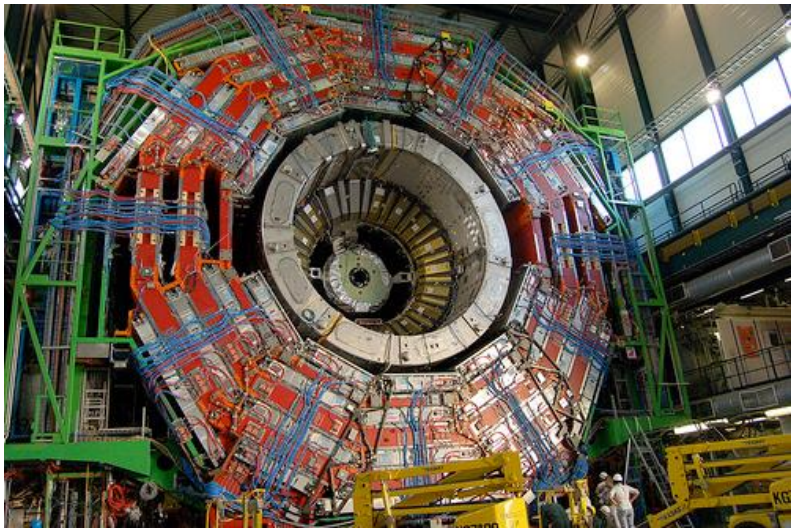
Lab session on
RD53 Pixel Front-End Characterization

Valerio Re, Luigi Gaioni
(valerio.re@unibg.it, luigi.gaioni@unibg.it)
Università di Bergamo and INFN Pavia, Italy

Focus of the lab

- Pixel front-end ASICs are located at the very beginning of the **signal processing chain** in pixel based detectors used in many fundamental and applied research fields
- **Experimental characterization** of front-end circuits in advanced microelectronic technologies is an **integral part of the implementation** of modern radiation detection systems
- The focus of the lab will be the **characterization of front-end channels for pixel detectors in a 65 nm CMOS technology**
- The circuit under test is a prototype chip for the **CMS phase 2 upgrade** designed in the framework of the international **RD53 collaboration**

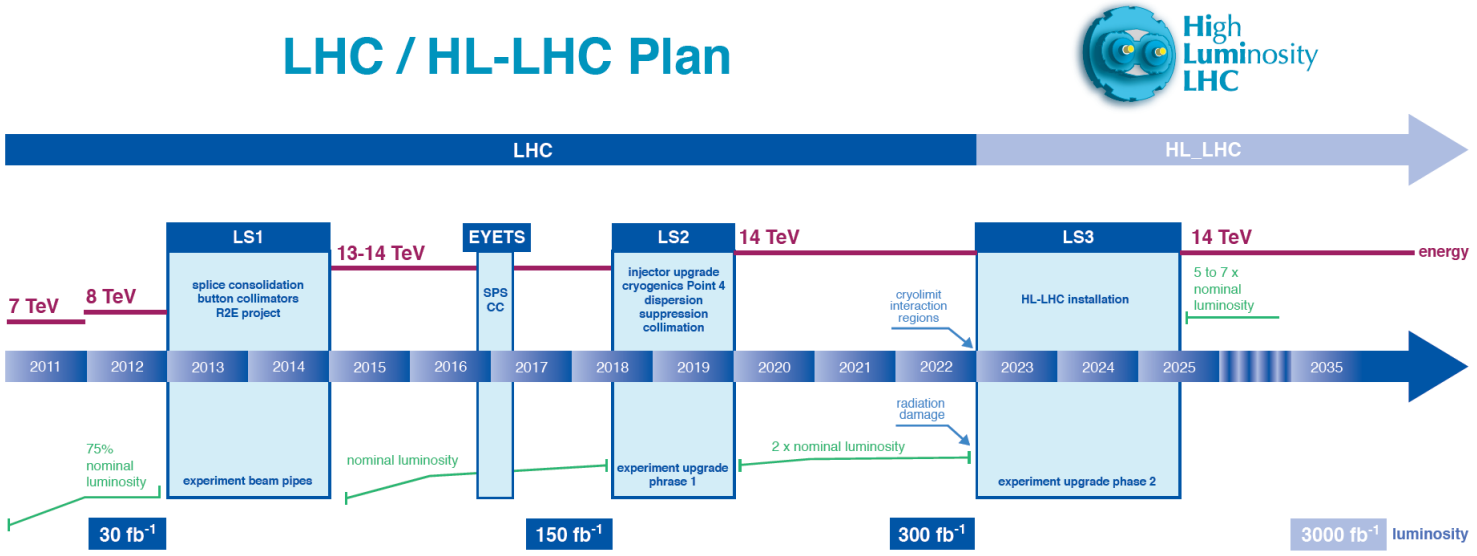




Pixel Detector Requirements at HL LHC

Very **challenging requirements** for the innermost layers of the pixel detectors in ATLAS and CMS @ the HL LHC

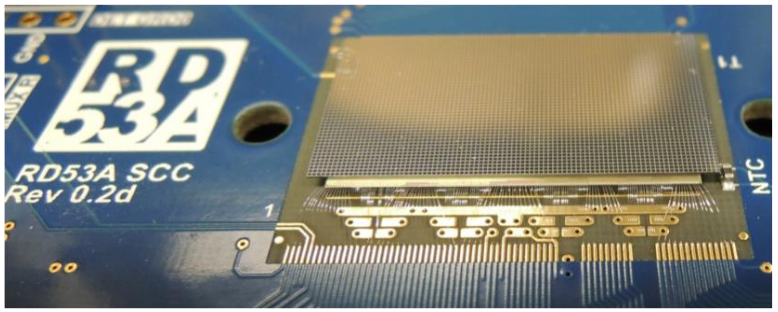
- Very **high particle rate** → pixel hit rates up to 3 GHz/cm^2
- **Small pixels**: 50x50um^2 → increased resolution, improved track separation
- **Large chips**: ~2cm x 2cm (1 billion transistors)
- **Low mass, low power systems**: ~10 uW per cell (including analog and digital sections)
- **Low threshold**: ~1000 e- → severe requirements on noise and dispersion
- **Harsh radiation environment**: 1 Grad(SiO_2) TID; 10^{16} eq. n/cm^2 fluence



RD53 – An overview

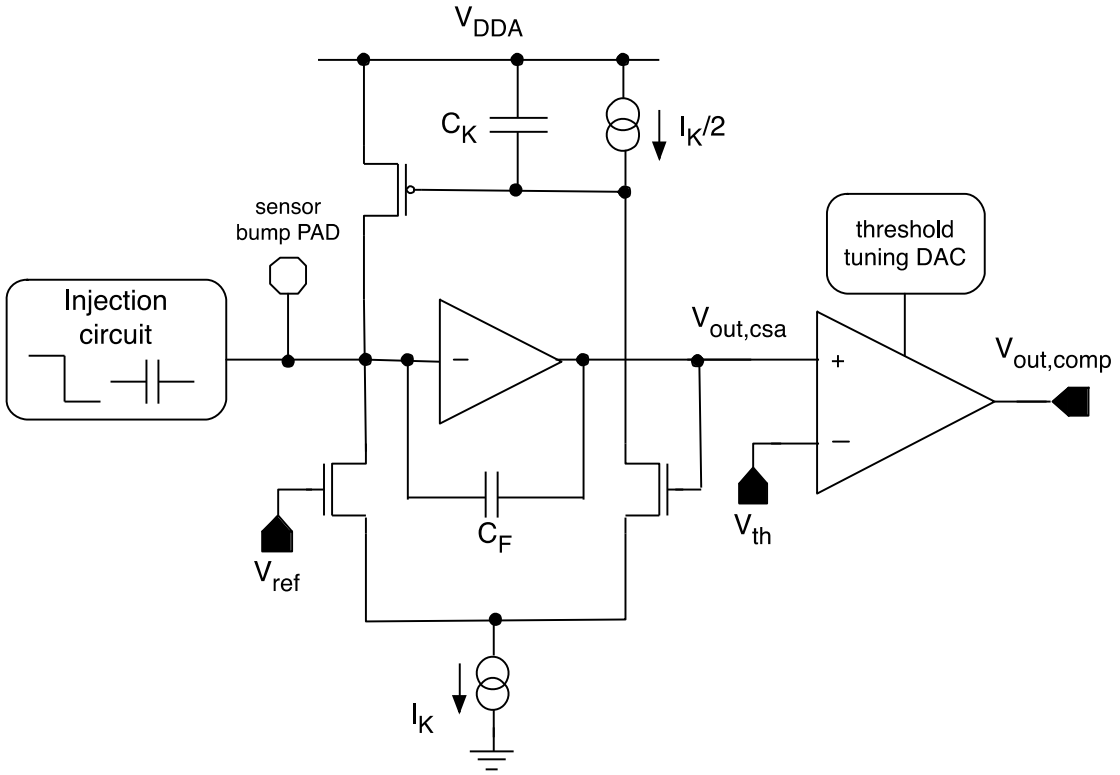
- Collaboration among **ATLAS** & **CMS** communities aiming at the development of large scale pixel chips for LHC phase-2 upgrades
- **65 nm CMOS** is the common technology platform

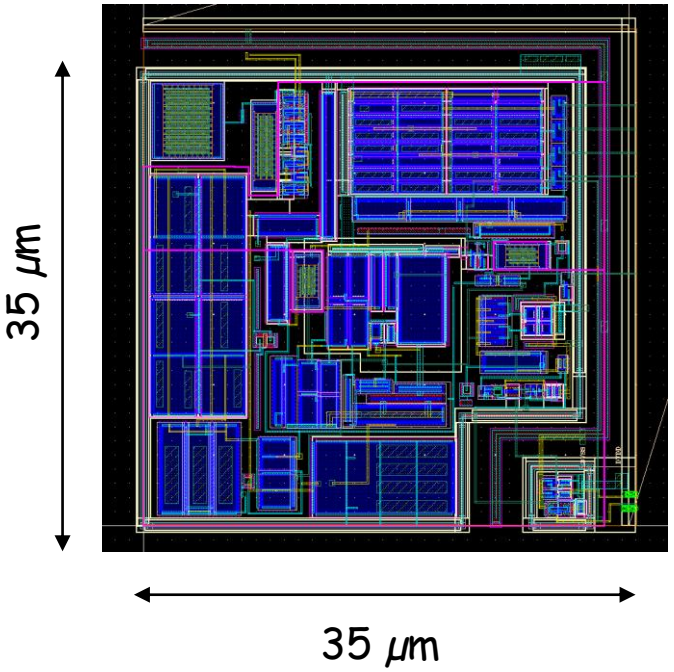
- **RD53 Goals**
  - Detailed understanding of **radiation effects** in 65nm → guidelines for radiation hardness
  - Design and characterization of **full size pixel array chip**



- The efforts of the RD53 collaboration led to the submission (2017) of the **RD53A chip including three different front-end flavors: Synchronous, Linear and Differential**
- Linear front-end has been adopted in the **RD53B CMS** chip (submitted in June 2021), including a matrix of 336x432 pixels (50x50 μm^2 each)
- A small prototype chip including **RD53A** and **RD53B** Linear front-end has been submitted and **will be characterized during lab activities**

RD53 Linear front-end

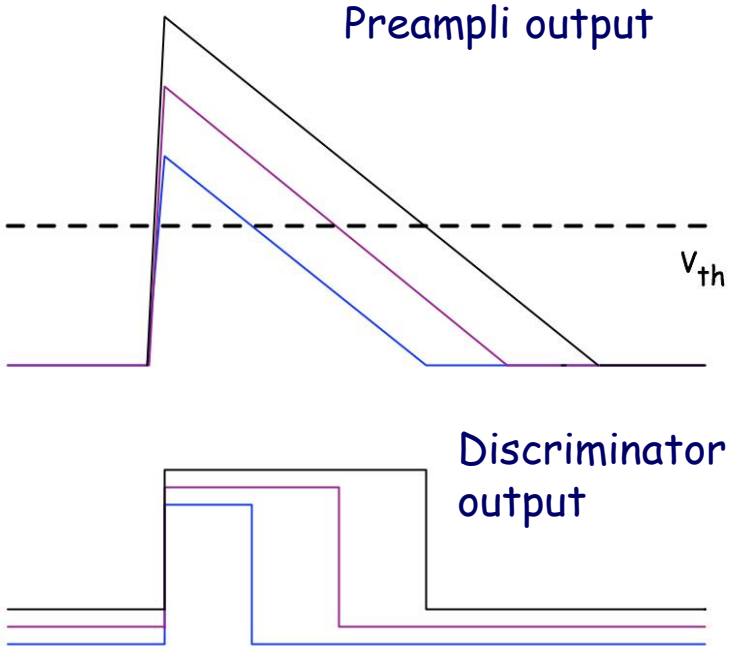




- **Single stage front-end** with **Krummenacher feedback** to comply with the expected large increase in the detector leakage current
- Low power asynchronous **current comparator** combined with a **40 MHz Time-over-Threshold (ToT) counter** for digitization of the signal
- 4 bit (RD53A) and 5 bit (RD53B) local DAC for **threshold tuning**

Time over threshold (ToT)

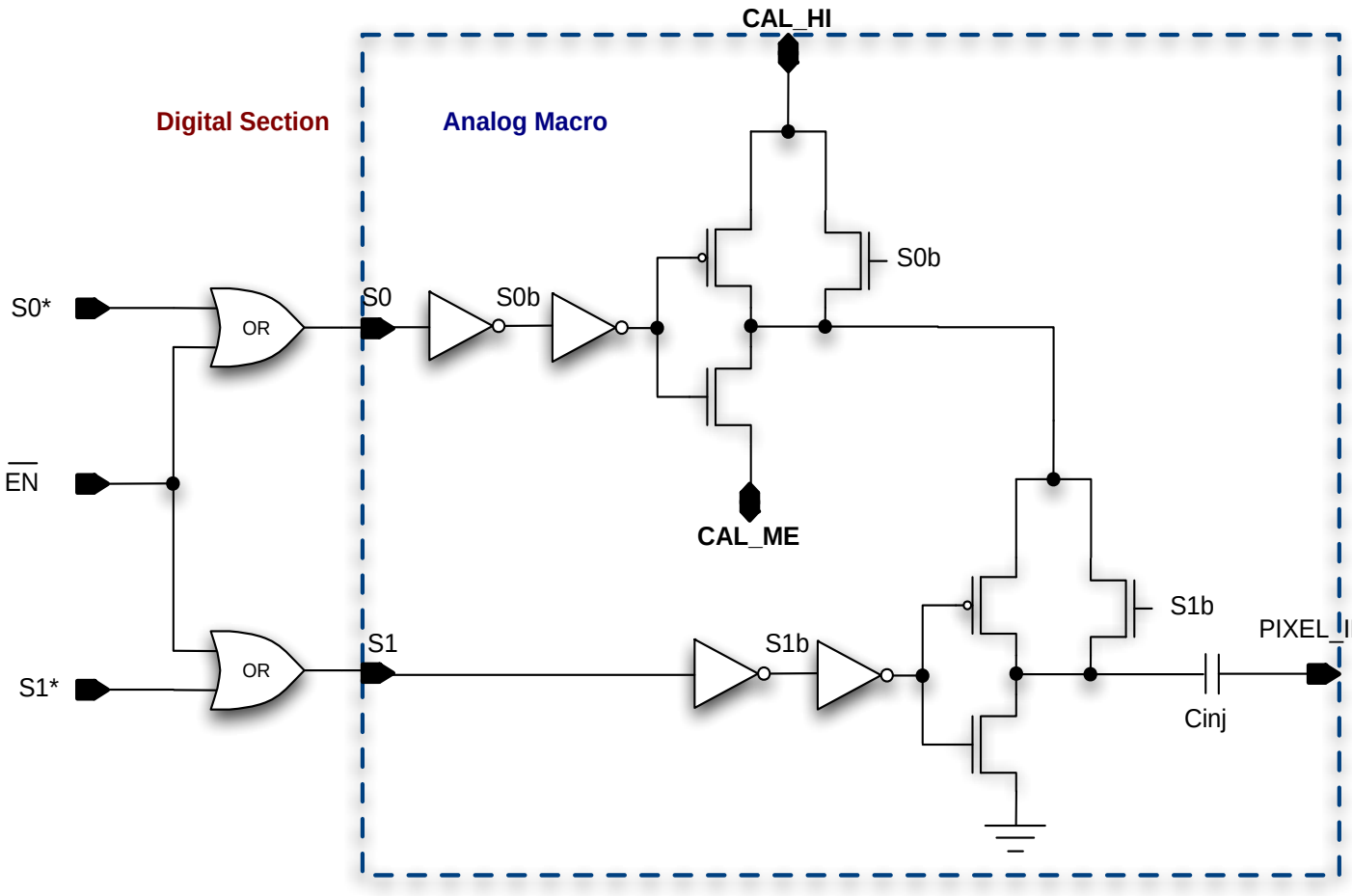
- The Time over Threshold (ToT) technique provides a direct amplitude-to-time conversion; the signal at the preamp output is compared to a fixed voltage at the input of a threshold discriminator; the signal at the output of the discriminator is a digital pulse, whose duration is equal to the time during which the signal at the preamp output exceeds the threshold; digitization is easily achieved by computing the logic AND between the discriminator pulse and a reference clock and by counting the number of clock pulses



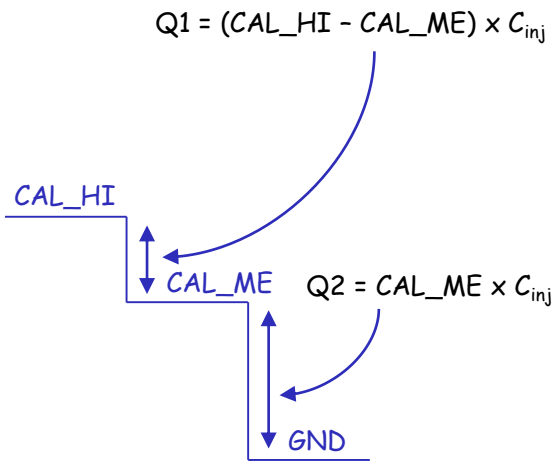
- If the signal at the preamp output returns to the baseline with a constant slope, then a linear relationship exists between the peak amplitude at the preamp output and the ToT duration (the rise time of the preamp output signal is assumed to be negligible)

$$ToT = \frac{V_{peak} - V_{th}}{\left| \frac{dV_{shaper}}{dt} \right|}$$

Analog scan



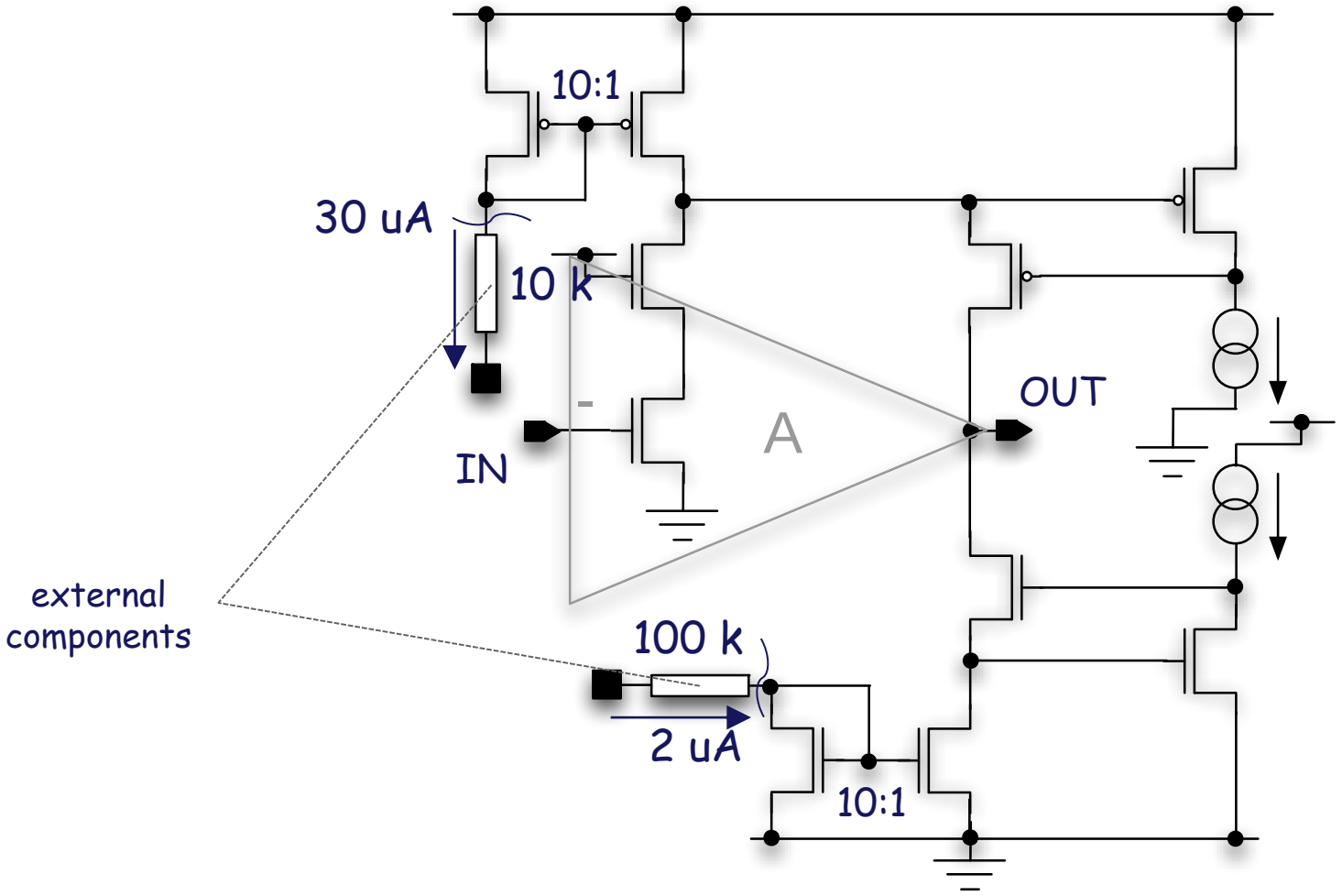
Q-V conversion factor → ~50 e-/mV



- Local generation of the analog test pulse starting from 2 defined DC voltages CAL_HI and CAL_MI distributed to all pixels and a 3rd level (local GND)
- It is possible to generate two consecutive signals of the same polarity

Amplifier schematic

- Gain stage based on a folded cascode configuration

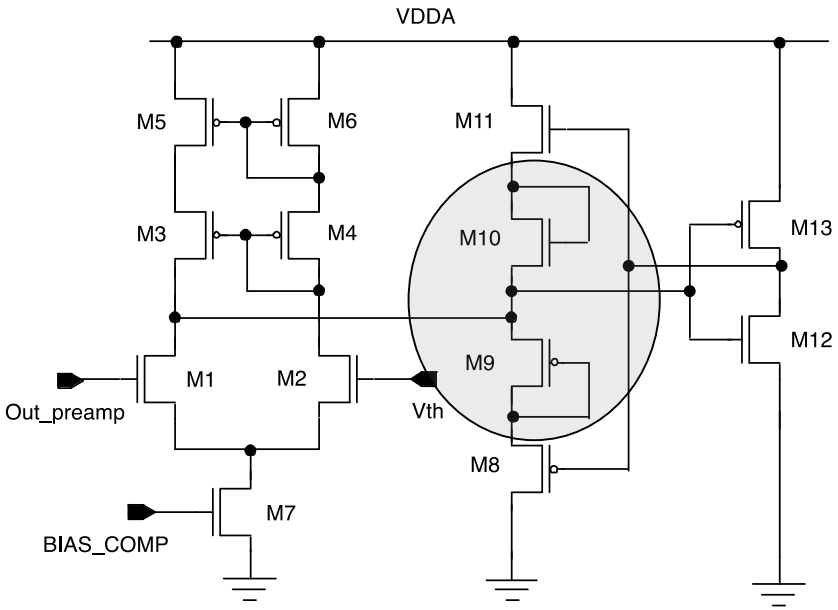


total power dissipation is about 3.8 uW (not considering power in the reference branch of the mirror – the same reference branch can be used for all the pixels in an array)

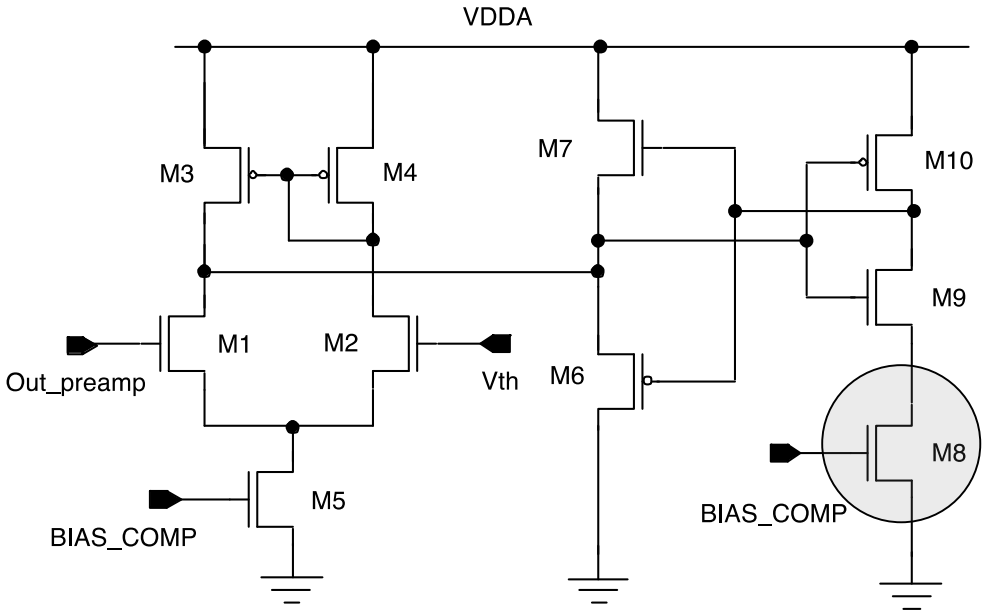
Boosting time-walk performance

- Partial re-design of the **comparator** led to improvement in front-end **time-walk** performance

RD53A

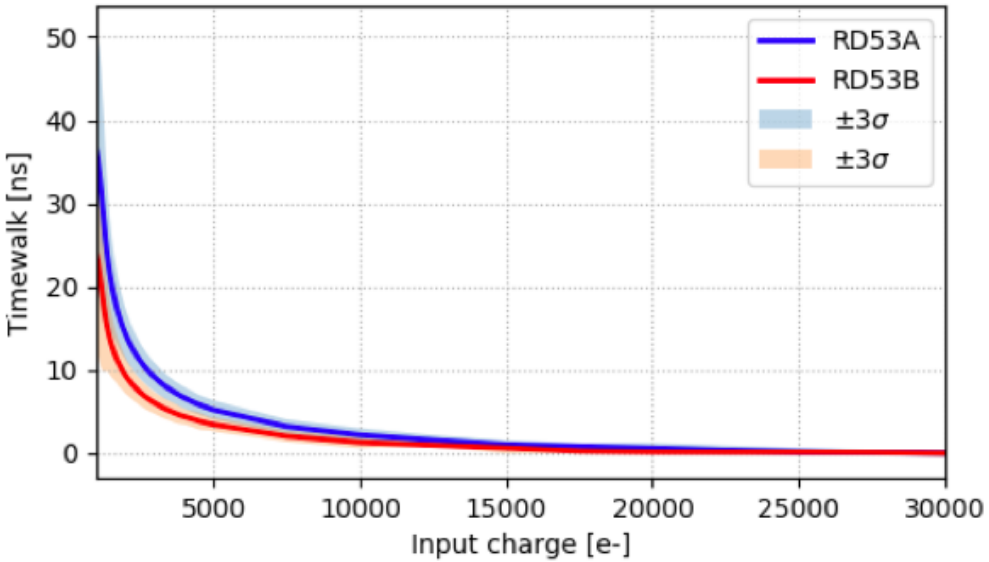


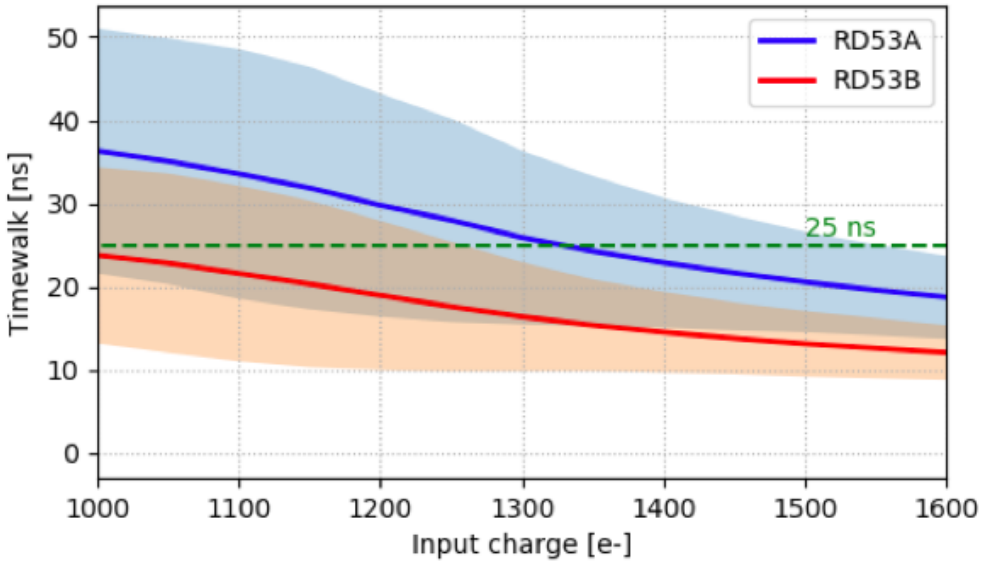
RD53B



- Fast turn-on time of M6 and M7 (RD53B) thanks to removal of M9 and M10 (RD53A)
- Current starving M8 (RD53B)

Time-walk test results

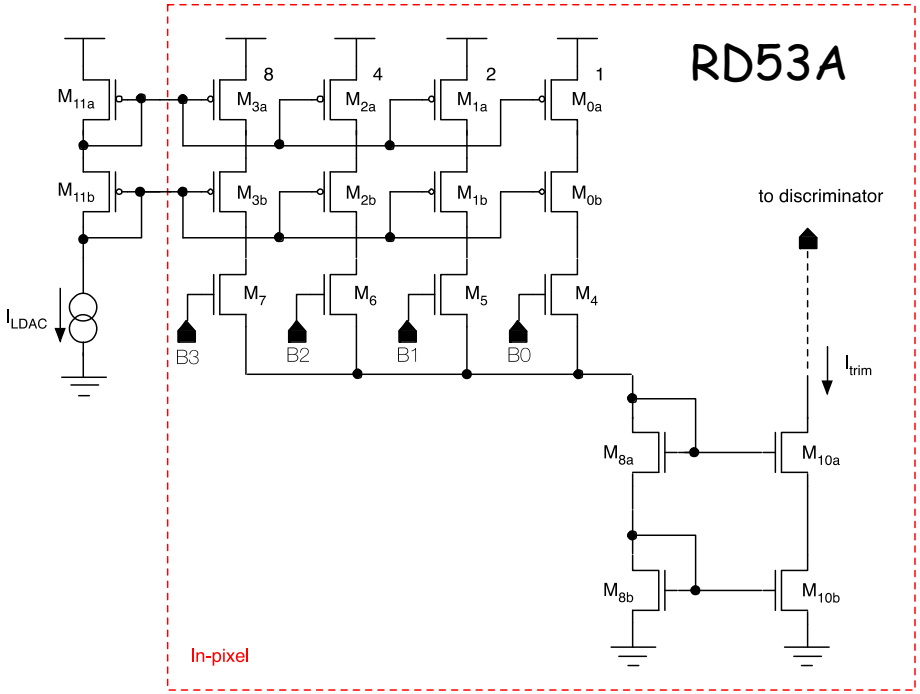


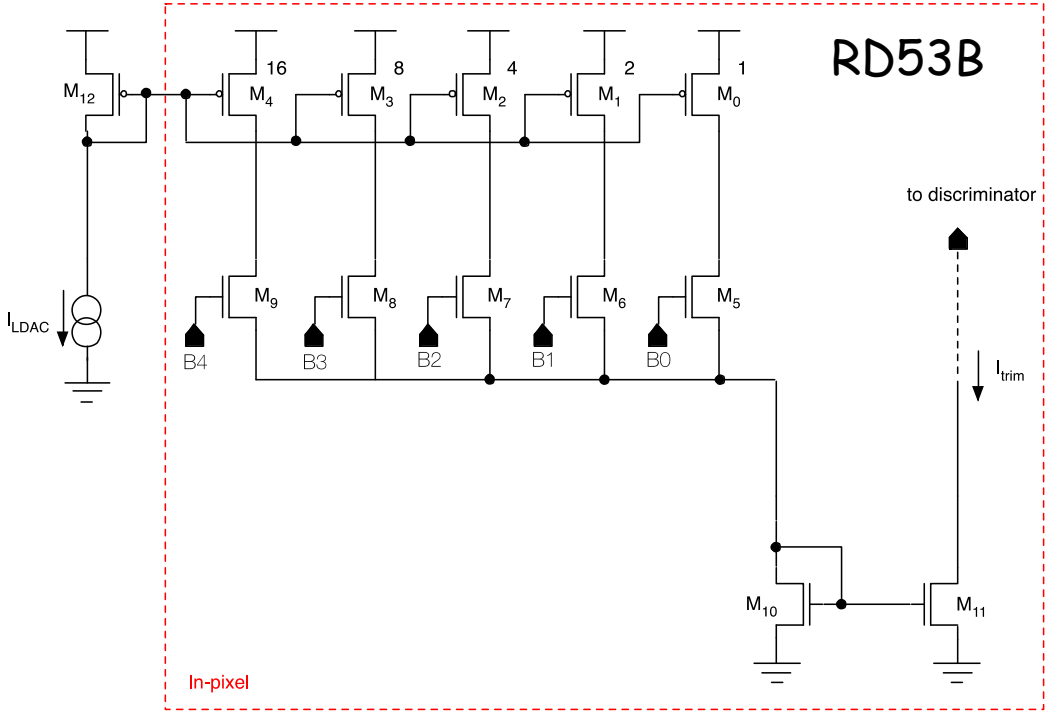


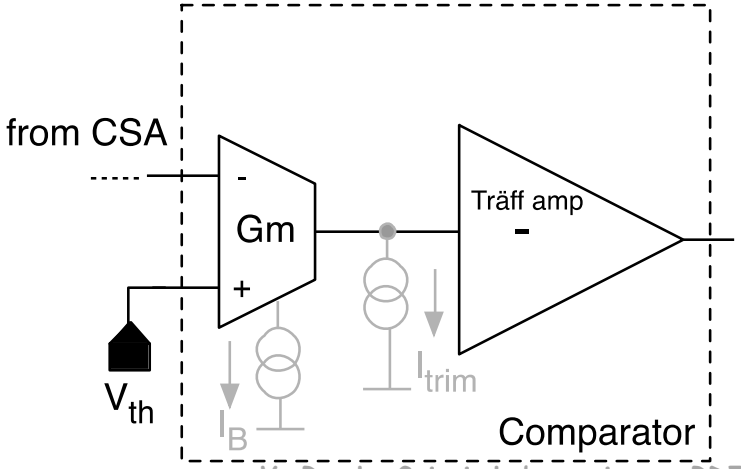
- Results on a sample chip at T=-20° C
- Threshold ~1000 e- , 5uA per-pixel current consumption, 133 ns ToT @ Q_{in}=6ke-, C_D=50fF

Significant **improvement in time-walk** at the cost of a marginal increase (~4%) in static current consumption

Threshold tuning DACs



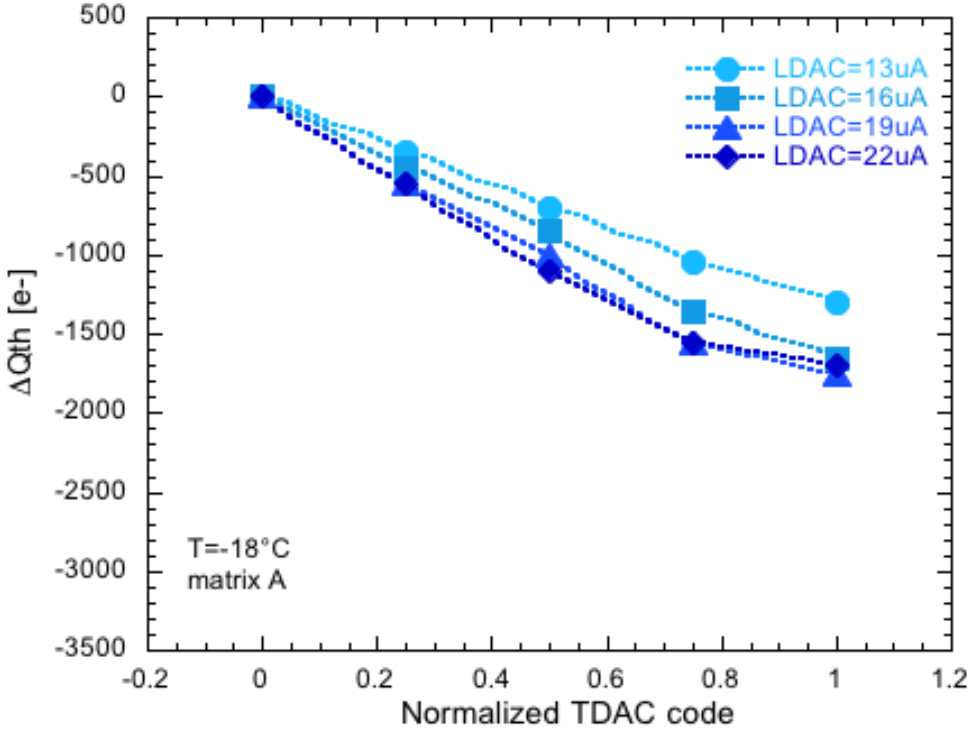




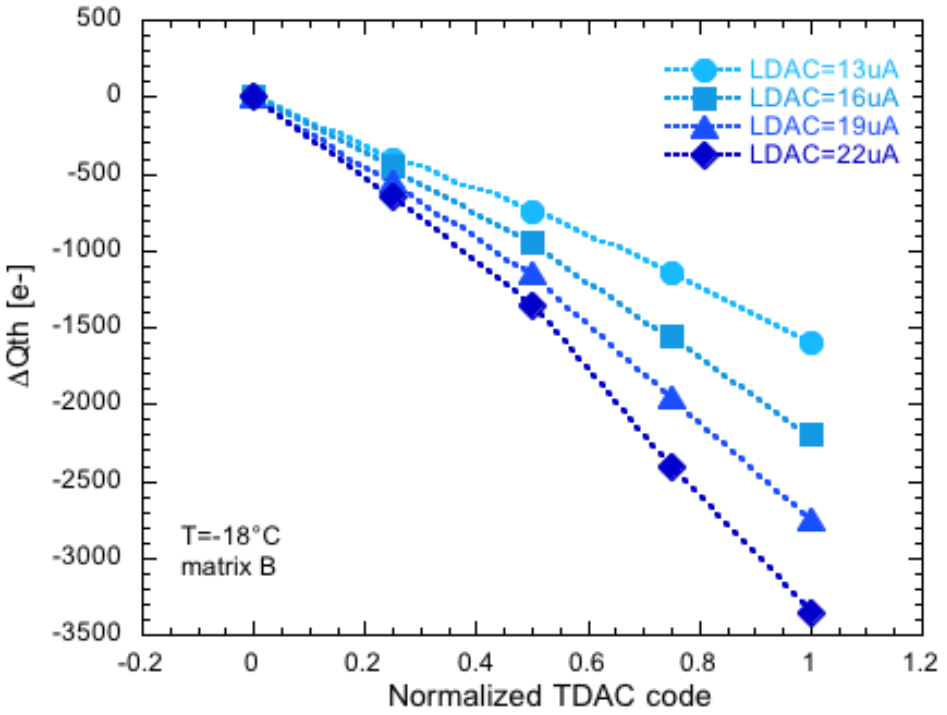
- Current-mode threshold tuning DACs
  - RD53A → **4 bits**, **cascoded** current mirrors
  - RD53B → **5 bits**, **regular** current mirrors
- **NMOS** switches

TDAC input-output characteristics

RD53A



RD53B

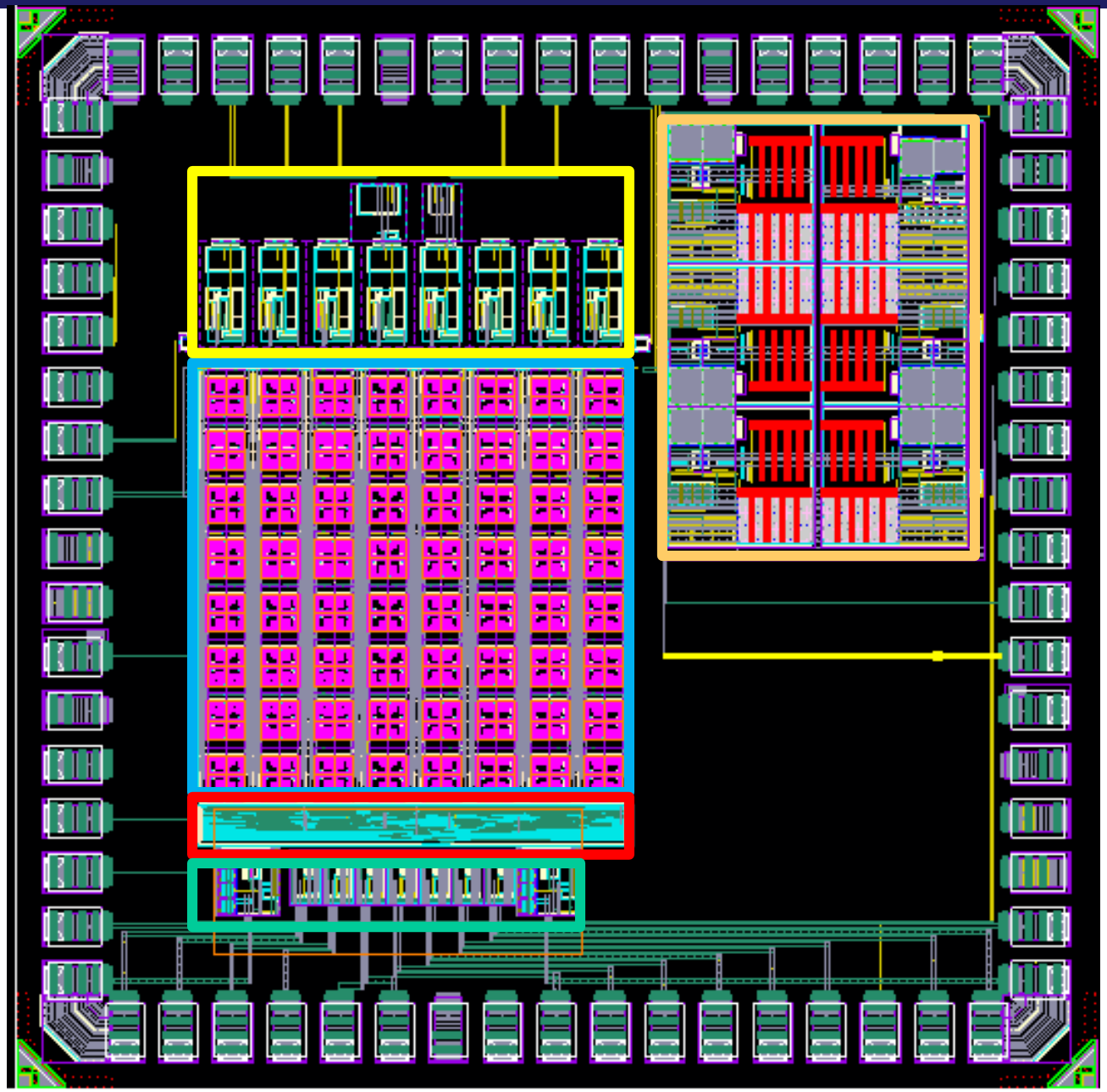


- TDAC **dynamic range** controlled by "LDAC" current (matrix periphery)
- **Saturation effect** taking place for RD53A at cold (for large I_{LDAC})
- The effect is **fixed** in the RD53B version

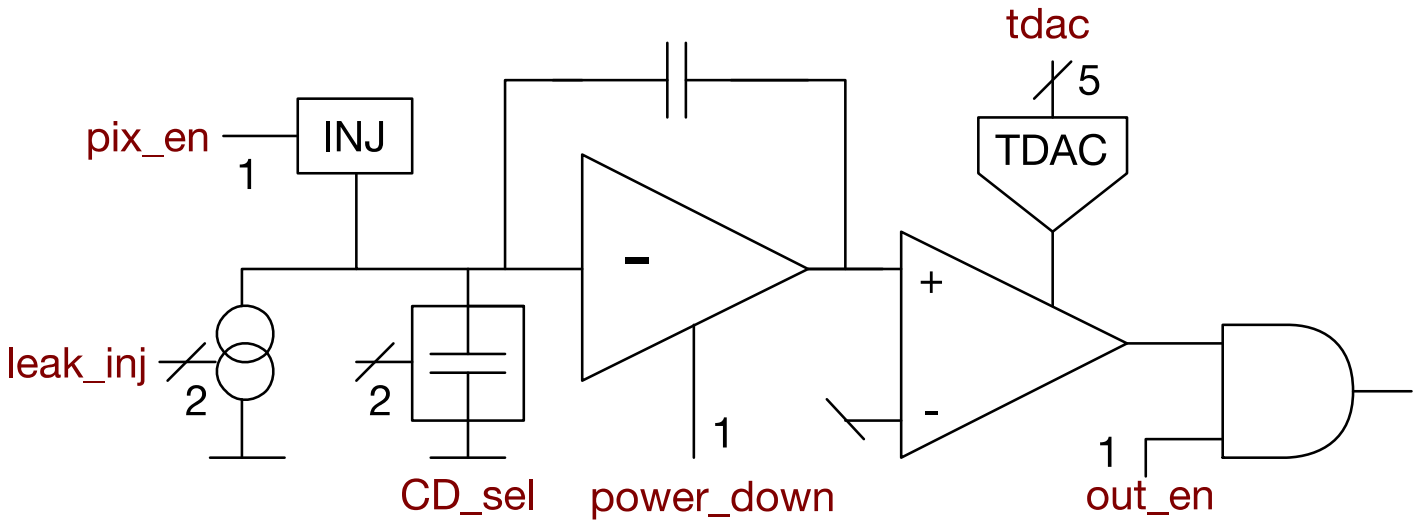
Device under test (DUT)

- 16x16 pixel matrix
  - Two regions: RD53A – RD53B
- Analog bias
- Configuration block
  - SPI-based
- Custom LVDS TX/RX
- Bandgap test structures

Top metal layers not shown



Pixel block diagram



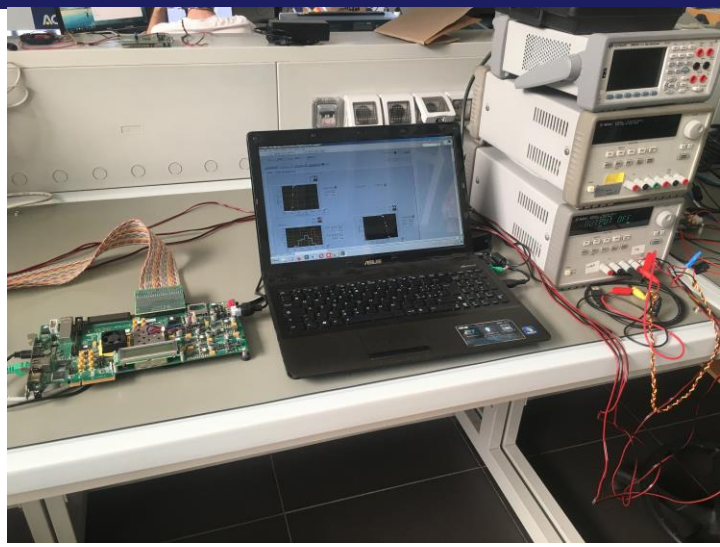
- 2 **detector emulating capacitors:** 50 fF and 100 fF

  → CD = 0, 50 fF, 100 fF, 150 fF

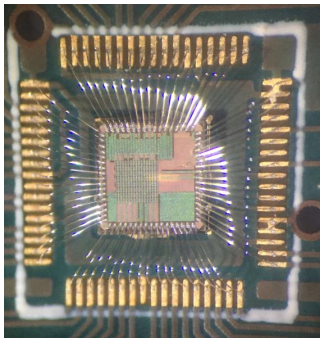
- **Leakage injection circuit** (possibility to inject "positive" or "negative" currents)

Test setup

Agilent 3631A power supply



Power cables



DUT

Ribbon cable

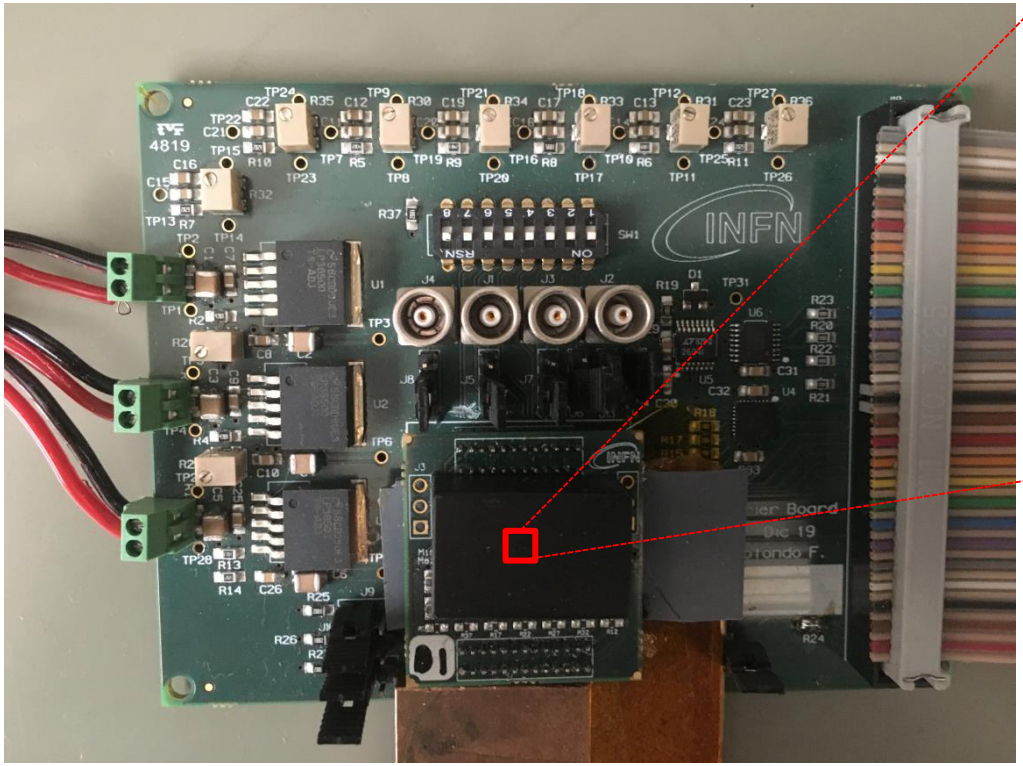
Kintex7 board

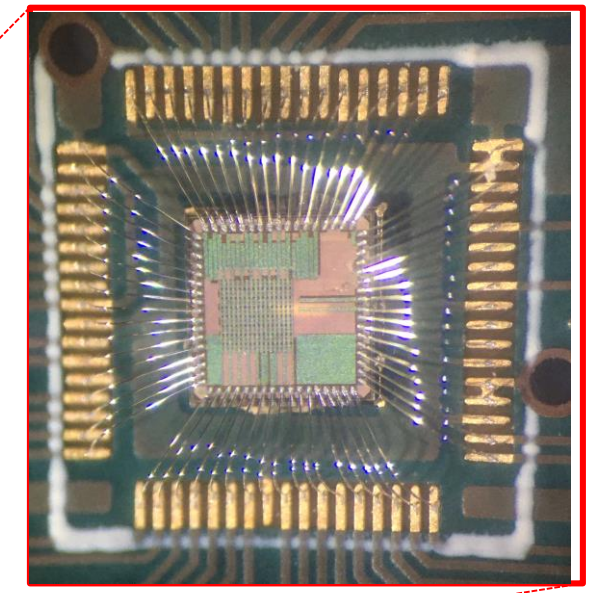
Ethernet + USB

Laptop

DUT

- 2 mm x 2 mm chip including a 16x16 matrix featuring the RD53A and RD53B version of the Linear Front-end

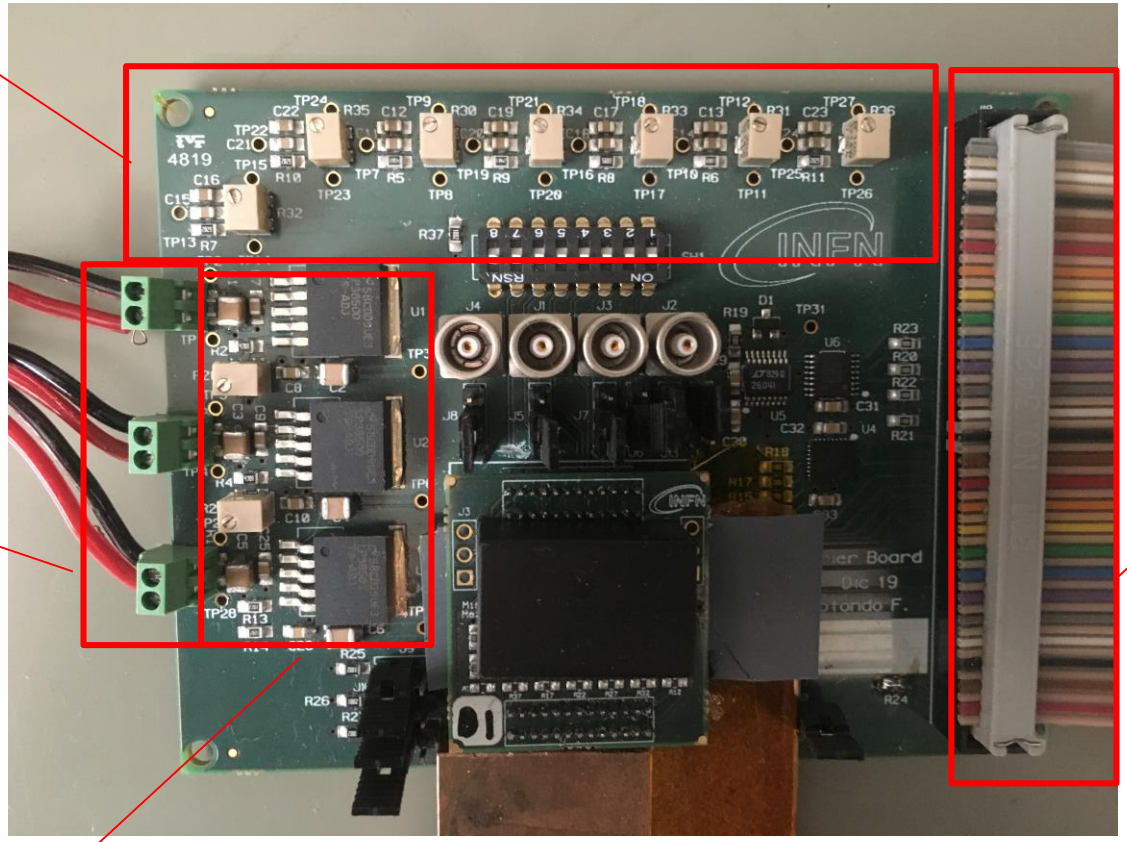




- Chip on a small daughter board mounted on a test PCB, including potentiometers for front-end bias setting

Test board

Potentiometers for front-end bias setting



Power connectors

(from top: analog, digital, aux)

Power supply regulators

FPGA connector

Main analog performance parameters

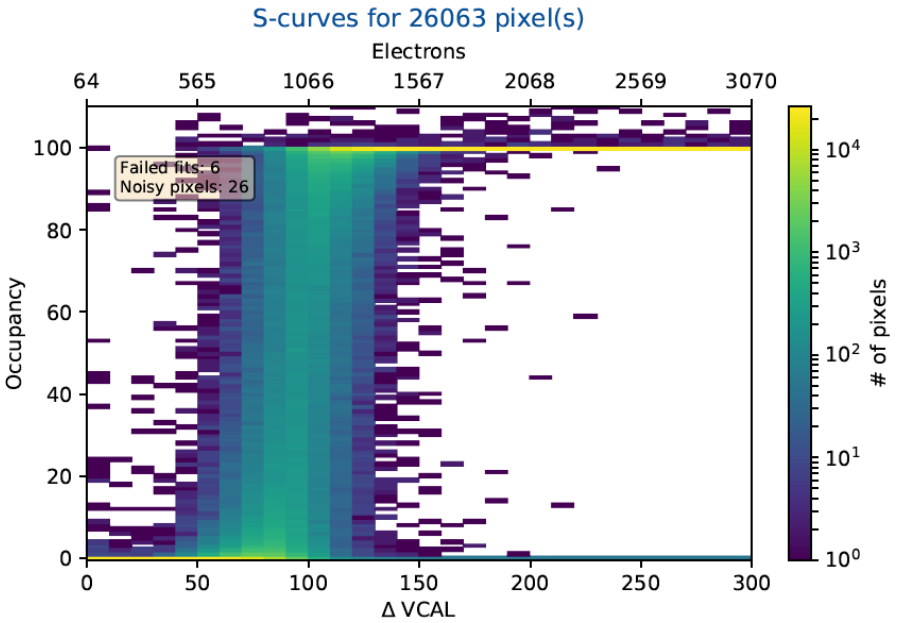
- Equivalent noise charge (ENC)
- Threshold dispersion
- Charge sensitivity
- Time-walk
- Time-over-threshold

Only the **comparator digital output** is available: how can we measure all these parameters?

Charge scans

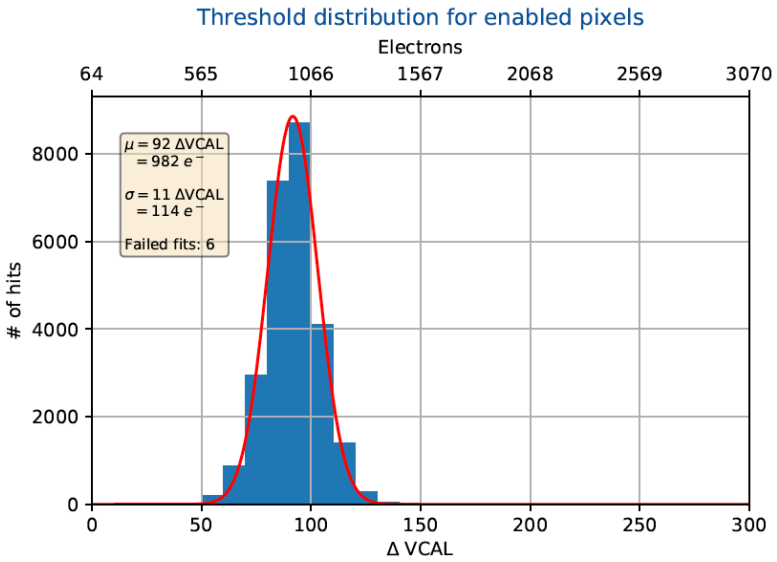
- Measures probability of discriminator to fire vs input charge
- Fitting S-Curve provides measurement of threshold and noise

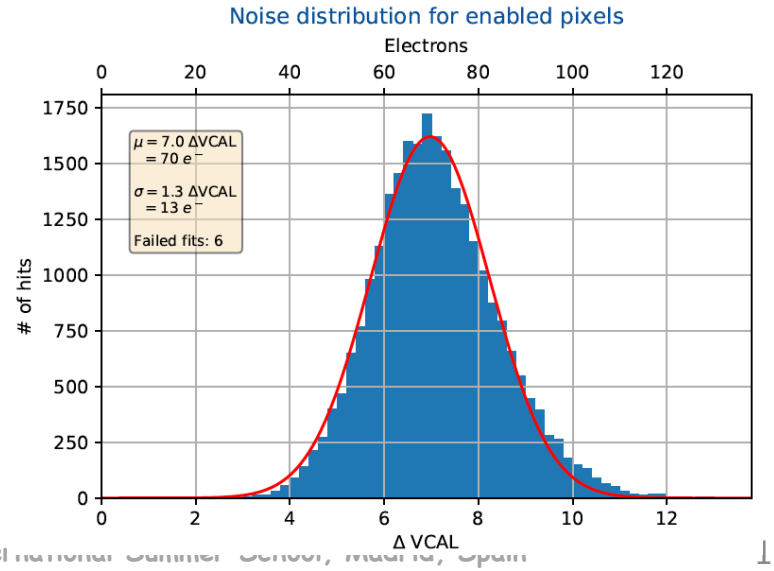
$$\eta_{hit} = \frac{1}{2}\left[1 + erf\left(\frac{Q_{in} - p_1}{\sqrt{2}p_2}\right)\right]$$



p1

p2

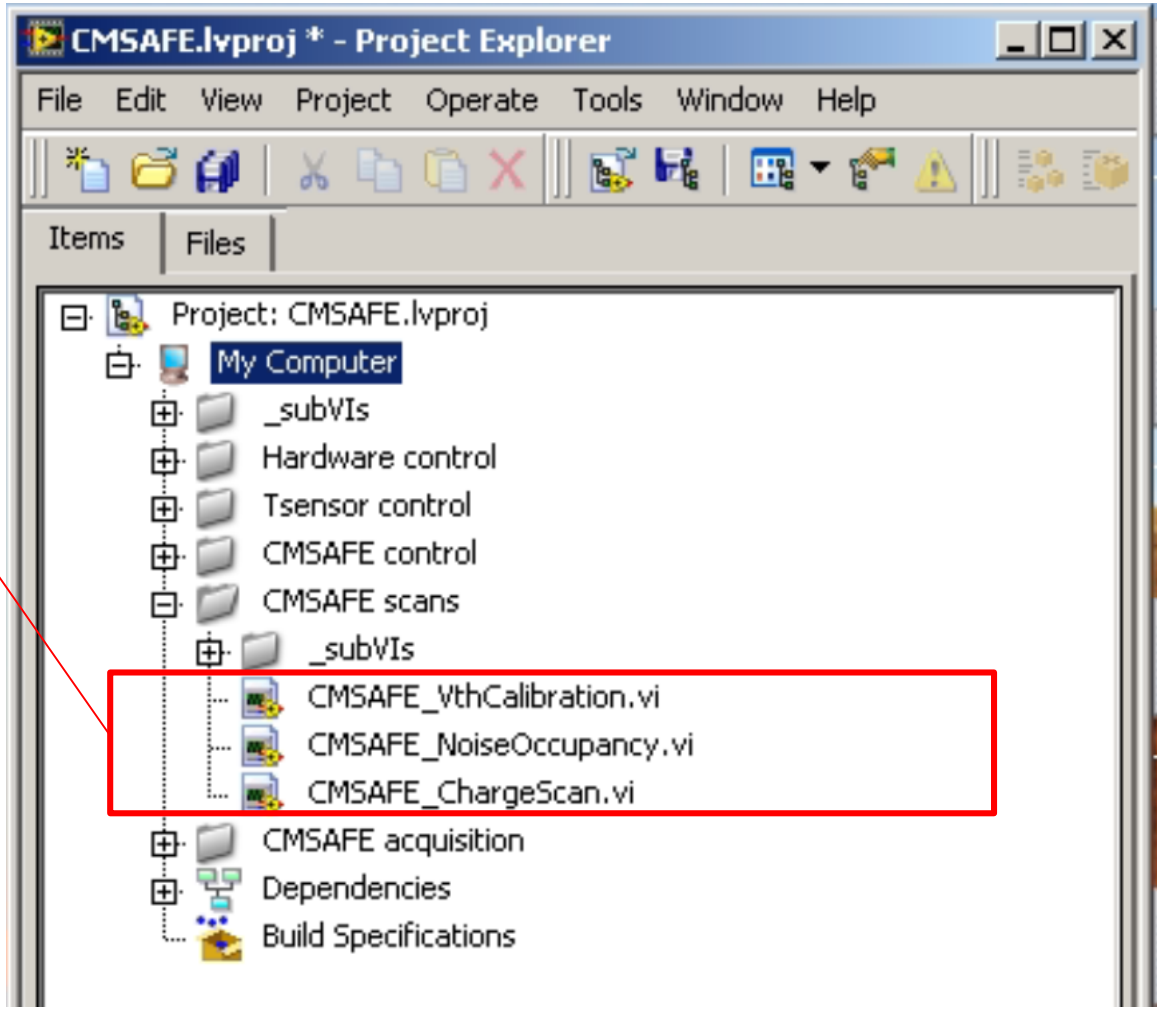




DAQ

- DAQ system based on LabVIEW
- Main virtual instruments (VIs):
  - Threshold calibration
  - Charge scan
  - Noise occupancy

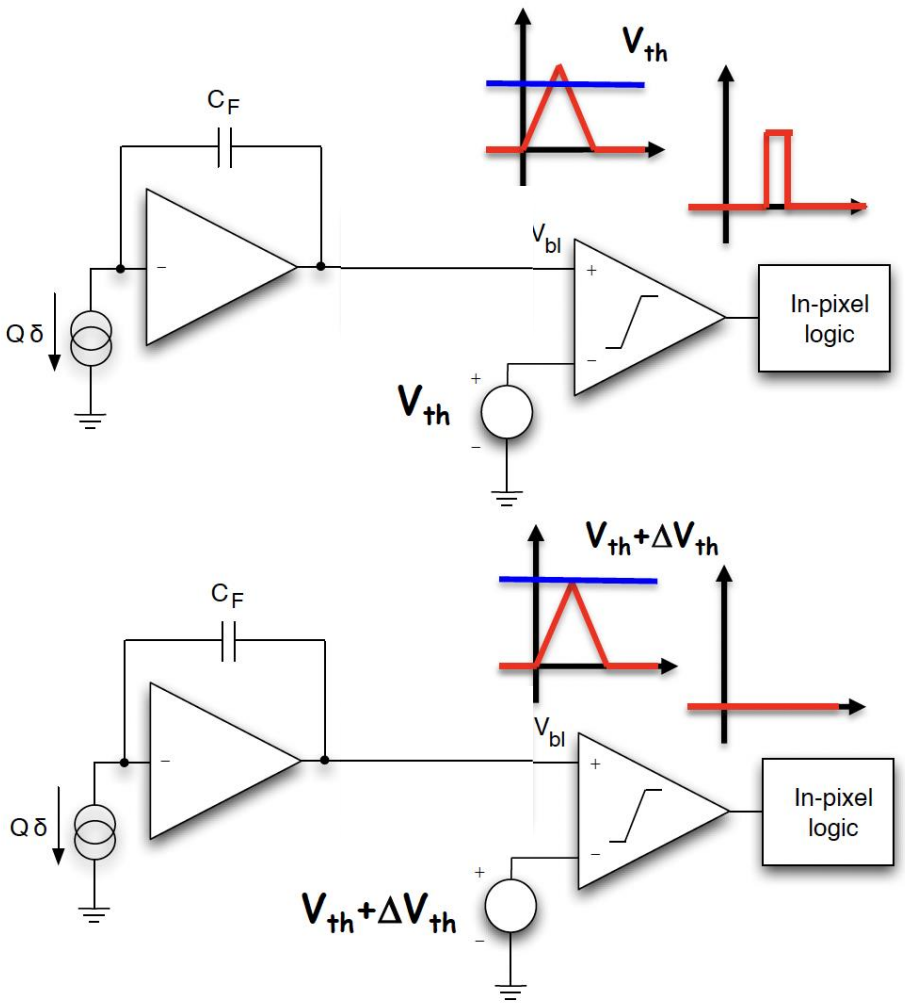
DAQ control panel



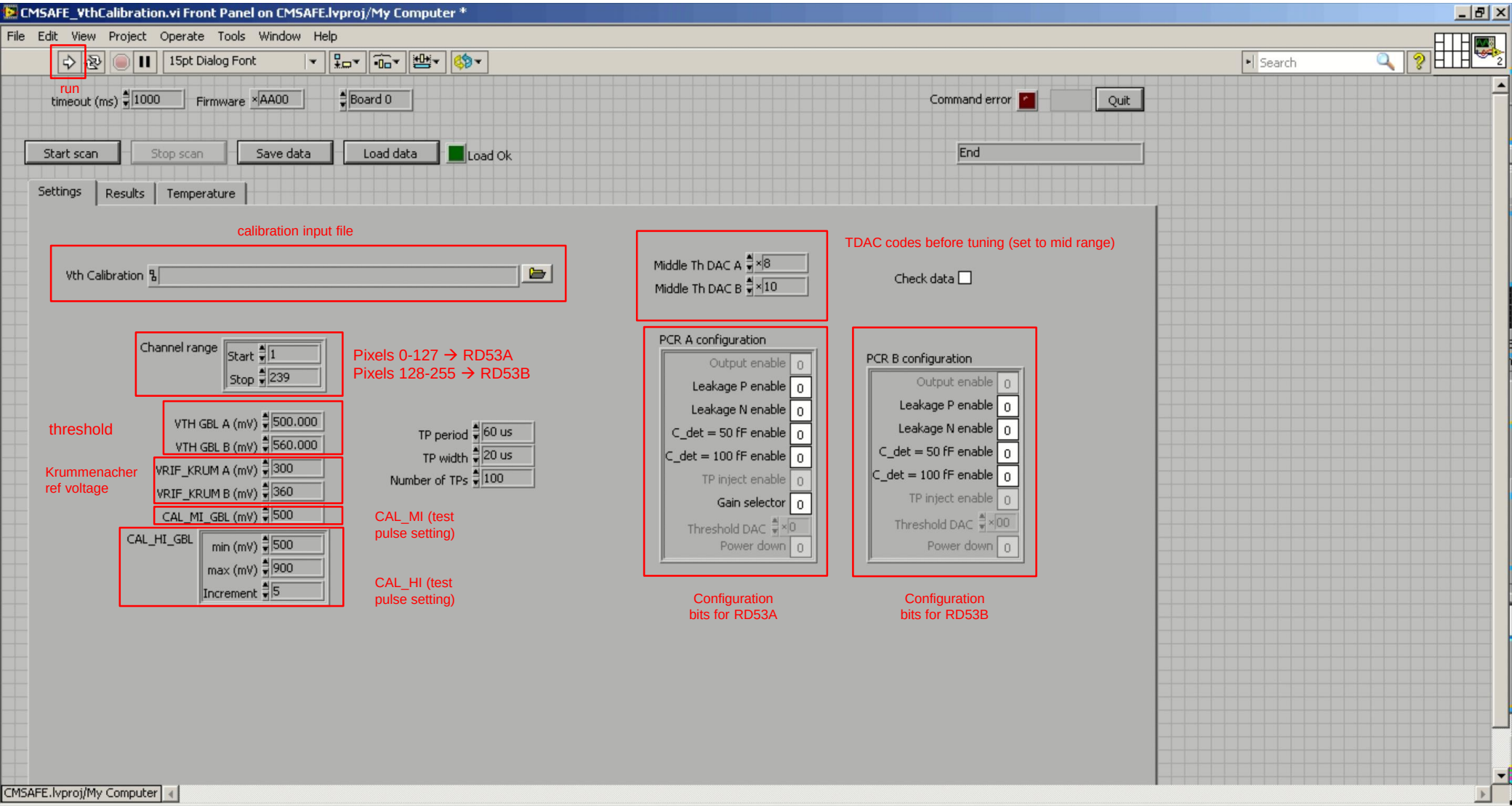
Threshold tuning

- In a multichannel binary readout circuit, random and systematic variations of process (doping) and geometrical (device dimensions, thickness of the various involved layers) parameters may be responsible for introducing non uniformities in the parallel path followed by the signals

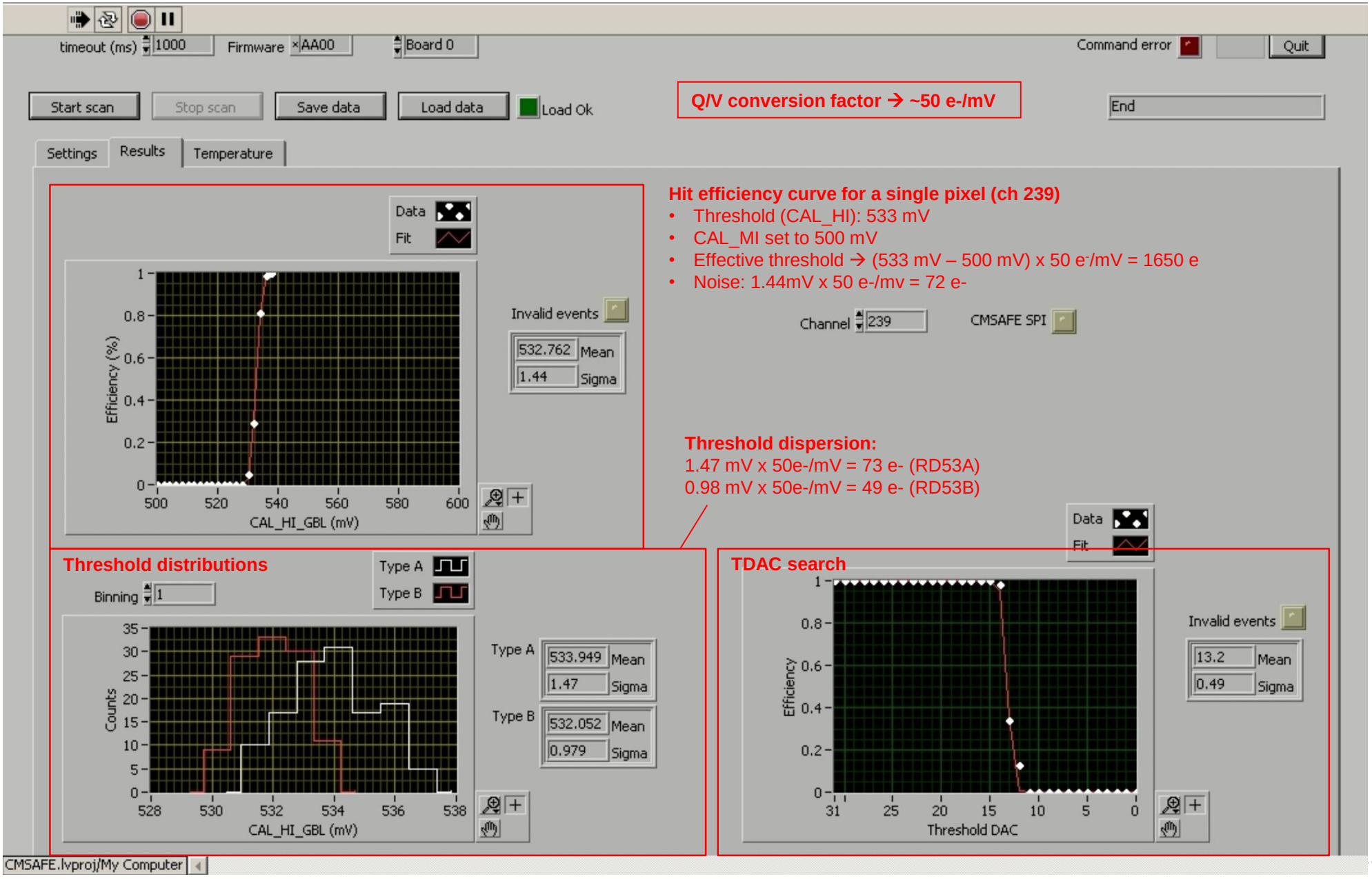
- Two channels, nominally identical to each other and featuring a common threshold at the inverting input of the discriminator, may provide different responses to the same charge pulse at the preamplifier input



Threshold tuning (VthCalibration.vi)



Threshold tuning

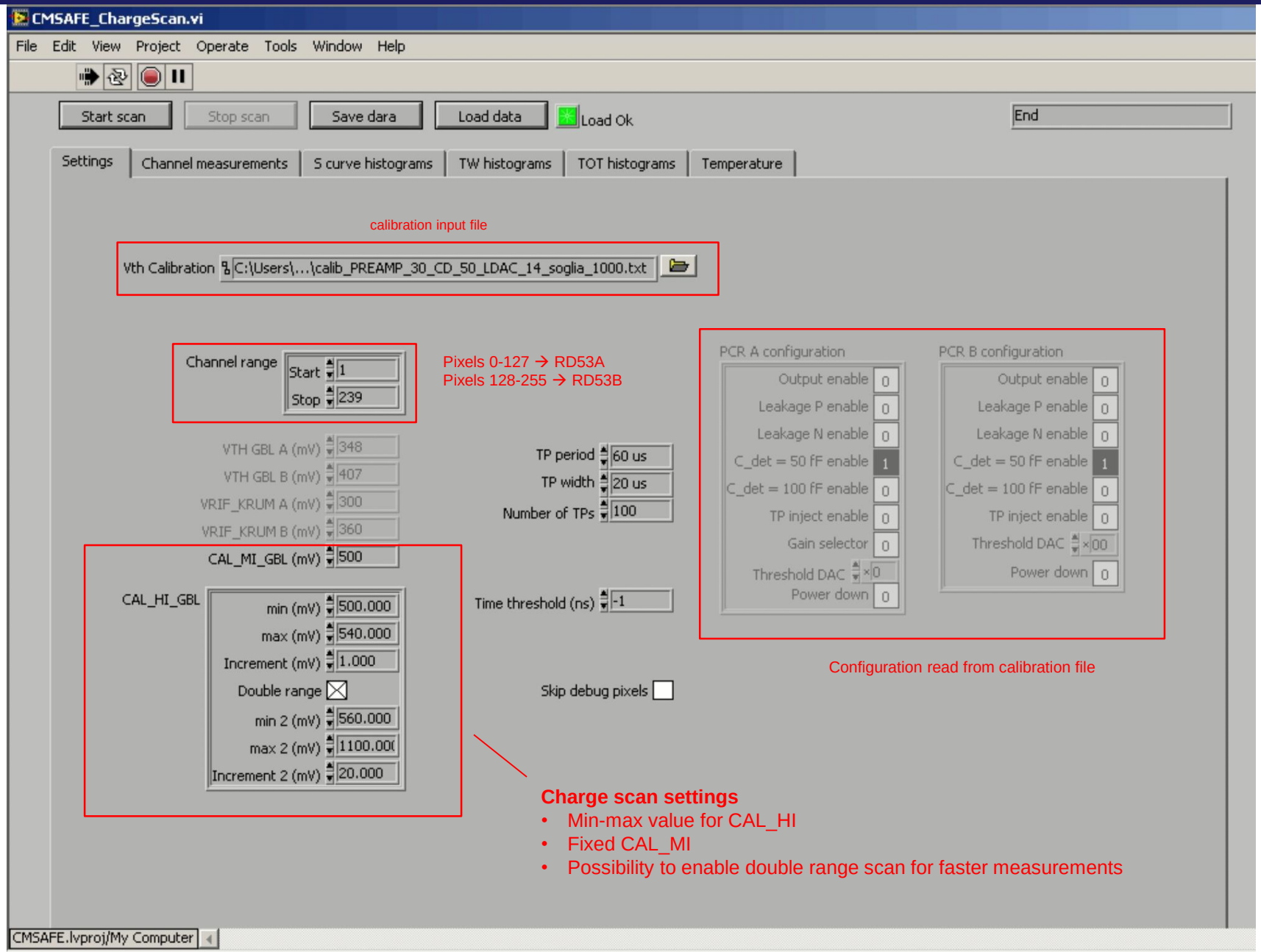


EXE1: threshold tuning

- Set detector capacitance to 50 fF and tune the matrix to 1000 e-
- What is the threshold dispersion for RD53A and RD53B?
- Why there is a significant difference between the two values?

- Hints → start tuning the matrix to higher threshold, than decrease the threshold down to 1000 e-

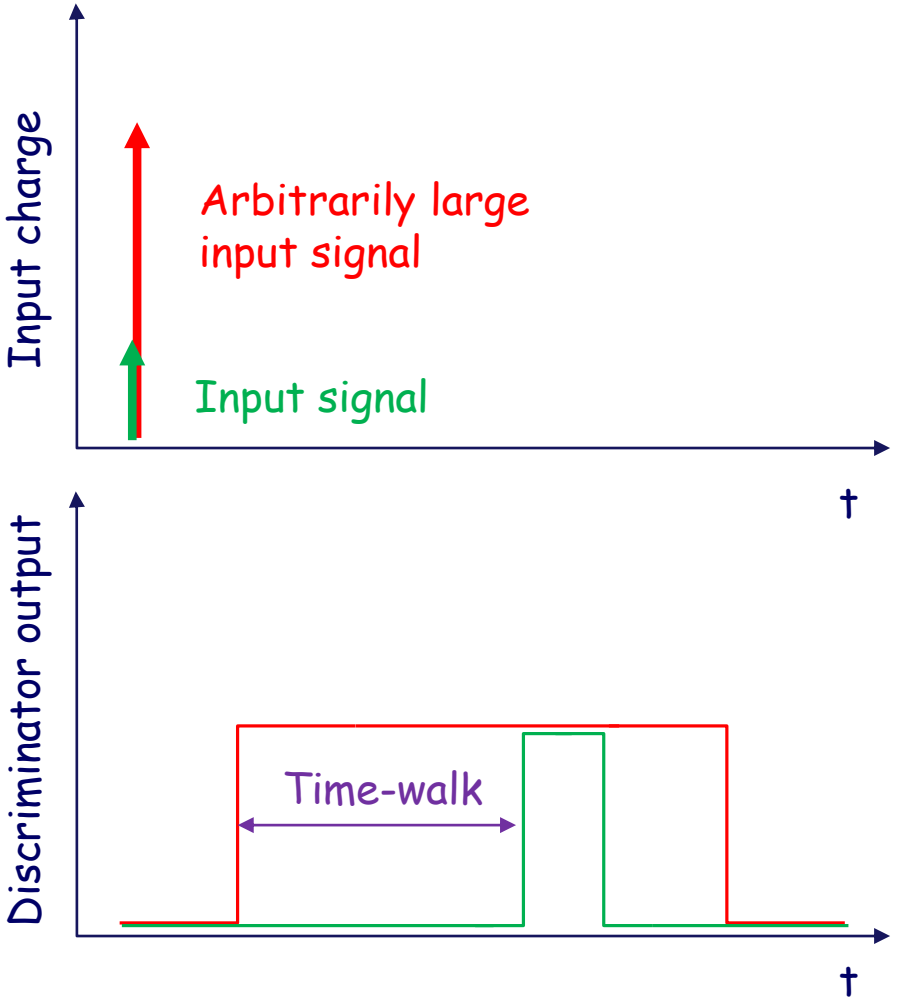
Charge scan (ChargeScan.vi)

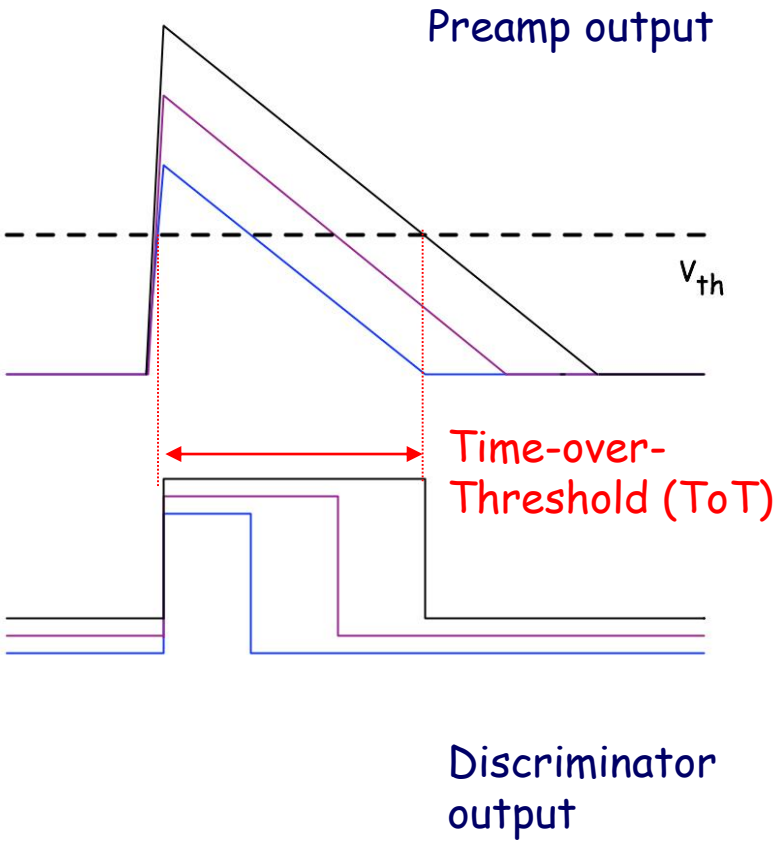


Charge scan settings

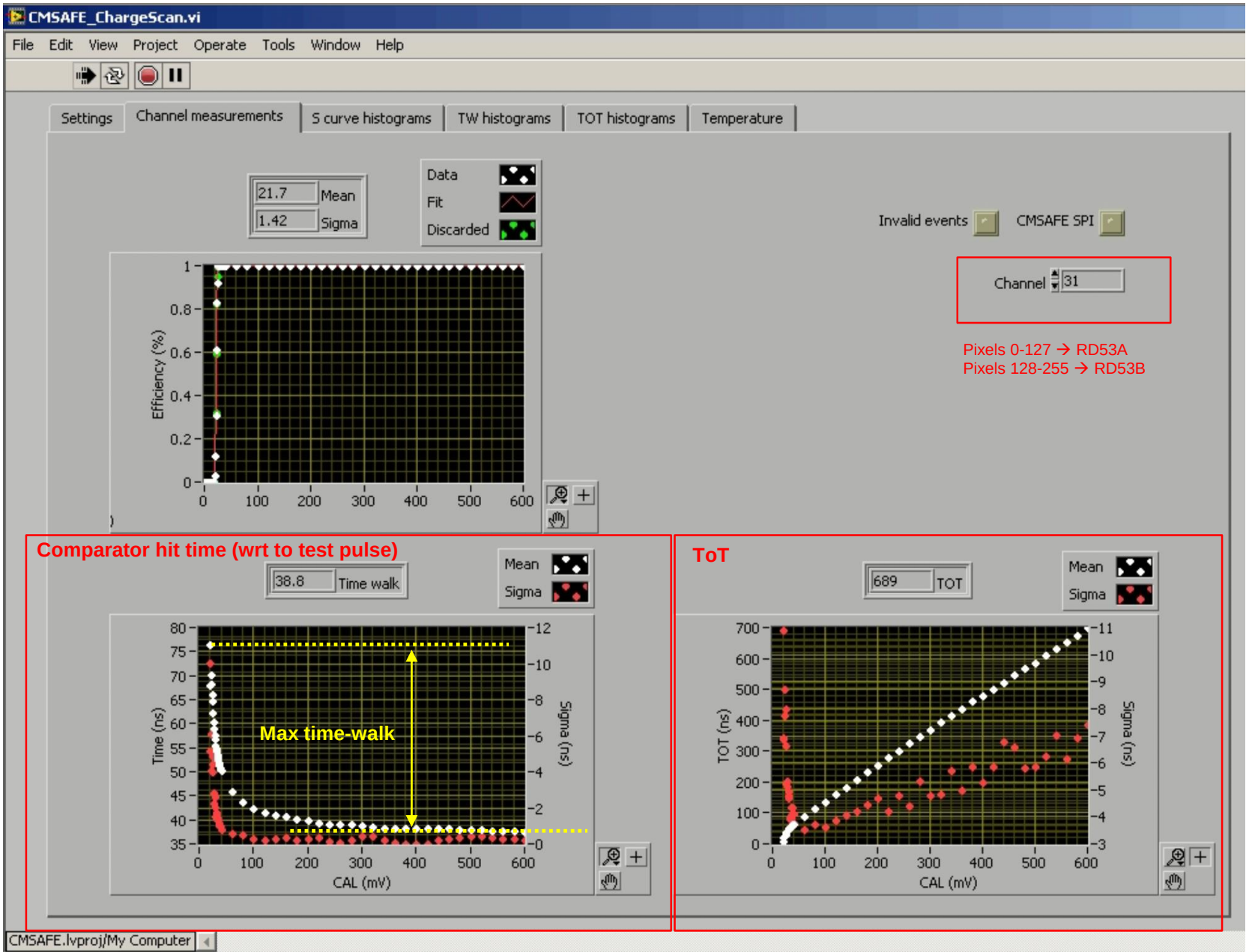
- Min-max value for CAL_HI
- Fixed CAL_MI
- Possibility to enable double range scan for faster measurements

Time-walk and Time-Over-Threshold (ToT)

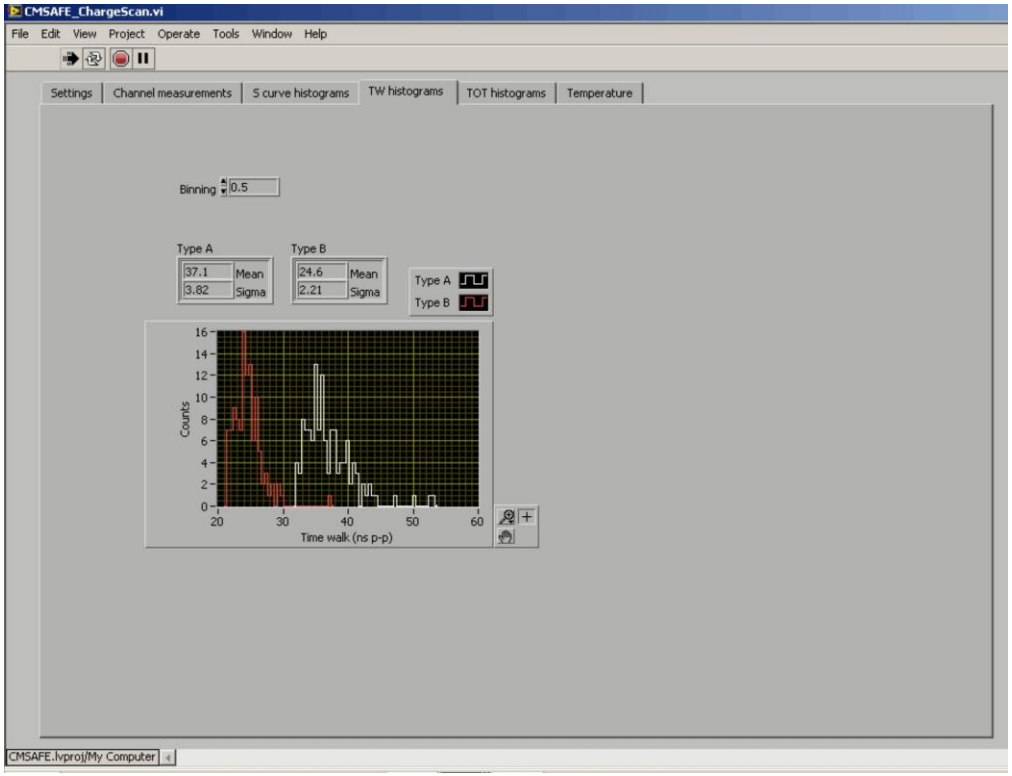


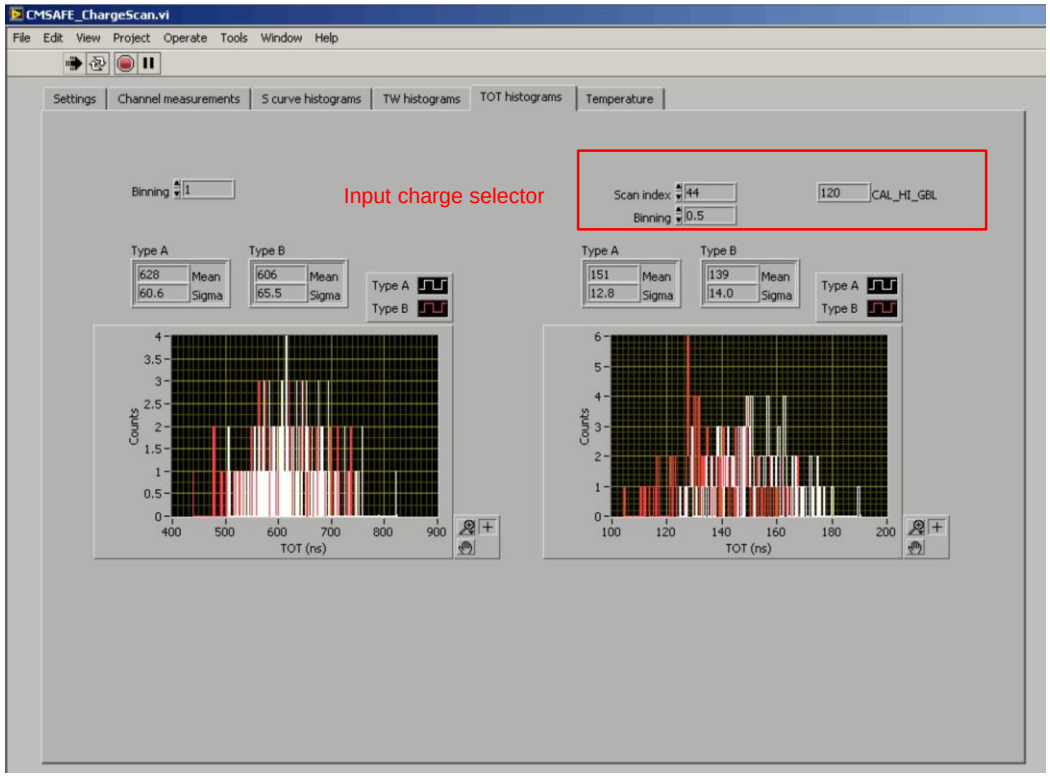


Time-walk and ToT

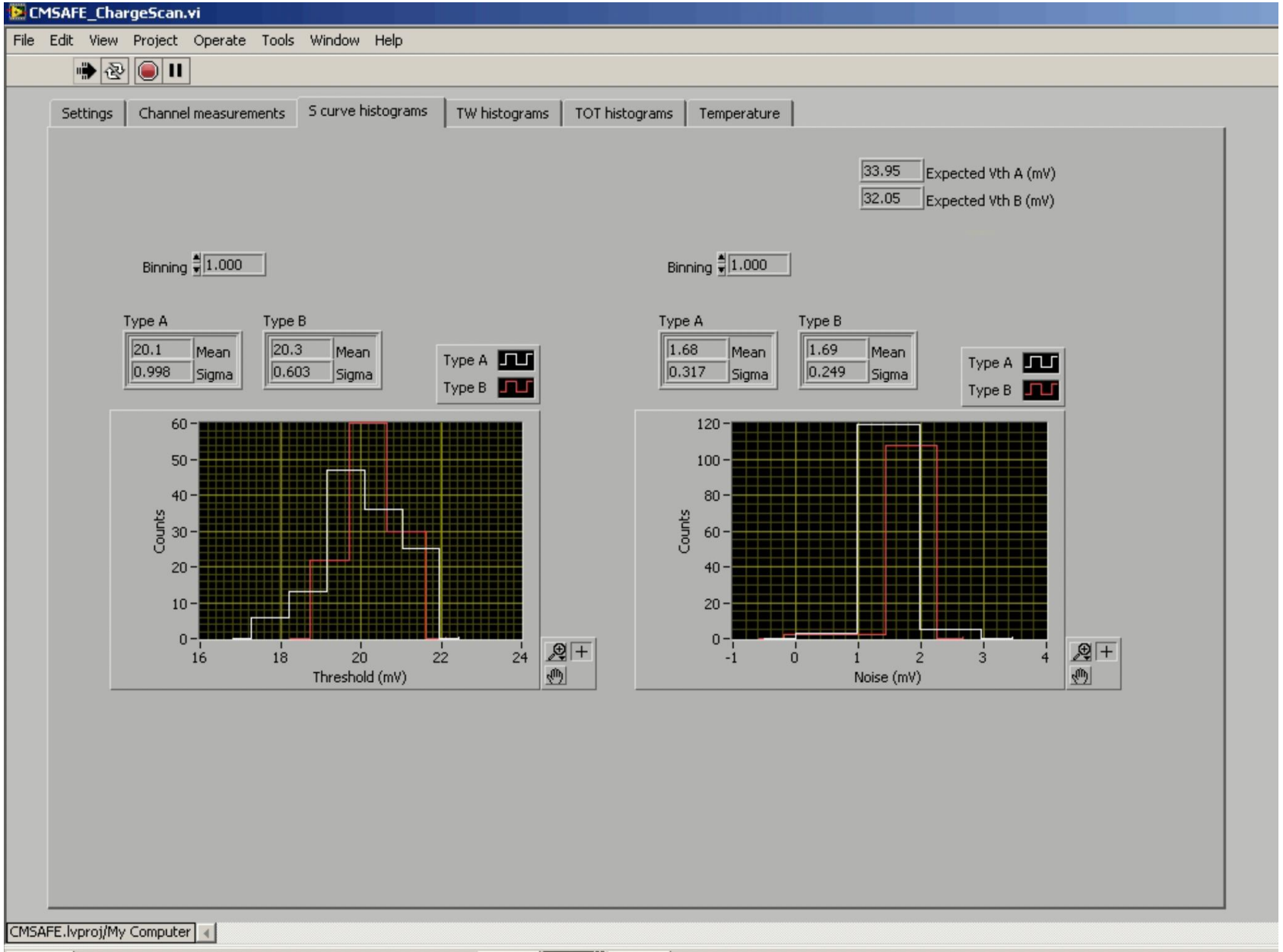


Time-walk and ToT histograms





Threshold and noise histograms



Noise and equivalent noise charge (ENC)

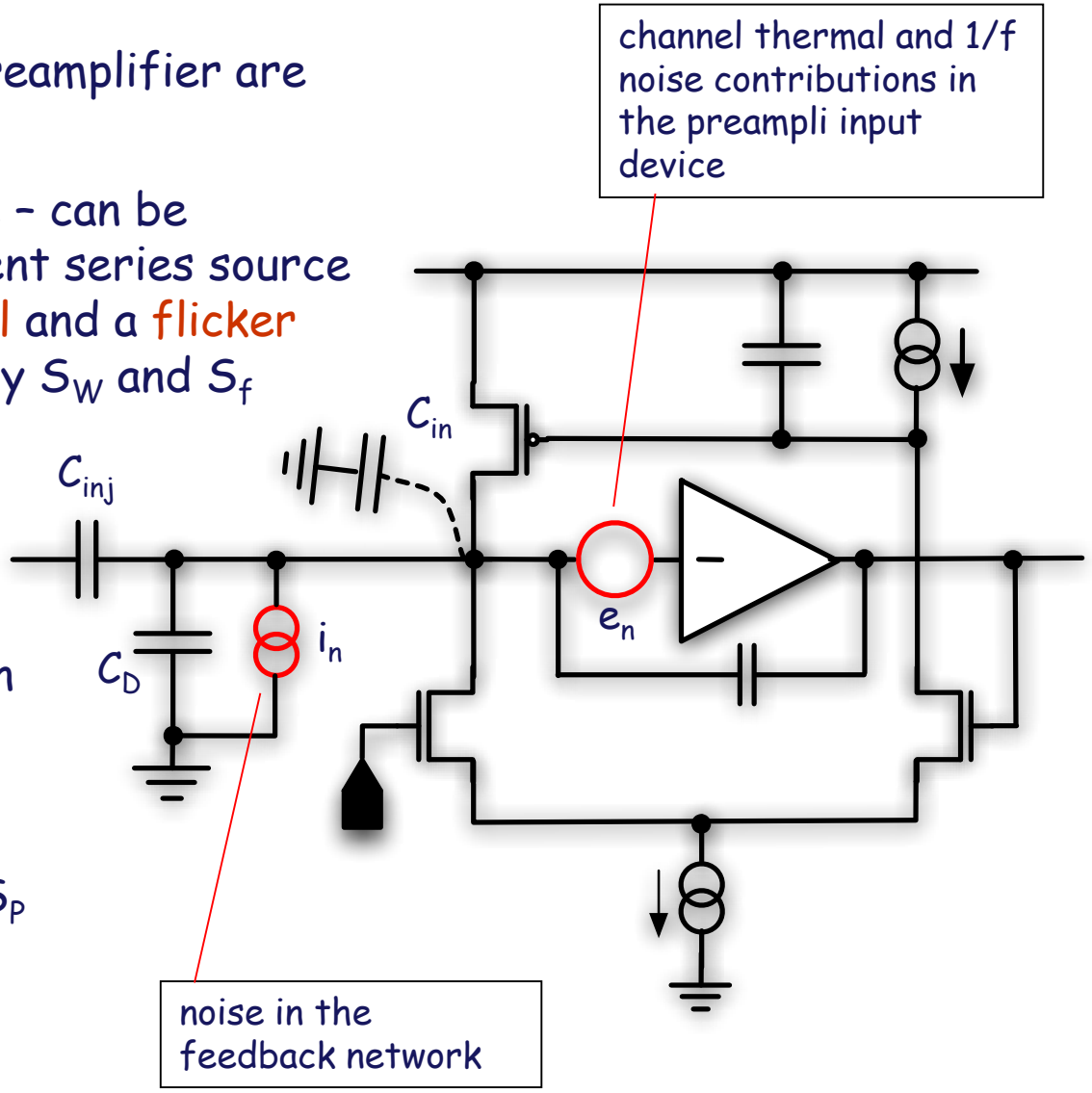
- The main noise sources in the preamplifier are located

  •in the preamplifier input device – can be represented through an equivalent series source (e_n) and includes a white thermal and a flicker term with power spectral density S_W and S_f respectively

$$\frac{\overline{de_n^2}}{df} = S_W + \frac{S_f}{f}$$

  - in the feedback network – can be represented through an equivalent parallel source (i_n), mostly with a white spectrum with power spectral density S_P

$$\frac{\overline{di_n^2}}{df} = S_P$$

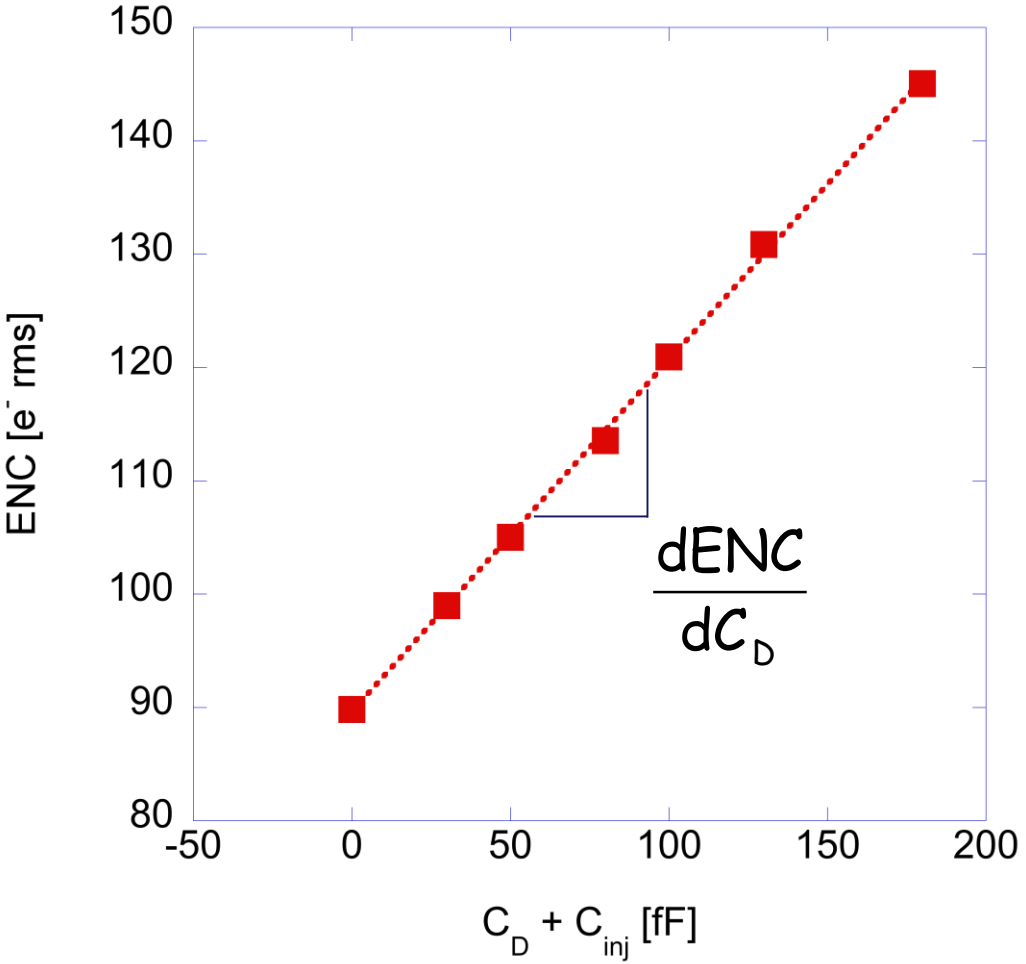


ENC and detector capacitance

- A quite general expression for the ENC is the following, accounting for the different noise contribution

$$ENC^2 = C_T^2 A_1 S_W \frac{1}{t} + C_T^2 A_2 S_f + A_3 S_p t$$

$C_T = C_D + C_{in} + C_F + C_{inj}$
A_1, A_2, A_3=shaping coefficient
τ=shaping time (has some relationship with t_p)



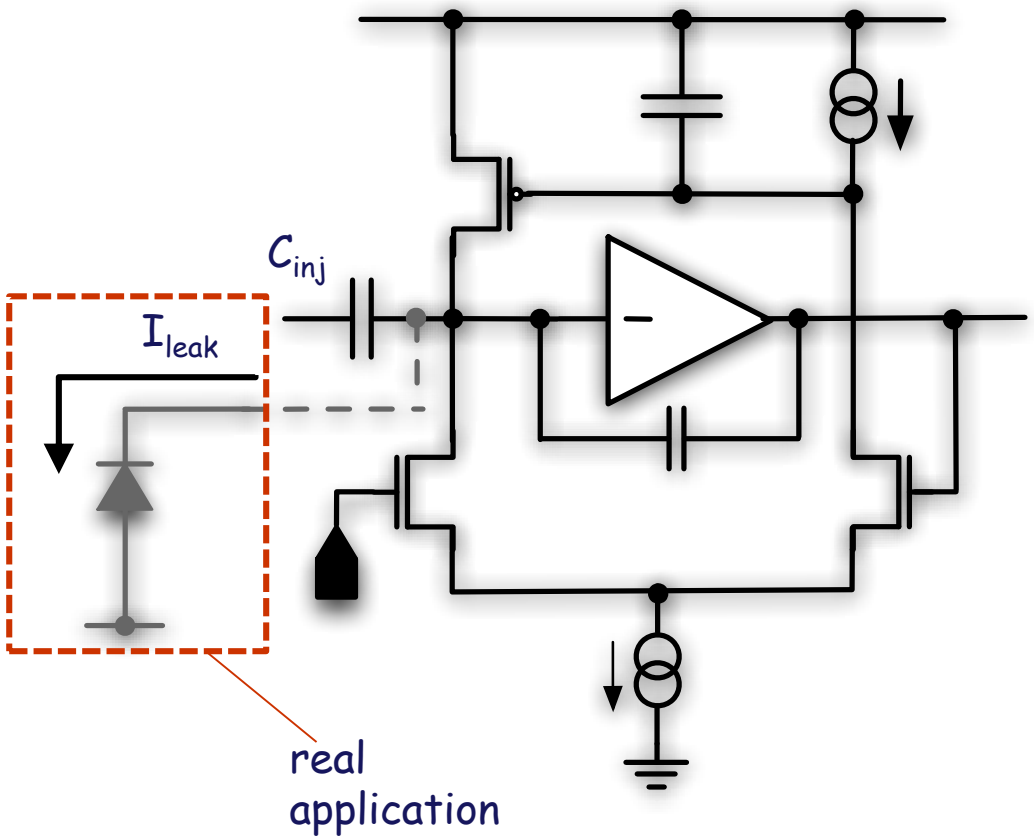
- The effect of the series noise source on the overall noise performance gets more pronounced as C_T (the capacitance shunting the circuit input terminal) increases
- The slope of the ENC vs C_D is a figure of merit telling us how the noise performance of the circuit degrades as the detector capacitance increases

EXE2: charge scan

- Set the detector capacitance to 50 fF and tune the matrix to 1000 e-
- Measure the maximum time-walk for RD53A and RD53B
- Measure the ToT for an input charge of 6000 e-
- Set the threshold to around 2000 e- and evaluate the ENC for CD=0, 50, 100 and 150 fF. What is the dENC/dCD slope for the front-end channels?

Measurements in the presence of a leakage current

- The readout channel has to work correctly also in the presence of a leakage current at the input terminal
- In the real application, this leakage current comes from the detector and may exceed 10 nA when the detector is exposed to very high ionizing radiation doses - ~1 Grad for 10 year operation is expected for the inner layers of the CMS detector at the HL-LHC
- In the DUT, a leakage emulator circuit can be enabled, providing a DC current I_{leak} at the preamp input



EXE3: detector leakage current

- Set the threshold to around 2000 e- and the detector capacitance to 50 fF.
- Measure the ENC.
- Enable the leakage current emulator (default values is around 20nA/pixel). How does the ENC vary?

Noise hit rate

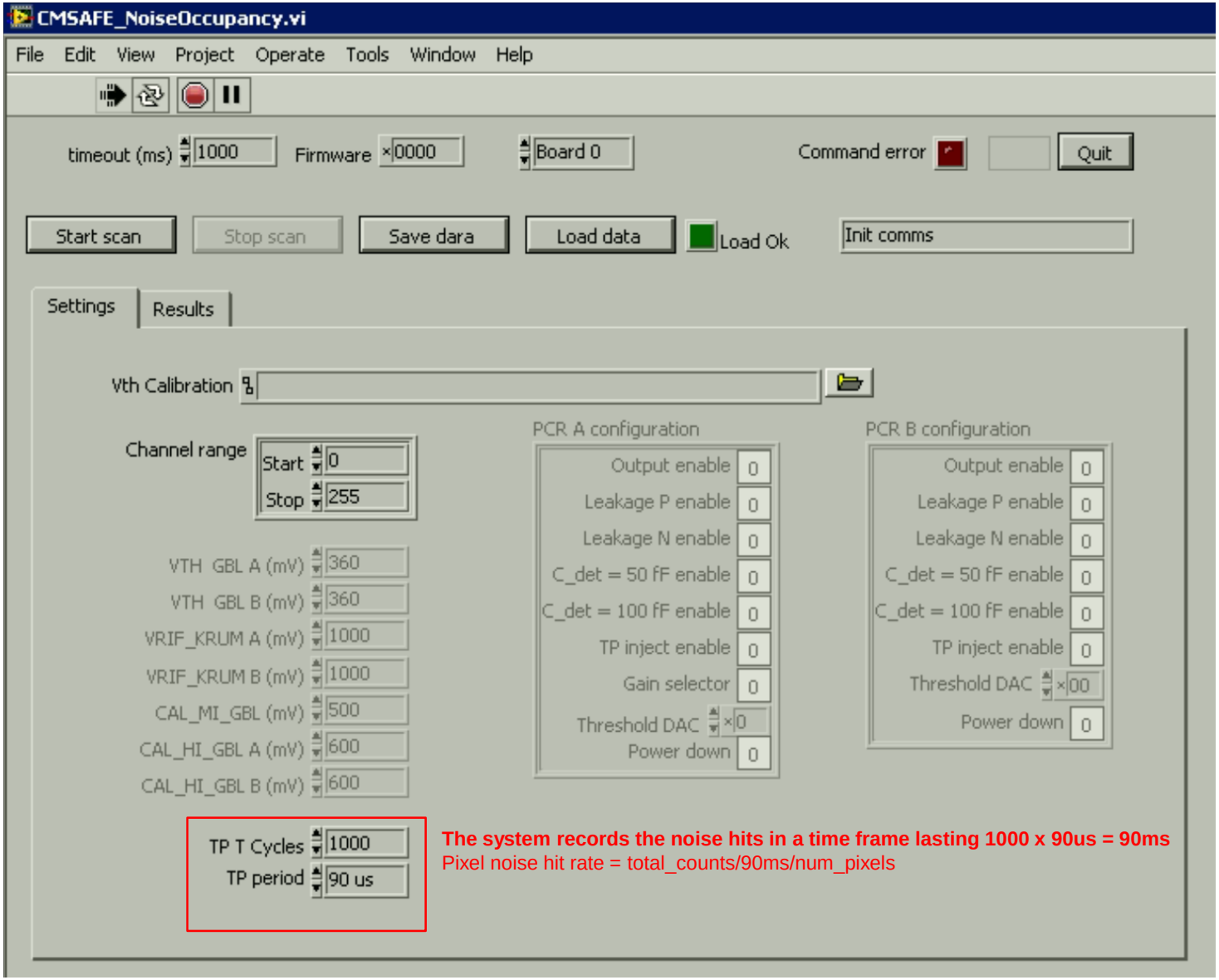
- An important figure of merit for a front-end chip is the **noise hit rate** at a given threshold.
- Ideally, we would like to have a low threshold for better efficiency. This actually translates in larger number of hits due to noise.
- **Optimum efficiency** is generally constrained by the maximum rate of noise induced transitions at the discriminator output, or maximum noise hit rate, due to the signal at the preamplifier output randomly crossing the discriminator threshold. Such a noise hit rate limit is strongly dependent on the readout architecture and on the target readout efficiency. Under some very general assumptions, in a binary channel the noise hit rate f_n, whose analysis represents a specific aspect of the more general level crossing problem, can be written as

$$f_n = f_{n0} \cdot e^{-\frac{Q_{t0}^2}{2ENC_{sl}^2}}$$

where Q_{t0} is the mean value of the threshold, and f_{n0} is the noise hit rate at zero threshold.

L. Ratti et al. "Design of Time Invariant Analog Front-End Circuits for Deep N-Well CMOS MAPS" DOI: 10.1109/TNS.2009.2024536

Noise hit rate (NoiseOccupancy.vi)



EXE4: noise hit rate

- Tune the matrix threshold to 1000e-.
- Measure the noise hit rate.
- Repeat the measure for smaller thresholds (900, 800, 700, 600, 500).
- Plot the noise hit rate as a function of the threshold.