AI on chip – Algorithm to Accelerator

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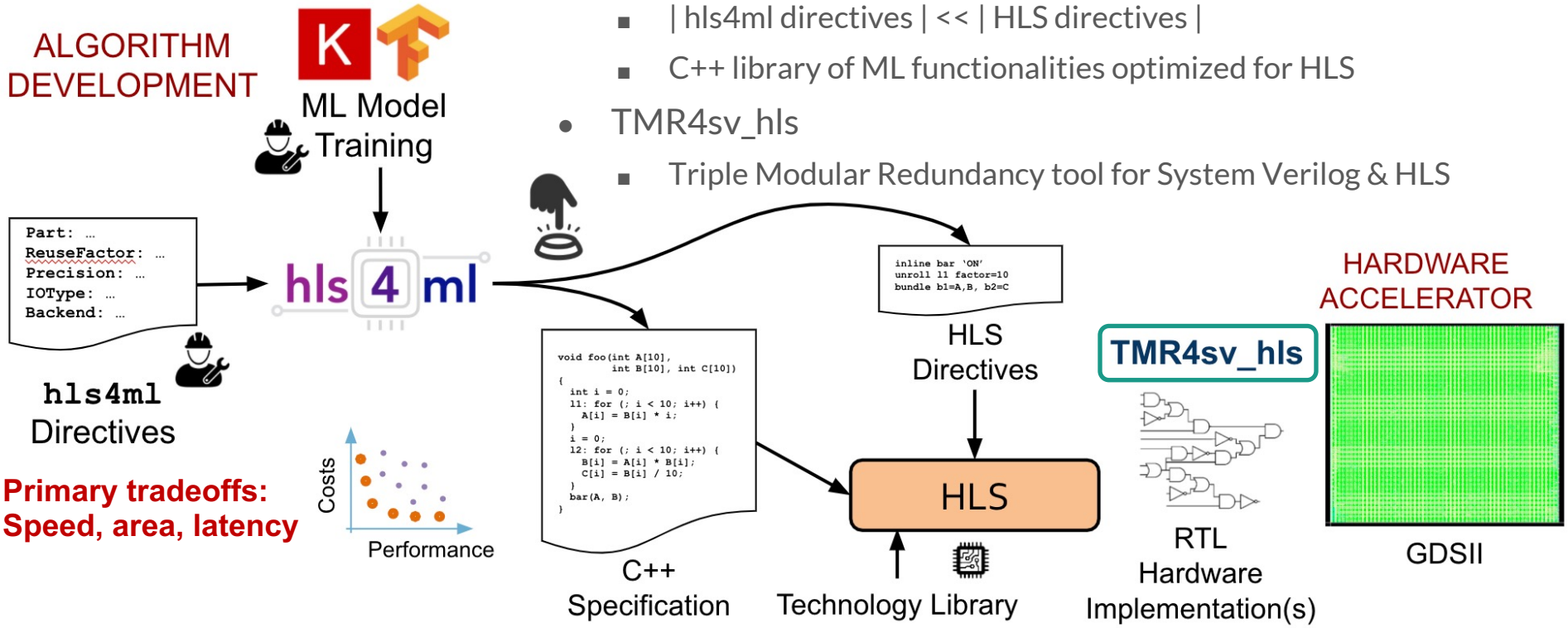
Physics Driven Hardware Co-design

- Algorithm development based on Physics data
- **hls4ml** simplifies the design of on-chip ML accelerators
  - | hls4ml directives | << | HLS directives |
  - C++ library of ML functionalities optimized for HLS
- TMR4sv_hls
  - Triple Modular Redundancy tool for System Verilog & HLS



1st half of the lab is common with

IA tools & real-time HEP Trigger

LAB PRESENTATION BY Dr. Nhan TRAN (FERMI, National Laboratory, USA)

- hls4ml: From C to HLS