Fast clock transmission systems for HL-LHC

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CEA-Saclay/Irfu

Introduction

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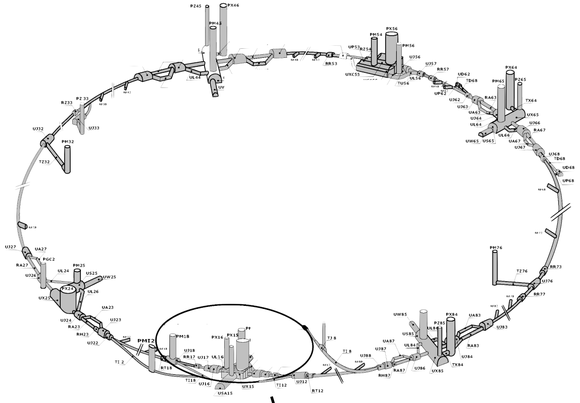
- More than 10s of thousands of readout units need to receive this collision clock with a very high precision.



Collision clock
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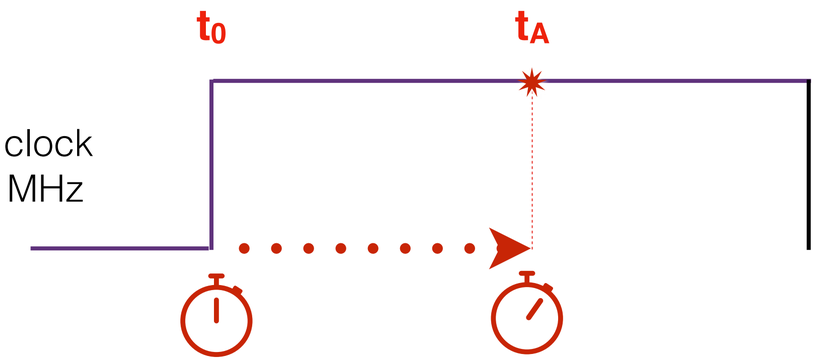

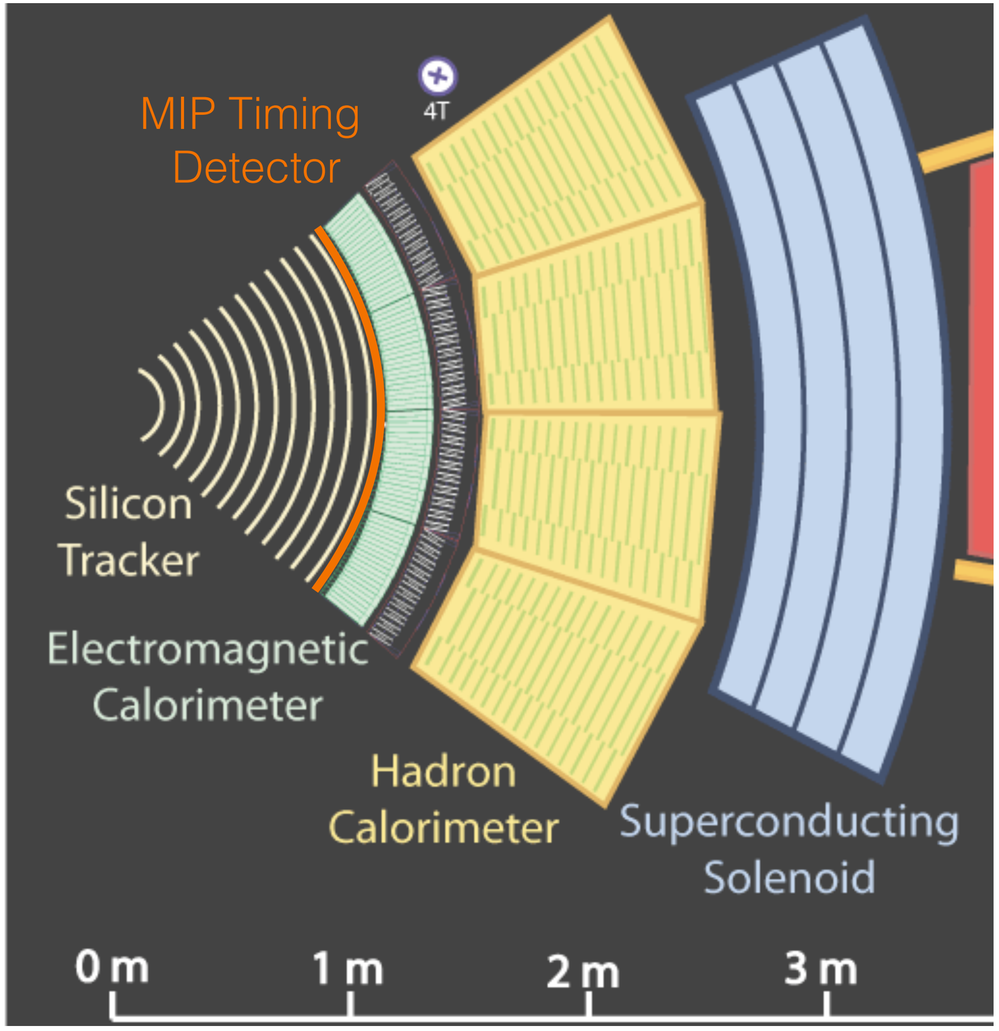

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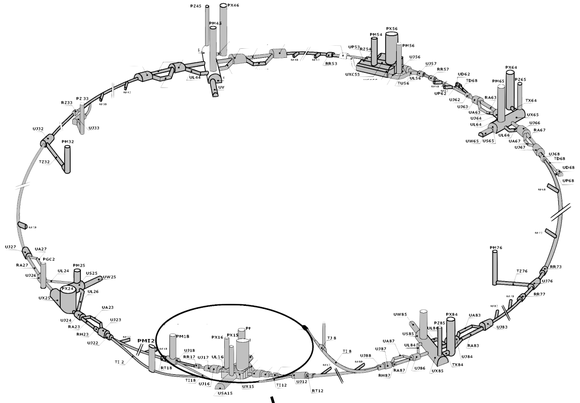

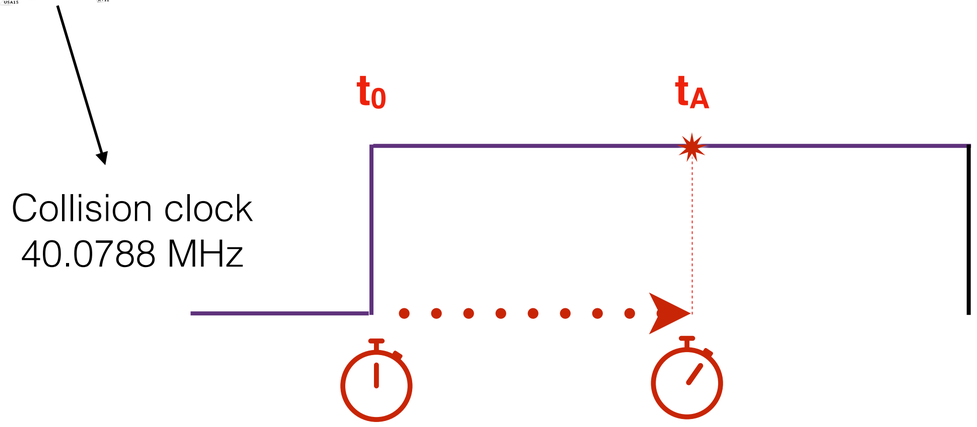

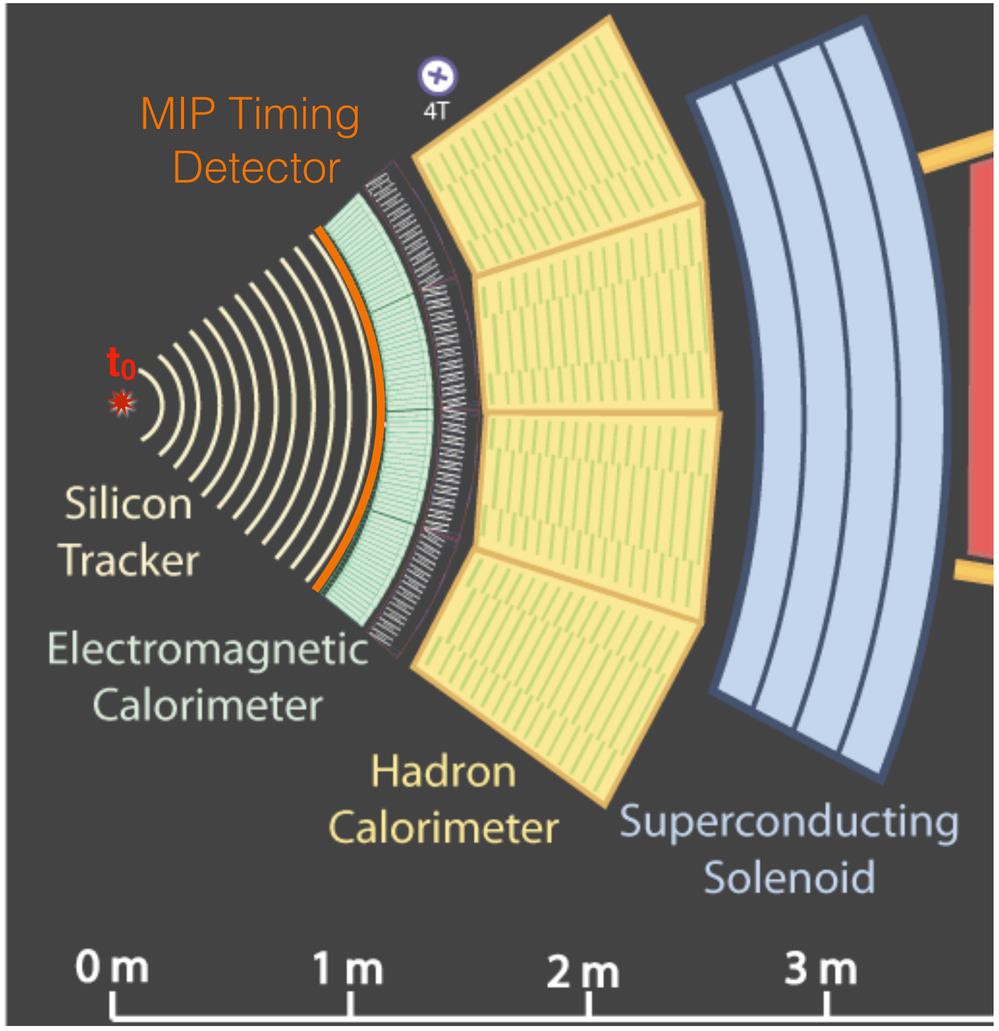

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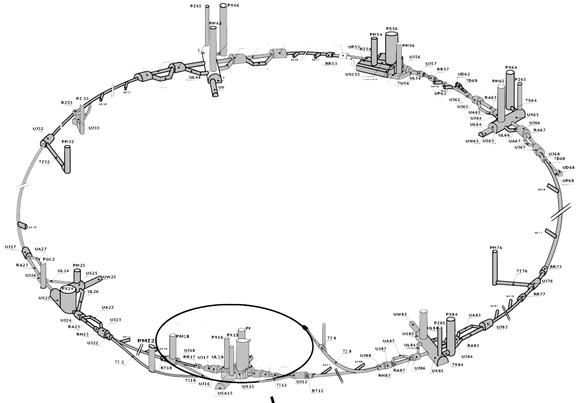

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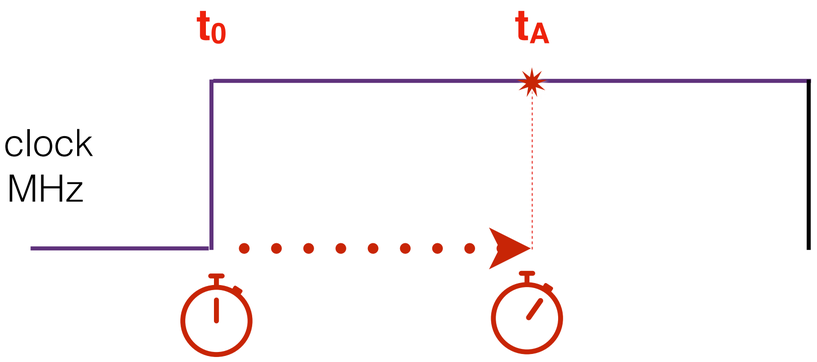

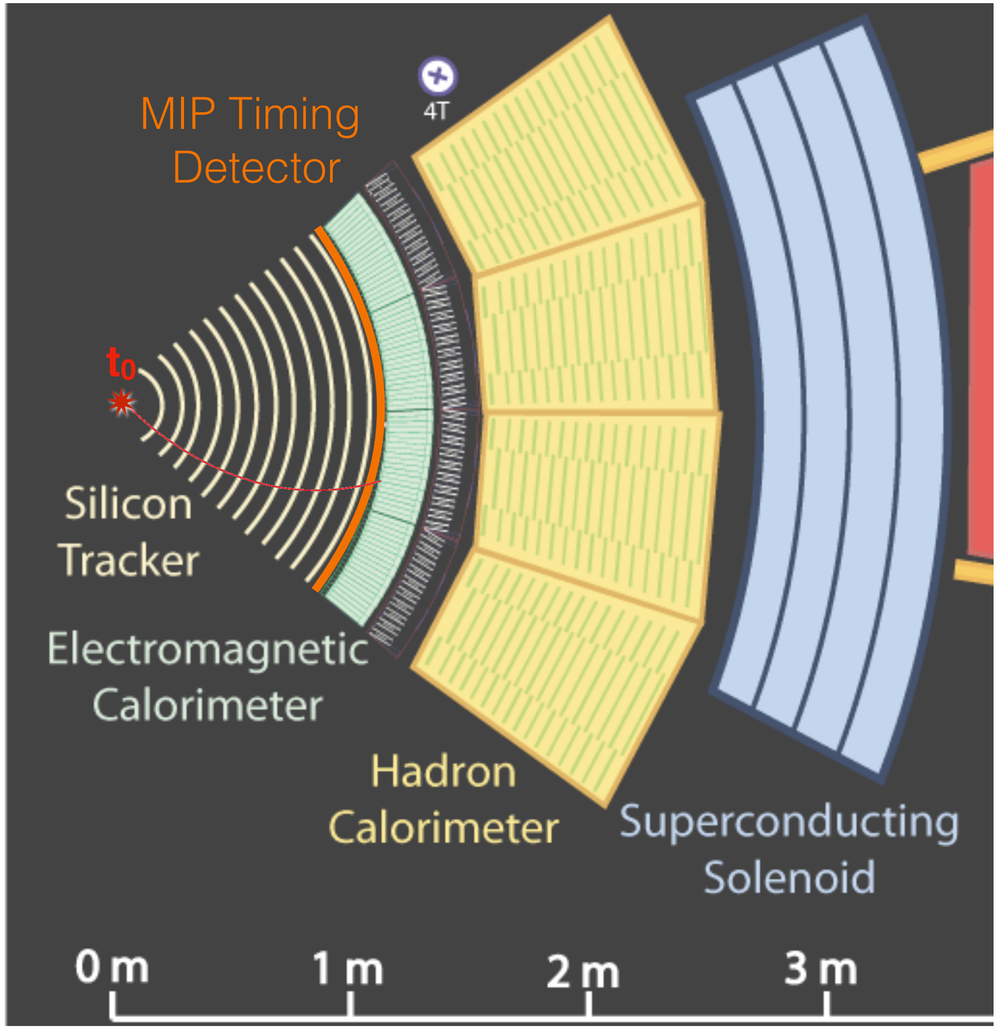

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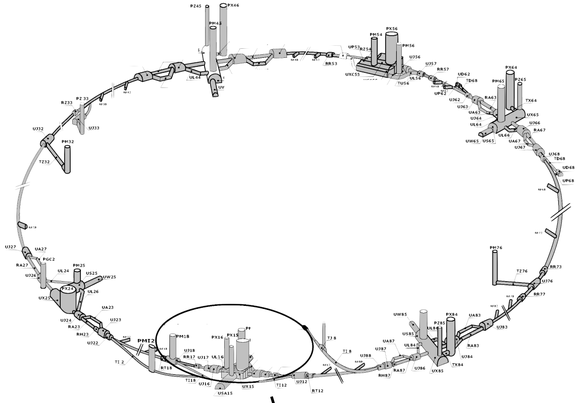

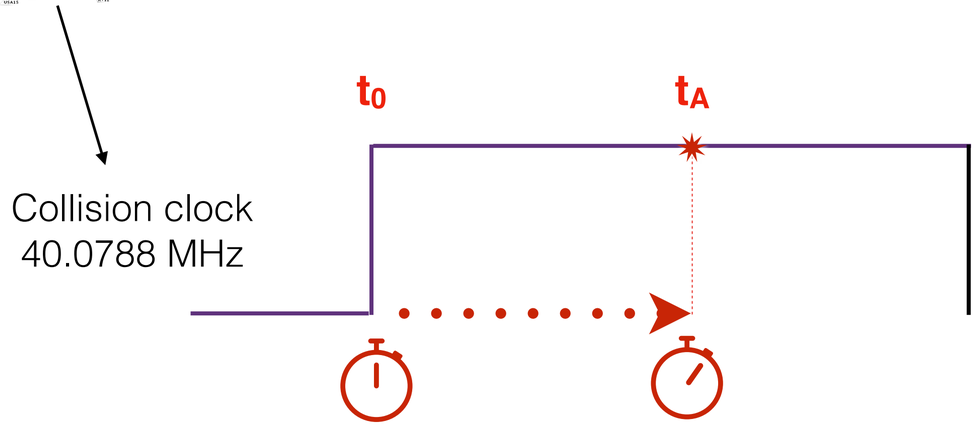

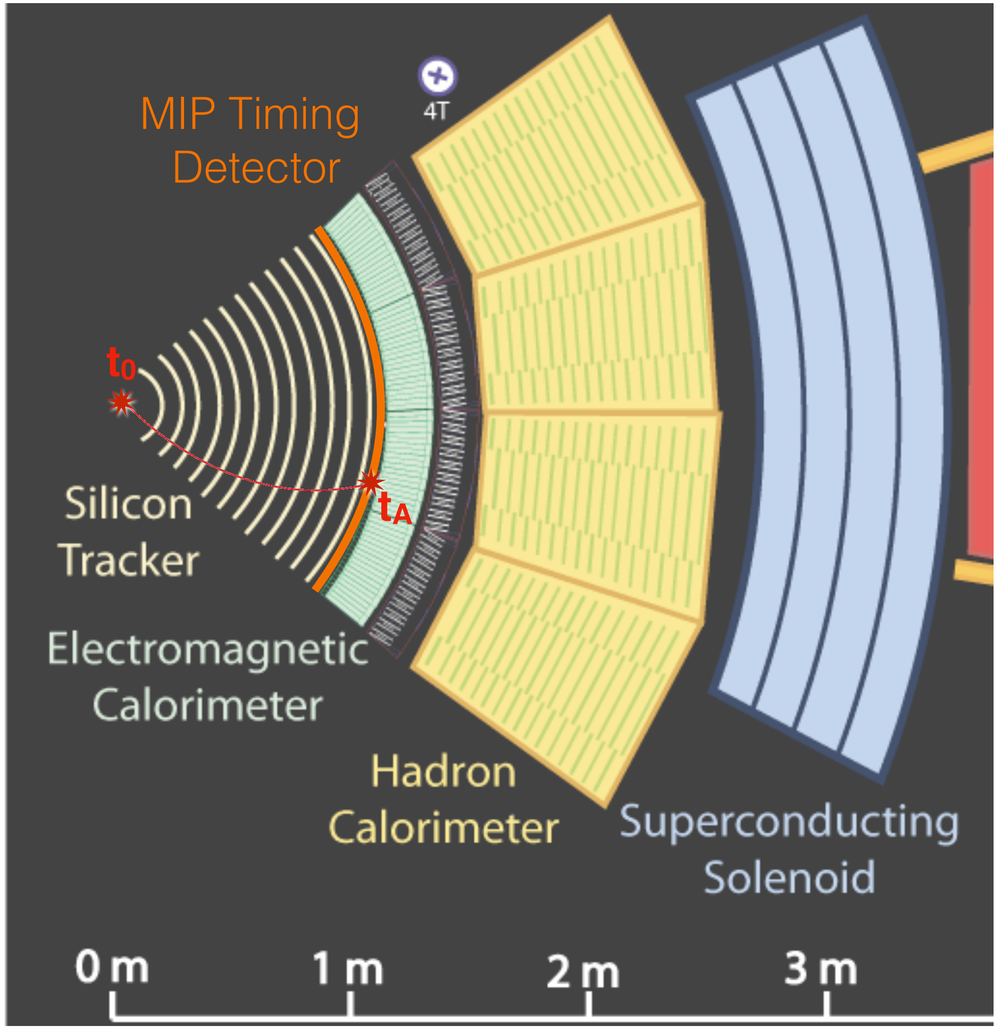

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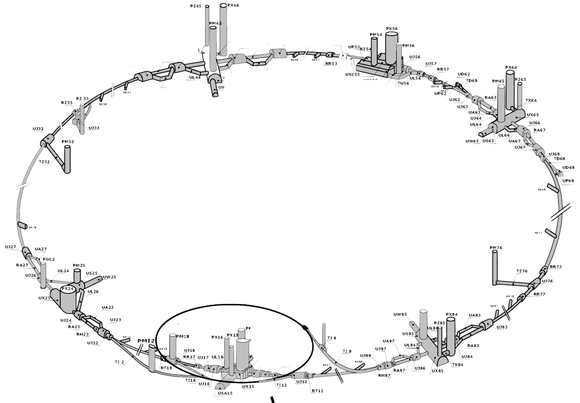

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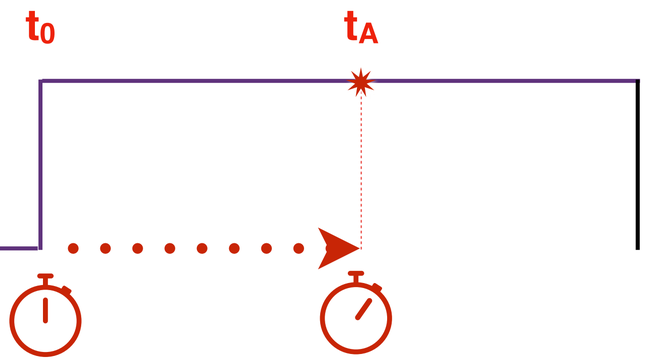
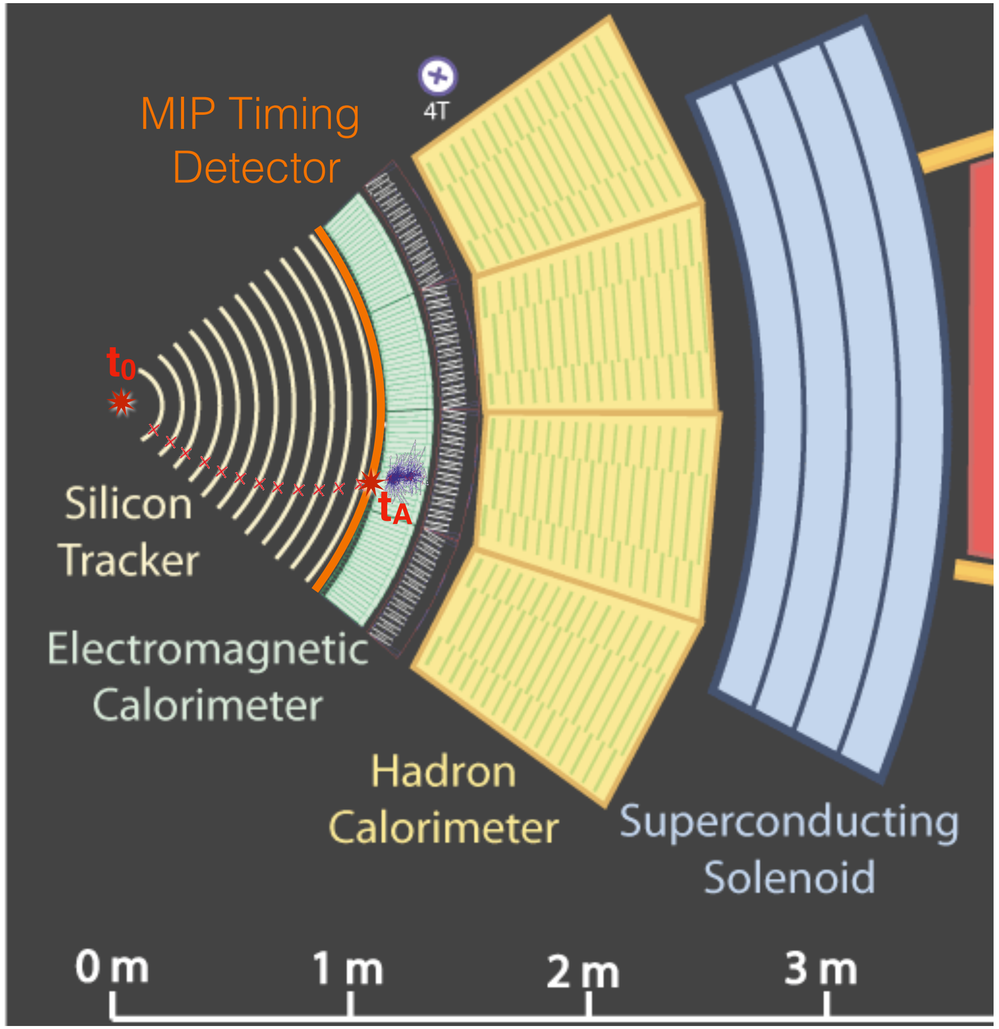
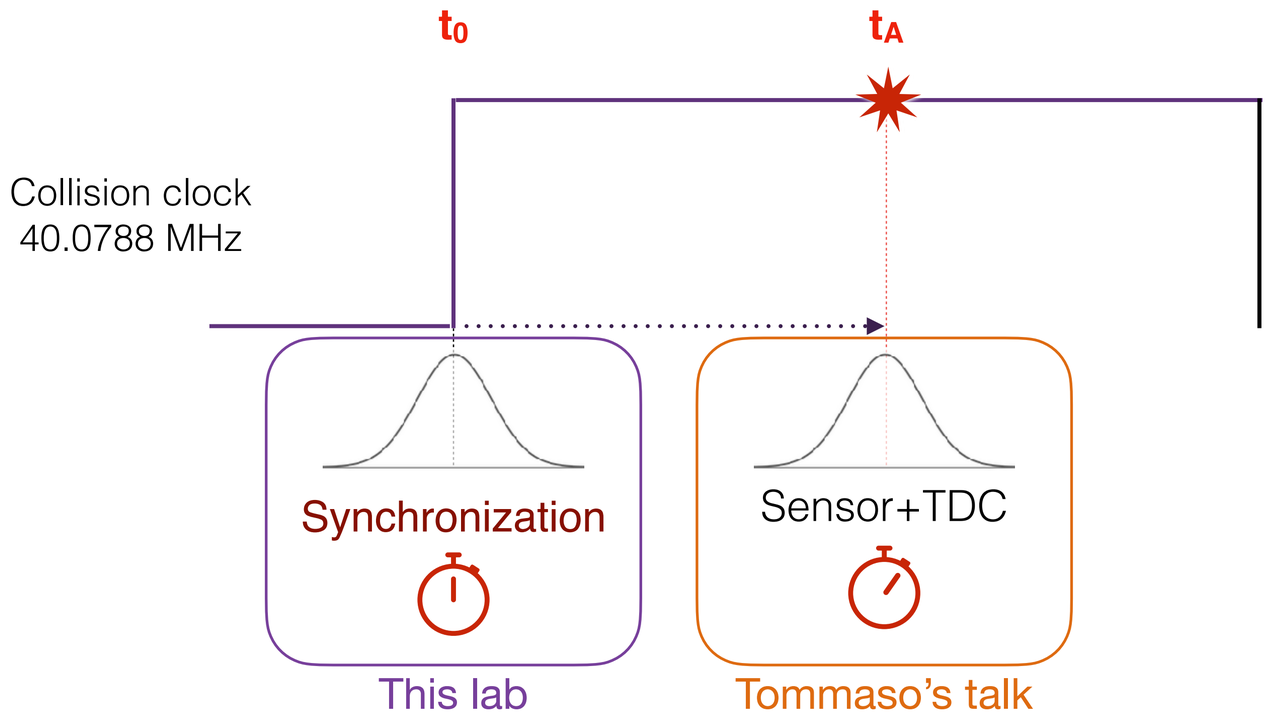


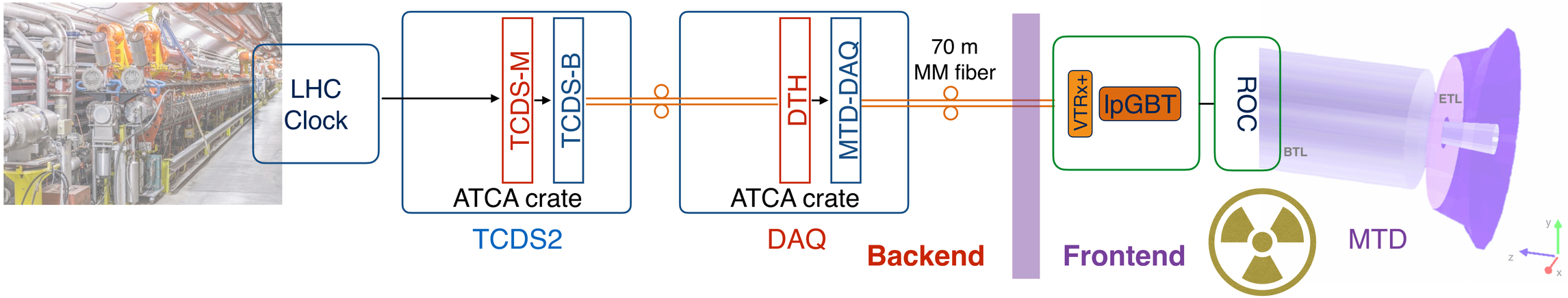


Timing measurement

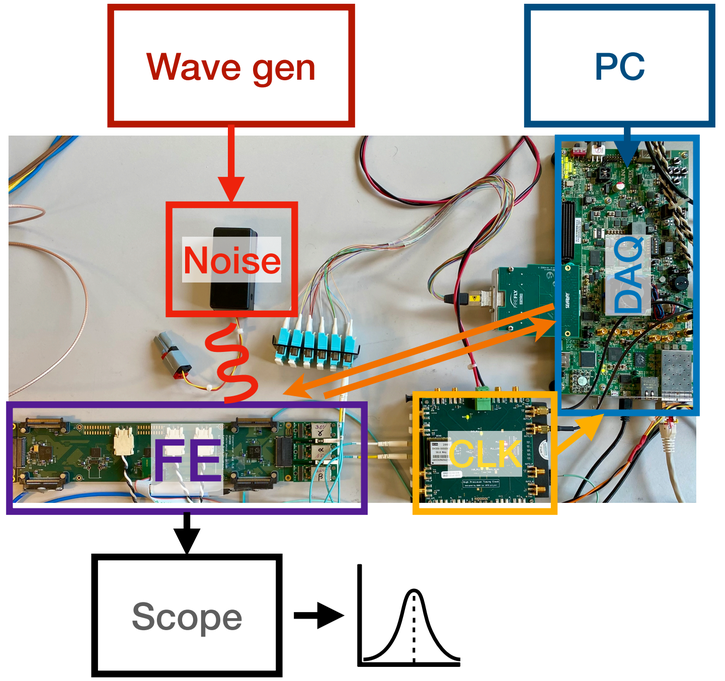


- The time to digital converter (TDC) on the detector opens a time window with the arrival of the synchronization (clock) signal.
- The window is closed with the arrival of signal from the sensor.
- The timing resolution directly depends on the Sensor and TDC resolution as well as the jitter from the clock distribution signal.

Synchronization system layout



- Precision timing distribution system at the HL-LHC is an extremely large and complicated system:
  - we will use a simplified table-top version for this particular lab.
- The backend (BE) system will be emulated with a precision clock generator and a commercial FPGA mezzanine board.
- The frontend (FE) system will be represented by an ‘lpGBT’ carrier board and connectors.



Components and goals

- Components:
  - DAQ system: Emulated with Xilinx KCU105 board and 10 Gb/s optical transceivers (VTRx+ and FireFly)
  - HPTC precision clock generator: less than 1 ps RMS jitter
  - CMS MIP Timing Detector Barrel layer Frontend Concentrator Card prototype: lpGBT
  - Custom noise generator
- Goals of the exercise:
  - Understand the individual components of the clock distribution tree
  - Characterize the clock distribution chain
  - Inject power noise and estimate the jitter per mV
  - Quantify the impact on the timing resolution
  - Try to mitigate the low frequency components of the jitter