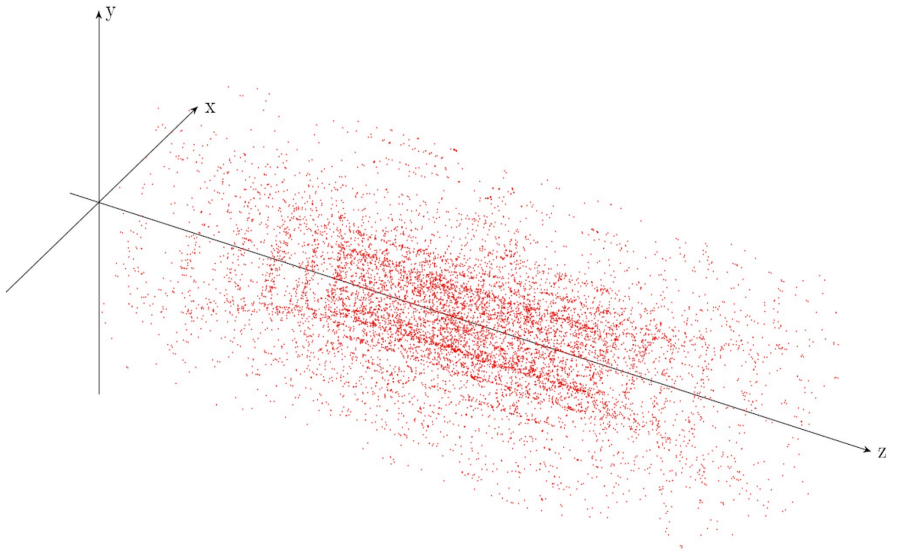
Lab: FPGA-based Track-Trigger for HL-LHC

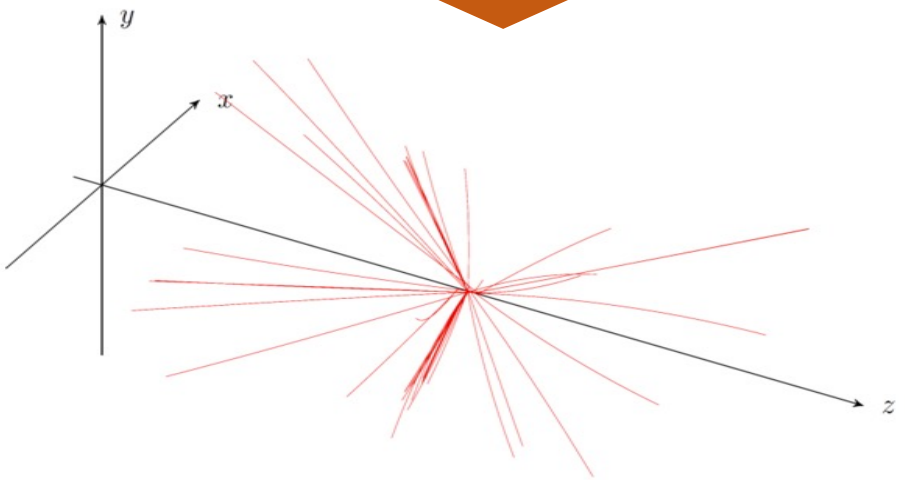
Context: CMS detector upgrade for HL-LHC (≥ 2027)

- Will reconstruct charged particle tracks, from all LHC p-p bunch crossings, in silicon tracker detector.
- Must process 1 trillion data points per second, finding tracks in < 4μs for use in L1 trigger event selection.
- Several years work by group of experienced physicists …



INFIERI Lab: Track reconstruction in an FPGA.

- Optimise a simple “Hough transform” tracking algorithm, implemented in the HLS language, and run in an FPGA.
- Can you find all the tracks? How fast does your algorithm run? Does it make efficient use of FPGA resources?
- 3 hours work by INFIERI student???



Lab. tutors: Giacomo Fedi (Imperial College/UK) & Ian Tomalin (RAL/UK)

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Lab. setup

- Hit data simulated from random particles crossing a multi-layer Tracking detector.
- An FPGA on the (commercial) KC705 board will read hits, reconstruct tracks & transmit them over serial link to a Linux computer. And show the number found on the KC705 LCD display.
- The FPGA algorithm is written in HLS code (+ a little VHDL).
  - You are given a basic algorithm, and asked to understand, optimise & improve it.

Programming skills

- This lab. will give you experience of HLS programming of an FPGA & of the Vivado tool. No previous experience of these is required. But you should already know C or C++.

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