How Advanced Packaging Is Changing Integrated Circuits

September 3, 2021

Advanced Packaging

- Advanced packaging is a general grouping of a variety of distinct techniques, including 2.5D, 3D-IC, fan-out wafer-level packaging and system-in-package.

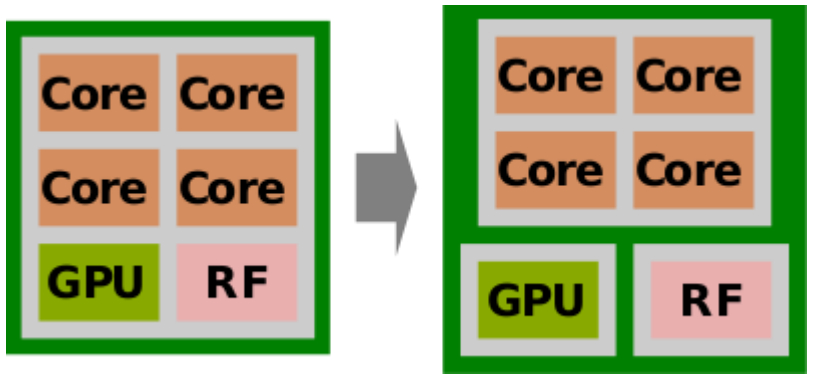
From Semiconductor Engineering

→ Appling semiconductor processes and techniques to packaging

Chiplet

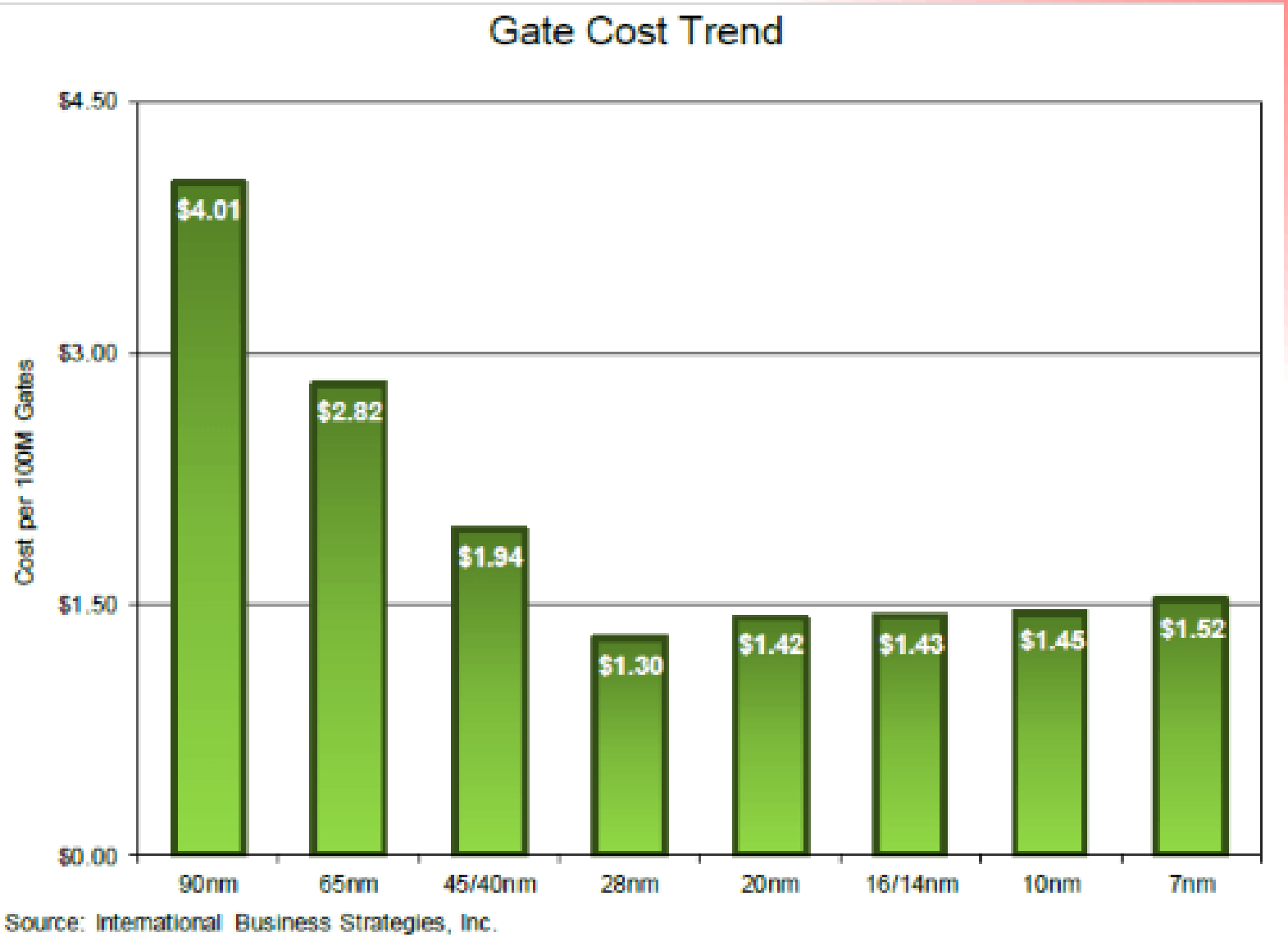
- A chiplet is an integrated circuit block that has been specifically designed to work with other similar chiplets to form larger more complex chips. In such chips, a system is subdivided into functional circuit blocks, called "chiplets", that are often made of reusable IP blocks.

From WikiChip



A NEED FOR CHANGE

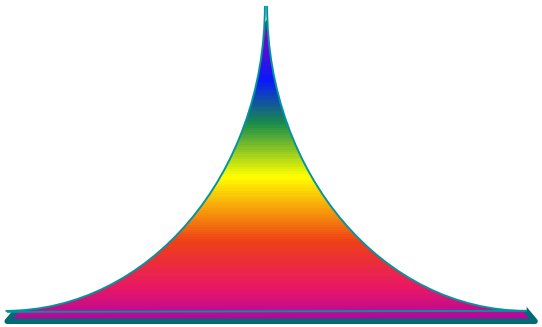
Cost Trend Reversal



Source: International Business Strategies, Inc.

More Moore

- The end is near…
  - 16nm, 14nm, 10nm, 7nm, 5nm, 3nm …
  - Maybe its now. Maybe it's in 3 years or 5 years, but the end of scaling is going to happen within the next decade
- 28nm - most cost effective node for years…?

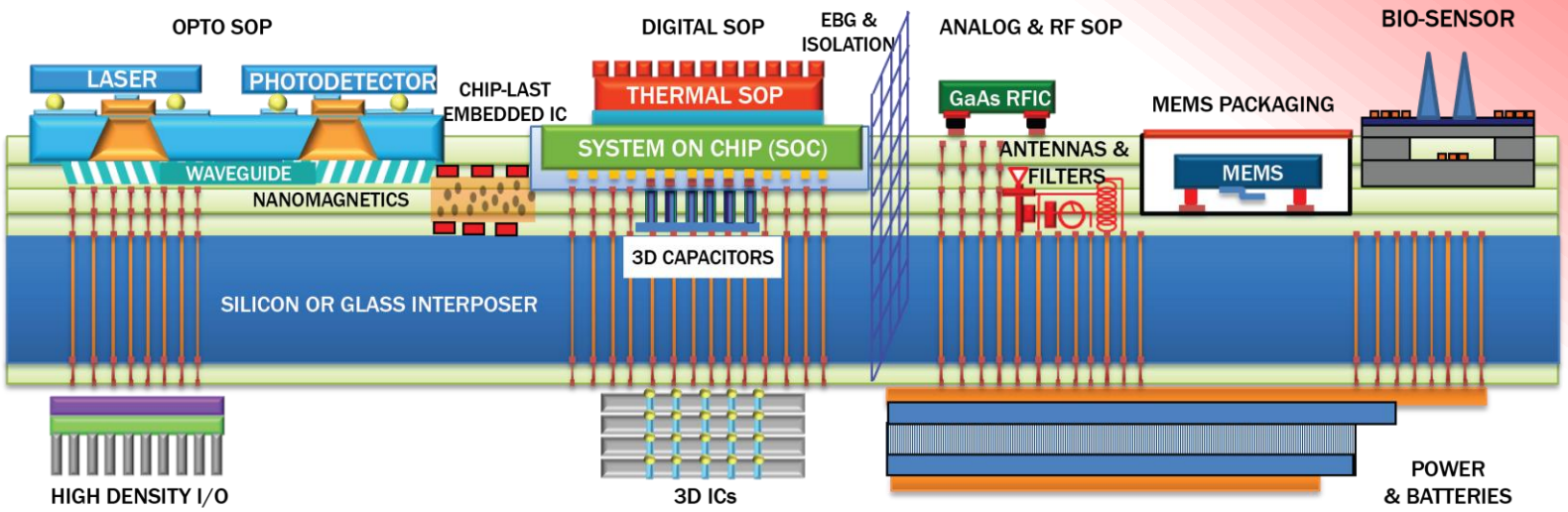


NHANCED SEMICONDUCTORS

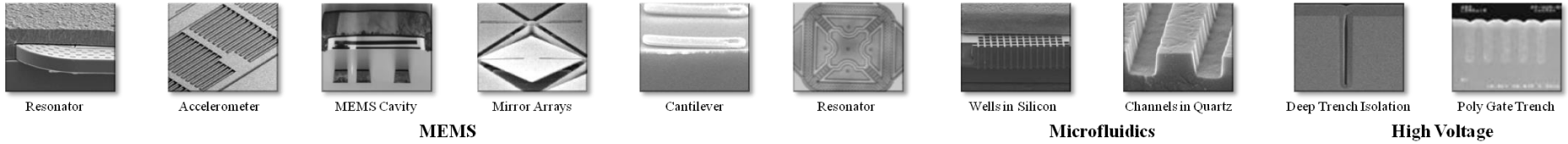
Internet Of Things

More Than Moore

1. THIN 2D AND 3D ACTIVES
2. THIN FILM PASSIVES
3. SYSTEM INTERCONNECTIONS
4. THERMAL INTERFACES AND STRUCTURES

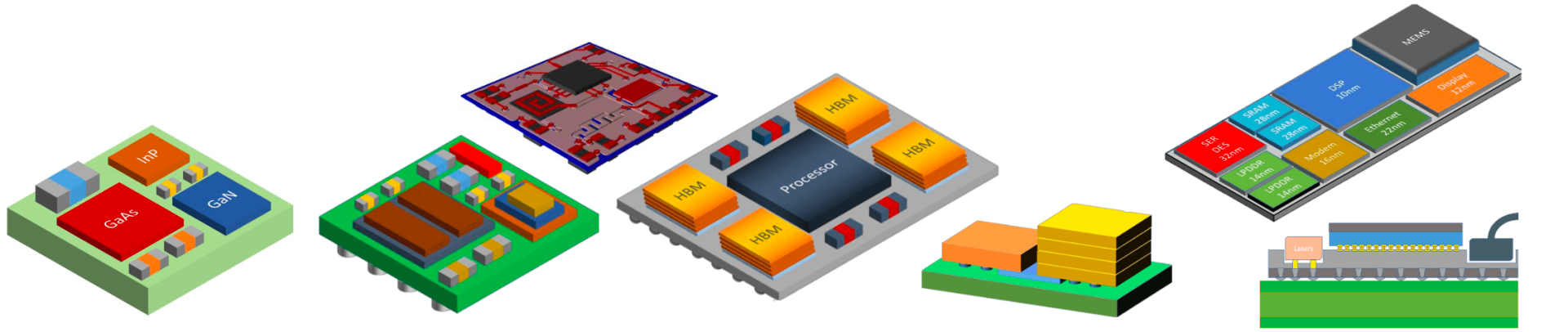


5. MULTI-FUNCTION MATERIALS
6. MIXED SIGNAL DESIGN AND TEST
7. MECHANICAL DESIGN AND RELIABILITY
8. POWER SOURCES



EVOLUTION AND REVOLUTION — ADVANCED PACKAGING AND CHIPLETS

Steps Toward Advanced Packaging and Chiplets



Multi-Chip Module (MCM) — 1980

System in Package (SiP) — 1998

RF Module — 2005

2.5D-IC (Silicon Interposer) — 2008

Embedded Bridges — 2014

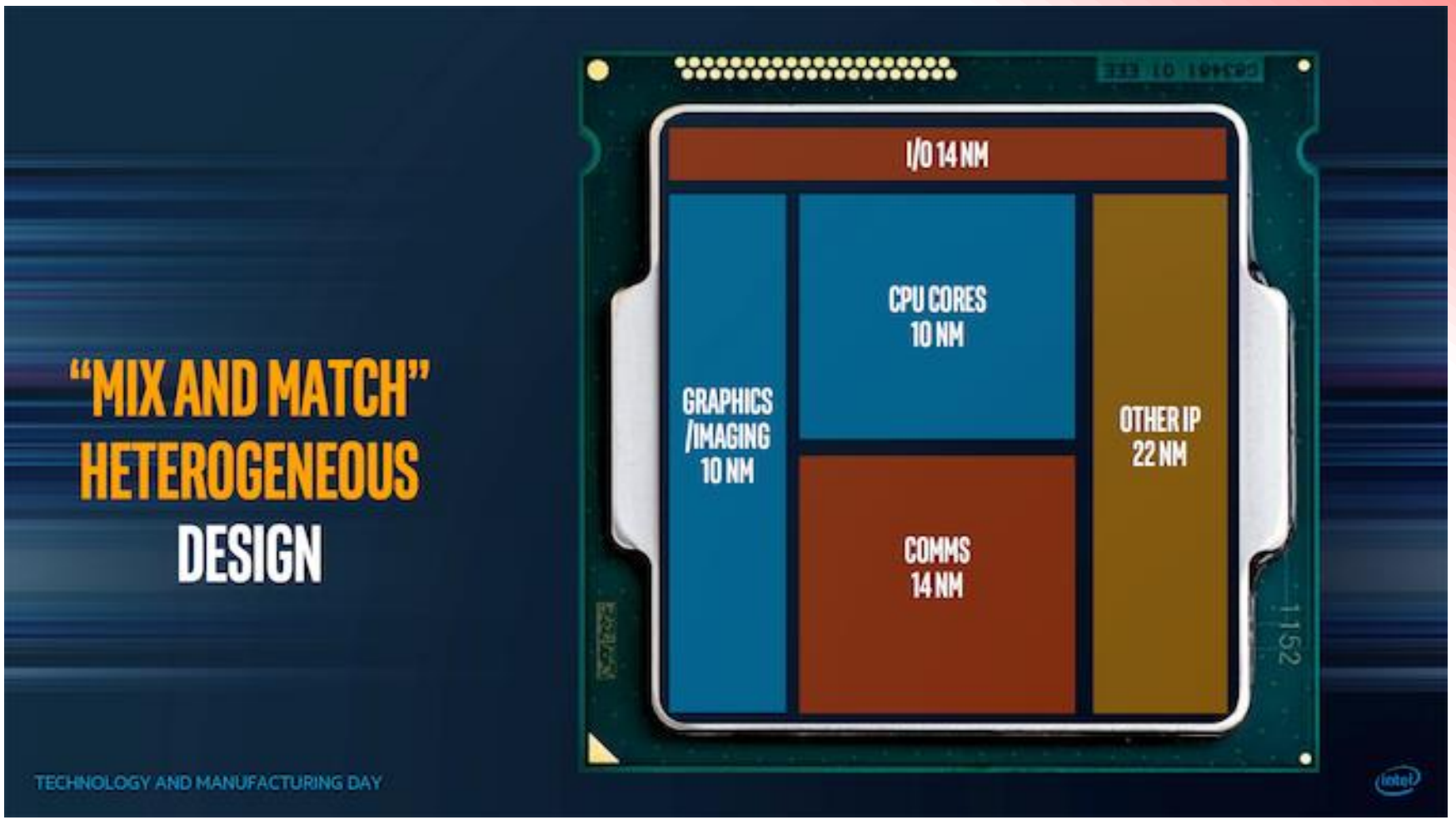
High-Density RDL/FOWLP — 2016

3D-IC (Chip on Wafer) — 2018

Heterogeneous Integration (Disaggregated SoC) Photonics — Now

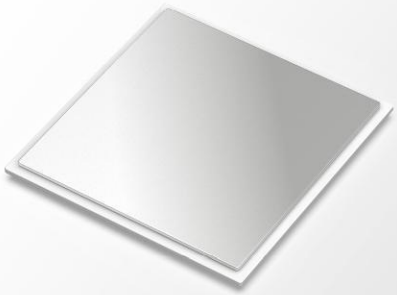
Semiengineering.com

New Possibilities



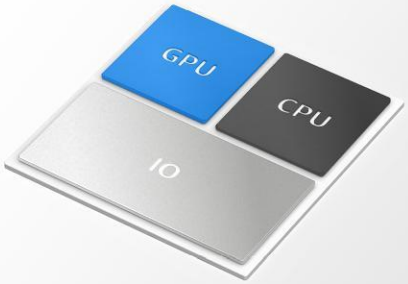
Better and Faster

IP/SOC Methodology Change



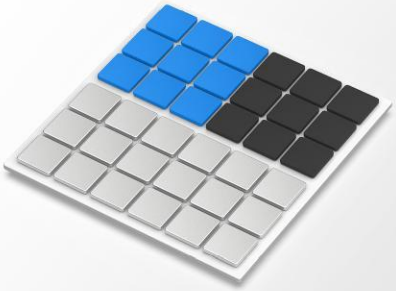
Monolithic | Integrated SOC

- Verified at SOC level
- **3-4 years** of Dev Time
- **100s of bugs** found in Silicon
- No reuse



Multiple Dies | in optimal process

- Verified at IP level
- **2-3 years** of Dev Time
- **10s of bugs** found in Silicon
- Some reuse

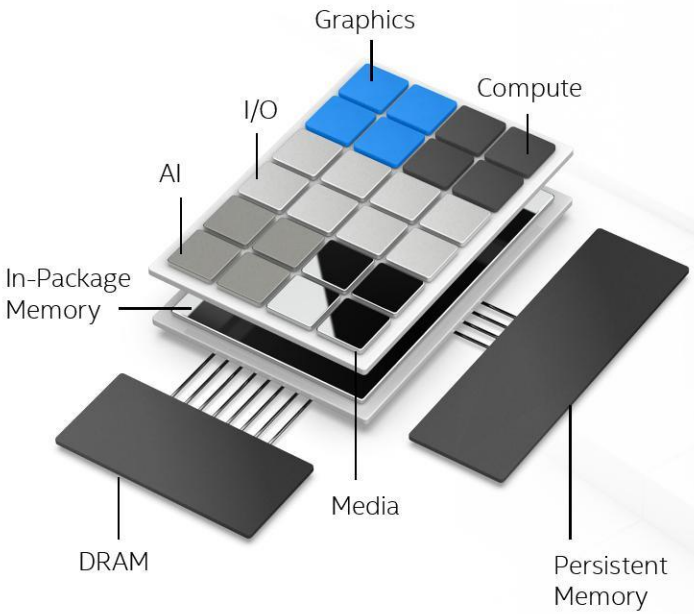


Individual IPs | in optimal process

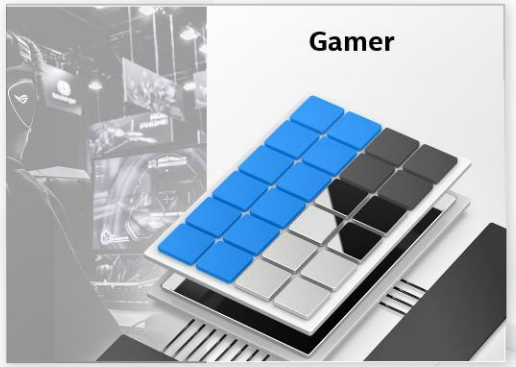
- Verified at IP/Chiplet level
- **1 year** of Dev Time
- **<10 bugs** found in silicon
- Significant reuse

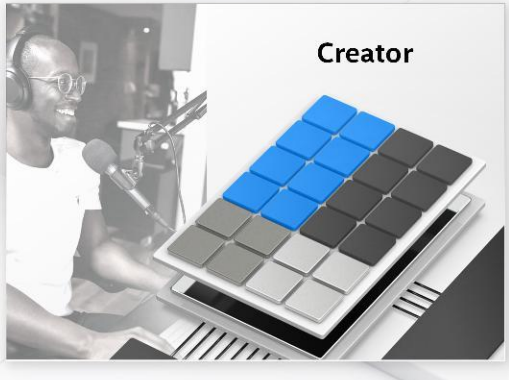
Easy Market Retargeting

Purpose Built Client



Long Term Vision



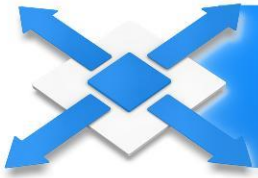


Intel's Vision of the Future

Client 2.0

EXPERIENCE FIRST

- Uniquely built to differentiate key experiences
- Uncompromised performance to deliver seamless experience



SCALABLE

- Ability to mix and match function/IPs to processes
- React faster with reuse and enable faster TTM
- Developer Friendly Platforms

ENERGY EFFICIENT

- KEI's can benefit from using "Efficient" Cores in SOC Chiplet
- Pick low power technology for IOs

OPTIMAL USE OF MOORE'S LAW

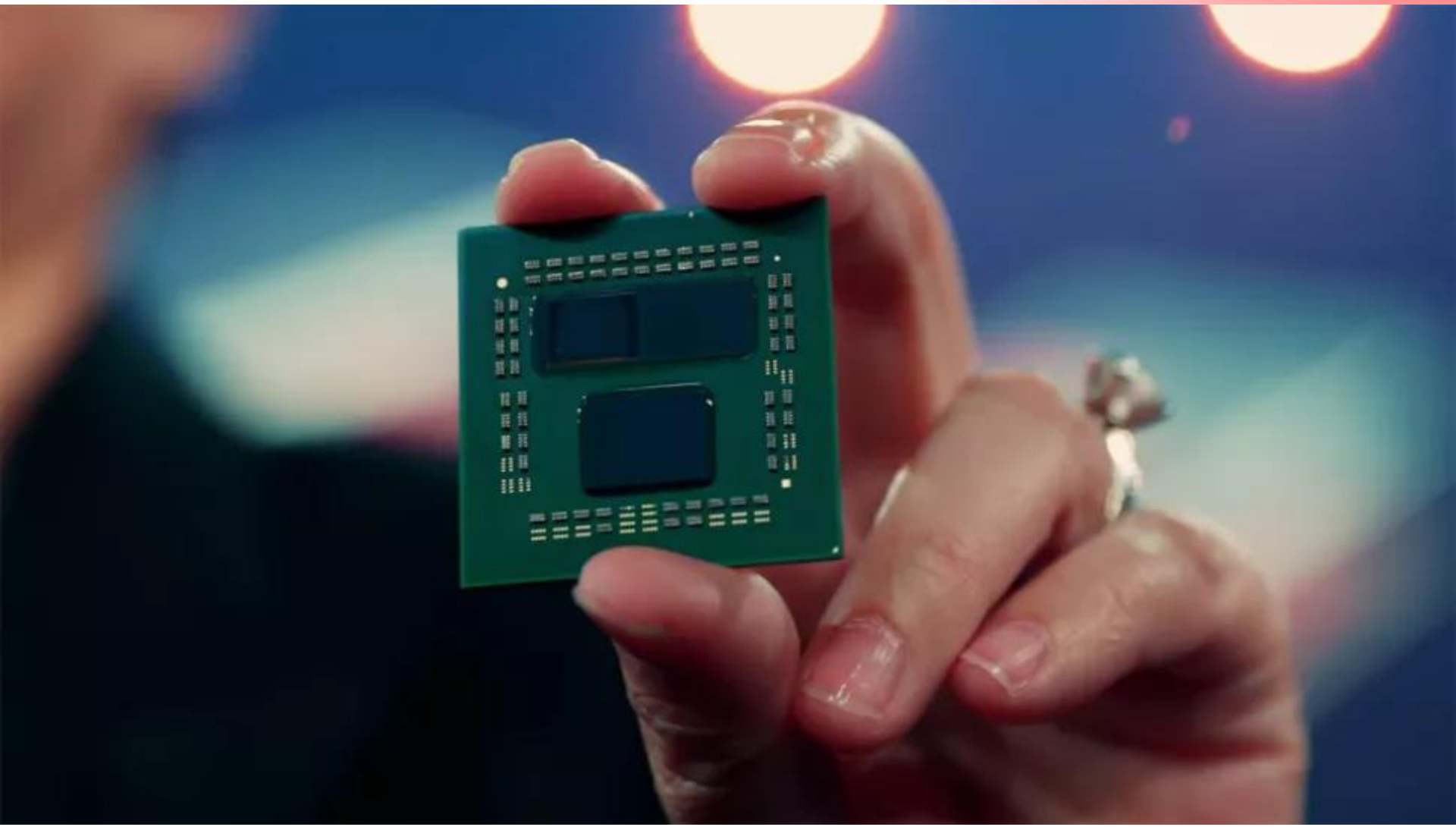
- Focus on Performance for General Purpose Compute (CPU)
- Focus on Density for scalable compute (GPU, AI etc.)

AMD – Enormous Benefits to Chiplets

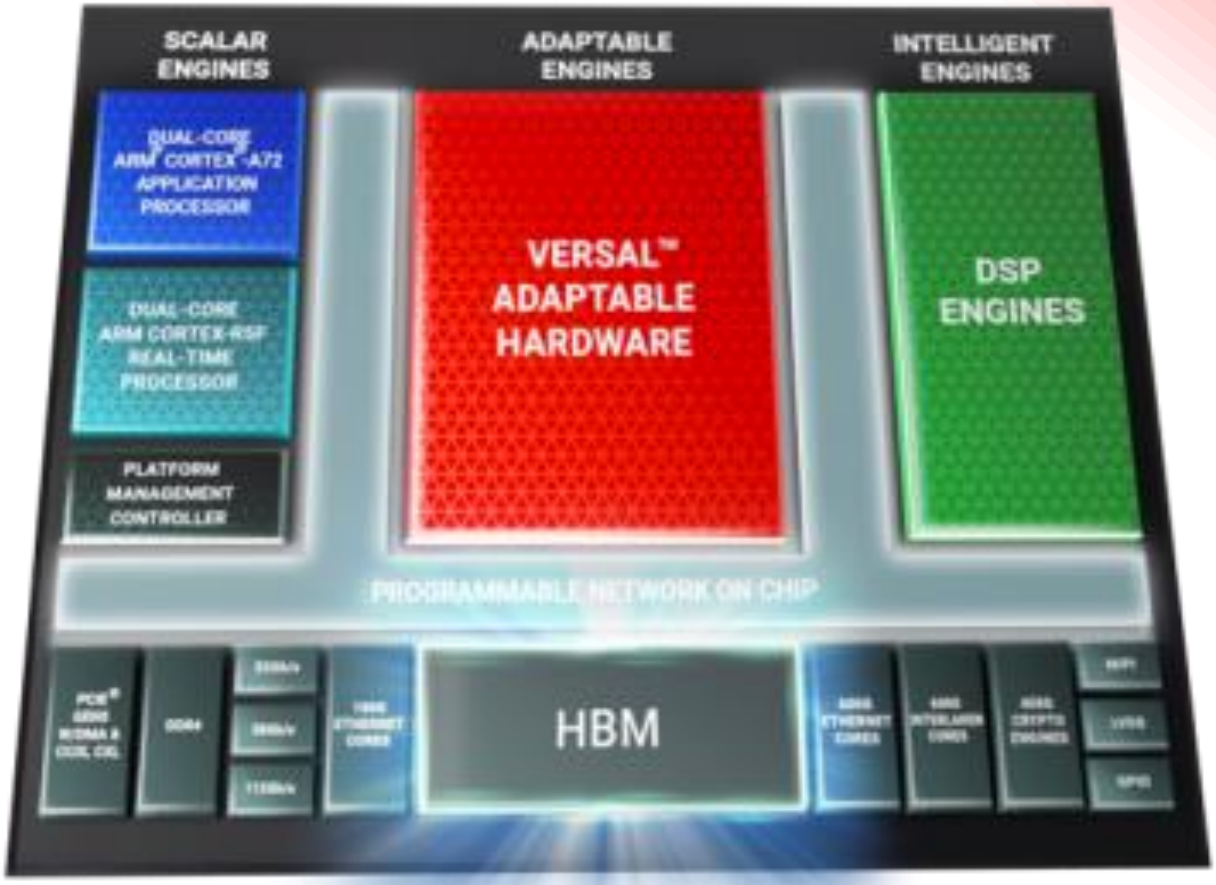
Monolithic 32-core Chip
777mm² total area
1.0x Cost

4 x 8-core Chiplet, 213mm² per chiplet
852mm² total area (+9.7%)
0.59x Cost

AMD Production Chiplets



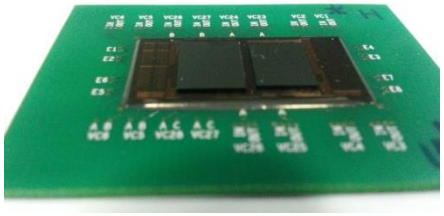
Xilinx – Using Chiplets For >10 Years

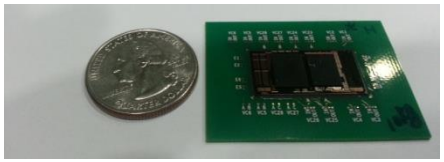


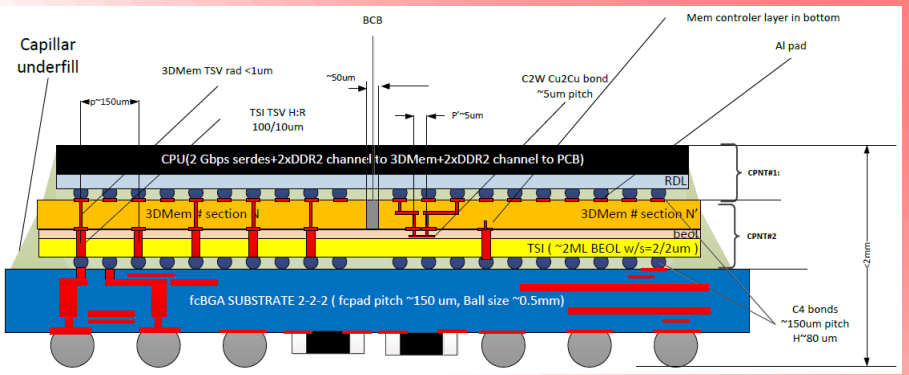
2.5D ADVANCED PACKAGING

2.5 Circuits

IME A-Star / Tezzaron Collaboration







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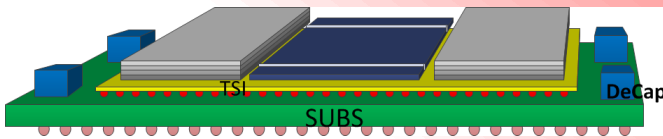
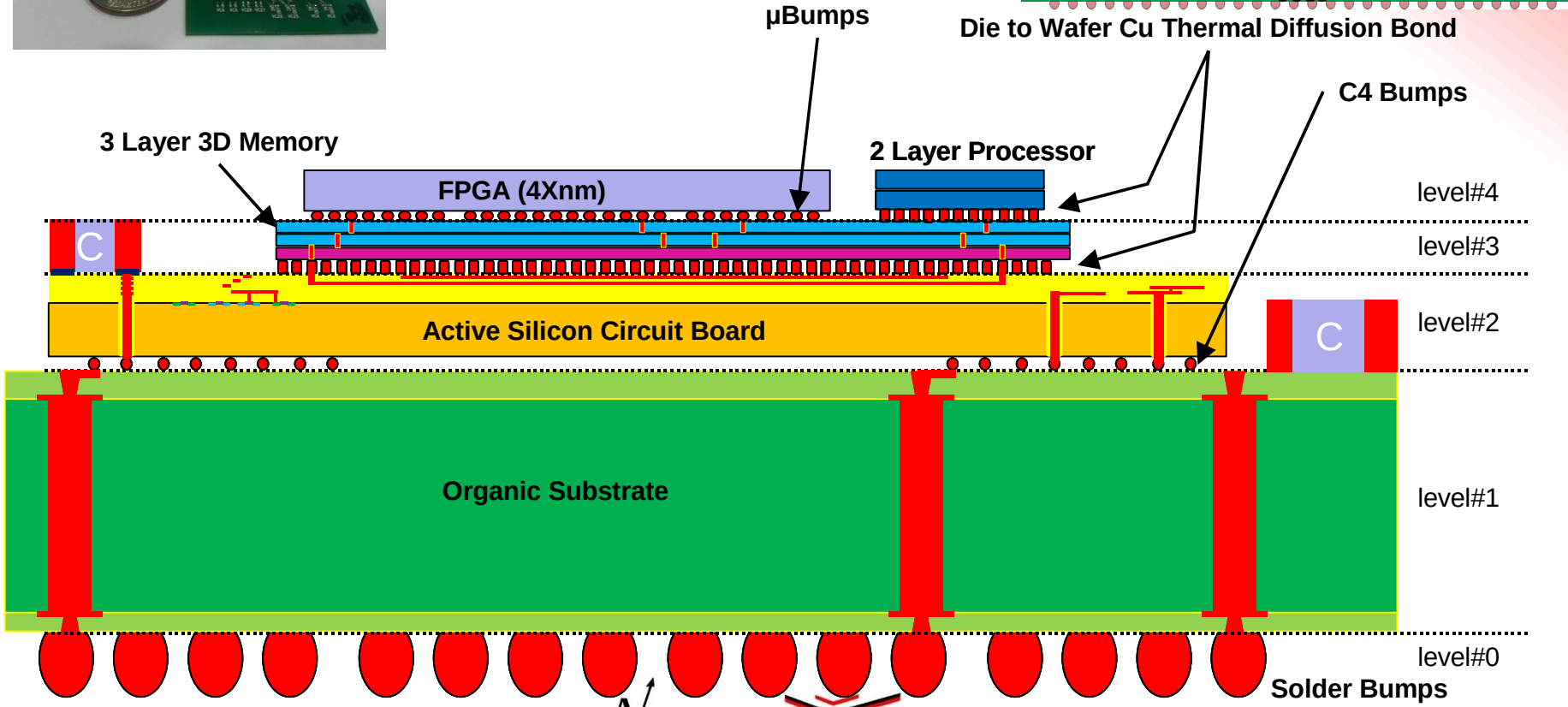
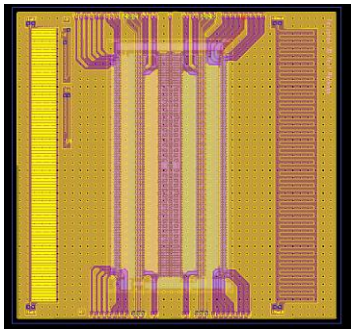
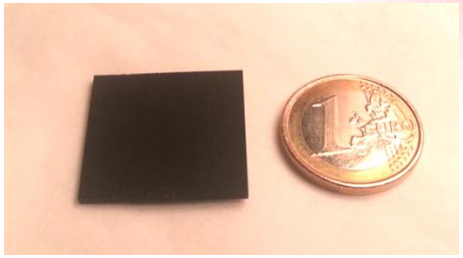




Si Interposers

Bigger, Better, Faster
>50x50mm, Up to 6 layers, Lower R,C





High Performance Driven By Interposers

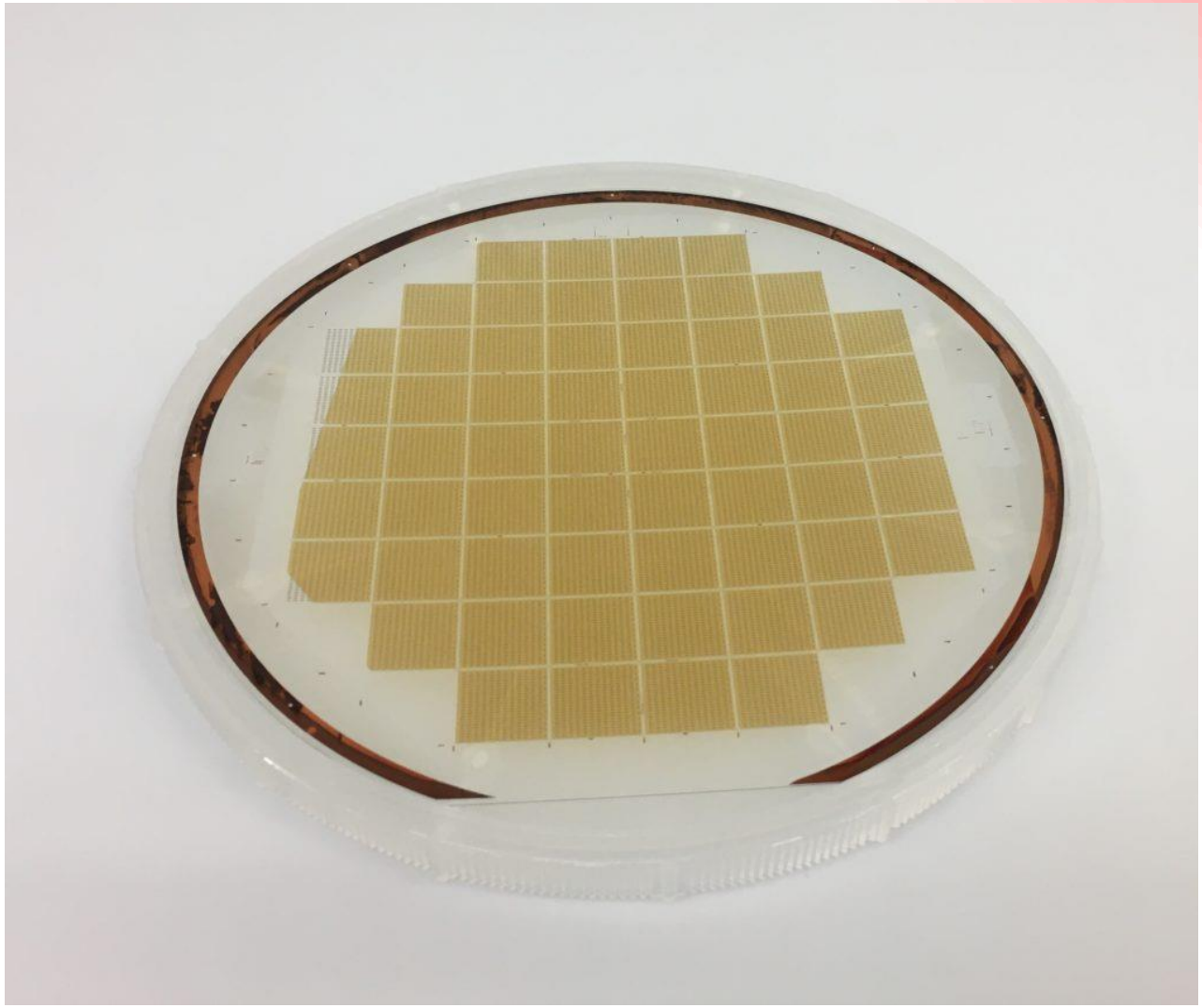
>90% performance improvement vs ideal case monolithic

>200% better (lower) signal delay vs ideal case monolithic

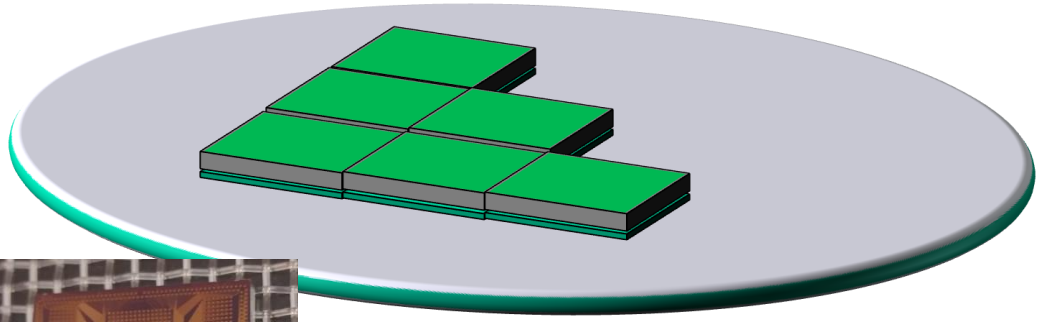
Layer	Metal thickness	R(mΩ/□) at DC	W	L	Cg (fF)
M1	2.5µm	7.2	10	2	2.3
			200	10	52
M2	2.5µm	7.2	10	2	1.5
			200	10	17
M3	2.5µm	7.2	10	2	1.1
			200	10	15
M4	2.5µm	7.2	10	2	0.74
			200	10	12

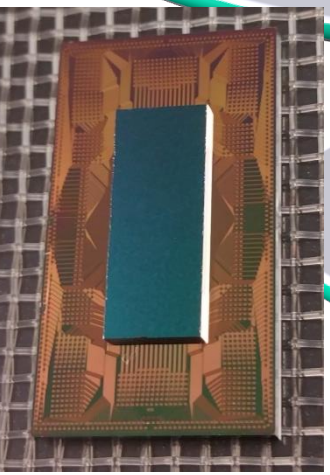
	TSV Diameter	TSV Height	Resistance	Cg (fF)
Filled	10µm	100µm	21.2mΩ	180
Filled	50µm	400µm	~4mΩ	~600

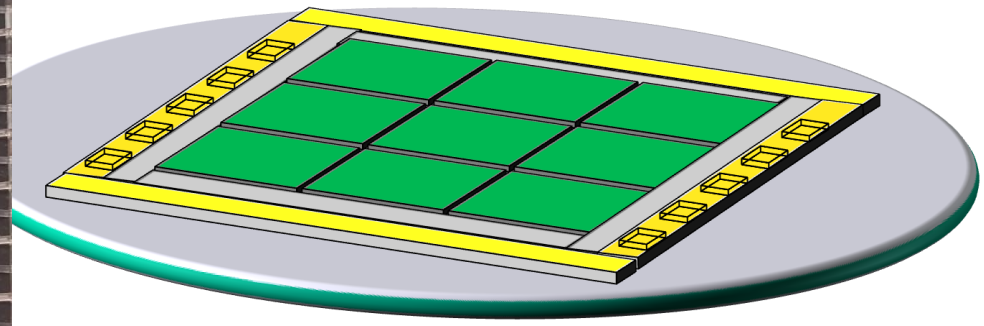
Glass Interposers

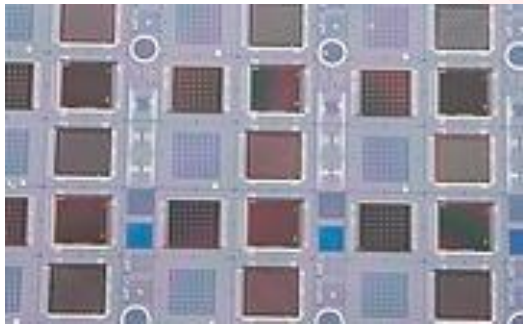


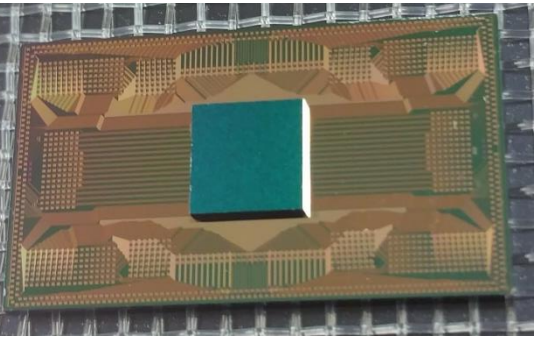
Die-on-Wafer and Wafer-scale FPAs

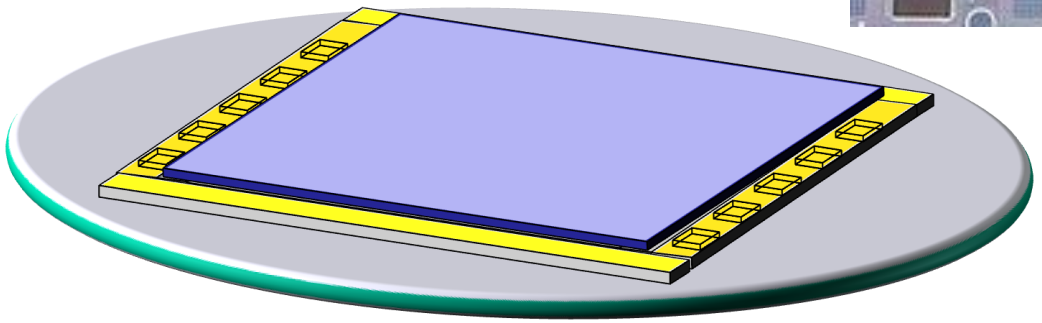










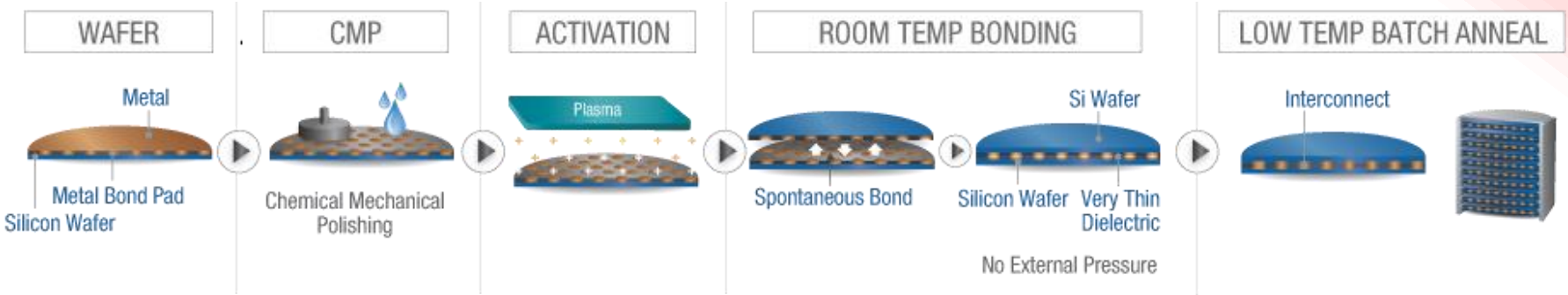


- Waferscale integration
- Up to 85 die assembly
- 10um die space
- 1um placement
- 150/200/300mm

NHANCED SEMICONDUCTORS

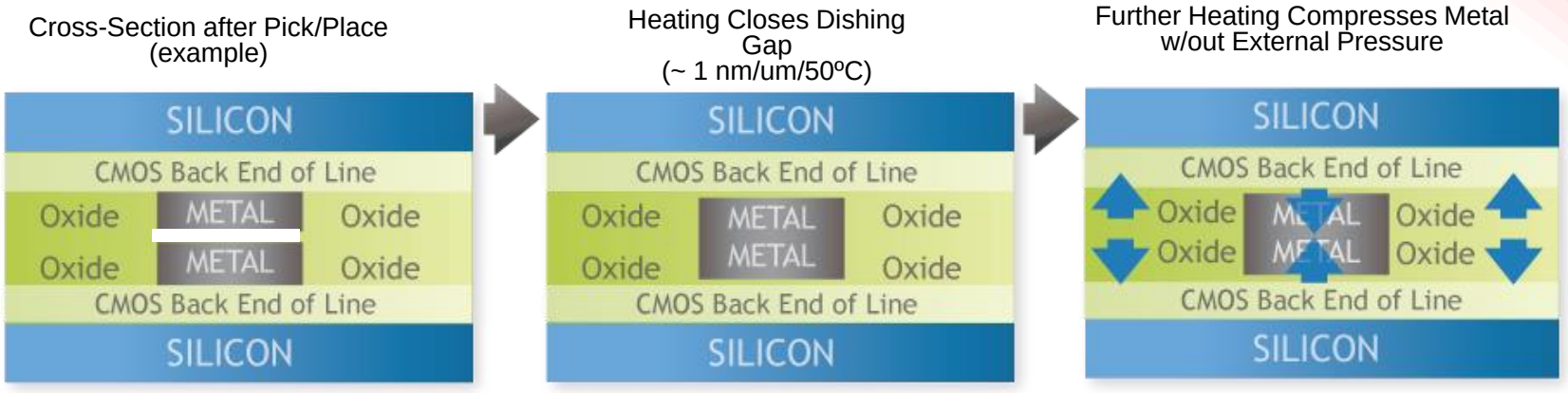
3D ADVANCED PACKAGING

DBI®: Low Temperature Hybrid Bonding Process



Hybrid Bonding Internal Thermo-Compression

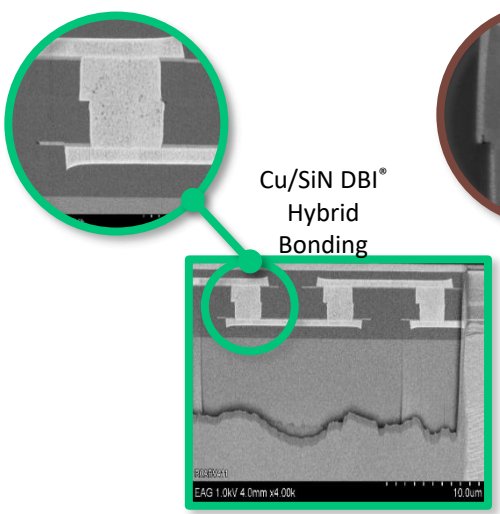
Electrical Interconnections without External Pressure
Minimizes Stress and Cost of Ownership



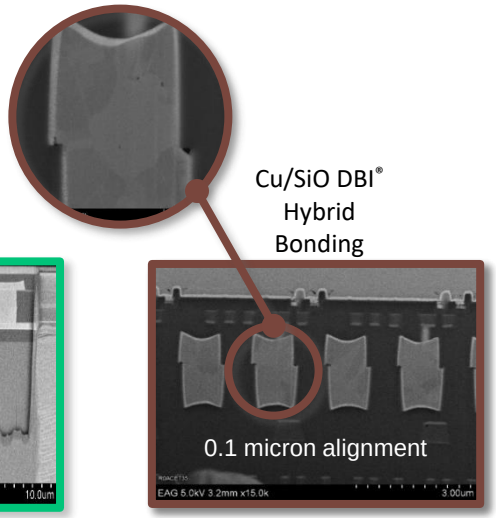
Spontaneous Chemical Reaction with Byproducts Diffusing Away from Bond Interface

NHANCED SEMICONDUCTORS

Hybrid Bonding Interconnect Pitch Scaling

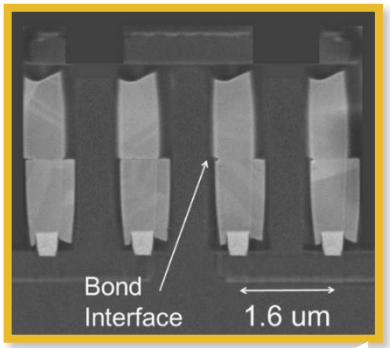


10 µm DBI® pitch, 300℃



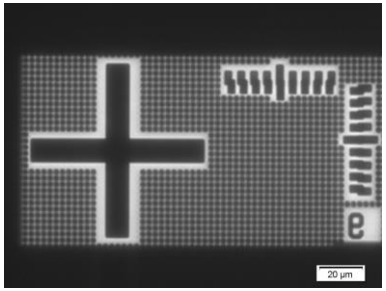
1.9 µm DBI® pitch, 300℃

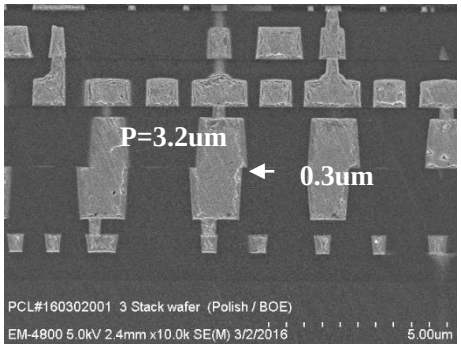
Scalable To < 1um Pitch



1.6 µm DBI® pitch, 300℃

- 3sigma < +/- 1um misalign performance
- Production Minimum pitch = 2.44um
- Best alignment is achieved with face-to-face bonding



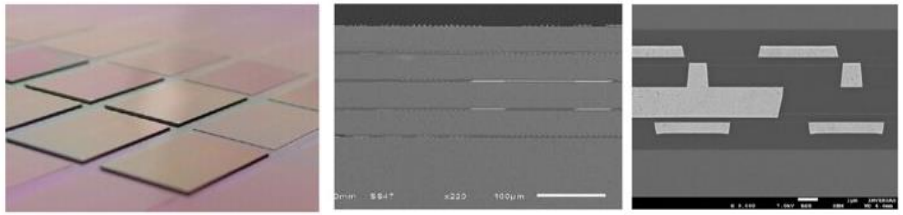


NHANCED SEMICONDUCTORS

Wafer-to-Wafer vs. Die-to-Wafer

- **Wafer-to-Wafer**
- Process implementable in foundry back end of line (BEOL) with a low cost-of-ownership
  - Particle control requirement easily met
  - Proven in many applications
    - CMOS BSI Image Sensors
    - RF switches
- Requires wafer and die sizes to be matched

50um die stacked 4-high, optical and SEM cross-sections



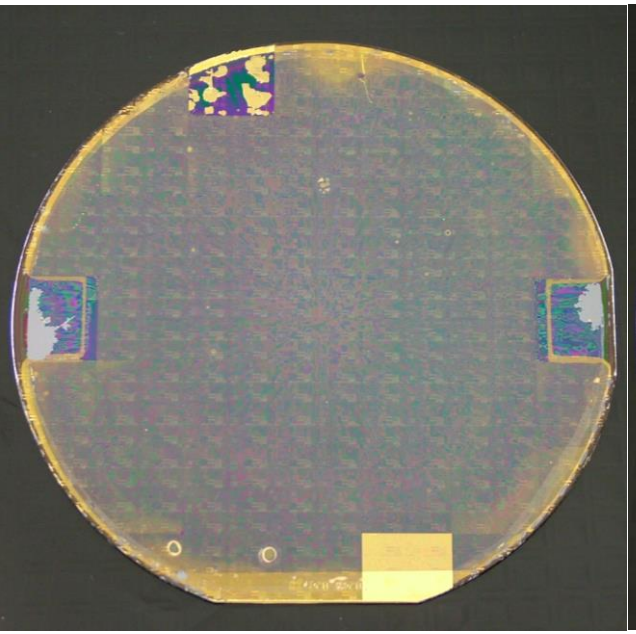
4-high 50um die stacks 4-high cross section Die bond interface

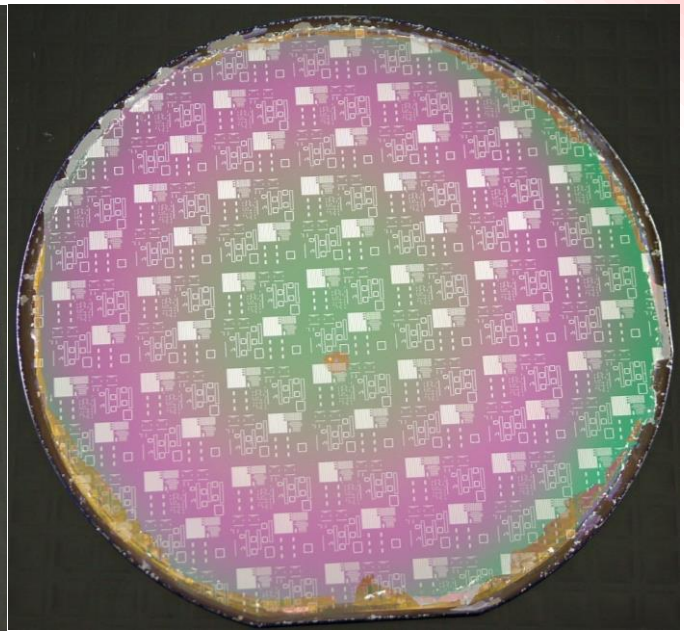
- **Die-to Wafer (DBI Ultra)**
- Accommodates die tiling, stacking and mismatched die/wafer sizes
- Additional process steps of die singulation and handling required
  - Additional particulate/handling challenges

Die Stack with DBI® Hybrid Bonding

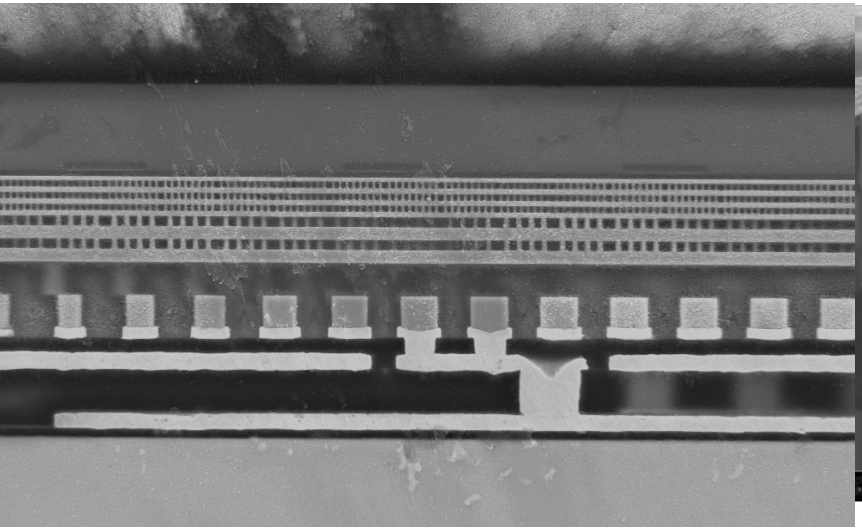
- Improved performance, cost, and yield/reliability potential
  - Throughput – no reflow/alloy, throughput improved x2
  - Thermals – no underfill, ΔT improved x5/10 for 4/8 high stack
  - Electrical parasitics – DBI® replaces bumps, RC improved ~ x20
  - Reduced stress – eliminate reflow/alloy and underfill
  - Reduced pitch – pick/place tool limited, throughput dependent

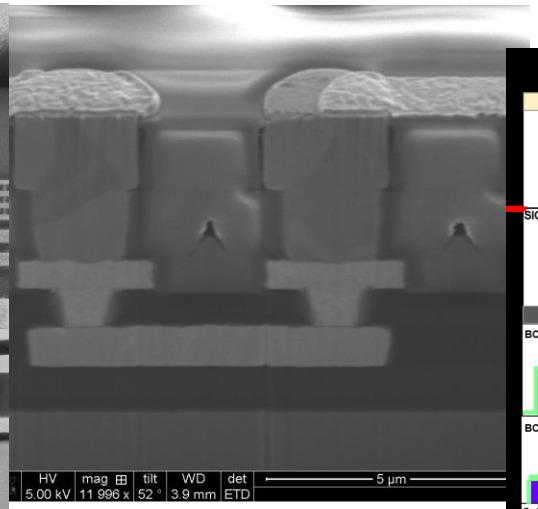
Mixed Materials – True Heterogenous Integration

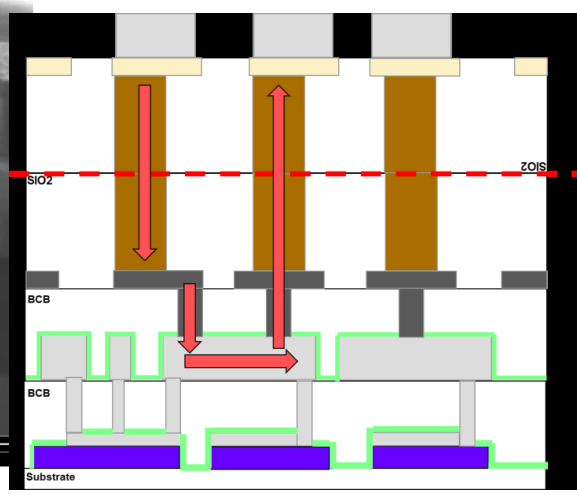




- GaN
- 3D CMOS/InP/GaN
- GaAs
- Graphene

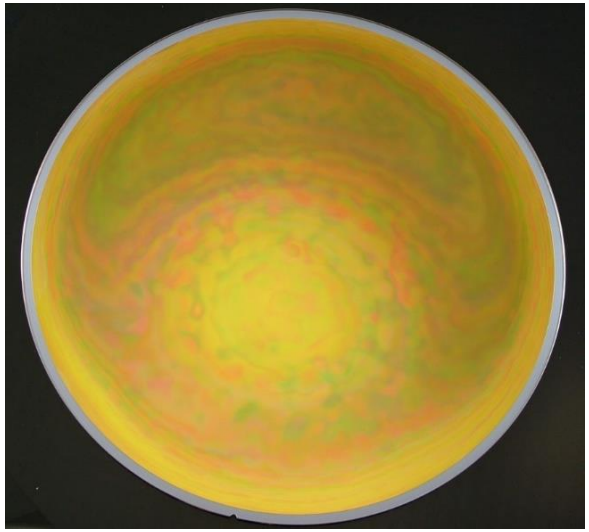




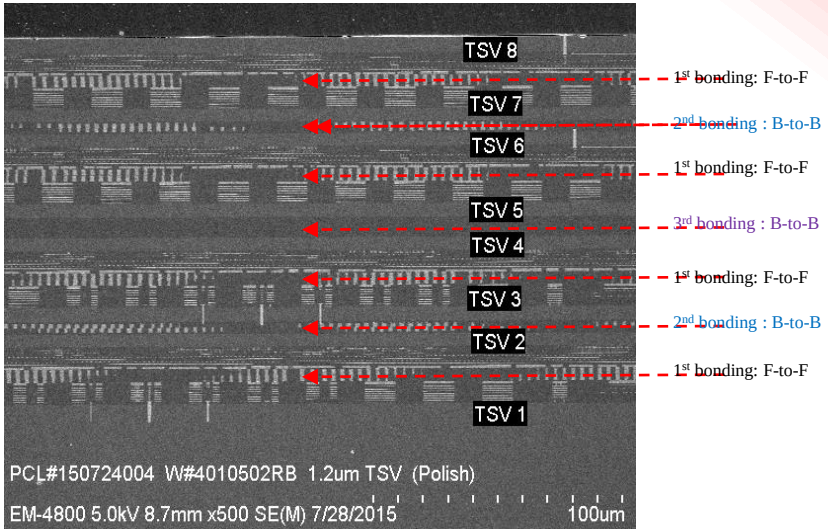


SiO2 Bonding and Hybrid Bonding for Multi-Wafer Stacking

- 4 wafer stack : SiO2 bonding
- 8 wafer stack : Hybrid bonding
- 16 wafer stack : SiO2 bonding
- 20 wafer stacks : Hybrid bonding
- Currently ~80% of NHanced processed wafers are used for customer “production”



(a) Picture of 4 wafer stack bonded using SiO2 bond
Top Si has been removed



(b) SEM cross sectional micrograph for 8 device wafer stack

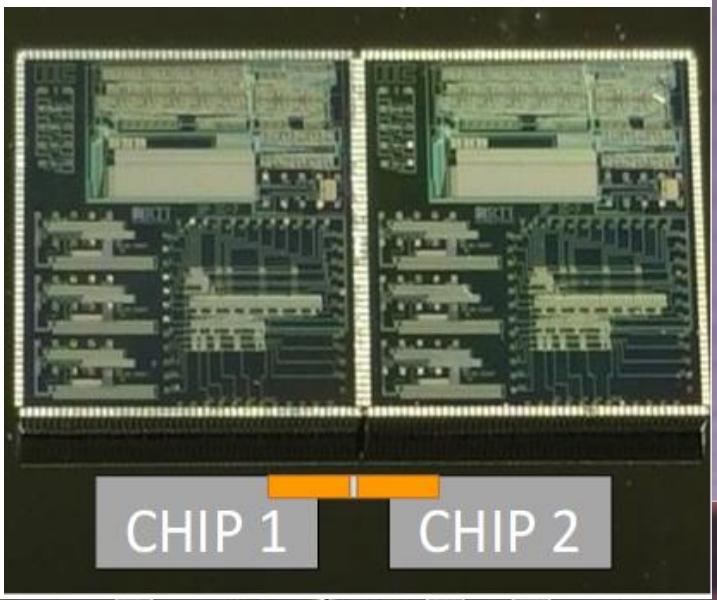
NHANCED SEMICONDUCTORS

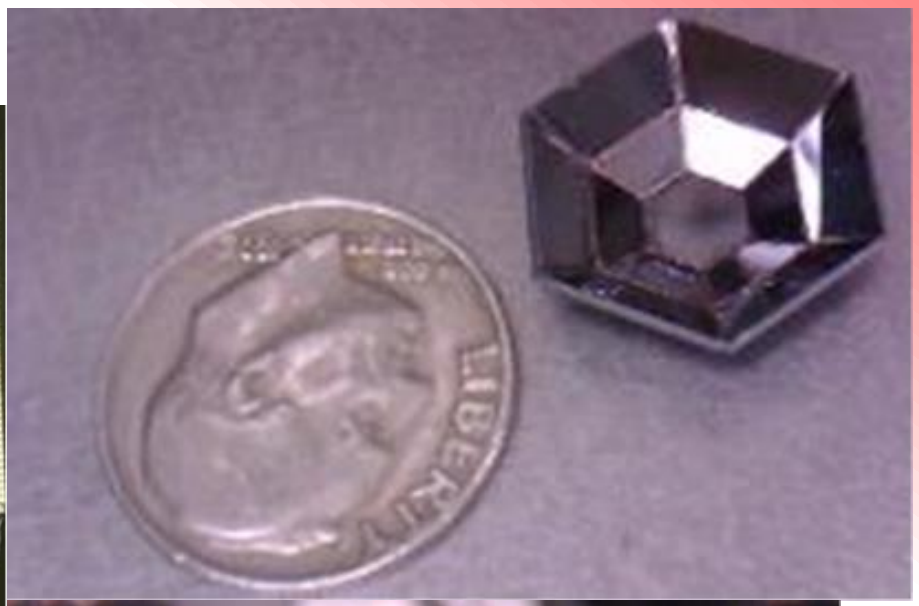
DBI Integration Capabilities and Roadmap

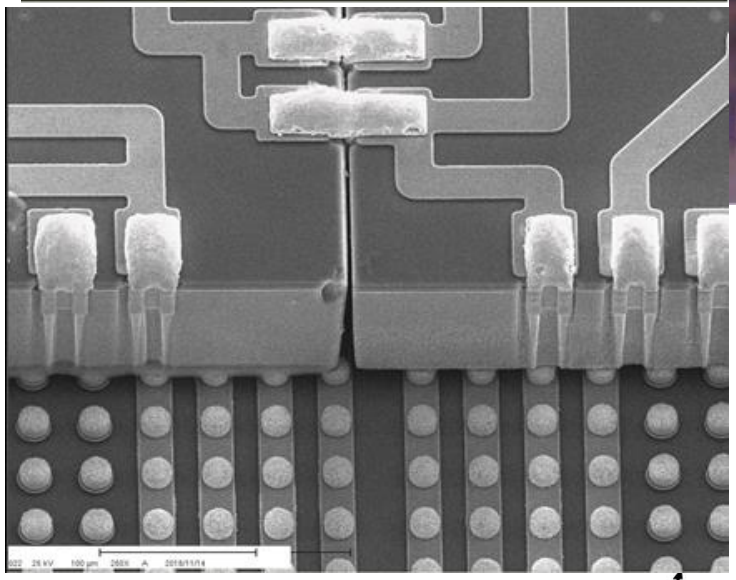
- Wafer-to-wafer
  - 200mm @ 2.4um pitch → 300mm @ <1um pitch
  - <100nm alignment error
- Die-to-wafer
  - 10um pitch → 3um pitch
- 8 layers → 20+ layers
- Low temperature
  - 150C → 125C
- TSV sizes
  - 80um to 0.6um
  - Up to 12:1 aspect ratio

NHANCED SEMICONDUCTORS

Quilt Packaging



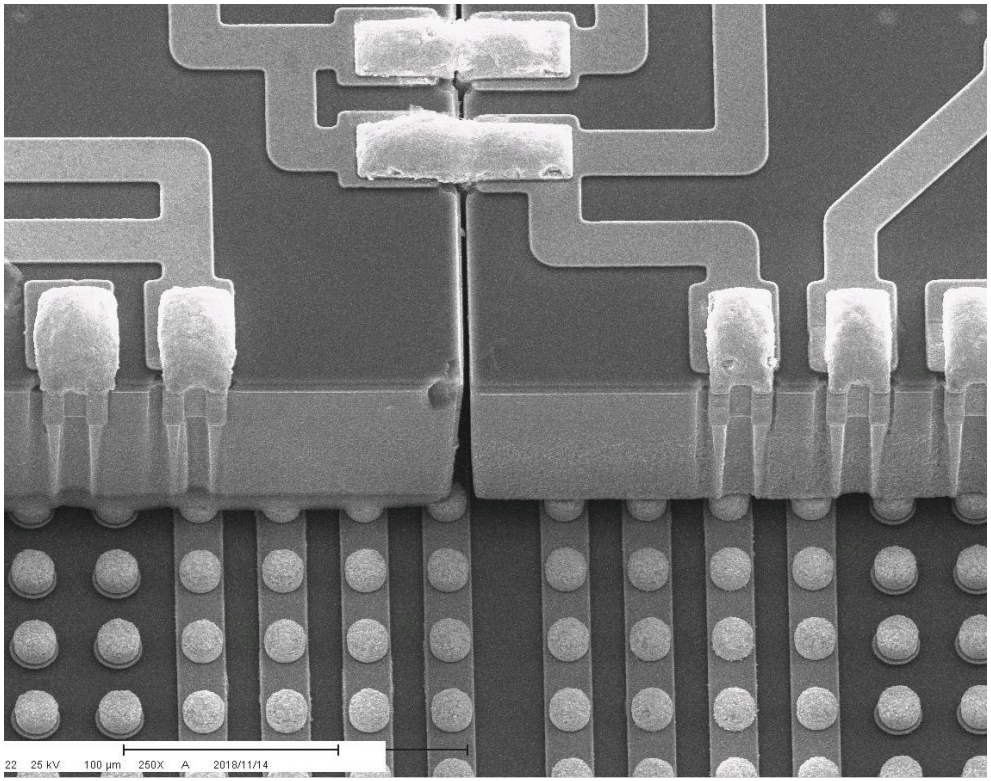




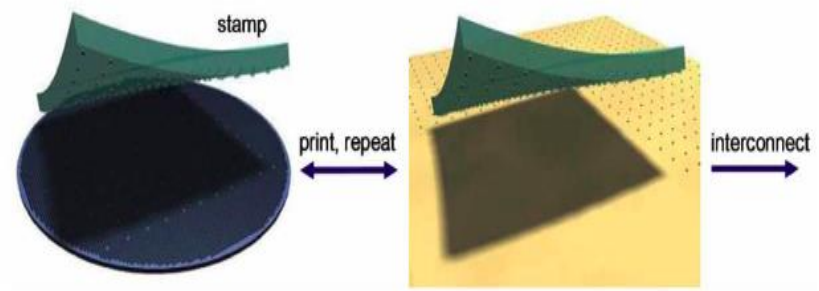
(top left) Quilt Packaging concept cross-section illustration & image of a post-reflowed QP CMOS quilt; (bottom left) SEM image of quilted chip-to-chip seam of >10 micron width; (top right) QP-enabled miniature curved array demonstration article; (bottom right) profile view of QP-enabled miniature curved array.

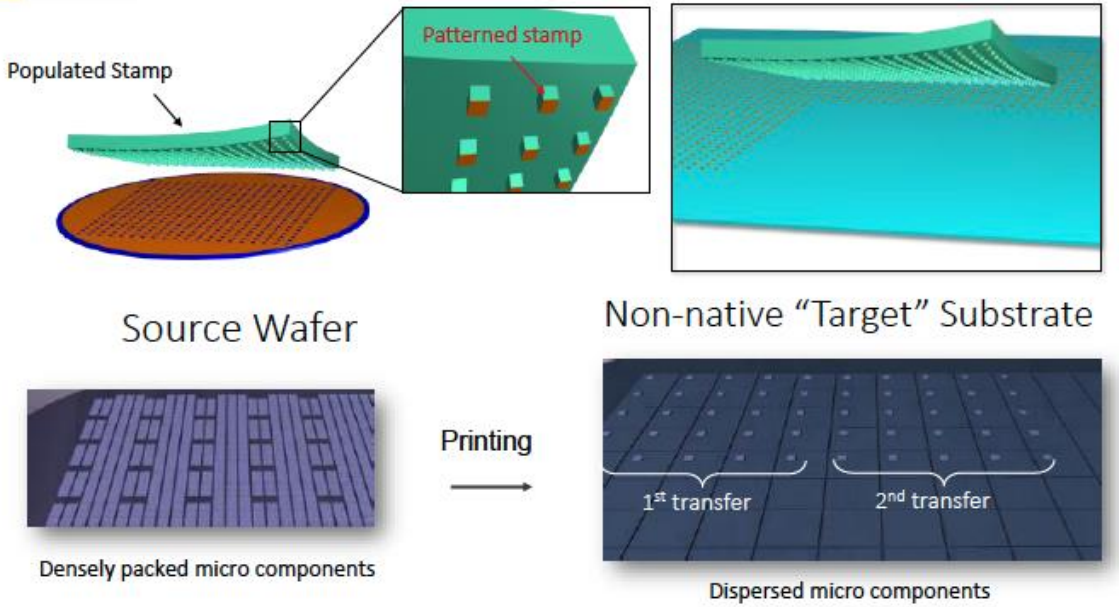
NHANCED SEMICONDUCTORS

5 mm – 2x1 Quilt, Thermal Compressed – 8 µm TSV, 35 µm Pitch - Quilt #: NGQ-5-2615-2410

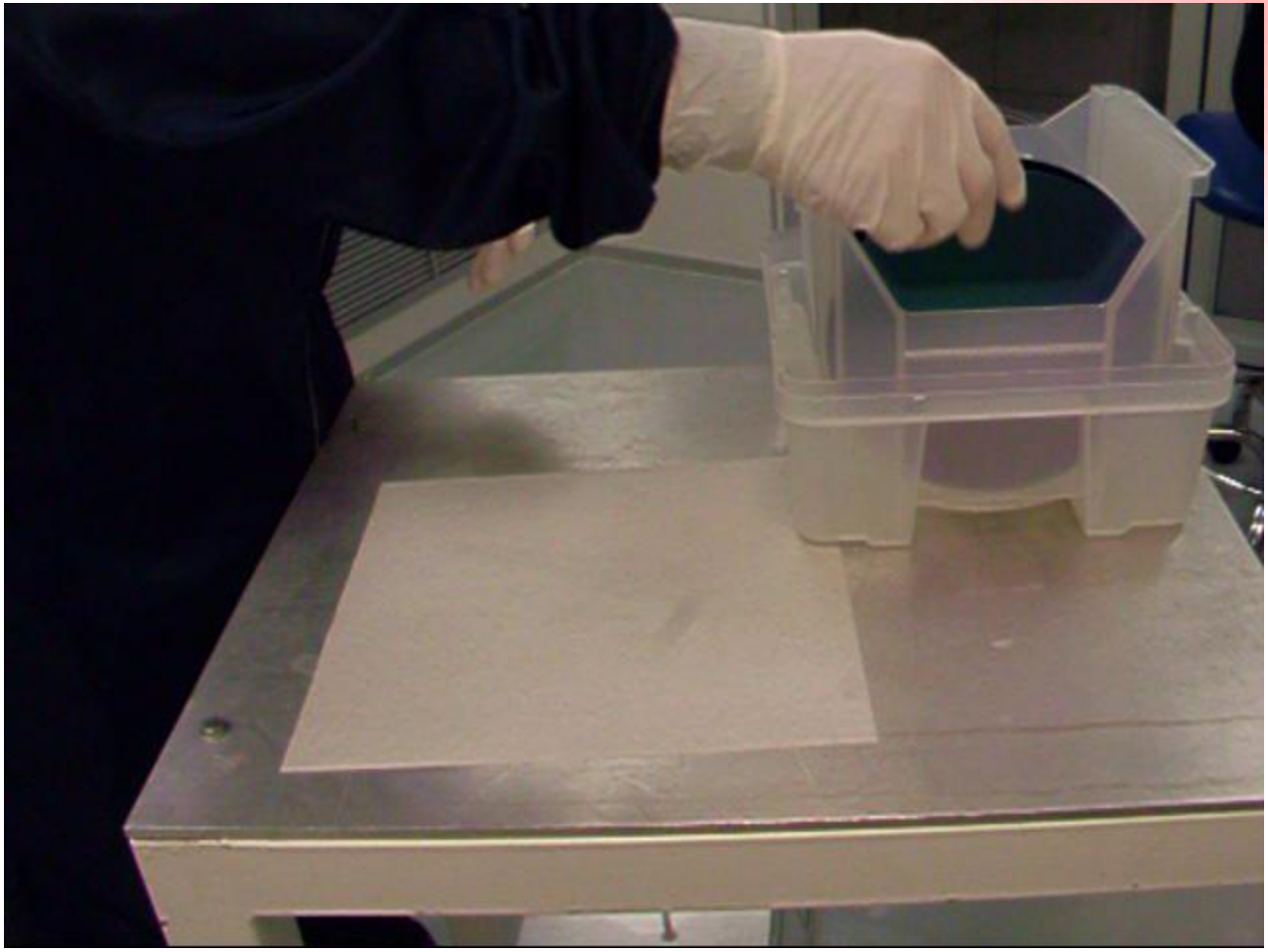


Transfer Printing µChiplet



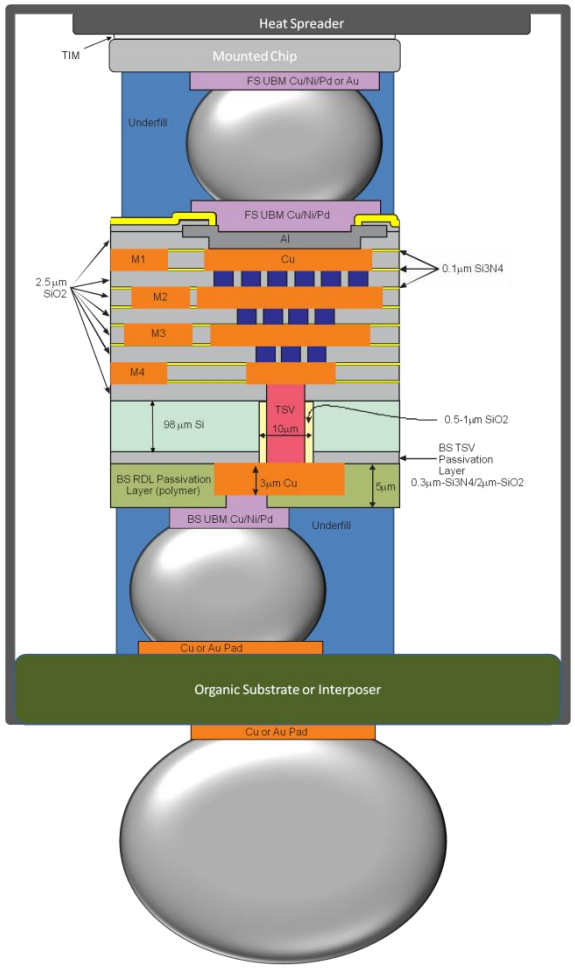


Bonding in Action



THE BAD AND THE UGLY

Supply Chain Complexity



Chiplet Suppliers

Advanced Packaging Manufacturers

- 2.5D
- 3D
- Transfer Printing
- Quilting

Interposer Manufacturers

- Silicon
- Glass
- Organics

Bumping

Pillars

Underfill

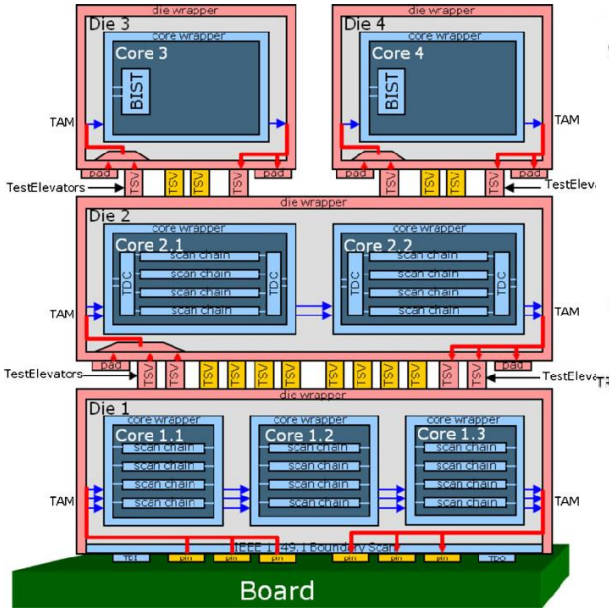
Thermal mitigation

New Singulation Needs

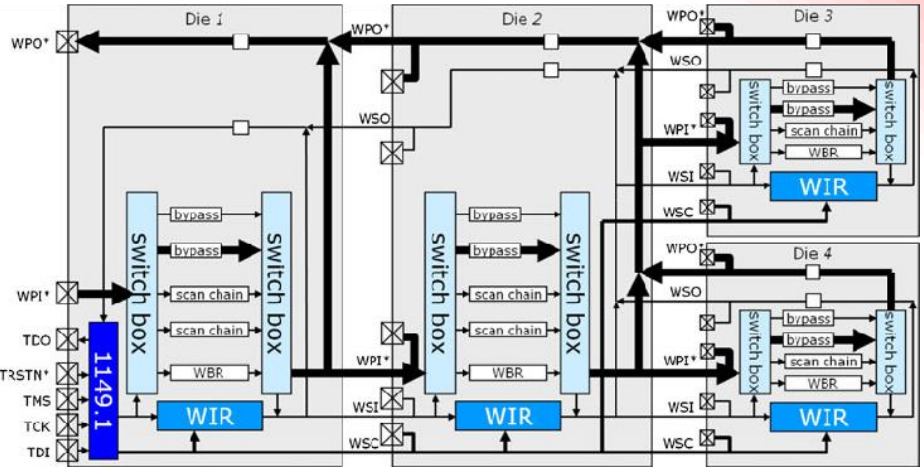
NHANCED SEMICONDUCTORS

Addressing Rel/Qual with DFT + 2.5/3D PCM

Images from: A DfT Architecture for 3D-SICs Based on a Standardizable Die Wrapper; Erik Jan Marinissen et al



Physical

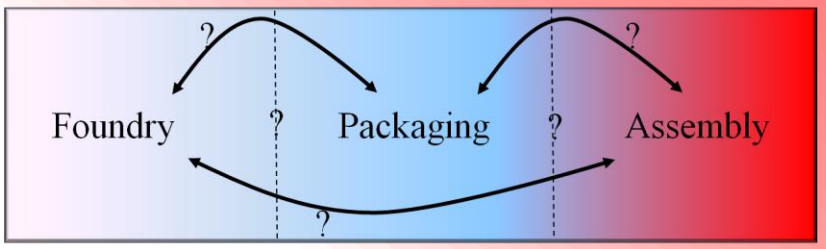


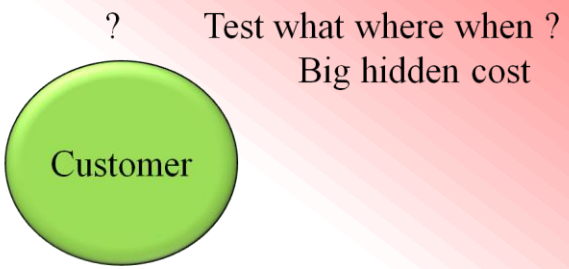
Logical

IEEE 1500 is well defined 2.5/3D DFT starting point building on 1394 standard. Plan is to add 1149.4 analog features targeting device manufacturing integrity.

Augmented JTAG based on IEEE 1500: Add alignment sensing, 3D interconnect R/C measurement, power, temperature, perhaps DARPA SHIELD like items… Being work by NEPP task group with others (NRO, AFRL, Honeywell, Tezzaron, Novati,...) Objective is to "prove" specific device quality and improve reliability data.

Testing





- Significant planning required
- Careful analysis of yield cost
- New methodologies
  - High I/O count requires self-test
  - Deep embedding requires more effort for visibility
- Self Calibrate / Self-repair / Self-redundancy
- Dynamic Self Adjustment

Managing Yield

- Optimizing assembly techniques
- Repair and redundancy

-- New tools

NHANCED SEMICONDUCTORS

The Revolutionary Path Forward

FOUNDRY 2.0

Foundry 1.0 – Todays Model

- Current semiconductor business has been focused on driving smaller transistors.
  - High development cost
  - High capital cost
  - Long development times
  - Expensive design tools
  - High risk
- Twilight of Moore's Law

Foundry 2.0 – New Model

- System solution focus
  - Best of class components
- Relies on Advanced Packaging (AP) and Chiplets
  - Heterogenous integration
  - Photonics
  - MEMS
  - RF
- Advantages
  - Low development cost
  - Low capital cost
  - Short development times
  - Inexpensive design tools
  - Low risk

Foundry 2.0 Opportunities

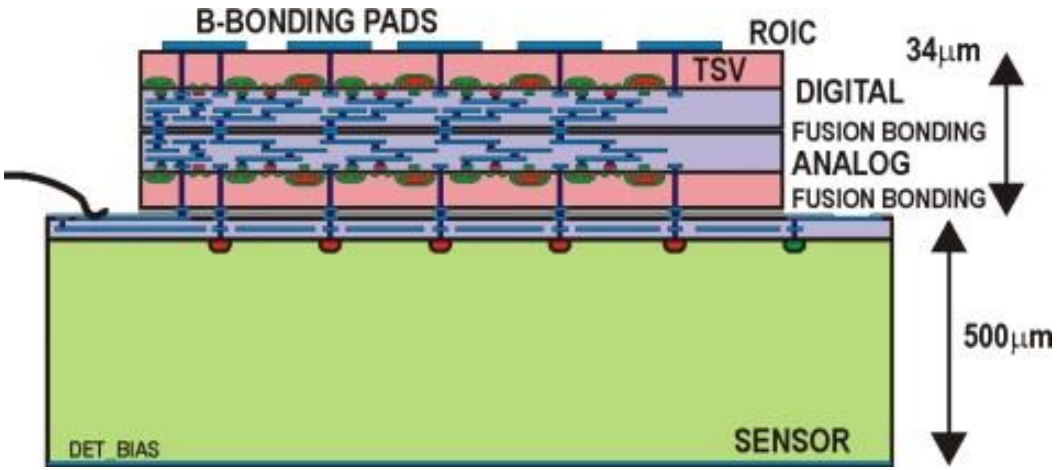
- Low capital costs – New suppliers
  - More than an order of magnitude lower capital costs
- Supports low and medium volume flows – High mix fabrication
  - R&D, startups, large swath of industry
    - More cost effective
  - Competition is FPGAs
    - 10x to 50x lower component cost
- IP centric
  - Knowledge based value
- Complement to Foundry 1.0
  - Partnering
    - Customers, Capital, Pile-on

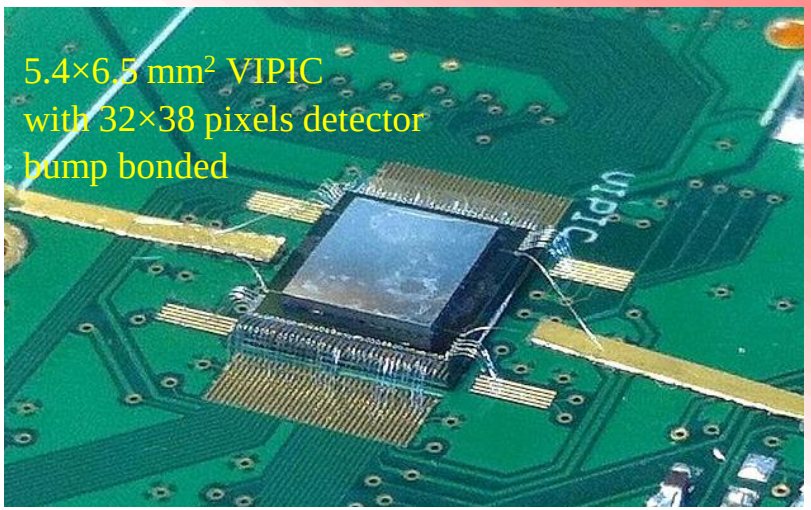
KILLER APPS!

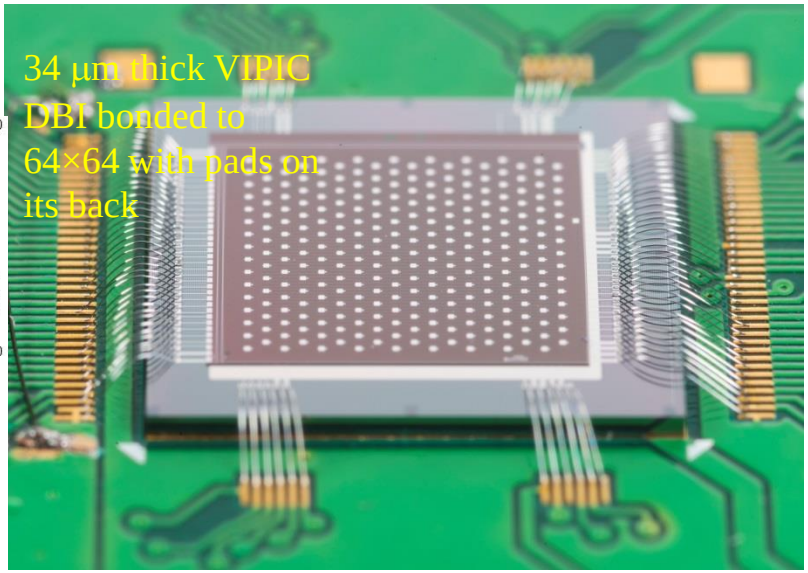
Applications

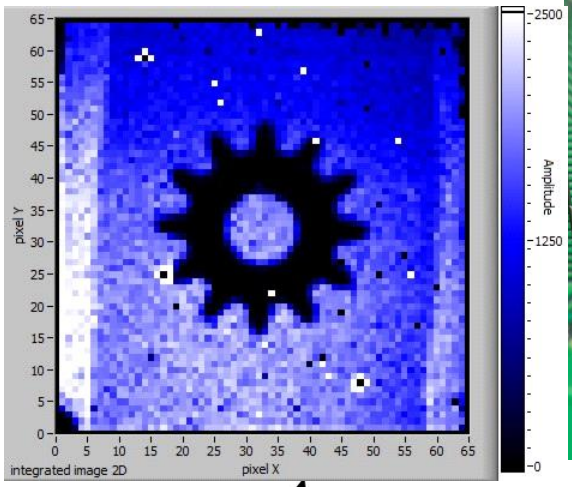
- Photonic Computing
- Integrated Photonic based Communication
- Sensors
- Memory Rich Processing
- RF and Power

Fusion Versus Bump Bonding









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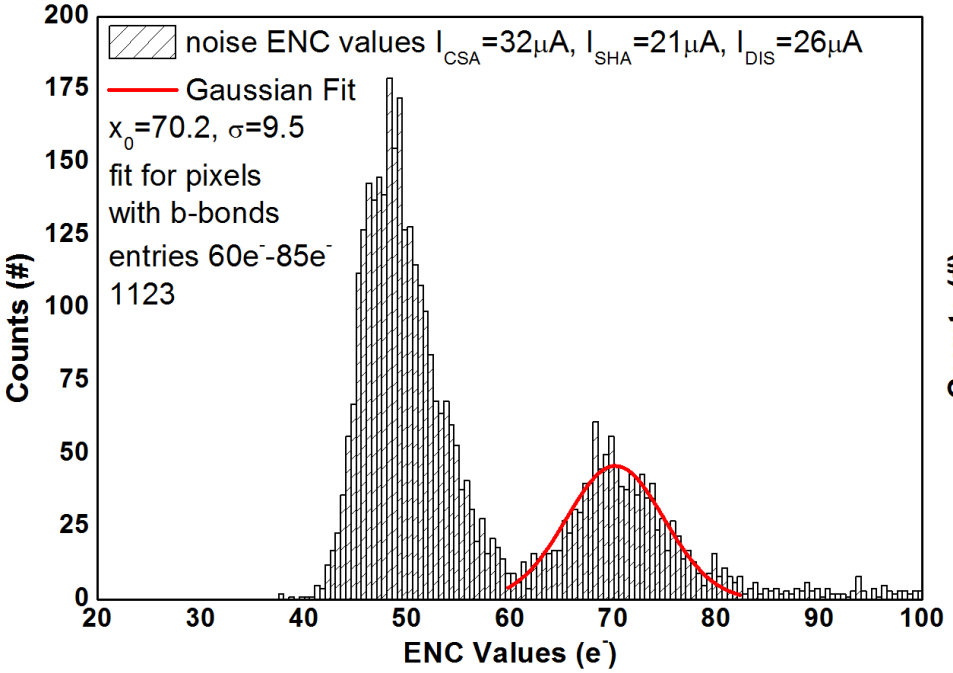
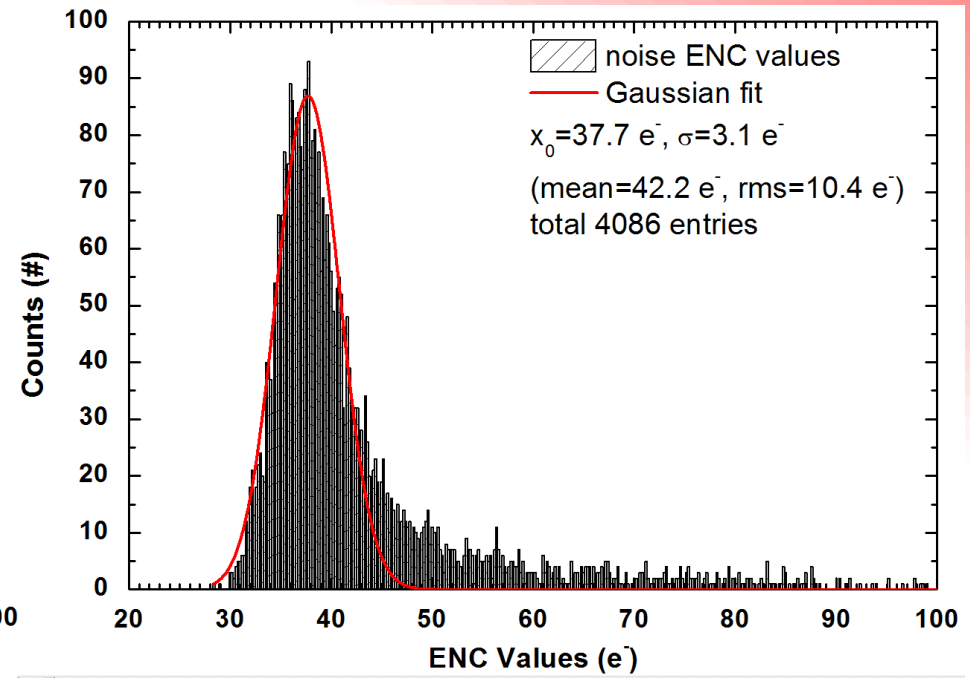
ENC comparison: Bump vs. fusion bond



Bump-bonded VIPIC



Fusion bonded VIPIC

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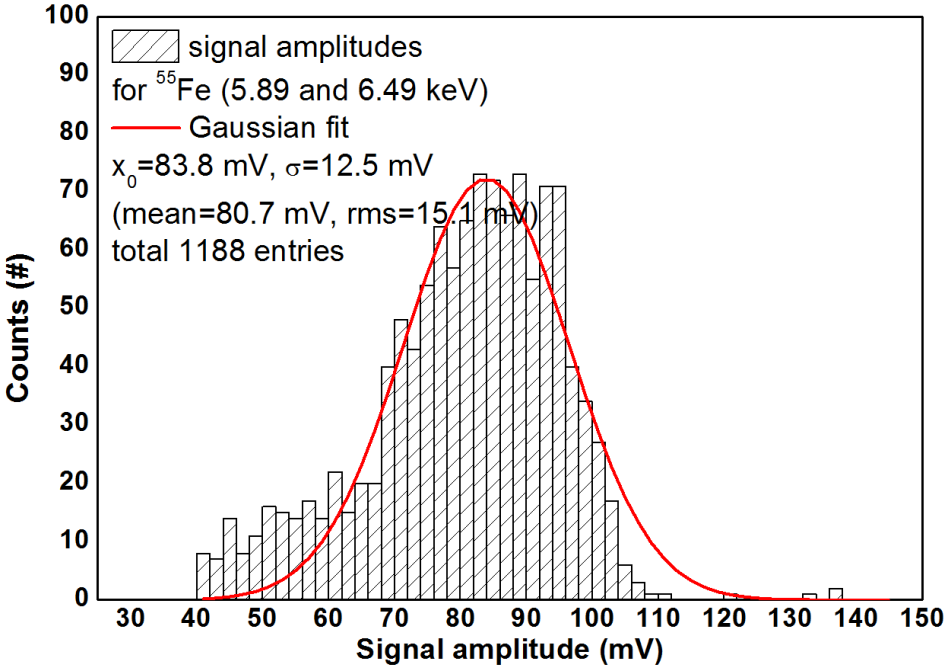
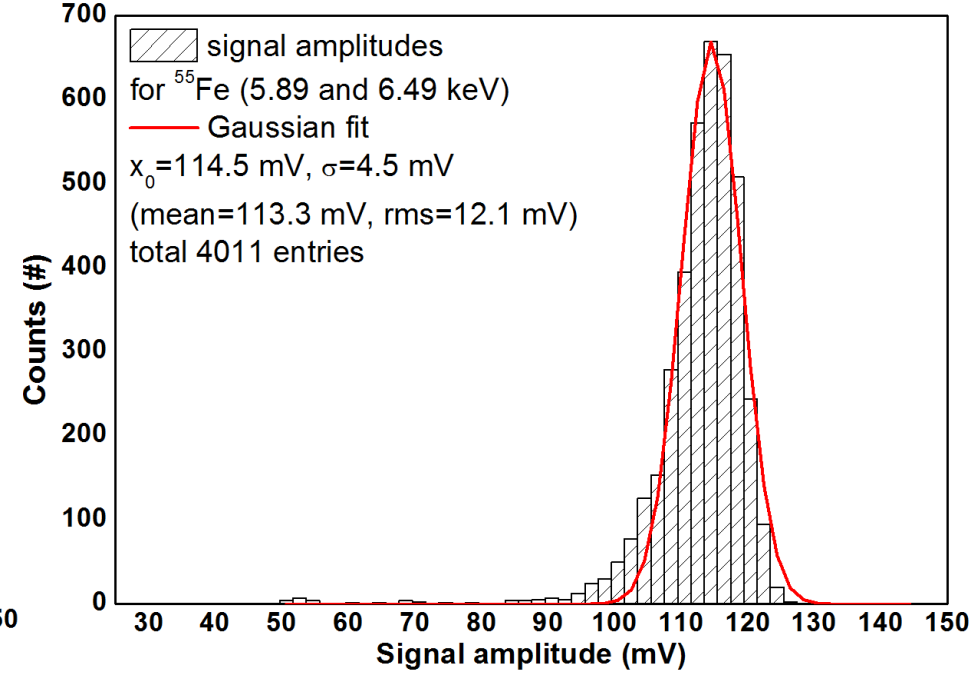
Signal amplitude comparison: Bump vs. fusion bond





Amplitude for bump-bonded VIPIC

Amplitude for fusion bonded VIPIC

Gain is higher for fusion bonded device

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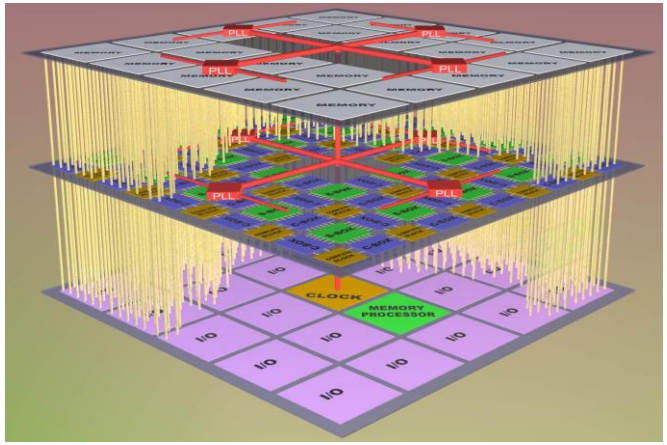
NHANCED SEMICONDUCTORS

Future is Foundry 2.0

- Lower Costs / Higher Performance
  - Manufacturing
  - Development
  - Better Yields
  - Mixed Technologies
  - Mixed Materials
- New design approaches – New opportunities
- Advanced Packaging
  - 2.5D
    - Interposers
      - Glass, Silicon, ?
  - 3D
  - Quilting
  - Transfer Printing



NHANCED SEMICONDUCTORS