FPGA Signal Processing for the Trigger System of a Space High Energy Particle Detector

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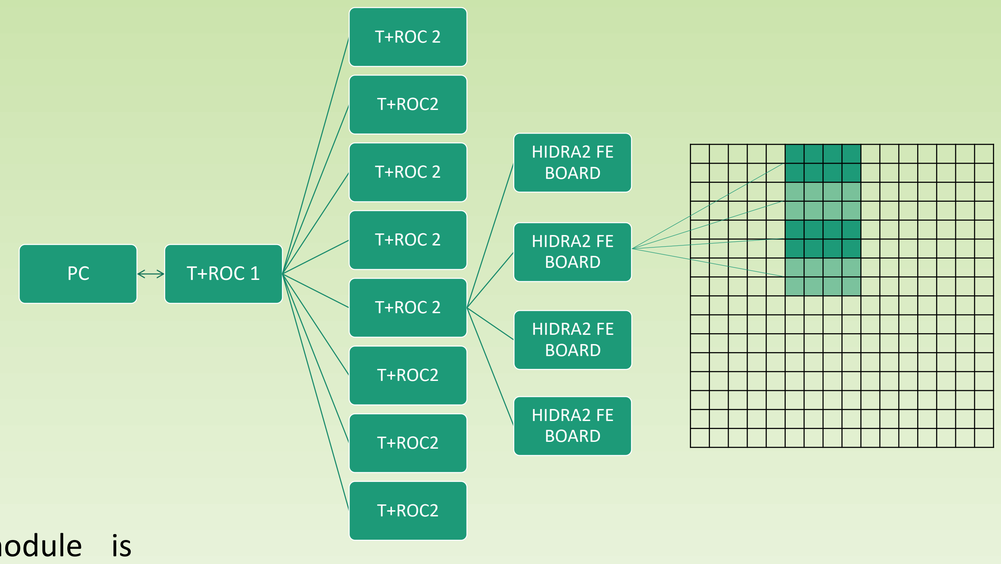
Introduction

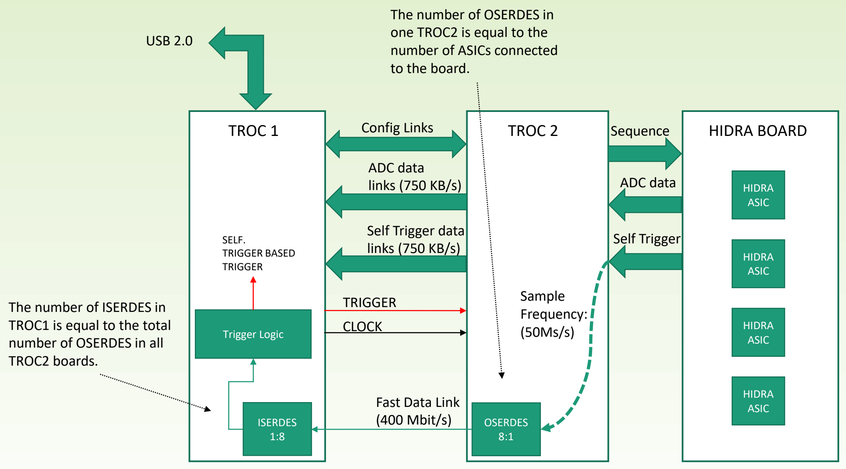
This contribution is focused on the operational concepts and first prototype implementation of an FPGA based trigger system for the operation of a high energy particle detector in space. The main goal of the system is to implement a topological trigger for the calorimeter, which consists of a three dimensional array of scintillating crystals optically coupled to photodiodes. The digital signals for the FPGA processing are obtained by a voltage discrimination applied to the integrated charge from each photodiode in the calorimeter front-end electronics ASIC.

The FPGA system follows a multi-level approach, with a low level that samples the discriminated signals from the front-end ASICs and performs fast data transmission to the trigger level FPGA, which runs the trigger processing algorithms on the three dimensional images generated by the shower of the high energy particle interaction in the detector, in order to perform online identification of interesting events for physics.

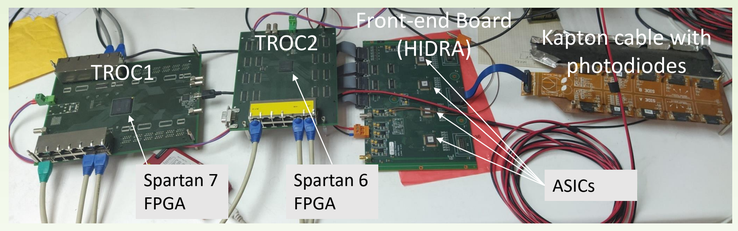
System architecture

The whole surface of the detector is covered with photodiodes, being each group of 8 of them correlated to an ASIC. In every front-end board (named HIDRA), 4 ASICs are integrated, and 4 HIDRA boards converge in every TROC2 (mid-level FPGA) board. Finally, a TROC1 (trigger-level FPGA) board integrates the signal of 8 TROC2 boards. To synchronize the parts of this highly modular system, the clock signal is provided by TROC1 and distributed to all TROC2 boards, being the uncertainty between clock phases at reception below 2 ns.



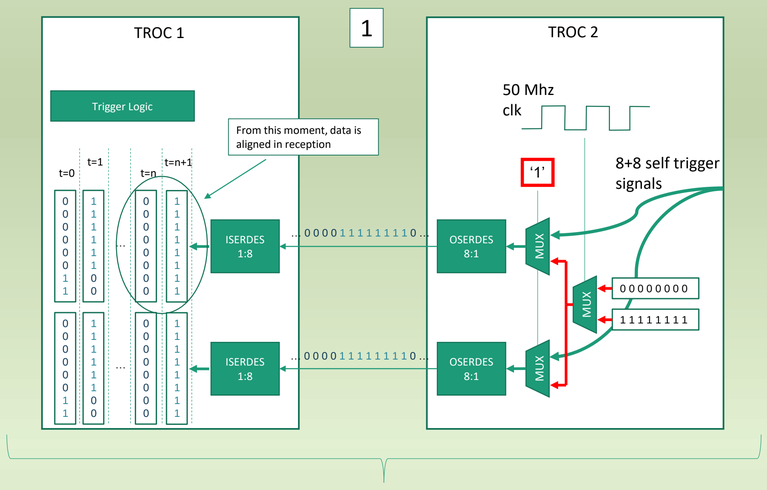


In TROC2, one OSERDES module is instantiated for each ASIC used in the system. This modules perform a parallel to serial conversion of each ASIC one-byte self trigger output (sampled at 50 Ms/s) and send the sequence to TROC1 through a LVDS line at 400 Mbit/s. Analogously, ISERDES modules are instantiated in TROC1 to deserialize self trigger data back to its original shape of on byte per ASIC, thus being ready to be used simultaneously in the trigger logic module.

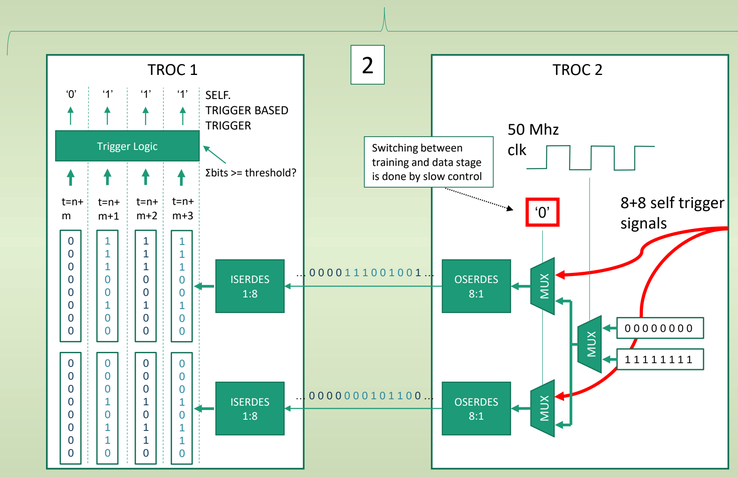


Implementation

In order to have an efficient trigger system, self trigger data must be properly aligned before being processed in the trigger logic module (ensuring that each byte regenerated at TROC1 is equal to the original byte at the output of the corresponding ASIC). To achieve that alignment, a two-stage system has been designed:



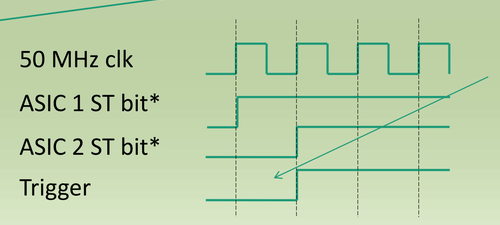
In the **data stage**, self trigger data from ASICs is sent to the OSERDES inputs. As the output of all ISERDES is now time aligned, each byte received in TROC1 corresponds unequivocally to a self trigger byte. All these bytes are sent to the trigger logic module at TROC1, where the state of the whole detector is evaluated every clock cycle and the trigger is activated if the logic conditions are met.



In the **training stage**, the OSERDES input is not self trigger data but an internally generated byte whose value oscillates between x"00" and x"FF" each clock cycle. TROC1 expects this pattern, so it slips the received sequence one bit every time that they do not match. Once the pattern is correctly received, TROC1 stops the bit-slipping and is ready to receive data.

What about synchronization between bytes from different ASICs?

No additional alignment system is required since self trigger signals are latch type: once activated, the time that they remain in high state is much higher than the temporal uncertainty of the system.



Trigger delay of 20 ns in a worst-case scenario, totally affordable for the system.

*At ISERDES output

Future work

Here are some of the main future research lines for this project:

- Evaluate FPGA technologies for space operation. Xilinx Spartan FPGAs will be replaced by suitable for space FPGAs (as Microsemi rad-tolerant models) that we still have to evaluate.
- Define number of bytes per link. Now we are sending each serialized byte through its own LVDS line, but, as the number of pins in TROC1 FPGA is limited, we are working on an new design to send bytes from several ASICs through the same line.
- New trigger processing logic. We are working on more complex logic schemes as the computation of XYZ axis projections for online recognition of electromagnetic shower image patterns to trigger the detector.

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