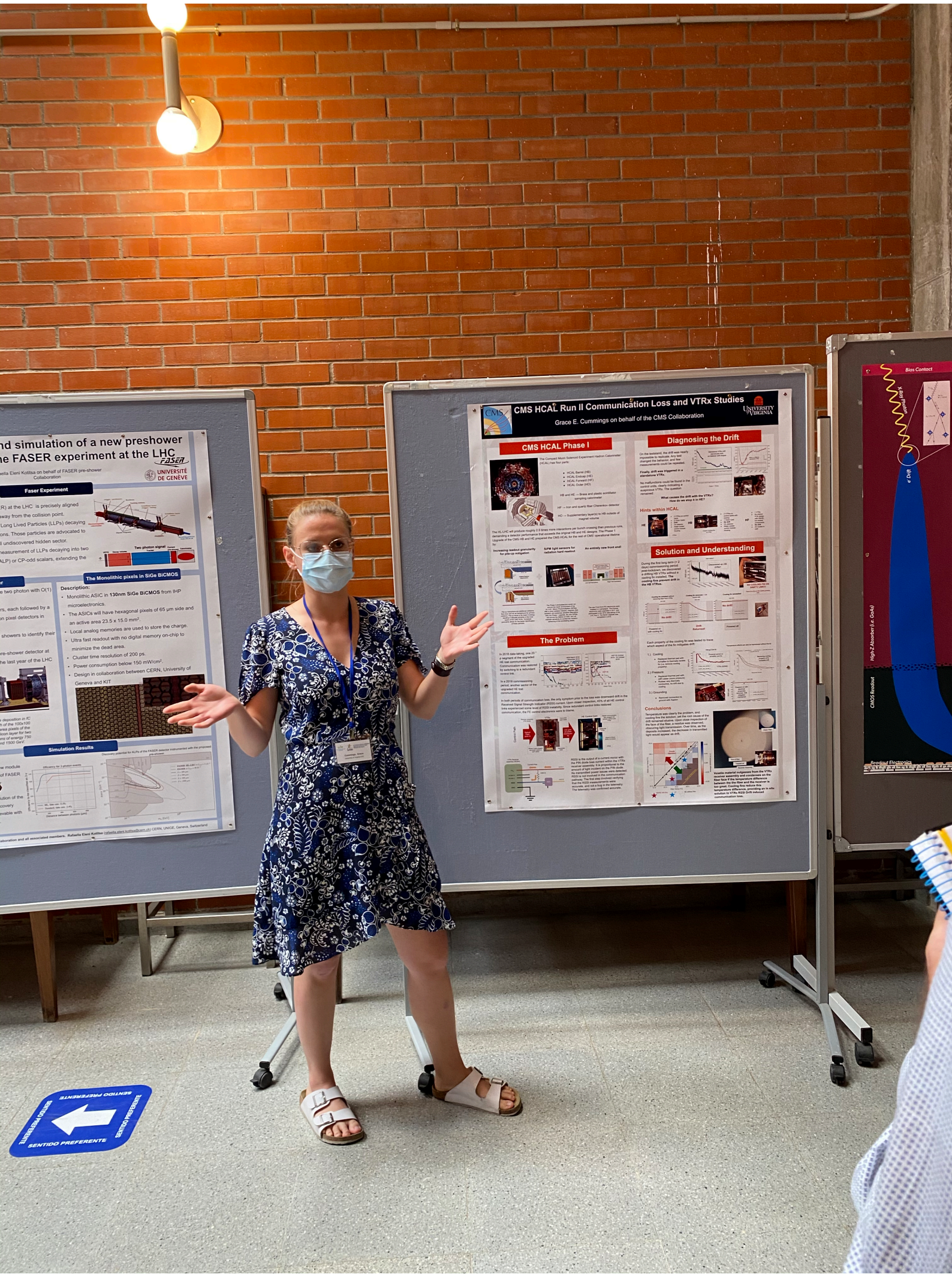
nd simulation of a new preshower
he FASER experiment at the LHC
FASER
UNIVERSITÉ DE GENÈVE
Faser Experiment
The Monolithic pixels in SiGe BiCMOS
Description:
Monolithic ASIC in 130nm SiGe BiCMOS from IHP microelectronics.
The ASICs will have hexagonal pixels of 65 µm side and an active area 23.5 x 15.0 mm².
Local analog memories are used to store the charge.
Ultra fast readout with no digital memory on-chip to minimize the dead area.
Cluster time resolution of 200 ps.
Power consumption below 150 mW/cm².
Design in collaboration between CERN, University of Geneva and KIT
Simulation Results
CMS HCAL Run II Communication Loss and VTRx Studies
Grace E. Cummings on behalf of the CMS Collaboration
UNIVERSITY of VIRGINIA
CMS HCAL Phase I
Diagnosing the Drift
Hints within HCAL:
Solution and Understanding
The Problem
Conclusions
Bias Contact
X-ray Photon
e⁻ Drift
High-Z Absorber (i.e. GaAs)
CMOS Readout
Readout Electronics
SENTIDO PREFERENTE