A real time sub-picosecond phase correction system

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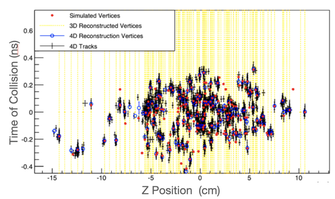
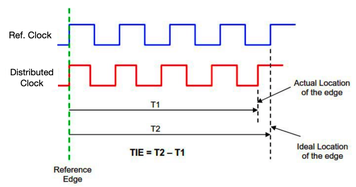
The Need for Precision Timing

The use of precision timing to measure time-of-flight or to distinguish events from the same bunch crossing in collider detectors has become a common feature of many modern experiments. These experiments are pushing the boundaries of timing measurements to improve background suppression and other precision measurements.



(a) HL-LHC:CMS Simulation of reconstructed vertices with 140 Pile Up Events per Bunch Crossing. Here, vertices which are overlapping in position can be resolved using the timing information on the y-axis



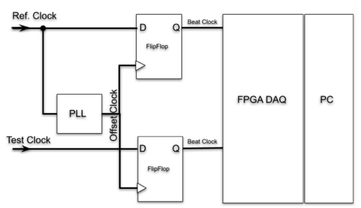
(b) Time Interval Error (TIE) is a metric useful for quantifying the stability of a distributed clock. It is defined as the time deviation of a real clock edge w.r.t the ideal clock edge.

An integral component of a precise timing detector is a stable clock that can be distributed to all the detector elements which are spatially separated.

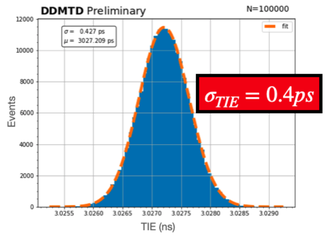
We introduce a system capable of measuring the slow frequency wander of a distributed clock and correcting for it in real time with sub-picosecond precision which can be used to enhance the stability of the distributed clock

Measuring Time Interval Error with Sub-picosecond Precision

Sub-picosecond measurements of the TIE between two clocks can be made using a Digital Dual Mixer Time Difference Circuit (DDMTD). The reference and the clock under test are heterodyned using two high-performance d-type flip-flops.



(a) Schematic of the DDMTD Circuit



(b) DDMTD noise-floor measurement made on a 160MHz clock coming out of a Si5344 Jitter-Attenuator.

Theoretical Precision of the DDMTD Circuit

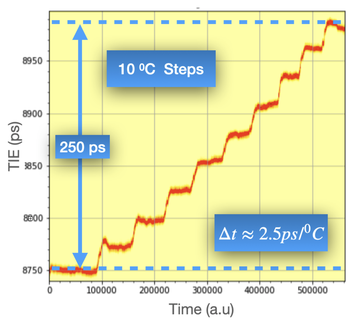
DDMTD performance depends on the frequency of the input clocks, and the heterodyne offset parameter N. With $f_{ref} = 160MHz$, and $N = 100k$ we get a theoretical precision of:

$$f_{offset} = \frac{N}{N+1} f_{ref}, \quad \Delta t_{min} = \frac{1}{N.f_{ref}}$$

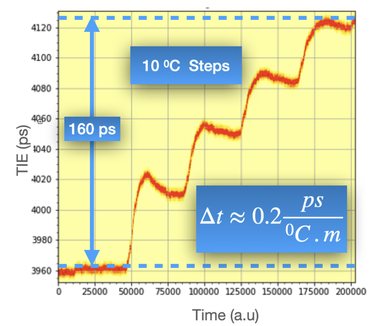
$$\Delta t_{min} = 62.5fs$$

Envrionmental Effects on the Clock

Envrionmental effects, such as temperature can introduce wander in the distributed clock. The propagation time changes by 20 ps/^{0}C for 100m of multi-mode optical fiber. To keep track of this low frequency wander and DDMTD offers sub-picosecond precision.



(a) Front-End in Climate Chamber

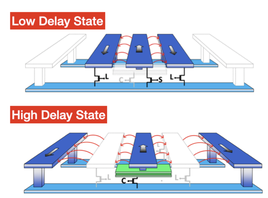


(b) Optical Fiber in climate Chamber

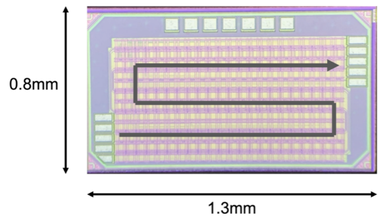
Figure 3. Temperature effects on a 40MHz clock that is distributed to the FE Electronics measured by the DDMTD Circuit. The temperature in the climate chamber was increased in steps of 10^{0}C and this corresponds to the steps in the figure. These measurements were taken at the HPTD Lab in CERN with the help of E. B. S. Mendes et. al.

Correcting Drifts of the Clock in Real Time

We have introduced a system capable of measuring the drifts in a clock with sub-picosecond precision. To correct the measured wander in the clock, we have designed and developed an ASIC capable of shifting the phase with sub-picosecond precision.



(a) 3D Structure of the delay unit



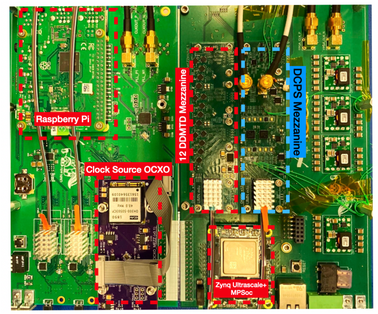
(b) Layout of the 66 delay units daisy-chained in the ASIC

Figure 4. Structures of the DCPS ASIC that was developed in-house and fabricated using the TSMC 65nm CMOS process

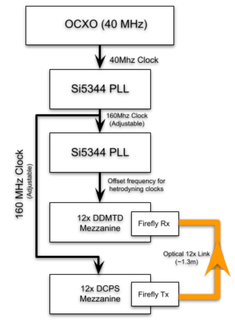
The Digitally Controlled Phase Shifter (DCPS) ASIC was fabricated using the TSMC 65nm CMOS process. It consists of 66 delay cells daisy-chained together. The unit cell of the DCPS is a coplanar wave-guide with ground return lines. Each cell can be set into a 'High-Delay' state or 'Low-Delay' state, with a difference of the delay of 200fs. The chip was wire-bonded onto a mezzanine card mounted on a custom board that distributes the clock through the DCPS and measures the TIE of the return signal using the DDMTD Circuit.

DCPS-DDMTD Test Board

The clock source is an oven-controlled crystal oscillator connected directly to an Si5344 Jitter Attenuator. The clock is distributed through the DCPS to a 12-channel Samtec Tx Firefly. The return signal is received by SAMTEC Rx Firefly, and the DDMTD is used for TIE measurements. A Zynq Ultrascale+ FPGA is use to collect the data and a Raspberry Pi is used for setup and control.



(a) DCPS-DDMTD Test Board



(b) DCPS-DDMTD Schematic

Measurements and Results

Delay measurements were made by activating the delay steps of the ASIC cumulatively (in steps of 8 units), and measuring the TIE between the distributed clock and the reference clock using the DDMTD. This was done for different carrier frequencies and we observed a consistent slope of 200fs/step.

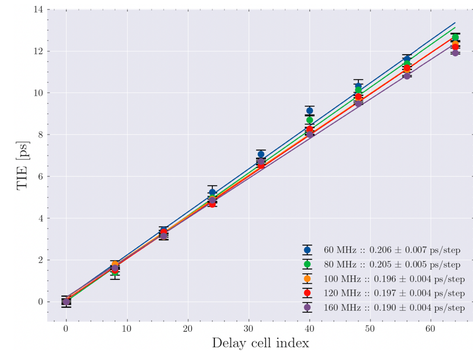


Figure 6. DCPS Response to different frequencies of clocks

References

[1] E. B. S. Mendes, S. Baron, R Rusack, R Saradhy, M. O. Sahin, and I. Mandjavidze. Timing week with cms pure timing link distribution teams, 2019. Rev. 1.0.

[2] P. Moreira and Izzat Darwazeh. Digital femtosecond time difference circuit for cern ' s timing system. 2011.

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