RD53B Single Chip Card

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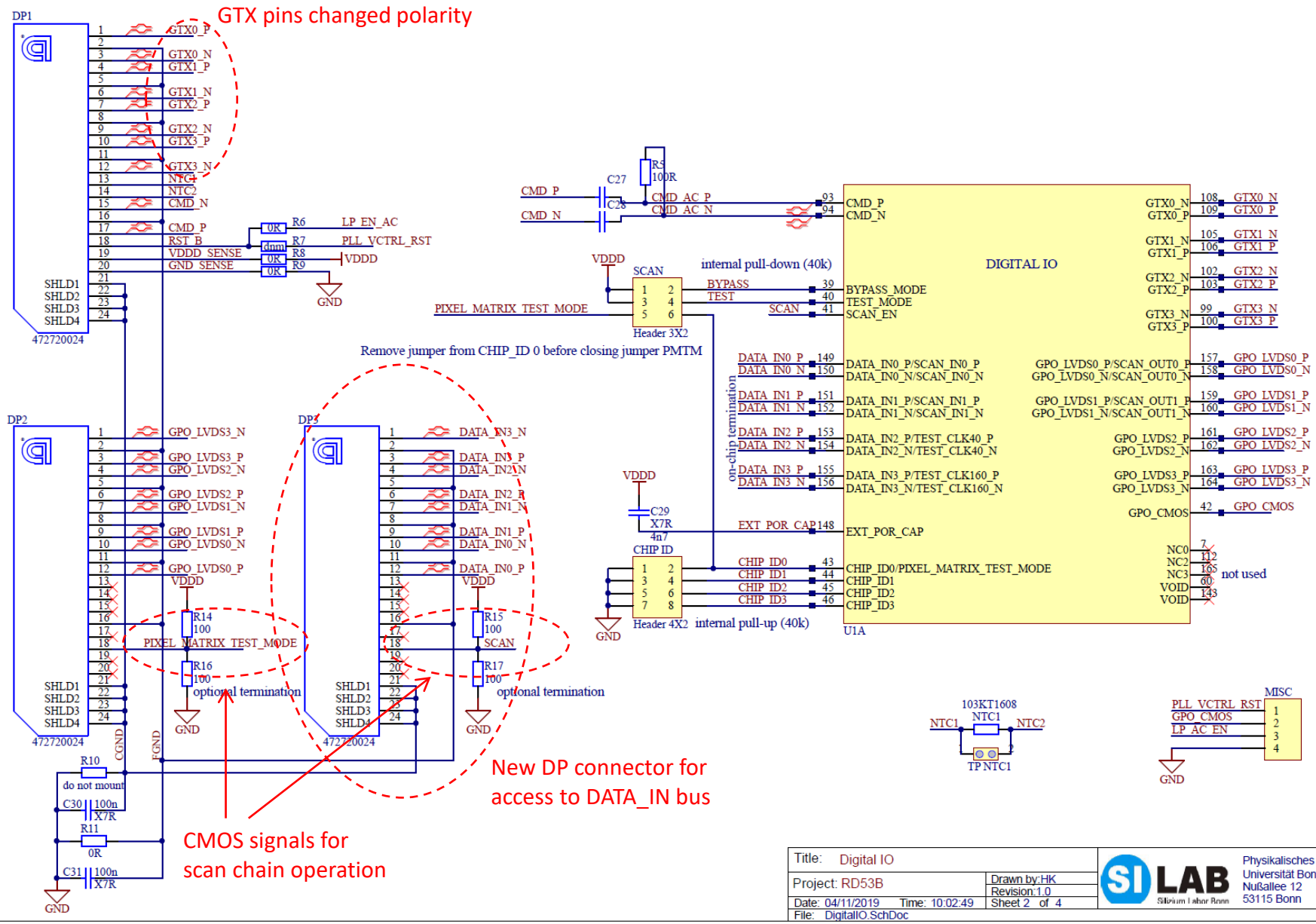
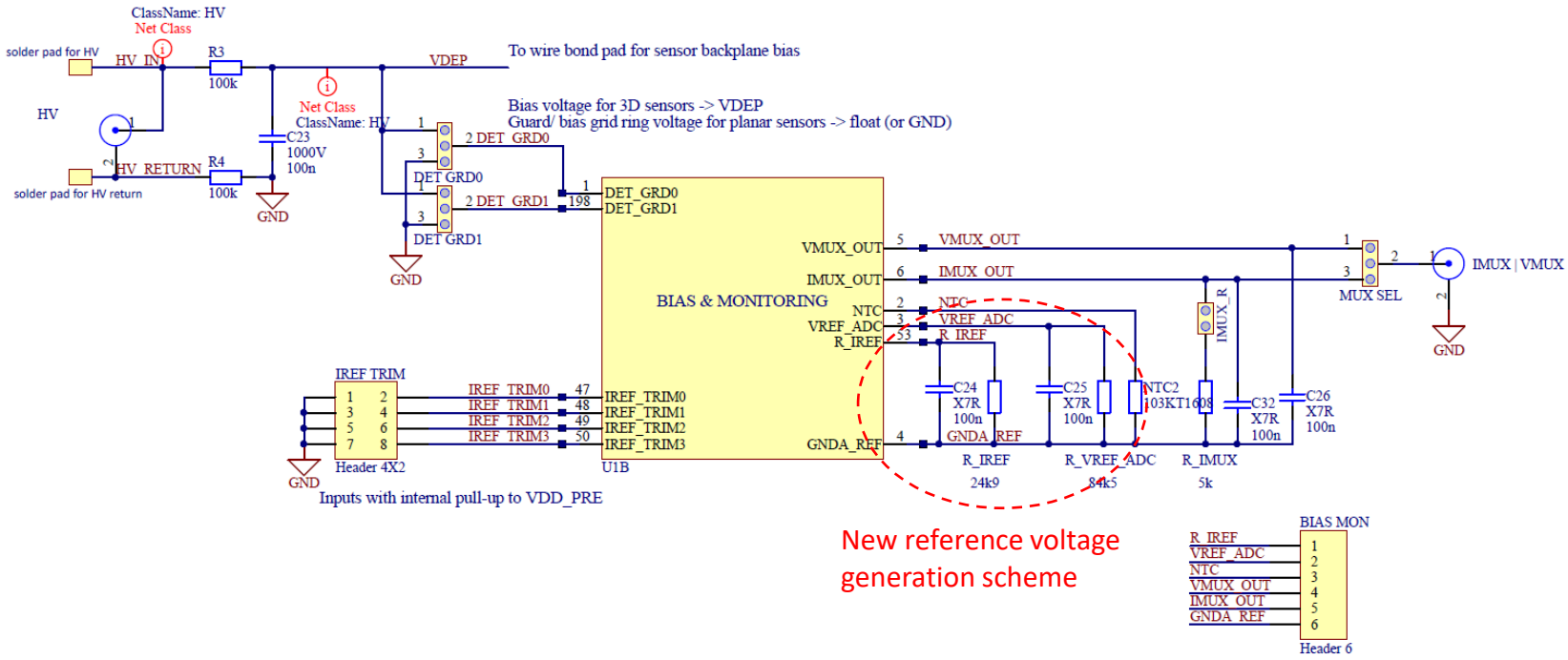
RD53B IO Changes

- Digital
  - Added DATA_IN[3:0] input (LVDS) for on-chip data aggregation
    - 100 Ohm on-chip termination
    - Dual mode: scan chain inputs during scan chain mode
  - Chip ID inputs
    - Added fourth address bit
    - Changed to internal pull-up resistors
  - HITOR outputs renamed GPO_LVDS
  - STATUS CMOS output renamed GPO_CMOS
  - GTX lanes swapped polarity (mirrored in layout)
  - Scan chain functionality (dedicated pads + dual mode pads)
    - CMOS inputs: TEST_MODE, SCAN_EN, PIXEL_MATRIX_TEST_MODE (CHIP_ID3)
    - LVDS inputs (DATA_IN): SCAN_IN[1:0], TEST_CLK40, TEST_CLK160
    - LVDS outputs (GPO_LVDS): SCAN_OUT[1:0]
  - In BYPASS_MODE: EXT_CMD_CLK, EXT_SER_CLK via DATA_IN bus
  - Removed pads:
    - EXT_TRIGGER, INJ_STRB[1:0], POR_OUT_B, EXT_CMD_CLK, EXT_SER_CLK
    - JTAG signals
    - PLL_VCTRL (generated internally)


GTX pins changed polarity
DP1
GTX0_P
GTX0_N
GTX1_P
GTX1_N
GTX2_P
GTX2_N
GTX3_P
GTX3_N
NTC1
NTC2
CMD_N
CMD_P
RST_B
VDDD_SENSE
GND_SENSE
R6 0R LP_EN_AC
R7 dnm PLL_VCTRL_RST
R8 0R VDDD
R9 0R
GND
SHLD1
SHLD2
SHLD3
SHLD4
472720024
DP2
GPO_LVDS3_N
GPO_LVDS3_P
GPO_LVDS2_N
GPO_LVDS2_P
GPO_LVDS1_N
GPO_LVDS1_P
GPO_LVDS0_N
GPO_LVDS0_P
VDDD
R14 100
PIXEL_MATRIX_TEST_MODE
R16 100
optional termination
GND
DP3
DATA_IN3_N
DATA_IN3_P
DATA_IN2_N
DATA_IN2_P
DATA_IN1_N
DATA_IN1_P
DATA_IN0_N
DATA_IN0_P
VDDD
R15 100
SCAN
R17 100
optional termination
GND
CGND
FGND
R10 do not mount
C30 100n X7R
R11 0R
C31 100n X7R
GND
CMD_P
CMD_N
C27
C28
R5 100R
CMD_AC_P
CMD_AC_N
VDDD
SCAN
PIXEL_MATRIX_TEST_MODE
Header 3X2
internal pull-down (40k)
BYPASS
TEST
SCAN
Remove jumper from CHIP_ID 0 before closing jumper PMTM
DIGITAL IO
BYPASS_MODE
TEST_MODE
SCAN_EN
on-chip termination
DATA_IN0_P
DATA_IN0_N
DATA_IN1_P
DATA_IN1_N
DATA_IN2_P
DATA_IN2_N
DATA_IN3_P
DATA_IN3_N
DATA_IN0_P/SCAN_IN0_P
DATA_IN0_N/SCAN_IN0_N
DATA_IN1_P/SCAN_IN1_P
DATA_IN1_N/SCAN_IN1_N
DATA_IN2_P/TEST_CLK40_P
DATA_IN2_N/TEST_CLK40_N
DATA_IN3_P/TEST_CLK160_P
DATA_IN3_N/TEST_CLK160_N
EXT_POR_CAP
CHIP_ID0
CHIP_ID1
CHIP_ID2
CHIP_ID3
CHIP_ID0/PIXEL_MATRIX_TEST_MODE
GTX0_N
GTX0_P
GTX1_N
GTX1_P
GTX2_N
GTX2_P
GTX3_N
GTX3_P
GPO_LVDS0_P/SCAN_OUT0_P
GPO_LVDS0_N/SCAN_OUT0_N
GPO_LVDS1_P/SCAN_OUT1_P
GPO_LVDS1_N/SCAN_OUT1_N
GPO_LVDS2_P
GPO_LVDS2_N
GPO_LVDS3_P
GPO_LVDS3_N
GPO_CMOS
NC0
NC2
NC3
VOID
VOID
not used
U1A
VDDD
C29 X7R 4n7
CHIP ID
Header 4X2
internal pull-up (40k)
GND
103KT1608
NTC1
NTC2
TP NTC1
MISC
PLL_VCTRL_RST
GPO_CMOS
LP_AC_EN
GND
New DP connector for access to DATA_IN bus
CMOS signals for scan chain operation
Title: Digital IO
Project: RD53B
Drawn by:HK
Revision:1.0
Date: 04/11/2019 Time: 10:02:49
Sheet 2 of 4
File: DigitalIO.SchDoc
SI LAB Silicium Labor Bonn
Physikalisches Institut
Universität Bonn
Nußallee 12
53115 Bonn

RD53B IO Changes

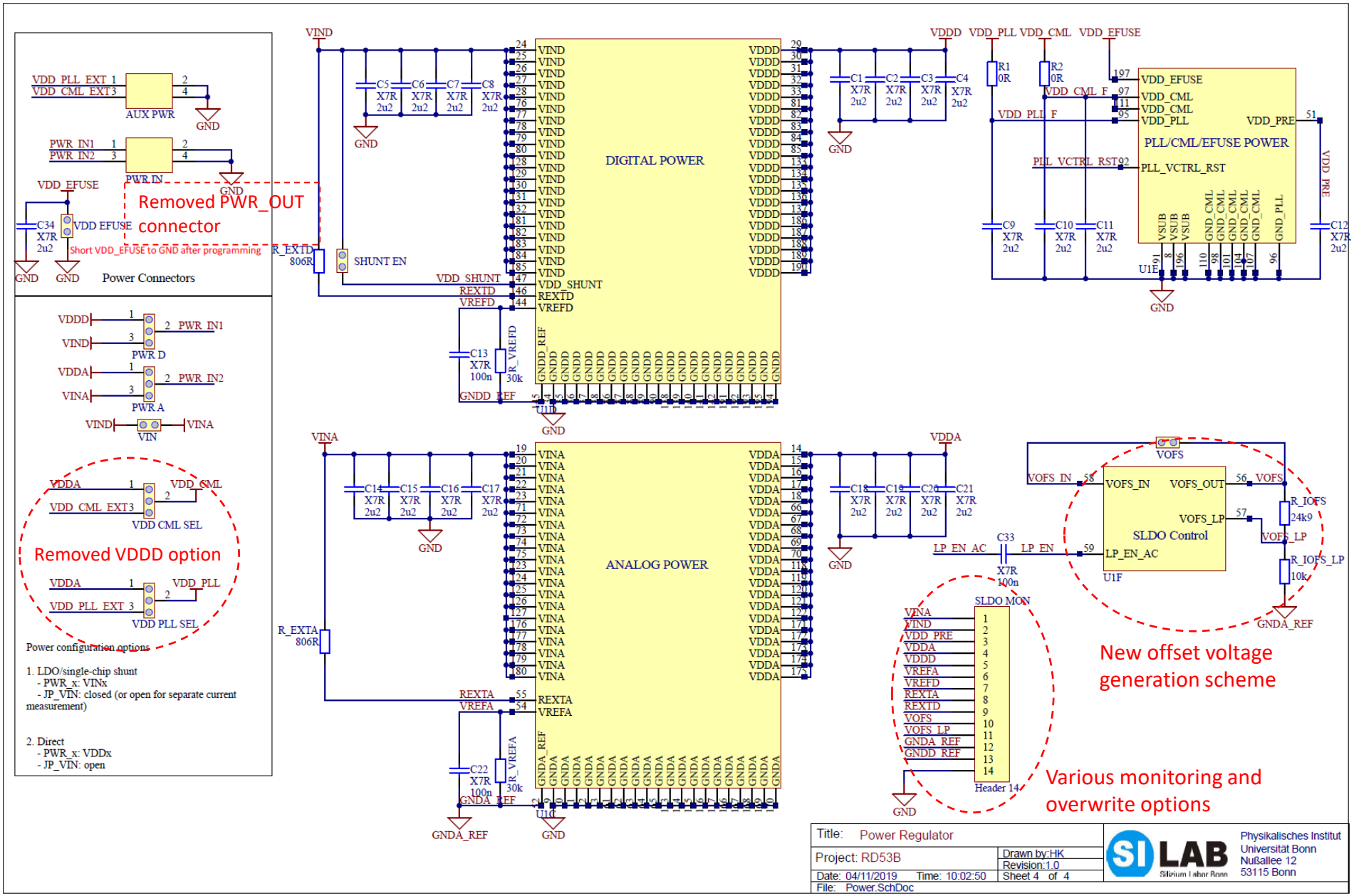
- Bias & Monitoring
  - Voltage reference generation with external
    - VREF_IREF = 20µA * R_IREF
    - VREF_ADC = 10µA * R_VREF_ADC
  - Added pad for VDD_PRE (new in RD53B) decoupling
  - Readout of external NTC
    - internal current DAC + connection to monitoring ADC
  - Added pull-ups to VDD_PRE for IREF_TRIM inputs
  - No more Top_Row pads



Title: Analog IO		Physikalisches Institut Universität Bonn Nußallee 12 53115 Bonn
Project: RD53B	Drawn by:HK Revision:1.0	
Date: 04/11/2019 Time: 10:02:50	Sheet 3 of 4	
File: AnalogIO.SchDoc		

RD53B IO Changes

- Powering
  - Voltage reference generation with external resistors
    - VREF_[A/D] = 20µA * R_VREF[A/D]
  - Common VOFS for analog & digital
  - Common VDD_SHUNT for analog & digital
  - Added GND_REF (ground sense) to analog and digital bias blocks
  - Added 5th VIN pad per regulator group
  - Removed:
    - Internal current setting resistor (SLDO_RINT)
    - Conf. SLDO compensation (SLDO_COMP_EN_B)
    - Bandgap start-up overwrite (SLDO_POR_BG)
  - Separate VOFS output and input pads (averaging of VOFS for multiple chips)
  - Added VOFS_LP to connect second resistor for low power mode offset setting
  - Added LP_AC_EN to connect ac-signal for LP mode activation
  - Added VDD_EFUSE pad for E-fuse programming (2.5V during programming, short to GND for normal operation)


Power Connectors
Removed PWR_OUT connector
Short VDD_EFUSE to GND after programming
Removed VDDD option
Power configuration options
1. LDO/single-chip shunt
- PWR_x: VINx
- JP_VIN: closed (or open for separate current measurement)
2. Direct
- PWR_x: VDDx
- JP_VIN: open
DIGITAL POWER
ANALOG POWER
PLL/CML/EFUSE POWER
SLDO Control
SLDO MON
New offset voltage generation scheme
Various monitoring and overwrite options
Title: Power Regulator
Project: RD53B
Drawn by:HK
Revision:1.0
Date: 04/11/2019 Time: 10:02:50
Sheet 4 of 4
File: Power.SchDoc
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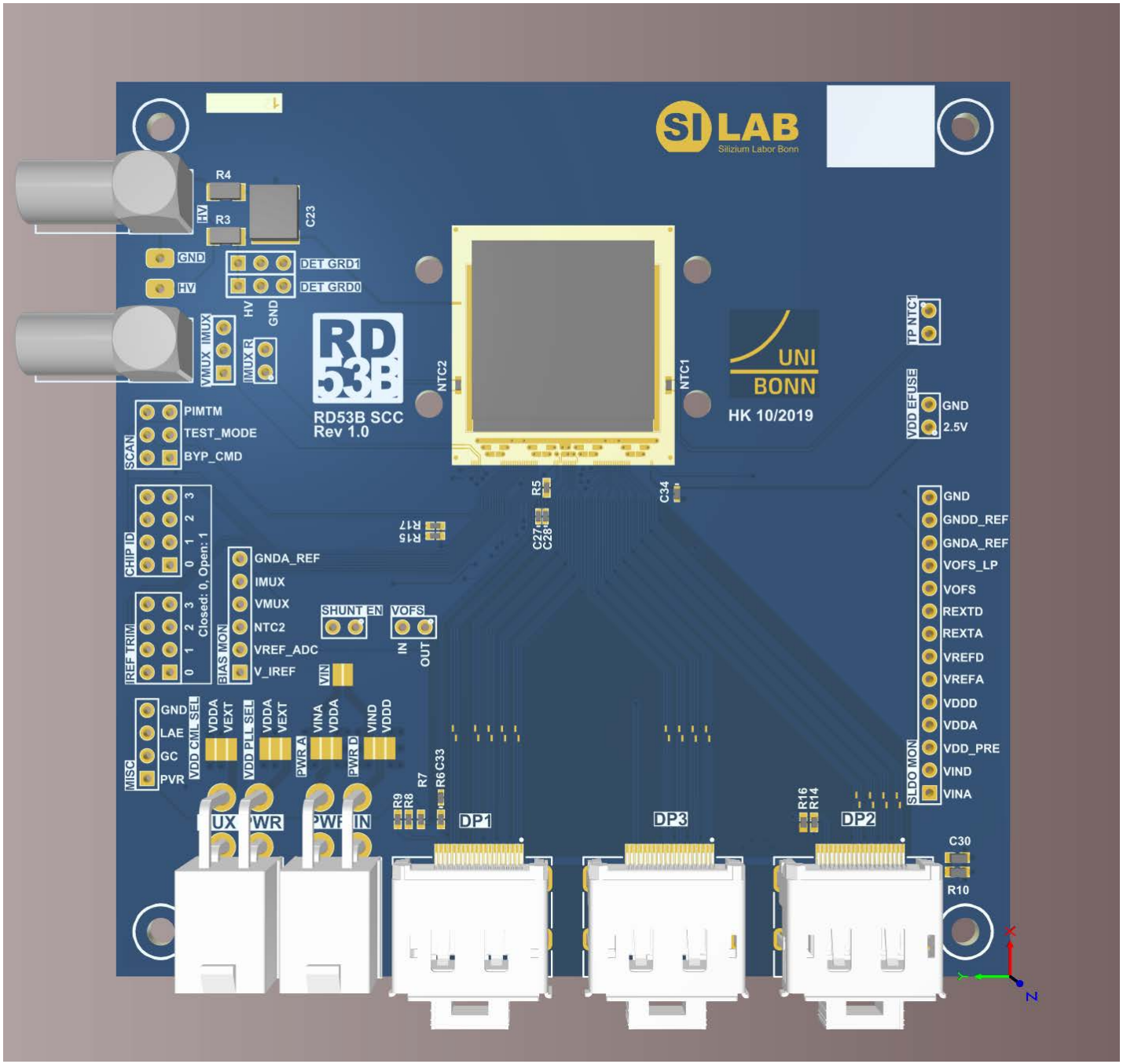
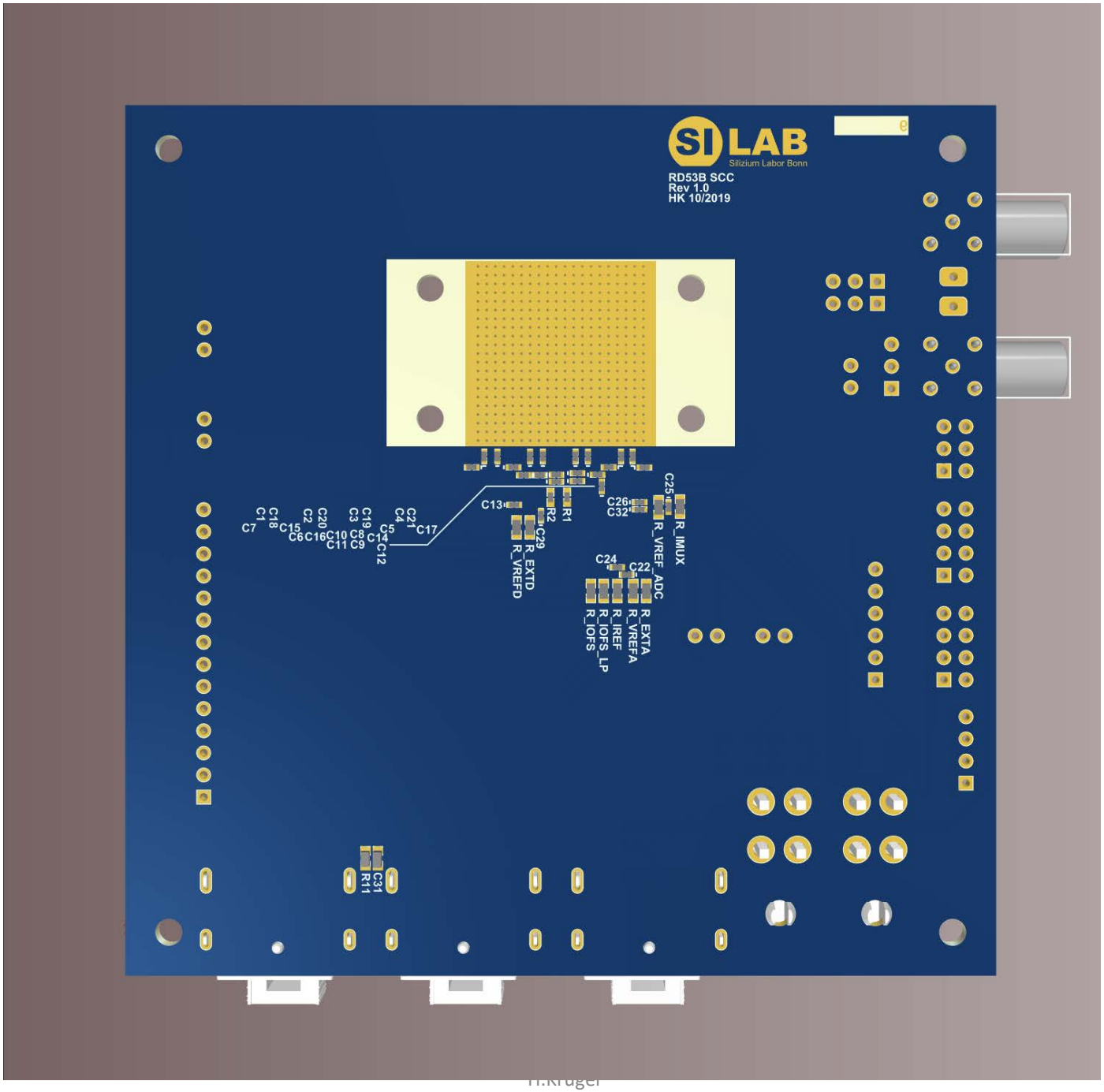
RD53B SCC Layout

- 6 layer, 100 µm PCB technology (RD53A SCC was 150 µm)
- Supports both ATLAS and CMS Chip size
  - ATLAS: 20.1 mm x 21.1 mm
  - CMS: 21.7 mm x 18.7 mm
- Optimized routing to improve SI
  - No vias in CMD traces, moved termination closer to chip
  - Removed configuration jumpers in data output (GTX) lines
  - Removed TH testpoints on GTX and CMD lines
  - Added solder mask opening for high-speed probe attach on all data lines
  - Did not foresee any jumper in CMD line for command forwarding test to avoid impact on SI, use external DP-SMA adapter instead
- Power configuration
  - Replaced std. pin headers for power configuration with solder jumpers
- Decreased PCB wirebond landing pad pitch from 300µm to 200µm
- Changed SMD footprint for voltage setting resistors from 0402 to 0603 for easier replacement/modification


SI LAB
Silizium Labor Bonn
RD53B
RD53B SCC
Rev 1.0
UNI
BONN
HK 10/2019
R4
R3
C23
HV
GND
HV
DET GRD1
DET GRD0
HV
GND
VMUX IMUX
IMUX R
NTC2
NTC1
TP NTC1
VDD EFUSE
GND
2.5V
SCAN
PIMTM
TEST_MODE
BYP_CMD
CHIP ID
IREF TRIM
Closed: 0, Open: 1
BIAS MON
GNDA_REF
IMUX
VMUX
NTC2
VREF_ADC
V_IREF
SHUNT EN
VOFS
IN
OUT
VIN
R5
C27
C28
C34
R15
R17
GND
GNDD_REF
GNDA_REF
VOFS_LP
VOFS
REXTD
REXTA
VREFD
VREFA
VDDD
VDDA
VDD_PRE
VIND
VINA
SLDO MON
MISC
GND
LAE
GC
PVR
VDD CML SEL
VDD PLL SEL
PWR A
PWR D
VDDA
VEXT
VINA
VDDA
VIND
VDDD
R9
R8
R7
R6
C33
R16
R14
C30
R10
DP1
DP3
DP2
X
Y
Z


SI LAB
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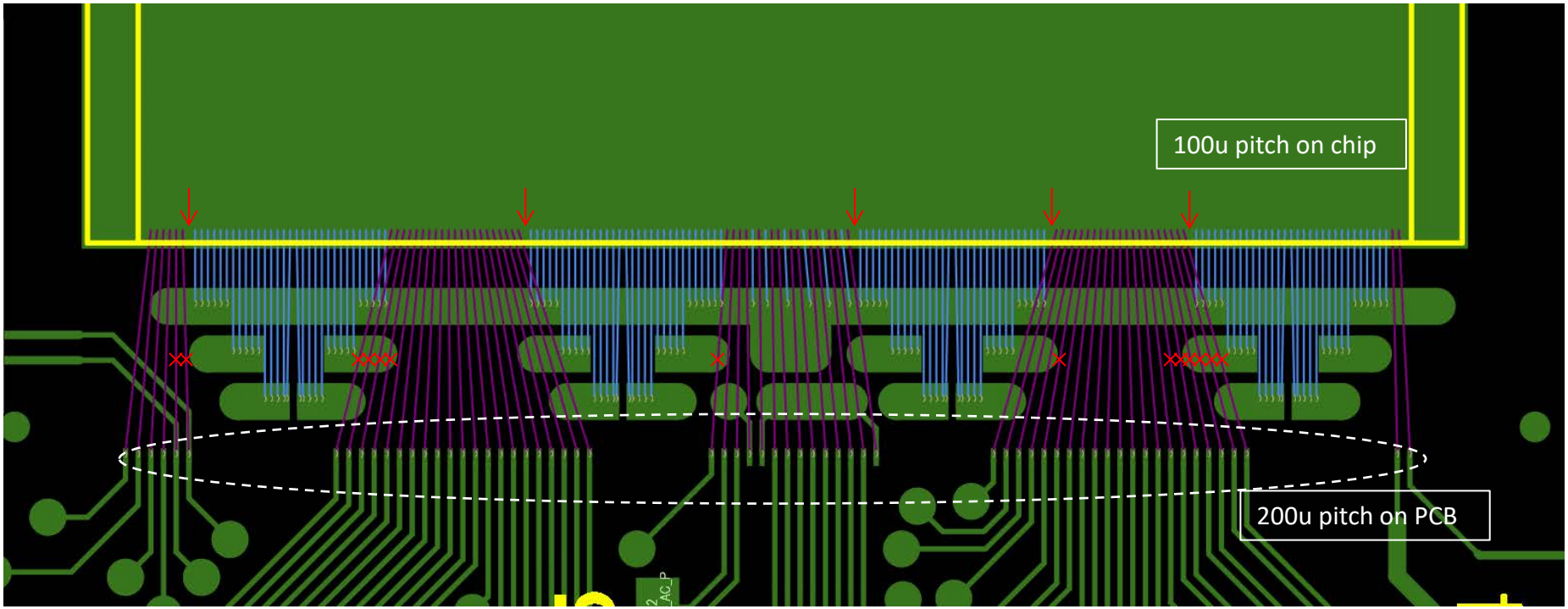
RD53B SCC
Rev 1.0
HK 10/2019
C7
C1
C18
C15
C6
C16
C2
C20
C10
C11
C3
C19
C8
C9
C5
C14
C4
C21
C12
C17
C13
R2
R1
C29
R_EXTD
R_VREFD
C26
C32
C25
R_IMUX
R_VREF_ADC
C24
C22
R_EXTA
R_VREFA
R_IREF
R_IOFS_LP
R_IOFS
C31
R11

RD53B Wire Bond Details

- Wire bond pad dimensions
  - Size increased from 58 µm x 86 µm to 68 µm x 101 µm
  - Pitch stayed the same (100 µm)
- 198 pads (like RD53A)
  - 193 pads used in total, all connected on SCC
  - 179 pads used on module (no monitoring & debugging)
- Placed non used pads between parallel power wire bonds and fan-out section of the signal wire bonds to reduce overlap
- Complete IO pad list: https://docs.google.com/spreadsheets/d/15JYR5KCmM0jfU1Jq1TeINLomZKa2B-XgKmDgdxv1aPA

RD53B SCC Wire Bond Diagram



↓: VOID WB pad

× : WB not used on module