

RPC Link System *Slow Controller* Development in CMS/HL-LHC Experiment Update II

Programa de Pós-Graduação em Instrumentação e Óptica - PPGIO
Doutoramento em Engenharias Áreas IV

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Agenda

CMS

Muon Systems

RPC Muon

Link Board System

Slow Controller

Overview

FPGA-Kintex7

Operação

Resultados



No CMS HL-LHC Upgrade (Phase-2): System Muon: Upgrade nas FE/BE readout e RPC Link Board

Technical proposal CERN-LHCC-2015-010 <https://cds.cern.ch/record/2020886>

Scope Document CERN-LHCC-2015-019 <https://cds.cern.ch/record/2055167/files/LHCC-G-165.pdf>

L1-Trigger/HLT/DAQ

<https://cds.cern.ch/record/2283192>

<https://cds.cern.ch/record/2283193>

- Tracks in L1-Trigger at 40 MHz
- PFlow-like selection 750 kHz output
- HLT output 7.5 kHz

Calorimeter Endcap

<https://cds.cern.ch/record/2293646>

- 3D showers and precise timing
- Si, Scint+SIPM in Pb/W-SS

Tracker <https://cds.cern.ch/record/2272264>

- Si-Strip and Pixels increased granularity
- Design for tracking in L1-Trigger
- Extended coverage to $\eta \approx 3.8$

Barrel Calorimeters

<https://cds.cern.ch/record/2283187>

- ECAL crystal granularity readout at 40 MHz with precise timing for e/γ at 30 GeV
- ECAL and HCAL new Back-End boards

Muon systems

<https://cds.cern.ch/record/2283189>

- DT & CSC new FE/BE readout
- RPC link -board
- New GEM/RPC $1.6 < \eta < 2.4$
- Extended coverage to $\eta \approx 3$

Beam Radiation Instr. and Luminosity, and Common Systems and Infrastructure

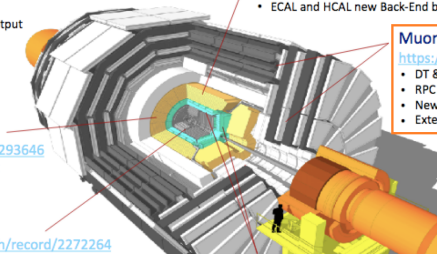
<https://cds.cern.ch/record/2020886>

MIP Timing Detector

<https://cds.cern.ch/record/2296612>

Precision timing with:

- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes

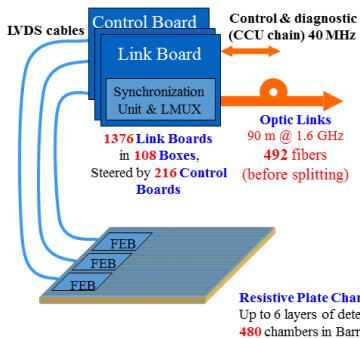


Innovative and extremely challenging new capabilities

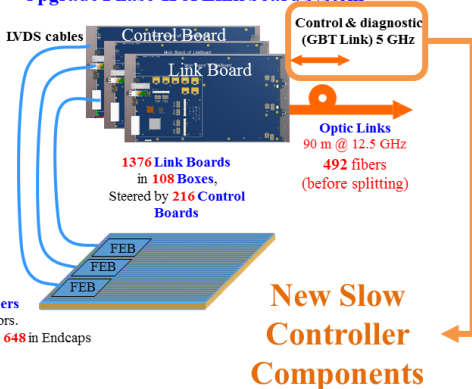
Link Board system Overview

Upgrade Motivação

Present Link board system



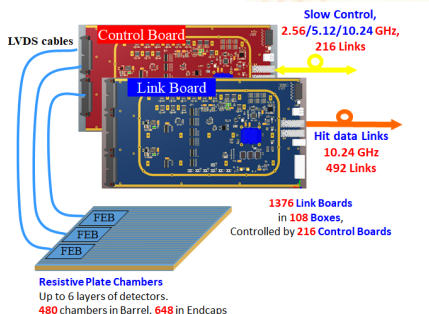
Upgrade Phase-II of Link board system



New Link System Overview

New Link system Upgrade Phase-II no LS2

Baseado numa FPGA Kintex-7 da Xilinx



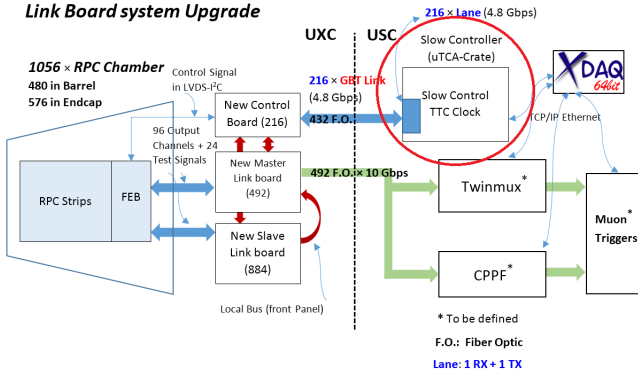
New Link Board System e Control Board

- FPGA XC7K160T - Versão Industrial
- Link óptico redundante
- Programação remota
- Transmissão de dados em alta velocidade em LATÊNCIA FIXA
- Conexão de fibra óptica ponto a ponto entre as placas de controle e o *Slow Controller*

O que é Slow Controller

Sistema: monitora/controla um ou mais sistemas

Present RPCs & Upgrade Phase-II of Link Board system Upgrade



Prevenção de falhas, monitoramento, controle direto pelo usuário ou controle automatizado

Desenvolvimento do *Slow Controller*

Implementação: FPGA-Kintex7, Rack μ TCA e AMC13

Software (Firmware) para o Slow Controller



FEE TTC Identification



BEE TTC decode

Firmware para um Protocolo com 256 bits

Item	Header + FEC [0..23]	L1A [24]	BC0 [25]	EC0 [26]	Hard Reset [27]	Command Type [28..30]	Command Value A [31..38]	Command Value B [39..54]	Command Value C [55..253]	End of Data [254, 255]
Bit	24	1	1	1	1	3	8	16	199	2

Perspectivas & Resultados do *Slow Controller*

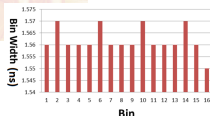
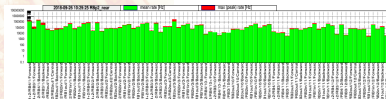
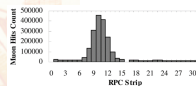
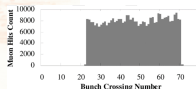
O Software ONLINE:

Requisita/controla serviços através do Slow controller

- CMS OnLine

- *Slow Controller*

- Calibration mode
 - Link Board Parameter Setting
 - Control Board Parameter setting
 - Physics RUN
 - Standby
 - Histogram
 - Diagnostic
 - FEB Test



CMS

Perguntas?



OBRIGADO PELA SUA ATENÇÃO!