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Looking for new physics in the LHC hardware trigger with Deep Autoencoders

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We show how to adapt and deploy anomaly detection algorithms based on deep autoencoders, for the unsupervised detection of new physics signatures in the extremely challenging environment of a real-time event selection system at the Large Hadron Collider (LHC). We demonstrate that new physics signatures can be enhanced by three orders of magnitude, while staying within the strict latency and resource constraints of a typical LHC event filtering system. This would allow for collecting datasets potentially enriched with high-purity contributions from new physics processes. Through per-layer, highly parallel implementations of network layers, support for autoencoder-specific losses on FPGAs and latent space based inference, we demonstrate that anomaly detection can be performed in as little as 80 ns using less than 3% of the logic resources in the Xilinx Virtex VU9P FPGA. Opening the way to real-life applications of this idea during the next data-taking campaign of the LHC.

Significance

This talk is cover the material in the paper https://arxiv.org/abs/2108.03986, where we explore for the first time in the LHC hardware trigger the potential of unsupervised and semi-supervised techniques for detecting new physics signatures, most notably anomaly detection algorithms enhanced with deep learning. Using such algorithms, one can learn how to identify out- of-distribution events directly from the LHC data. One can then select the most anomalous events, which are the most likely to contain new physics signatures, into a special data stream of anomalous events. The complications come from the fact that such algorithm have to fit into the strict restrictions of Level-1 trigger, in particular, it should have latency of O(1) μs, take up small fraction of the FPGA resources and have initial interval smaller than LHC bunch-crossing (i.e. 25 ns).
We have successfully designed such an algorithm and tested it performance on a several potential new physics scenarios with ability to enhance such signals by three orders of magnitude, while keeping the algorithm's performance is as fast as 80 ns, with initial interval of just 5 ns using less than 3% of FPGA resources.

References

Speaker time zone

Compatible with Europe

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