



**LFOUNDRY**

Solutions  
for great visions

# Technology development on CMOS Image sensors

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Sensor Group - Lfoundry

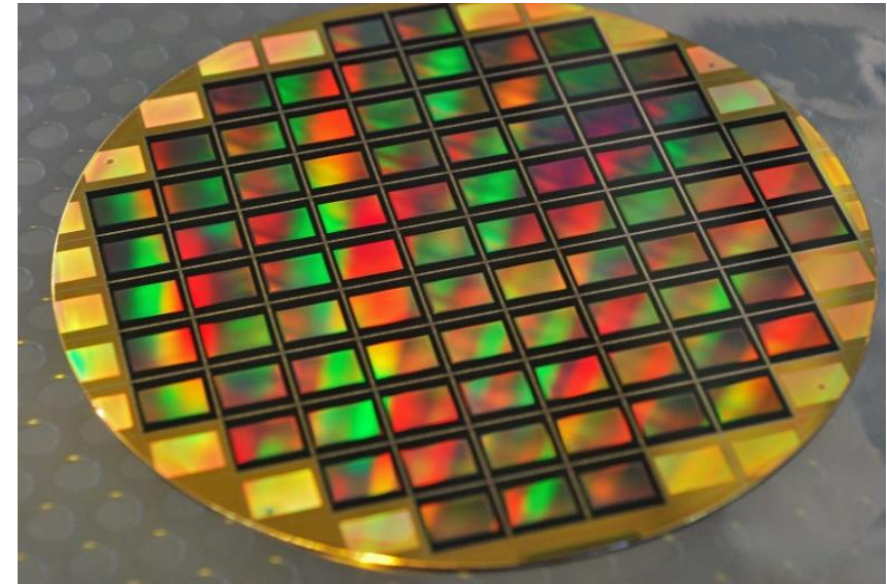
[andrea.delmonte@lfoundry.com](mailto:andrea.delmonte@lfoundry.com)

Genève - November 15, 2019

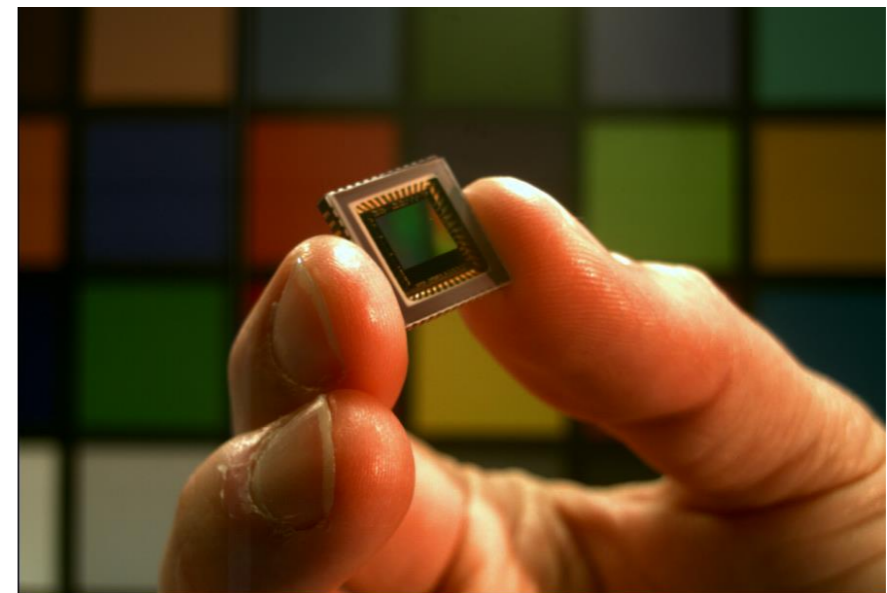
The wafer fab in Avezzano



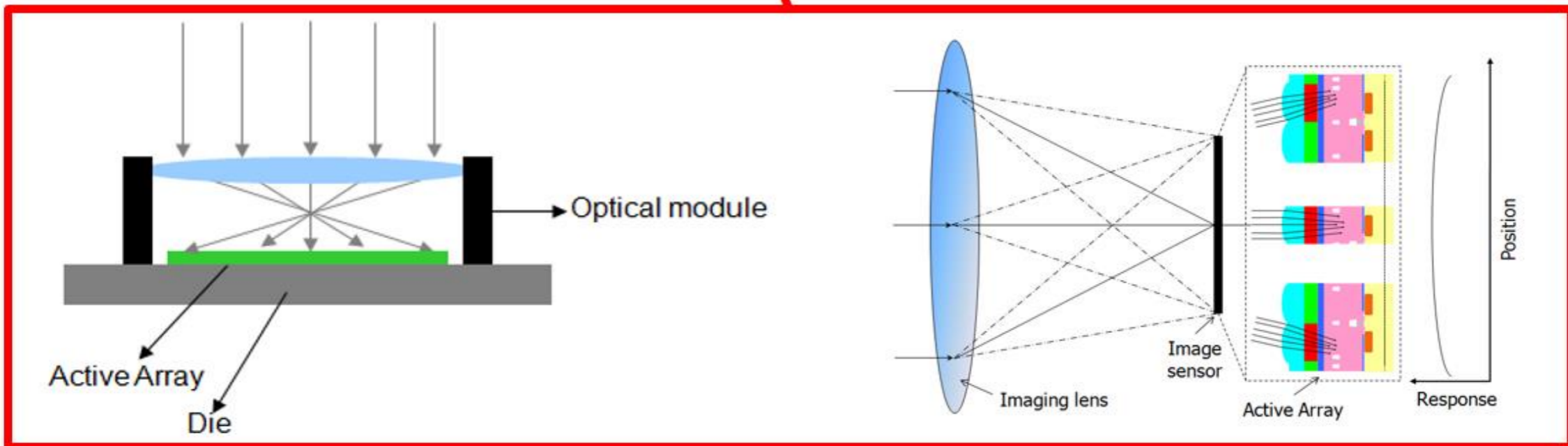
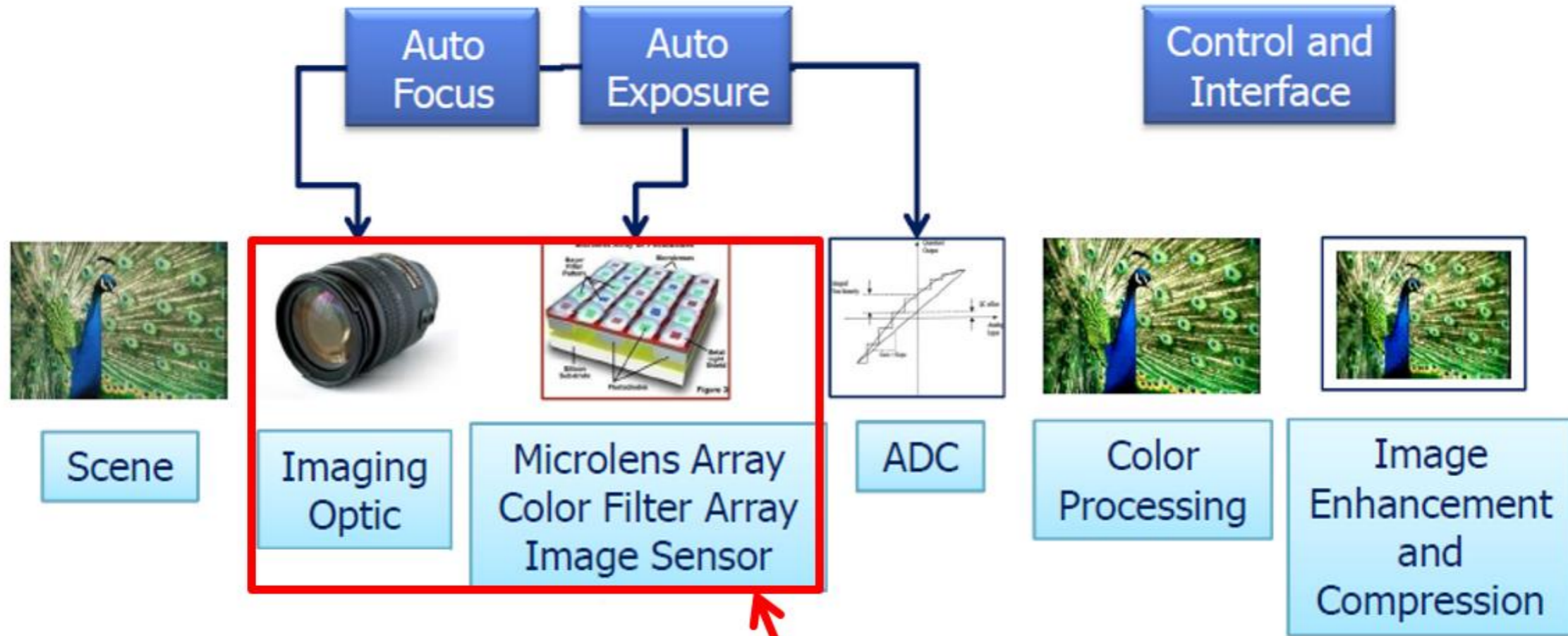
200 mm wafer

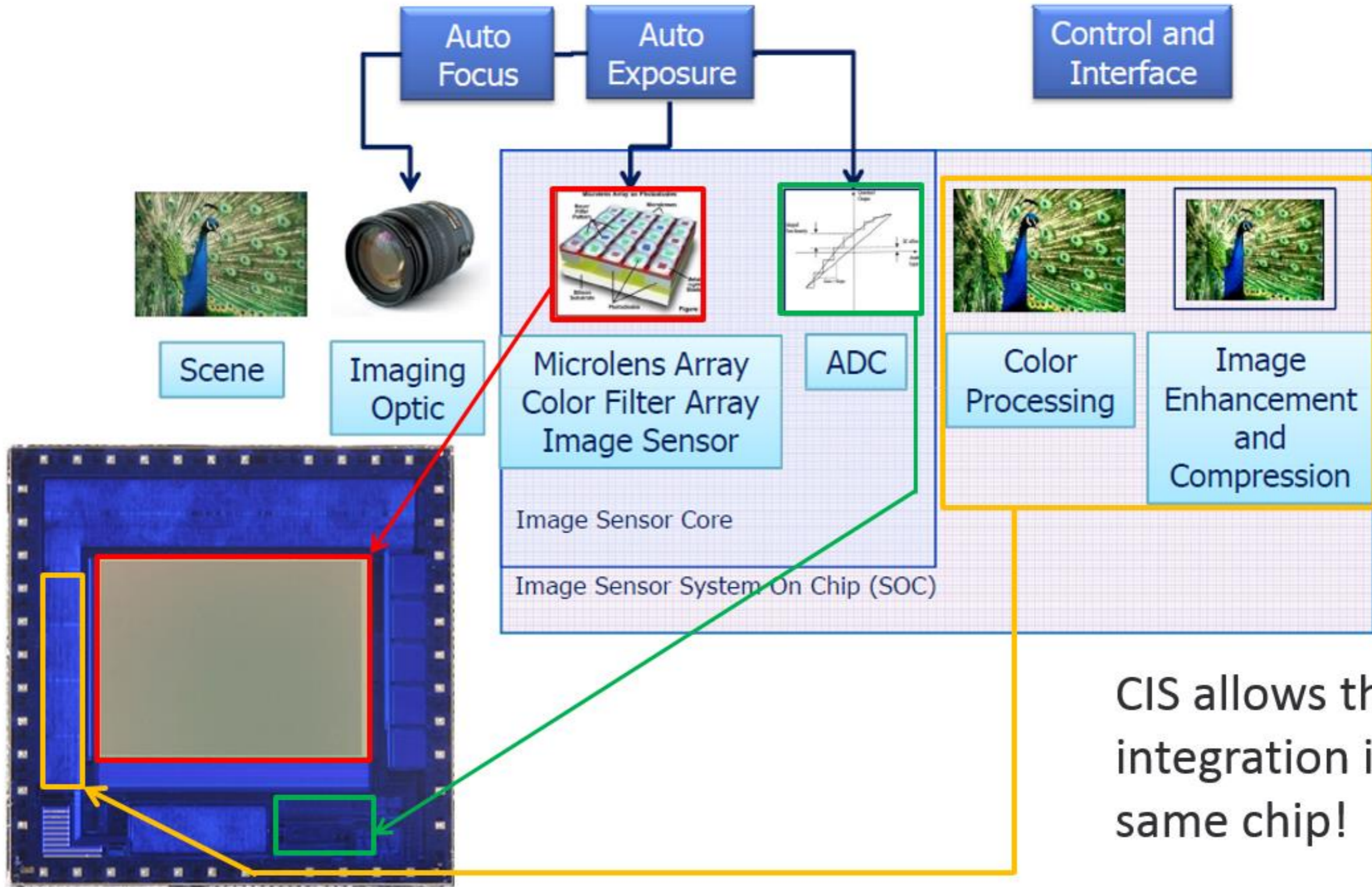


Packaged sensor



- **LFoundry** Fab is located in Avezzano, in Abruzzo region, currently employing about 1500 people. The fab is equipped with a 11.000 m<sup>2</sup> wide clean room area;
- The fabrication of the plant was completed on 1989, by Texas Instruments. In 1998 it was acquired by Micron Technology Inc and fully dedicated to DRAM mass production until the introduction of **CMOS Image Sensor** production in 2006;
- In May 2013 LFoundry acquired the site from Micron;
- In June 2016 SMIC acquired 70% of the company;
- In July 2019 the company has been acquired by Wuxi Xichanweixin Semiconductor;
- We have been developing and manufacturing CMOS image sensors since 2006. Our technology portfolio, based on 200 mm wafers, includes different process nodes down to 90 nm (minimum feature for transistor gate length).

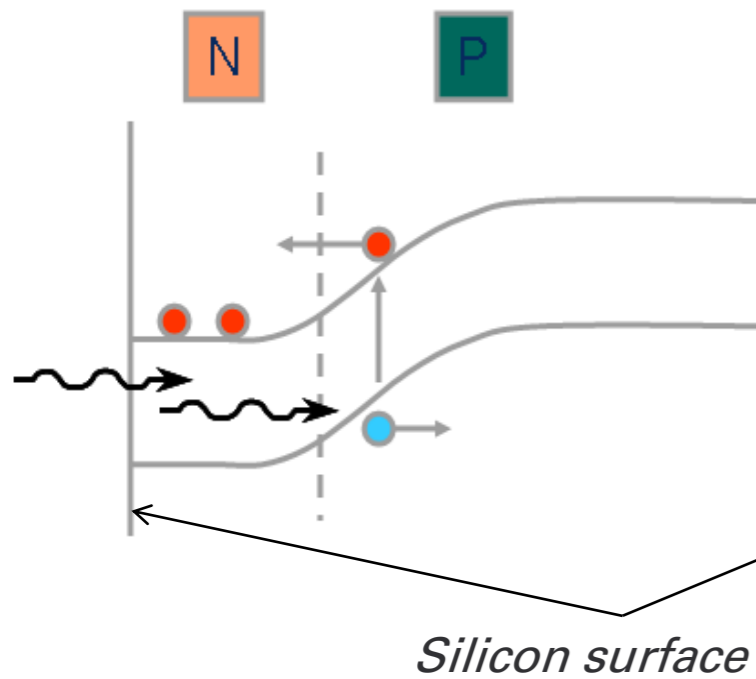




CIS allows the integration in the same chip!

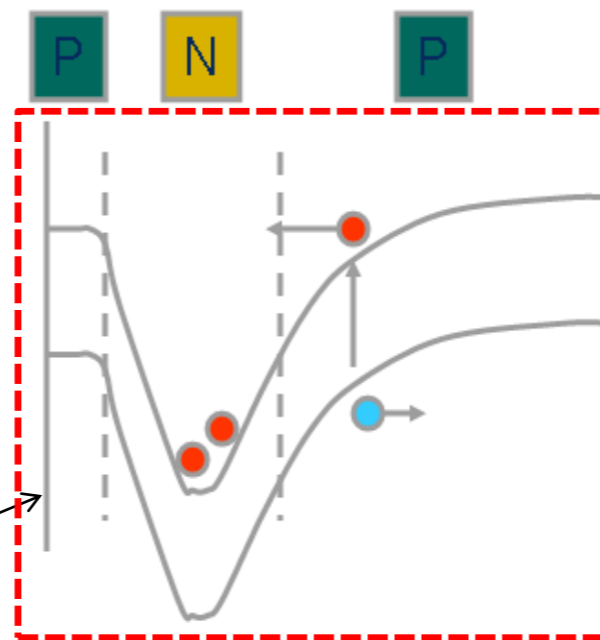
Conventional photodiode  
(p-n junction)

Conventional  
Photodiode

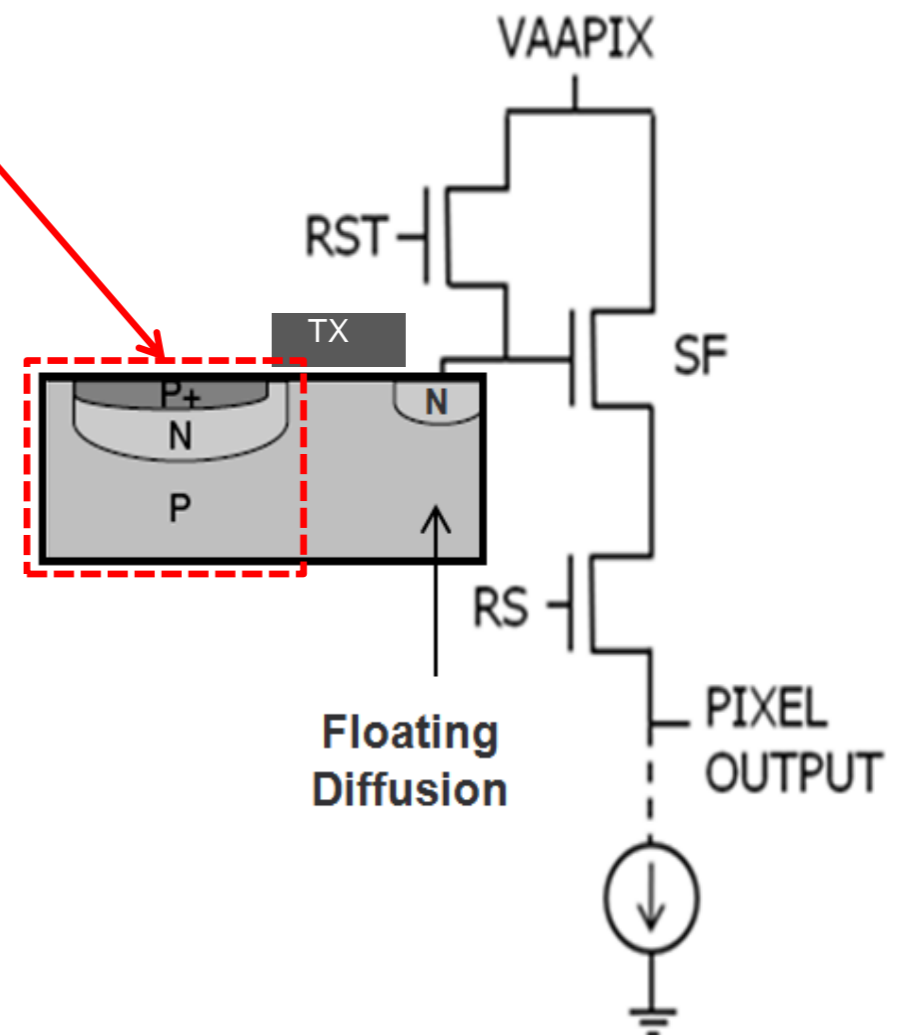


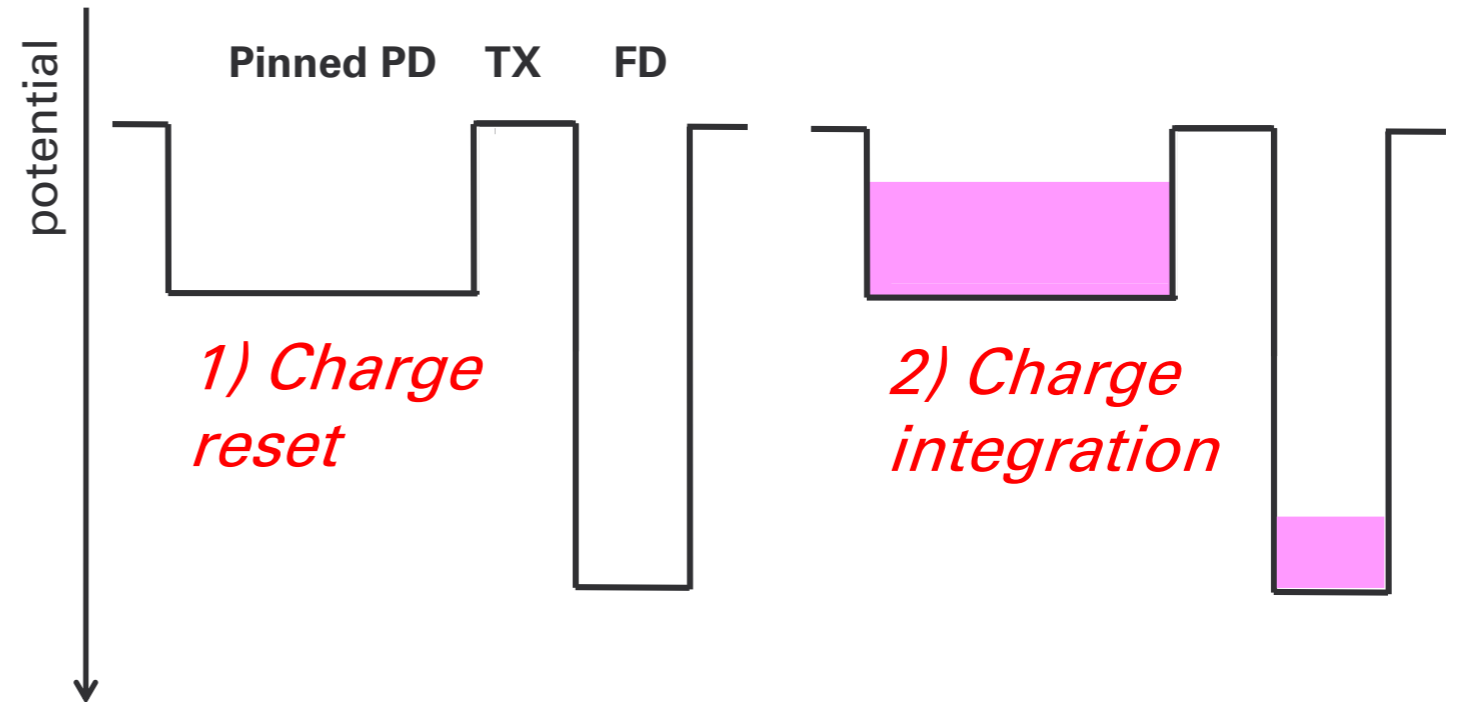
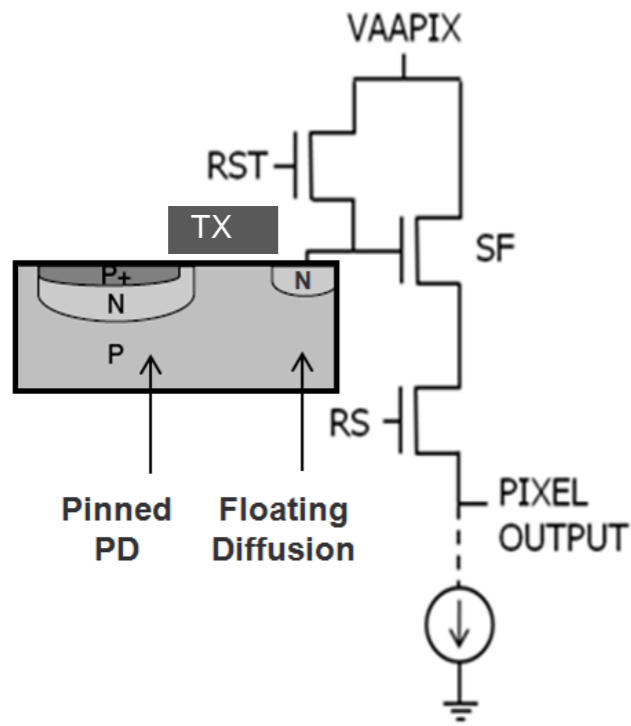
Pinned photodiode  
(p-n-p structure)

Buried  
Photodiode

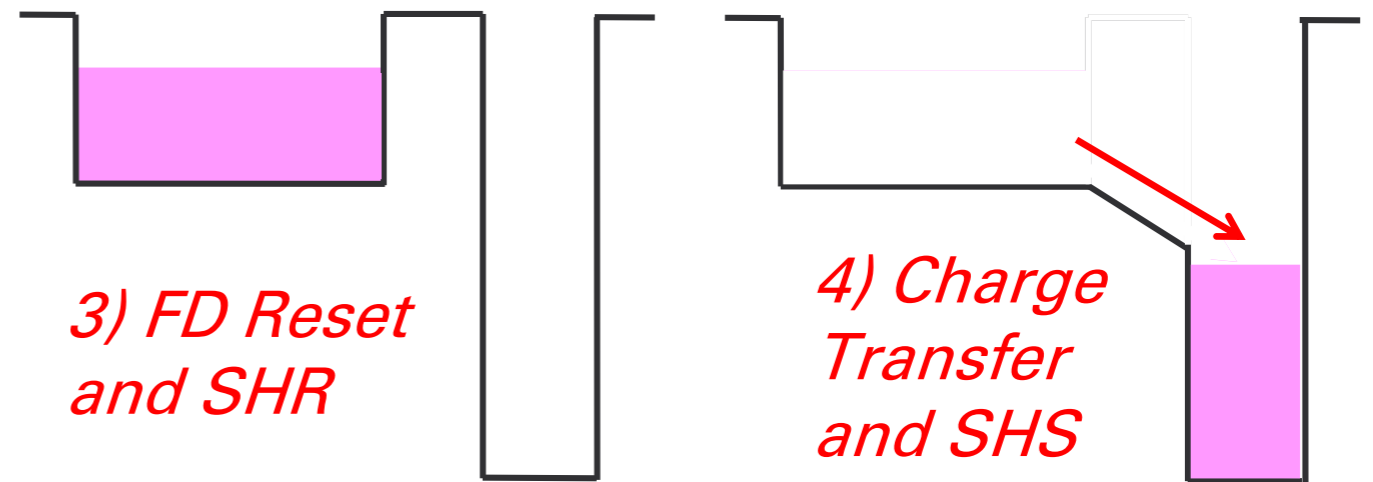
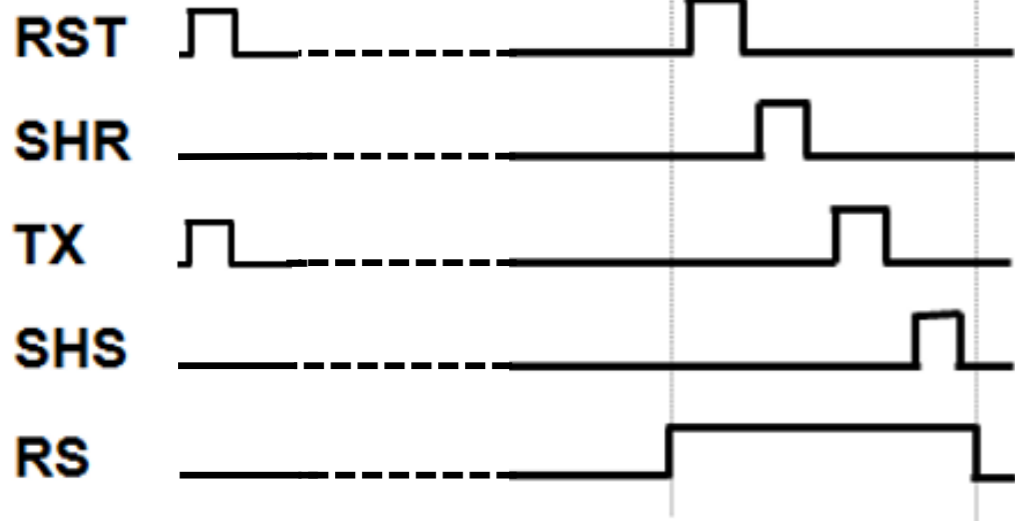
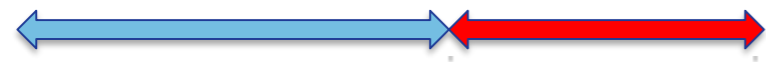


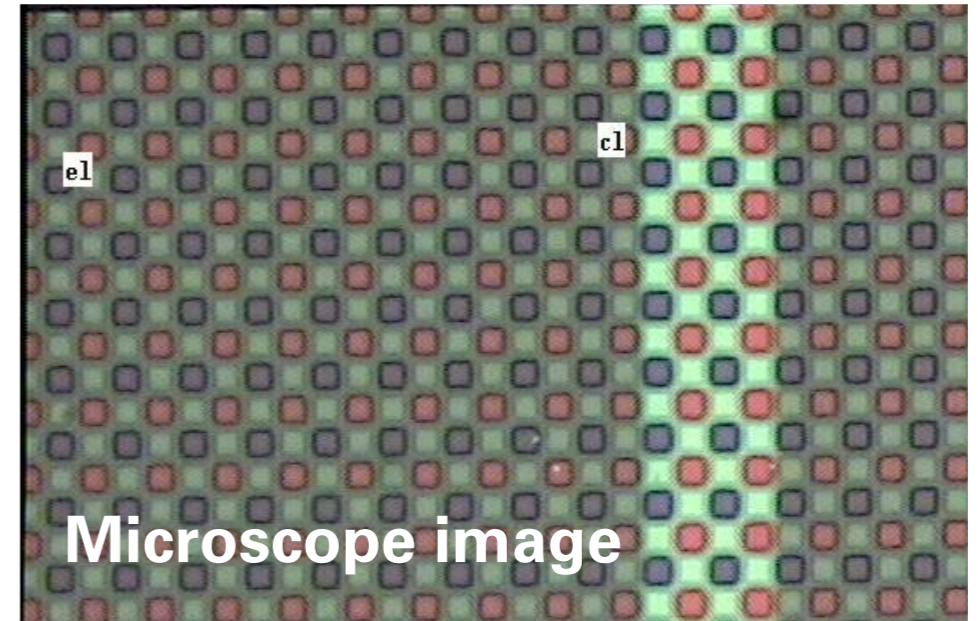
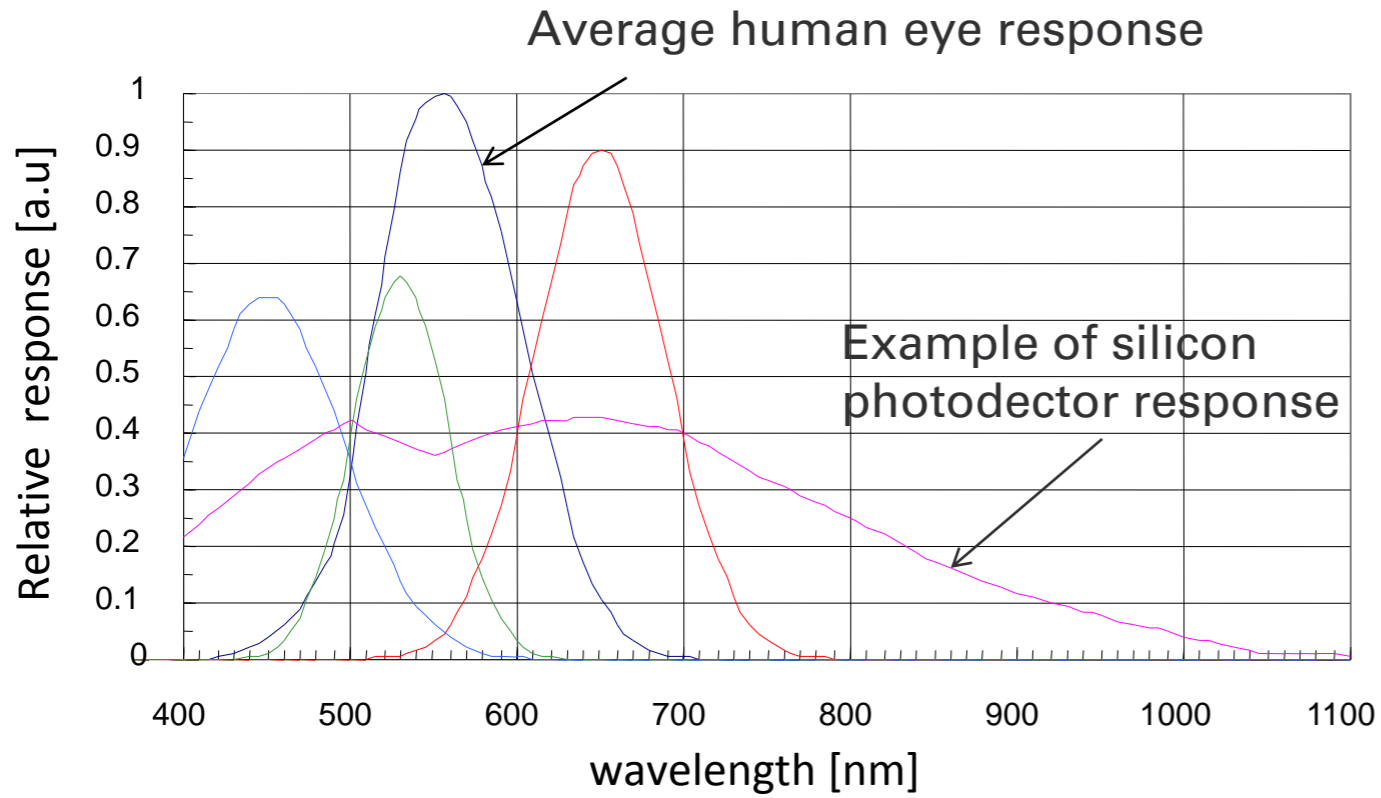
4-T cell



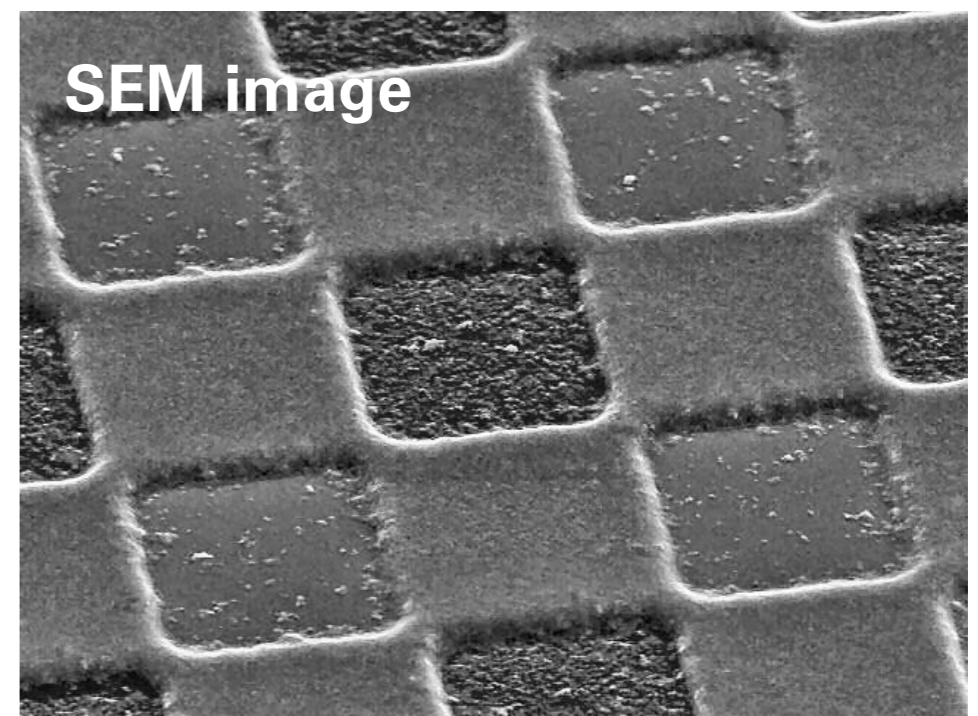
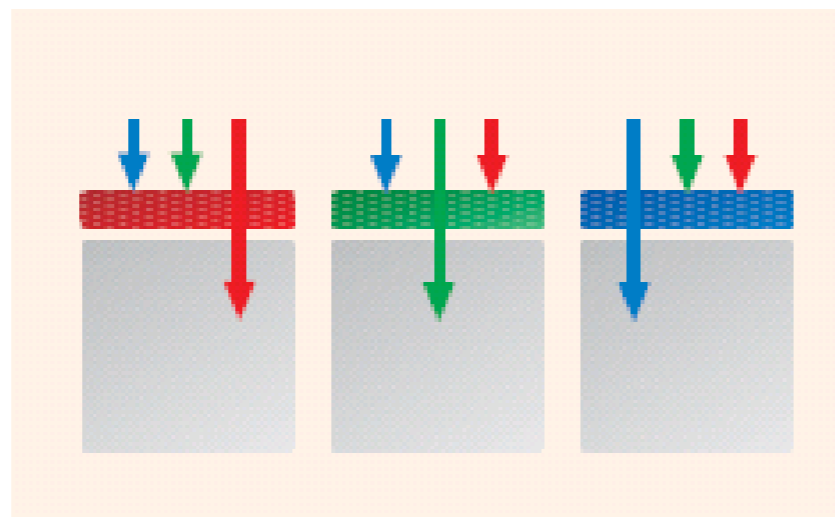
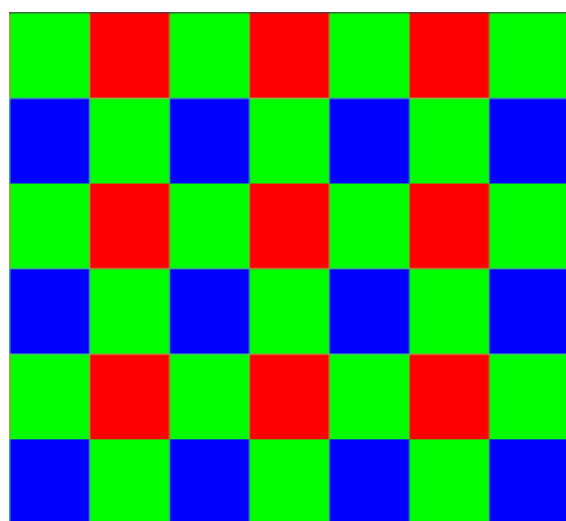


PD Reset    Integration    Readout





Bayer pattern

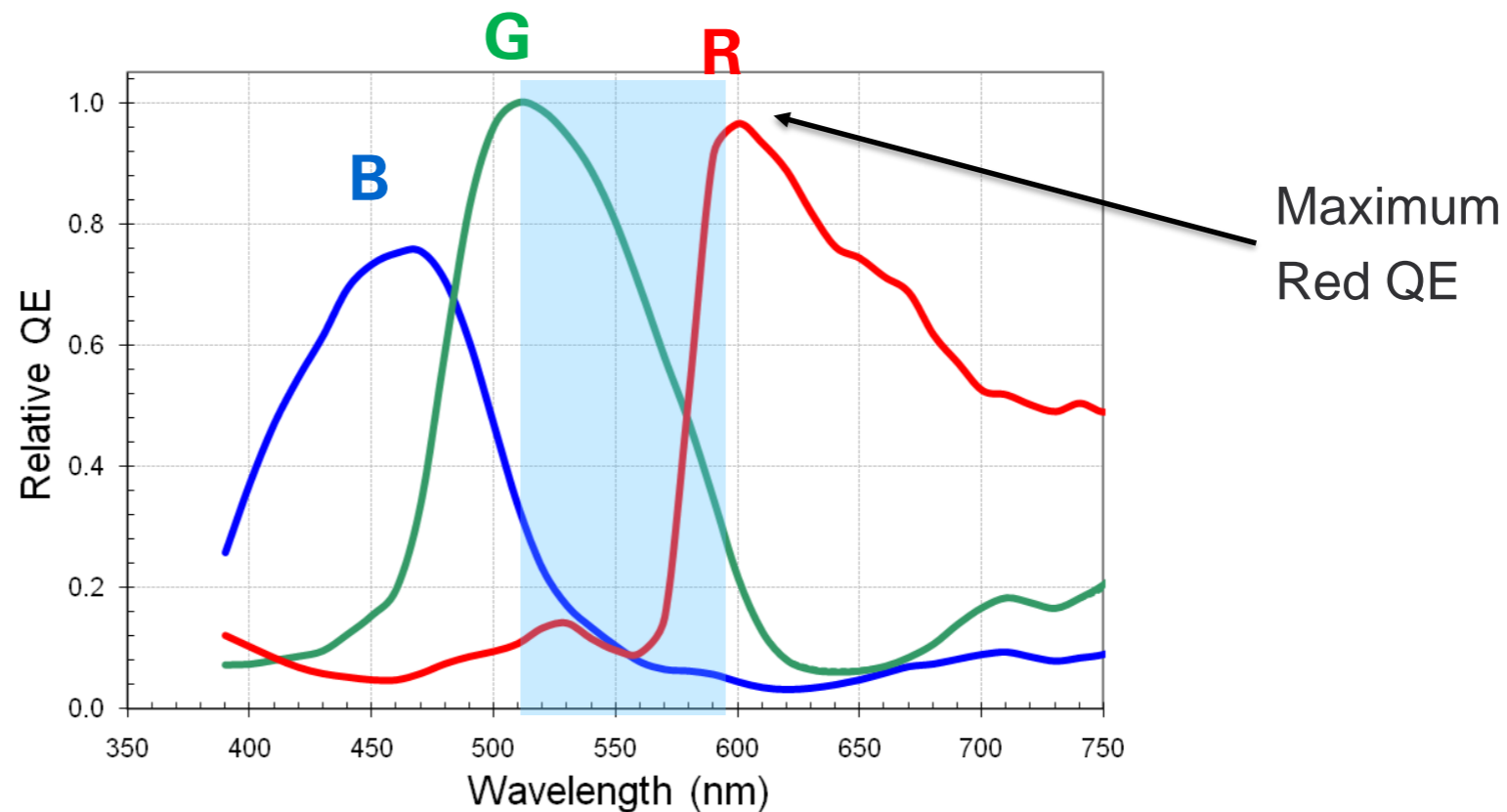




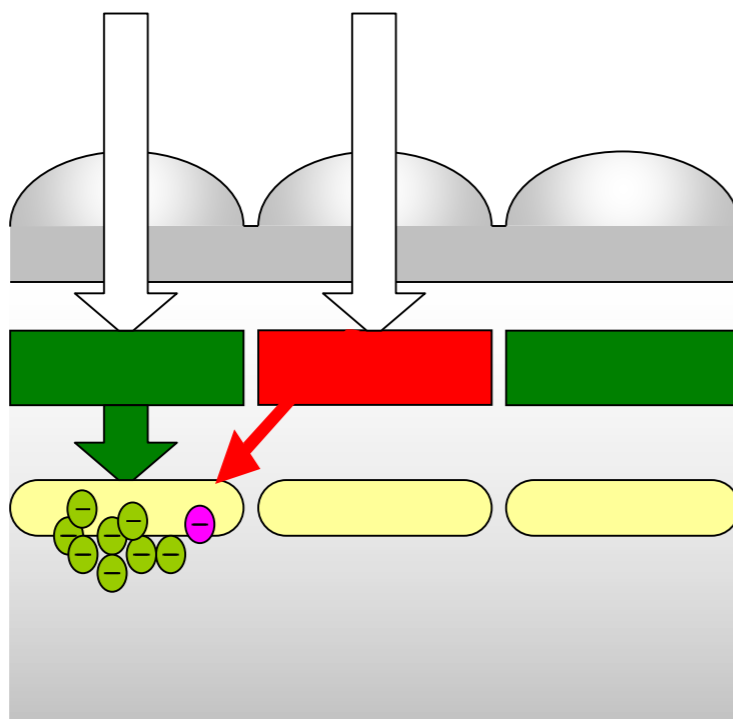
Crosstalk from blue and from red to green

$$C_{b \rightarrow g} = \frac{\int_{515}^{575} R_{blue} \cdot d\lambda}{\int_{515}^{575} R_{green} \cdot d\lambda}$$

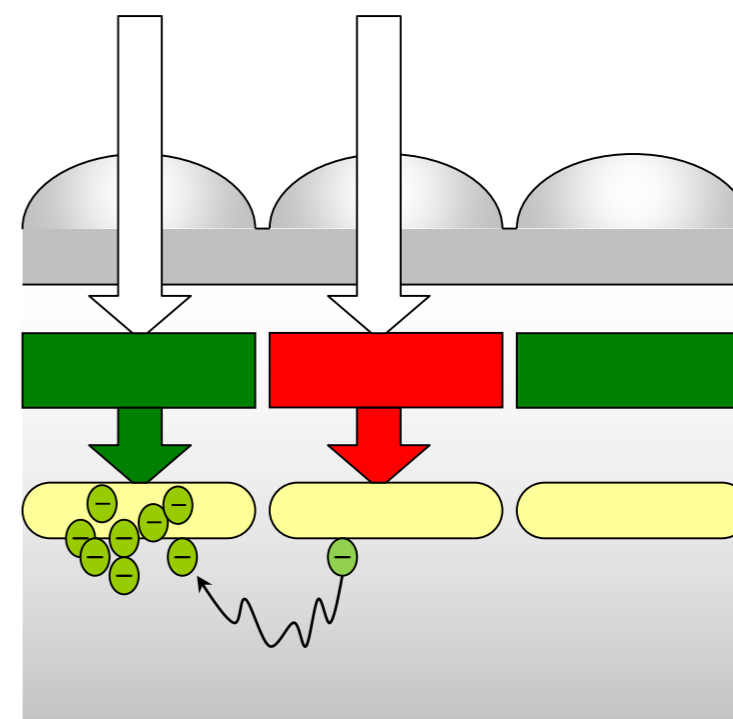
$$C_{r \rightarrow g} = \frac{\int_{515}^{575} R_{red} \cdot d\lambda}{\int_{515}^{575} R_{green} \cdot d\lambda}$$



Optical crosstalk



Electrical crosstalk

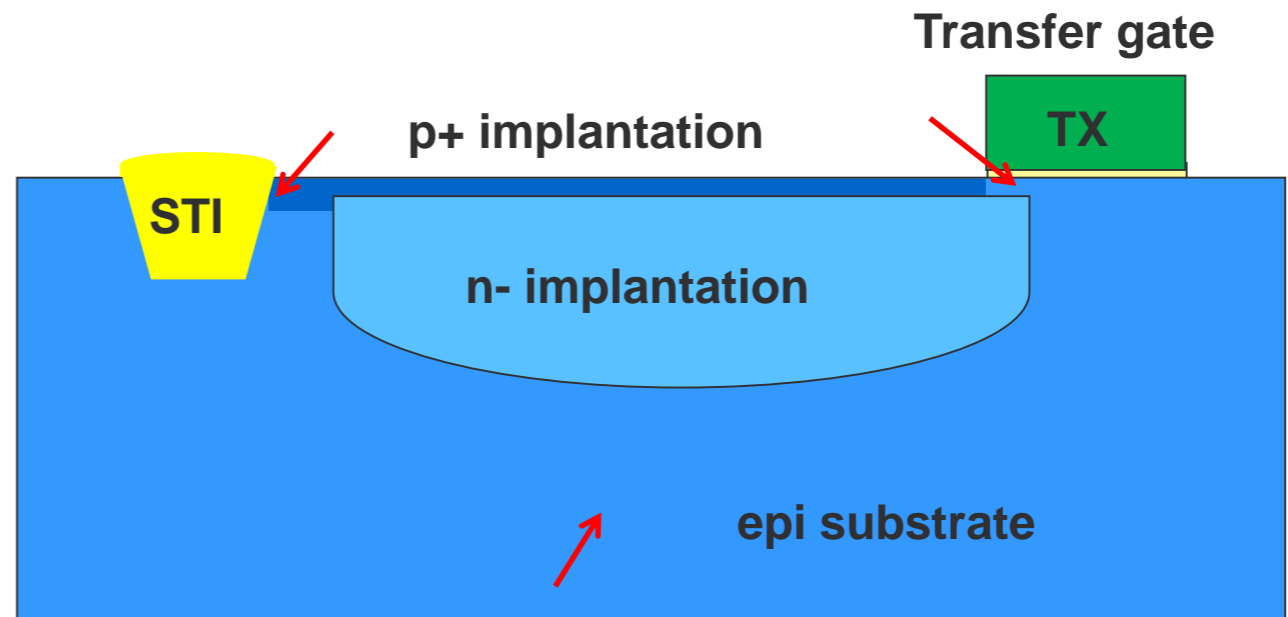


$$N_{dark} = \frac{I_{dark} \cdot t_{int}}{q}$$

Undesired signal integrated in dark conditions

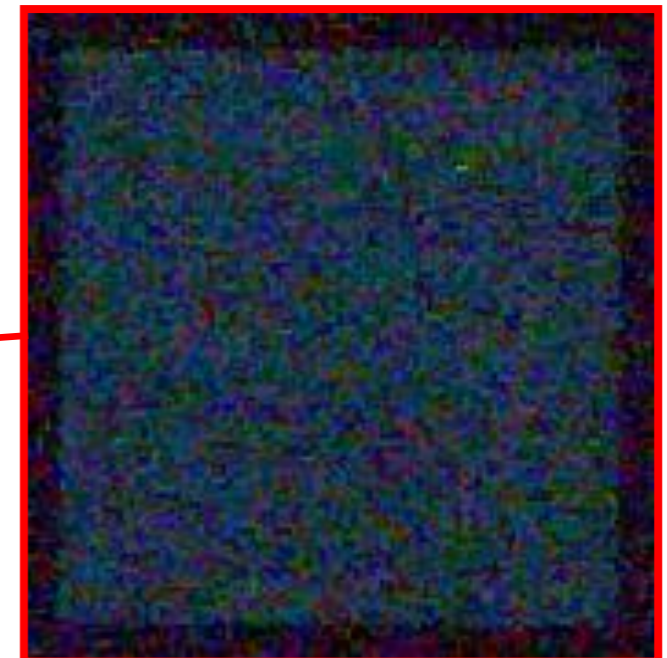
Sources of dark current and hot pixels

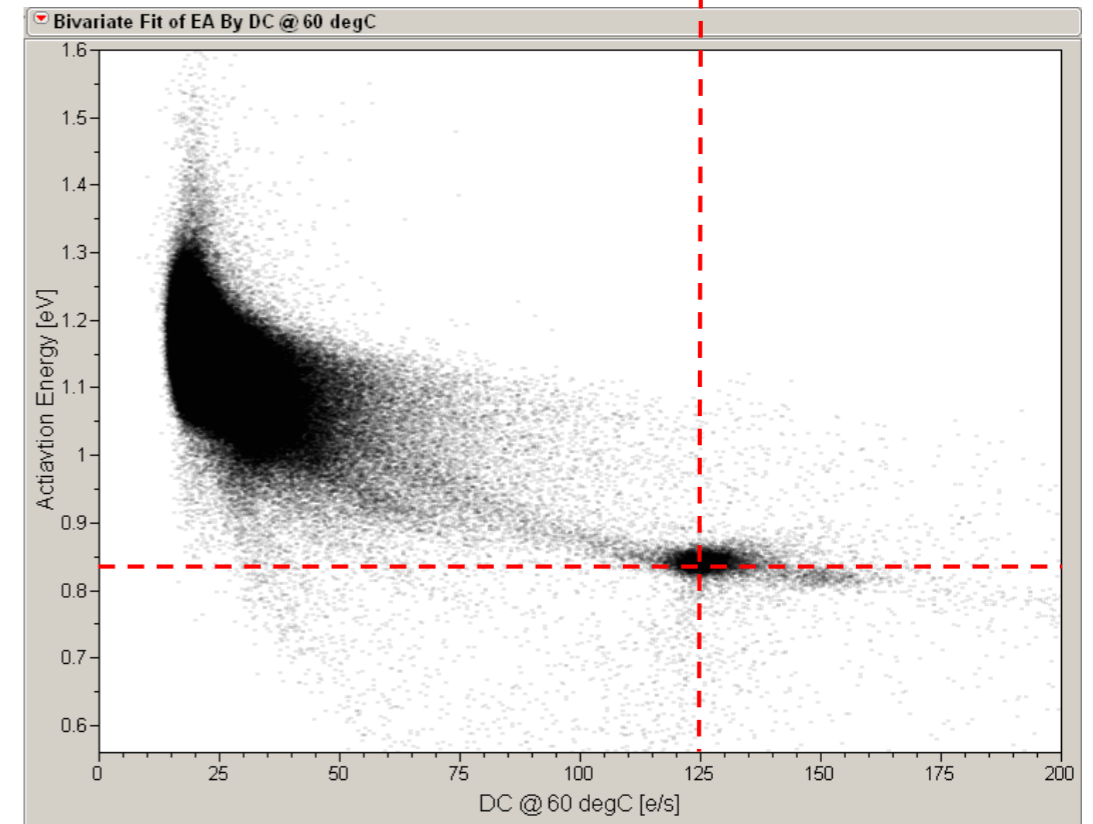
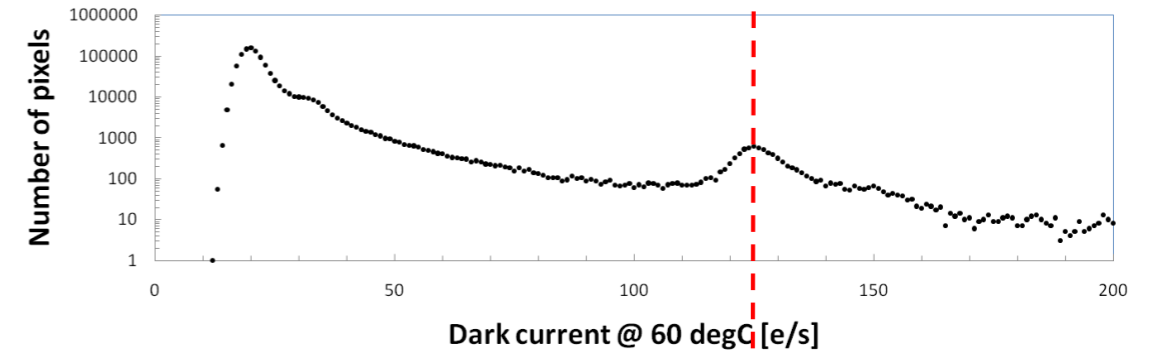
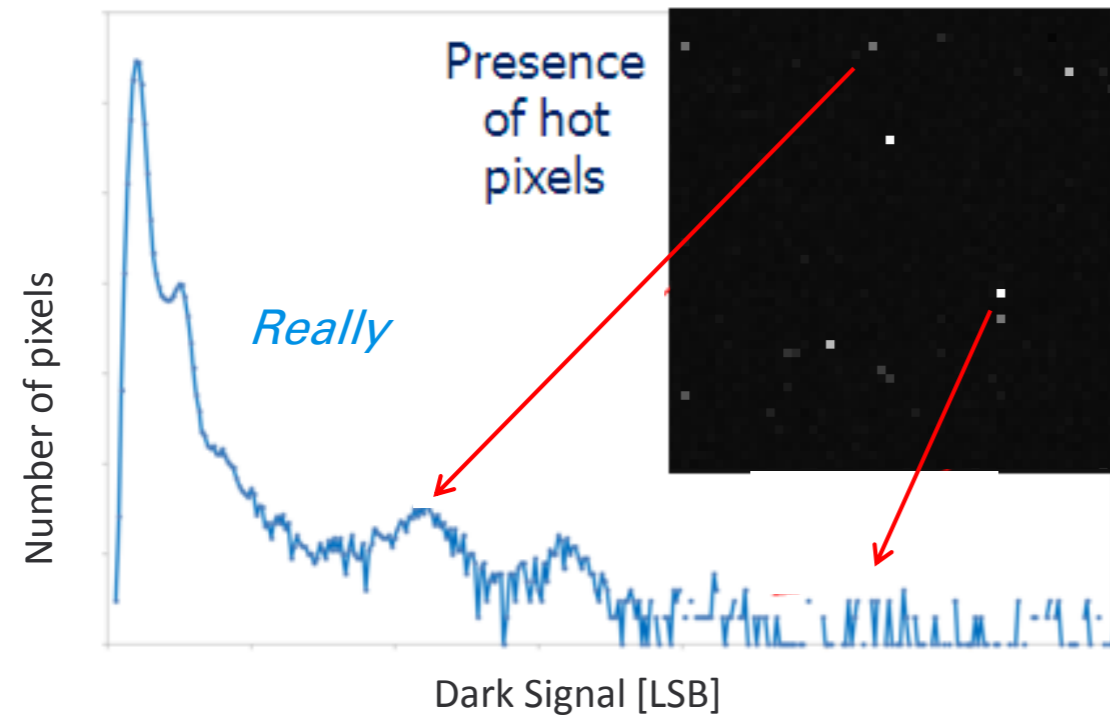
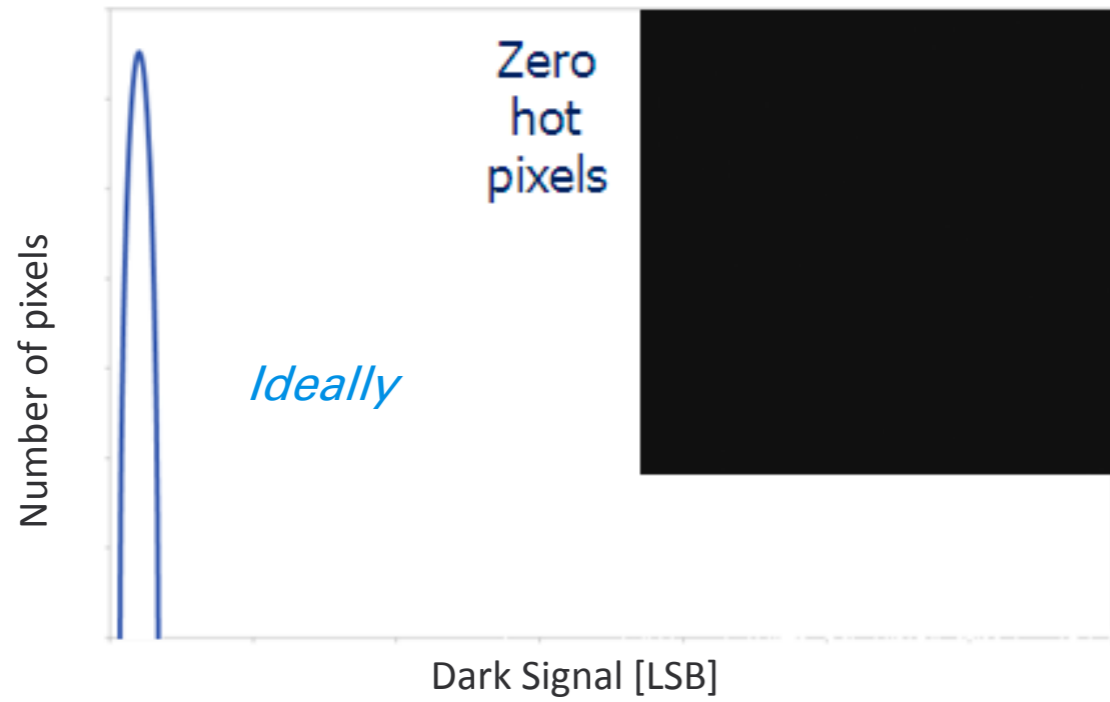
1. STI around the photodiode
2. Photodiode surface
3. Substrate
4. Overlap of PD with transfer gate
5. Contamination & defects



Medium light

Low light

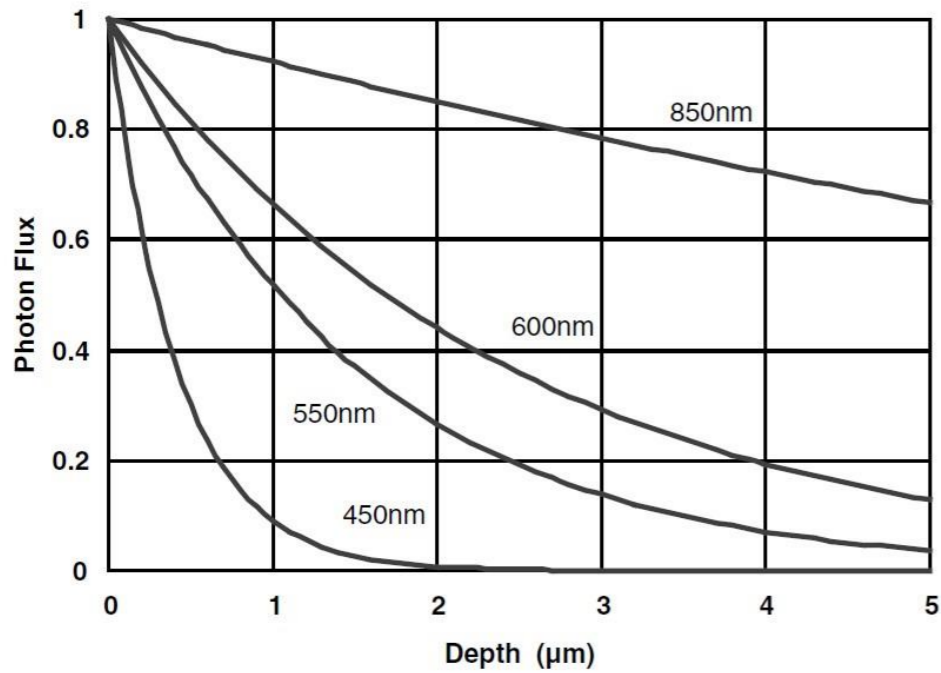




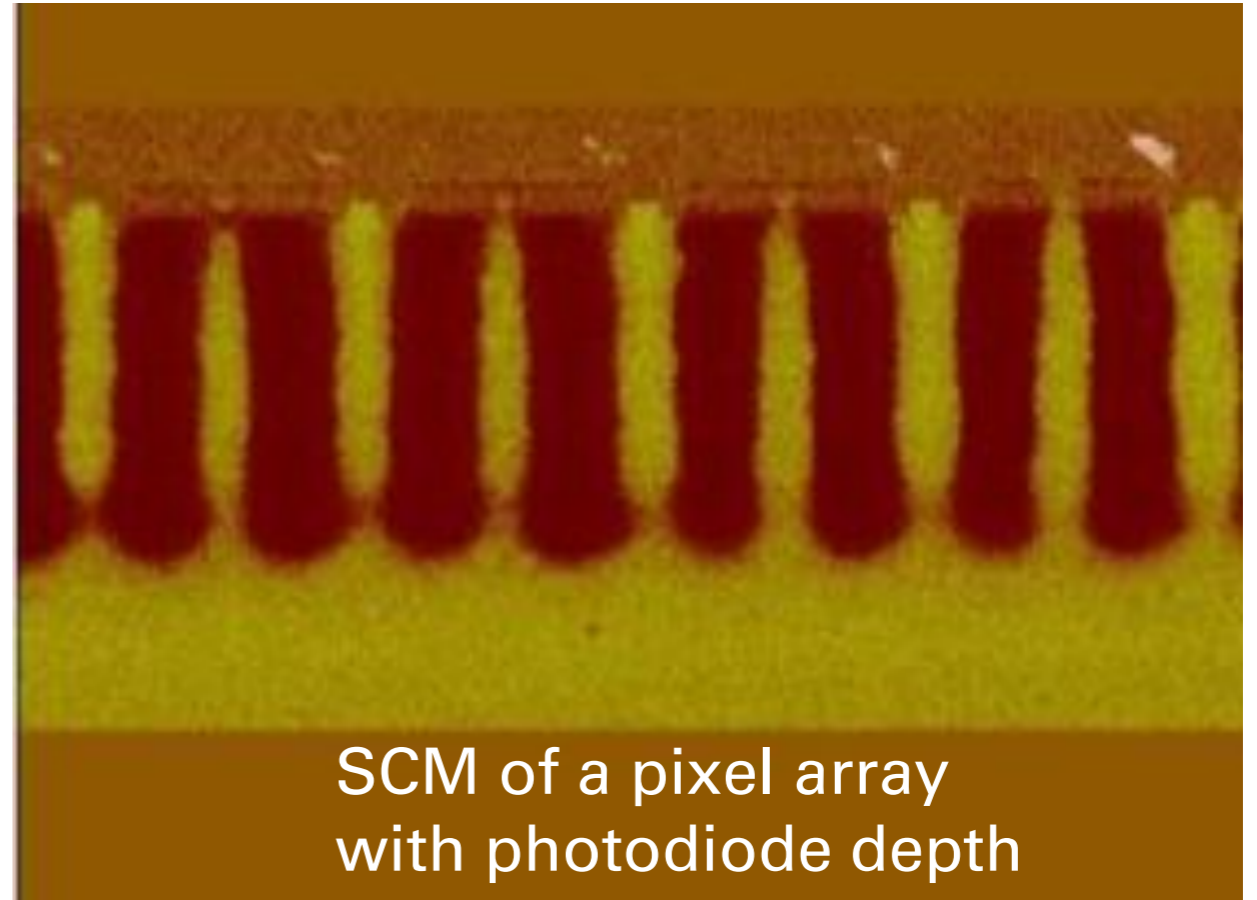
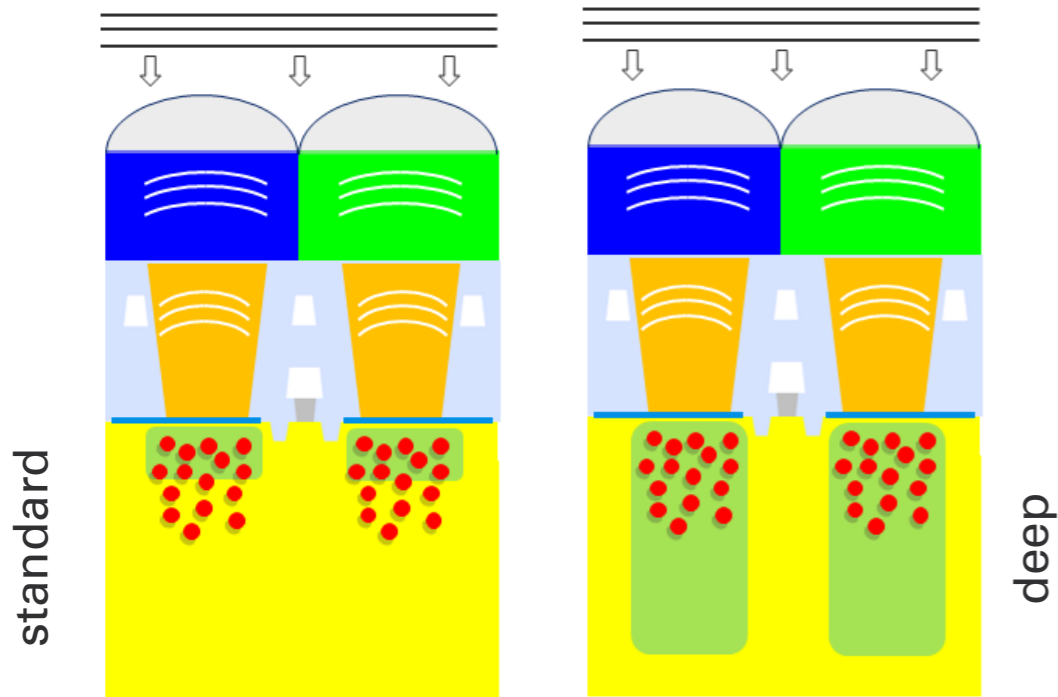
A specific dark current and activation energy value corresponds to the defect in silicon crystal causing the peak



Light absorption in silicon



Incident light

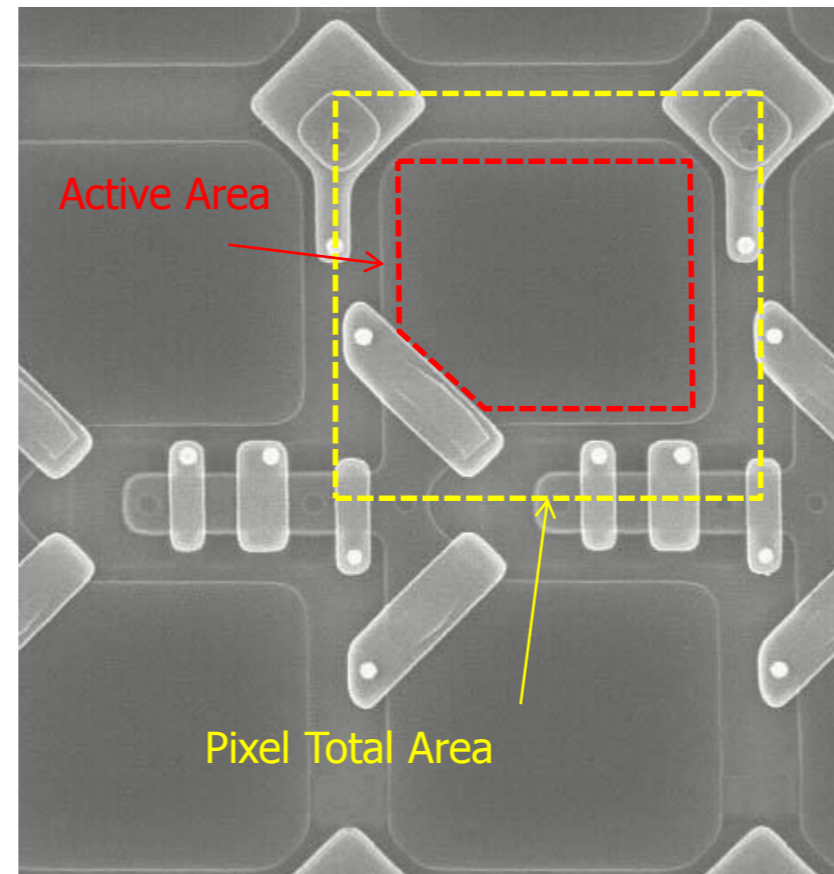


Max implant energy capability:

- Boron 2800 KeV
- Phosphorous 4800 KeV

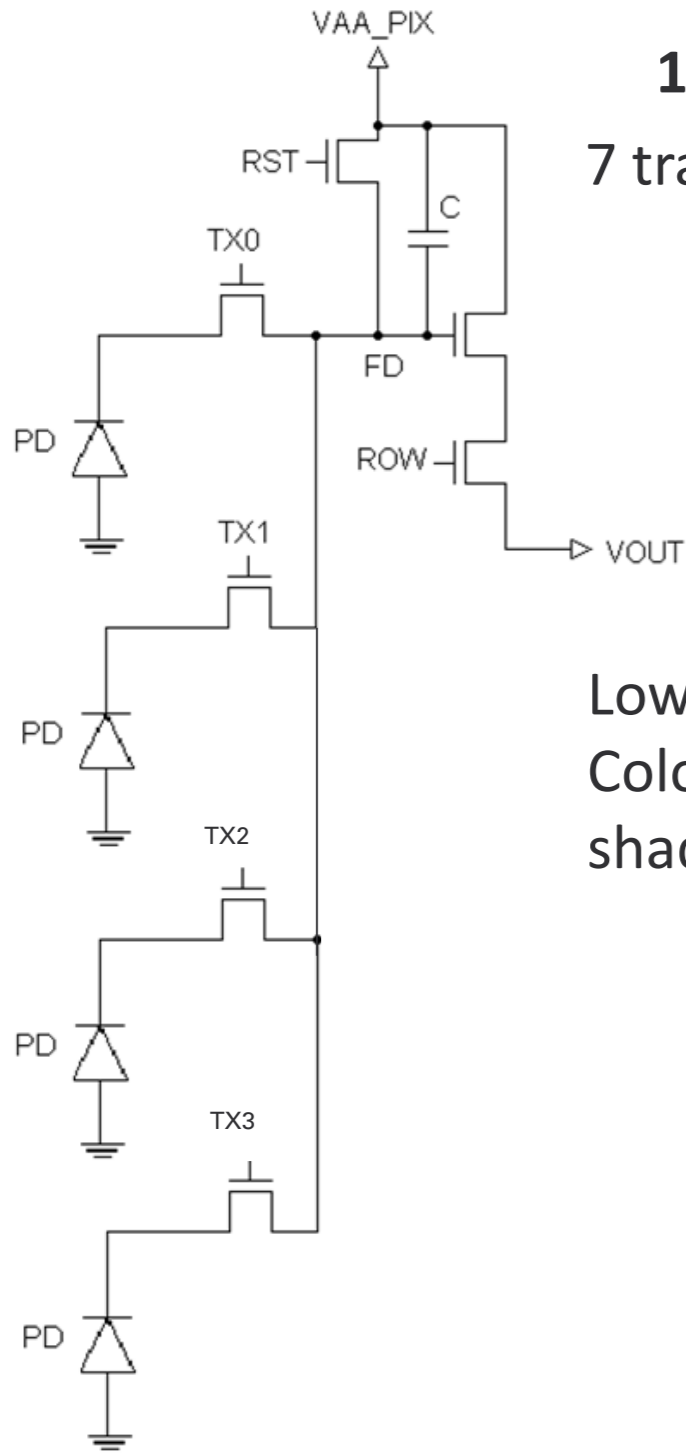
Implant masking approach:

- Resist up to 15:1 Aspect Ratio
- Hard mask

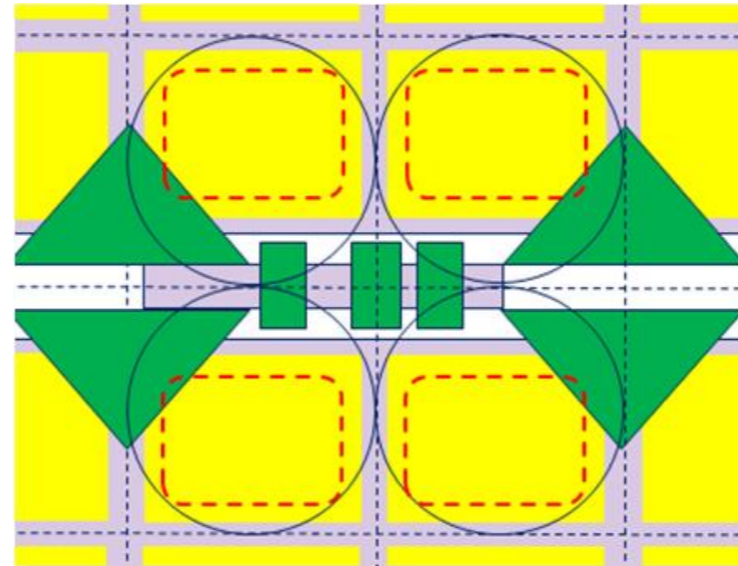


$$FF = \frac{\text{Active Area}}{\text{Pixel Area}}$$

The fill factor is the ratio between the photodiode active area and the pixel area



**1.75 T cell**  
7 transistors for  
4 pixels



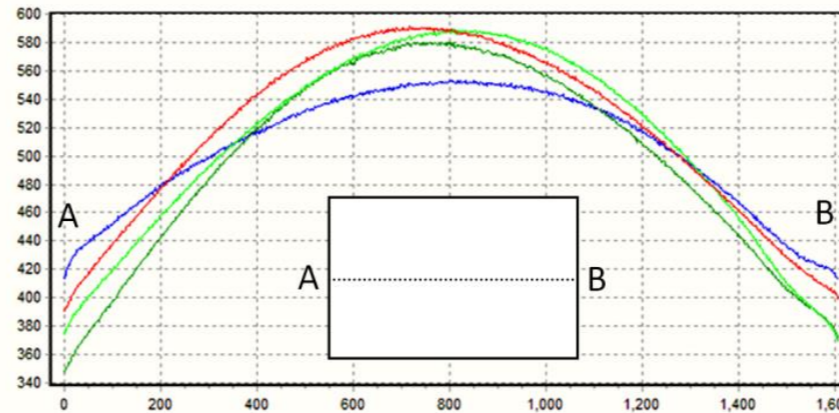
Asymmetry of layout!

Each color plane has its  
own angular response

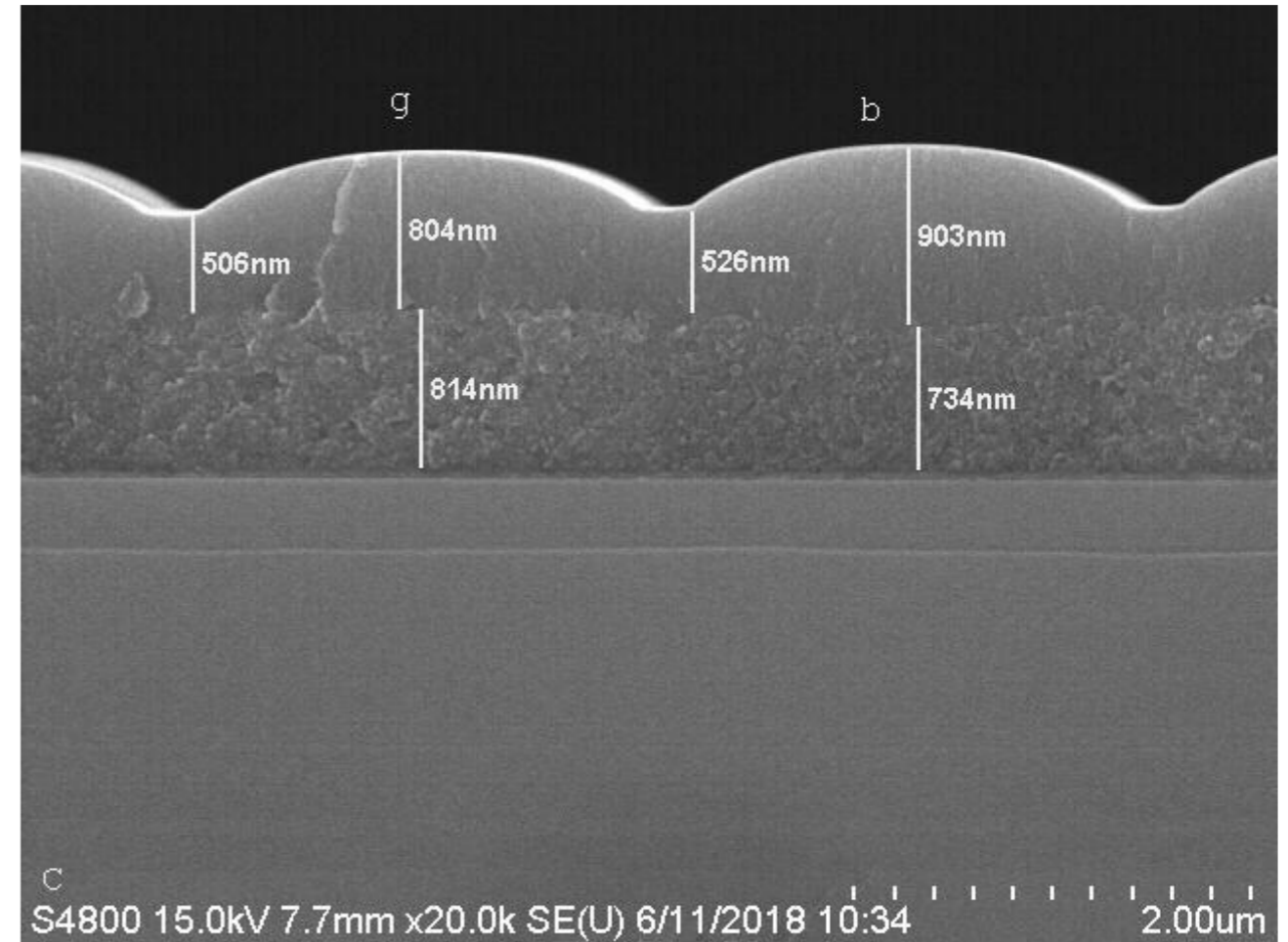
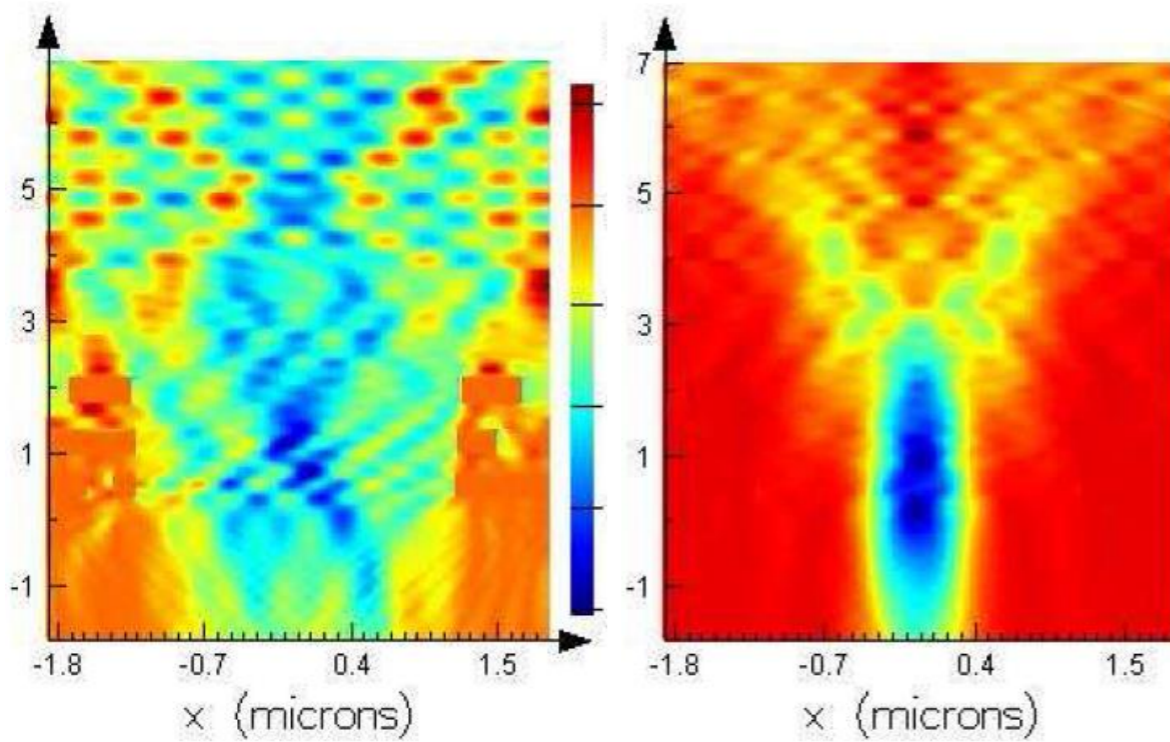
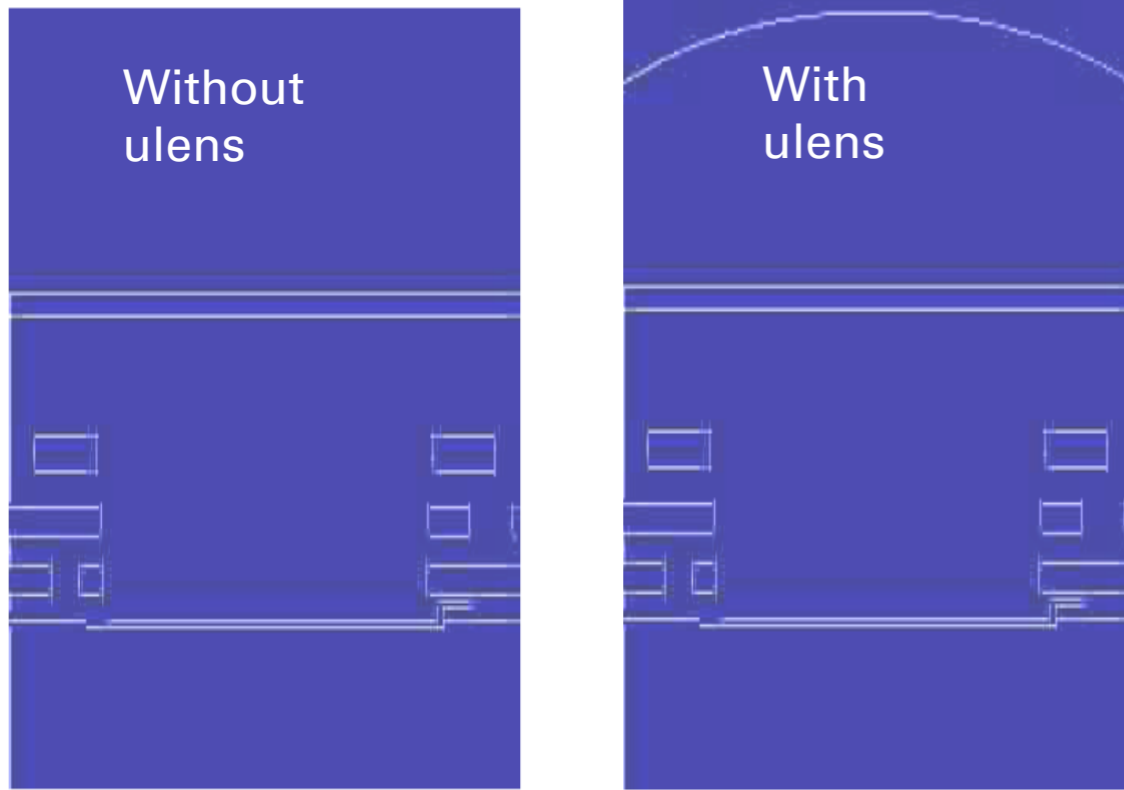
Low  
Color  
shading

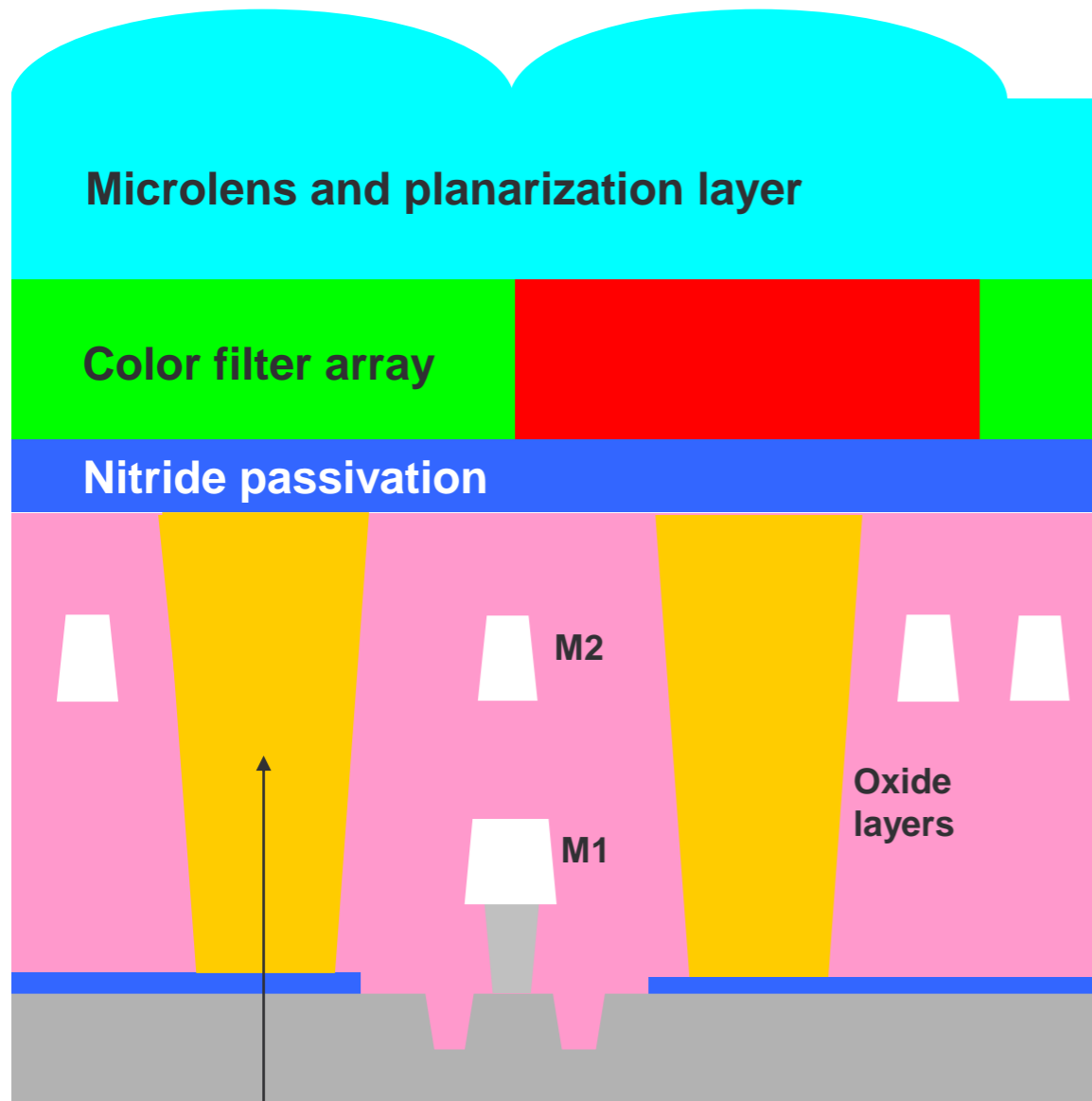


High  
Color  
shading



Response of the 4  
color planes



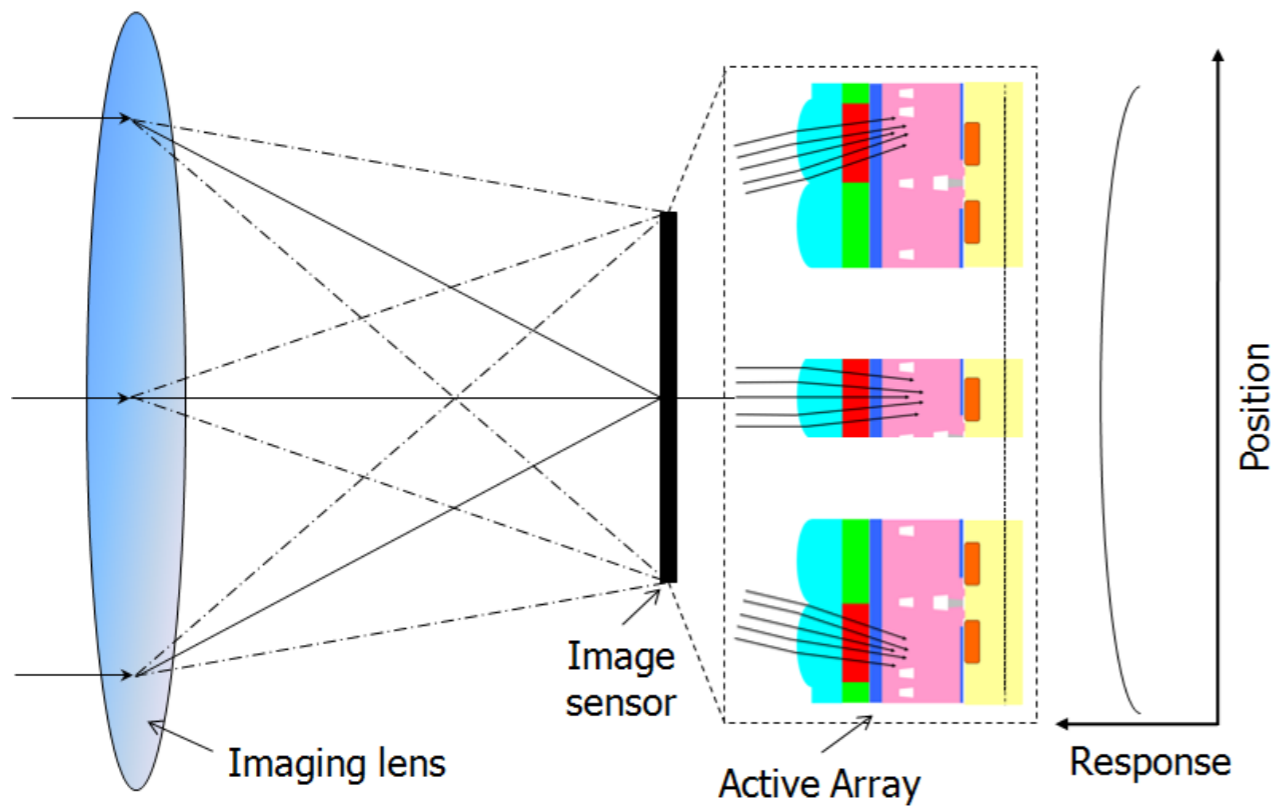


High refractive index  
Polymer ( $n = 1.6-1.7$ )

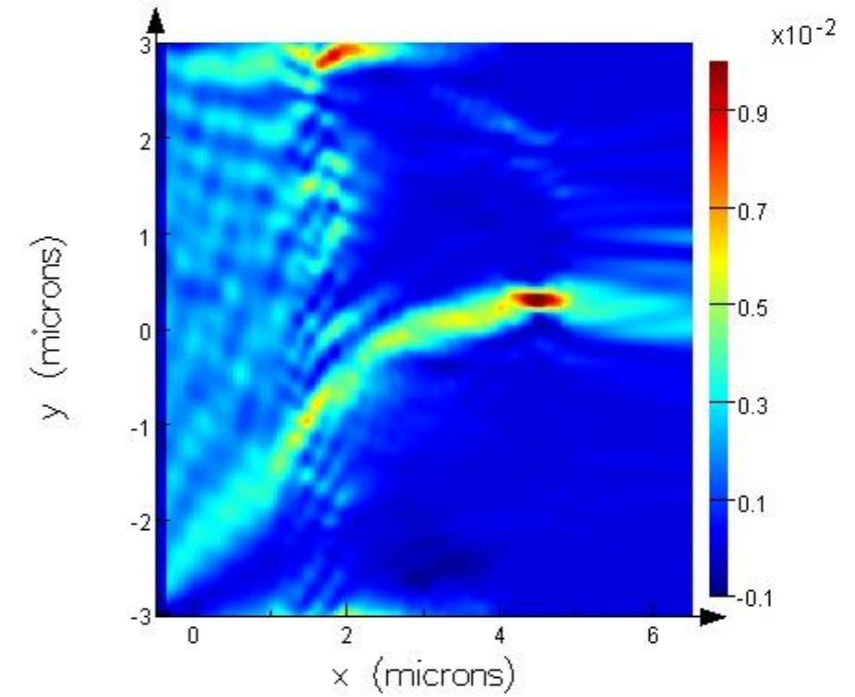
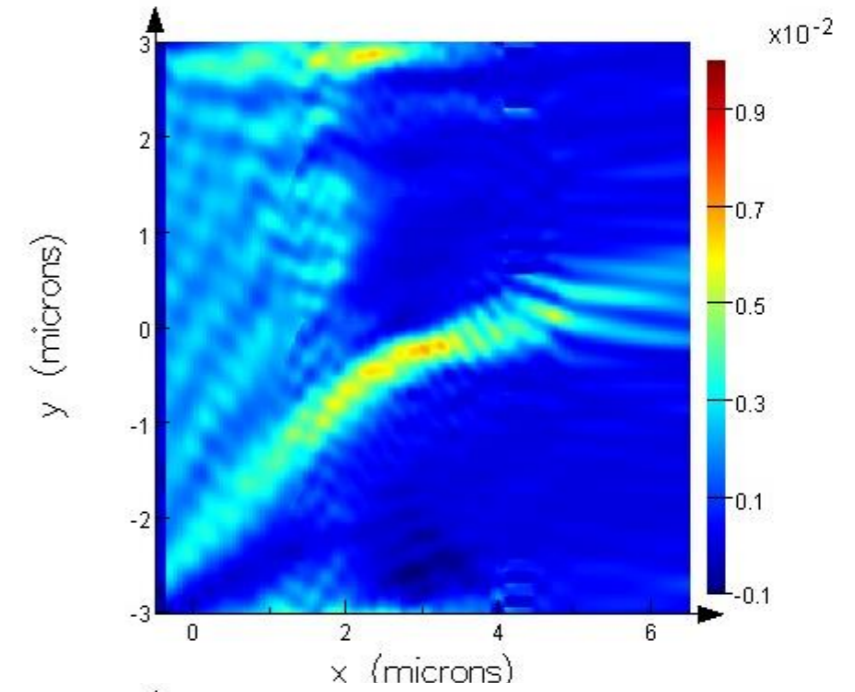




Simulation run with 25° angle of incidence



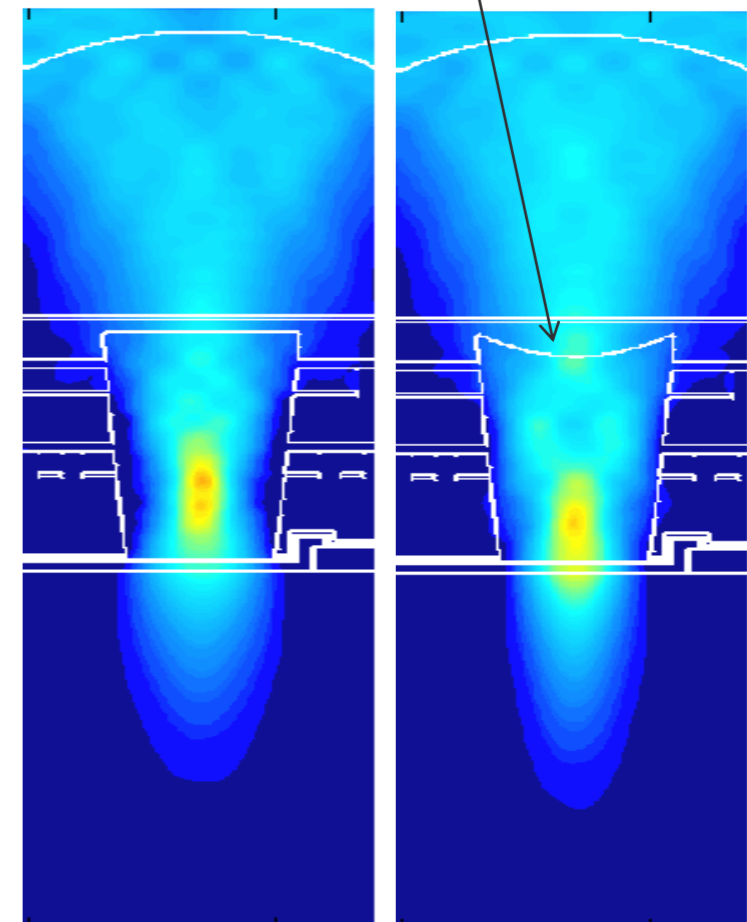
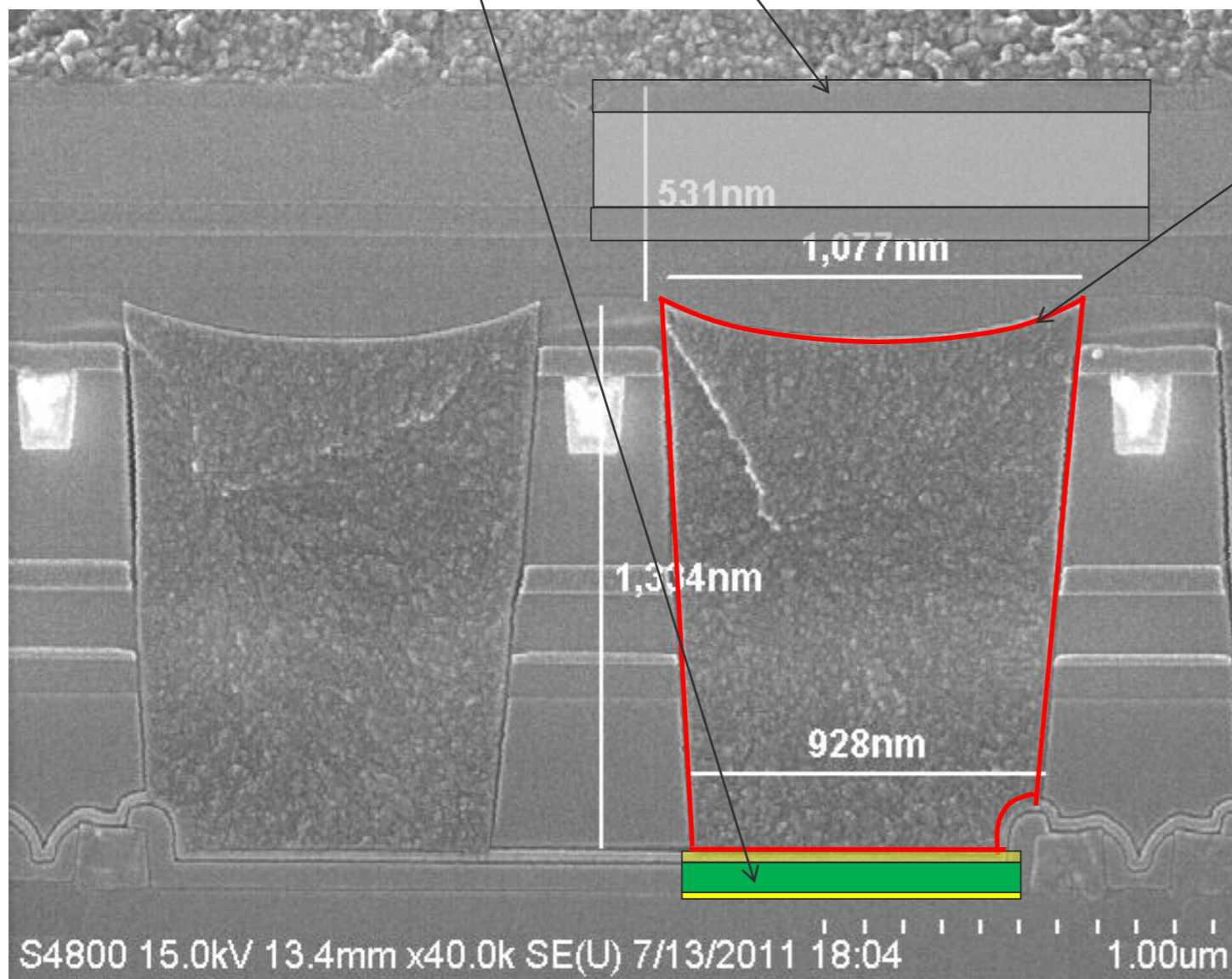
Without lightguide

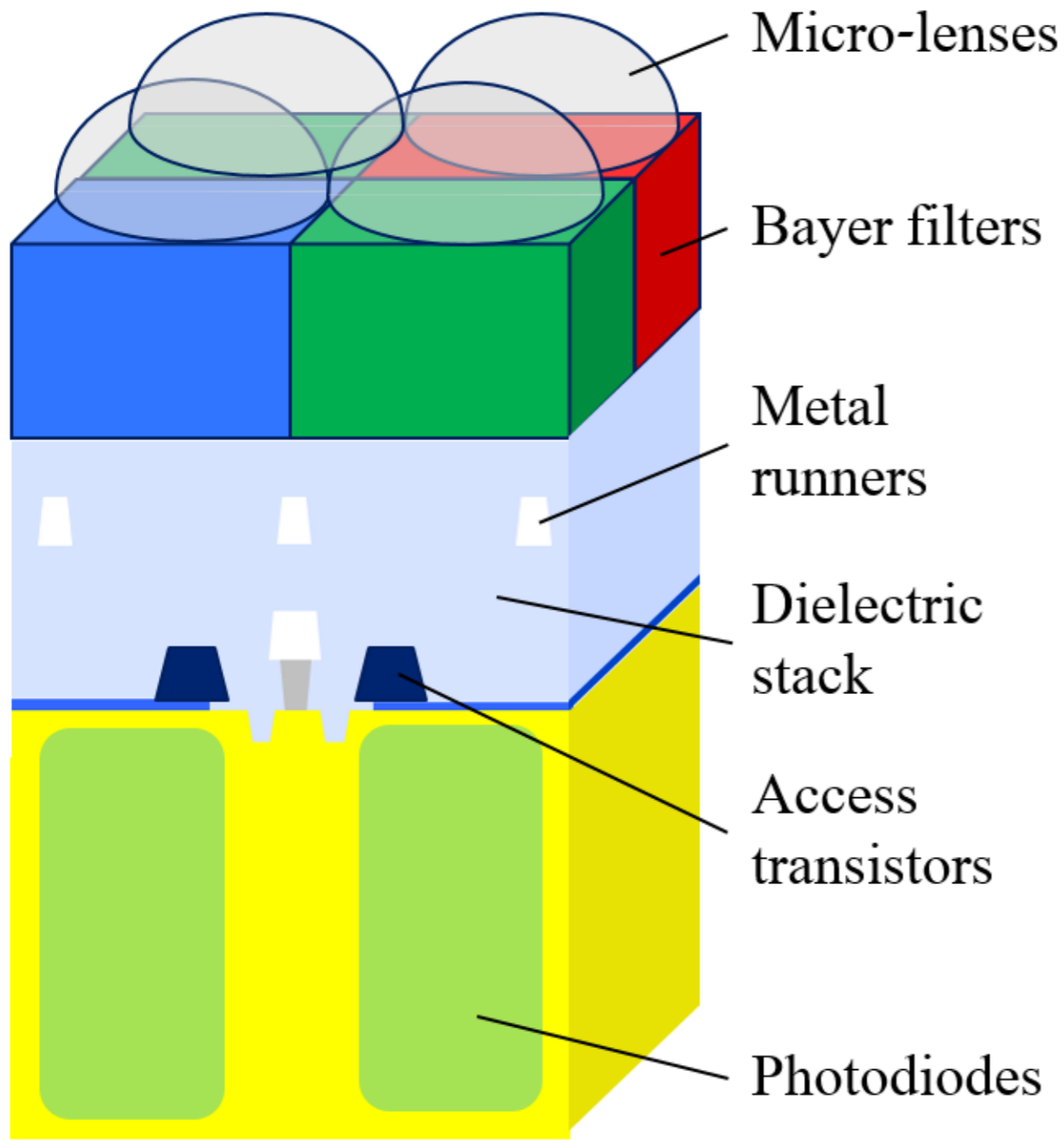


With lightguide

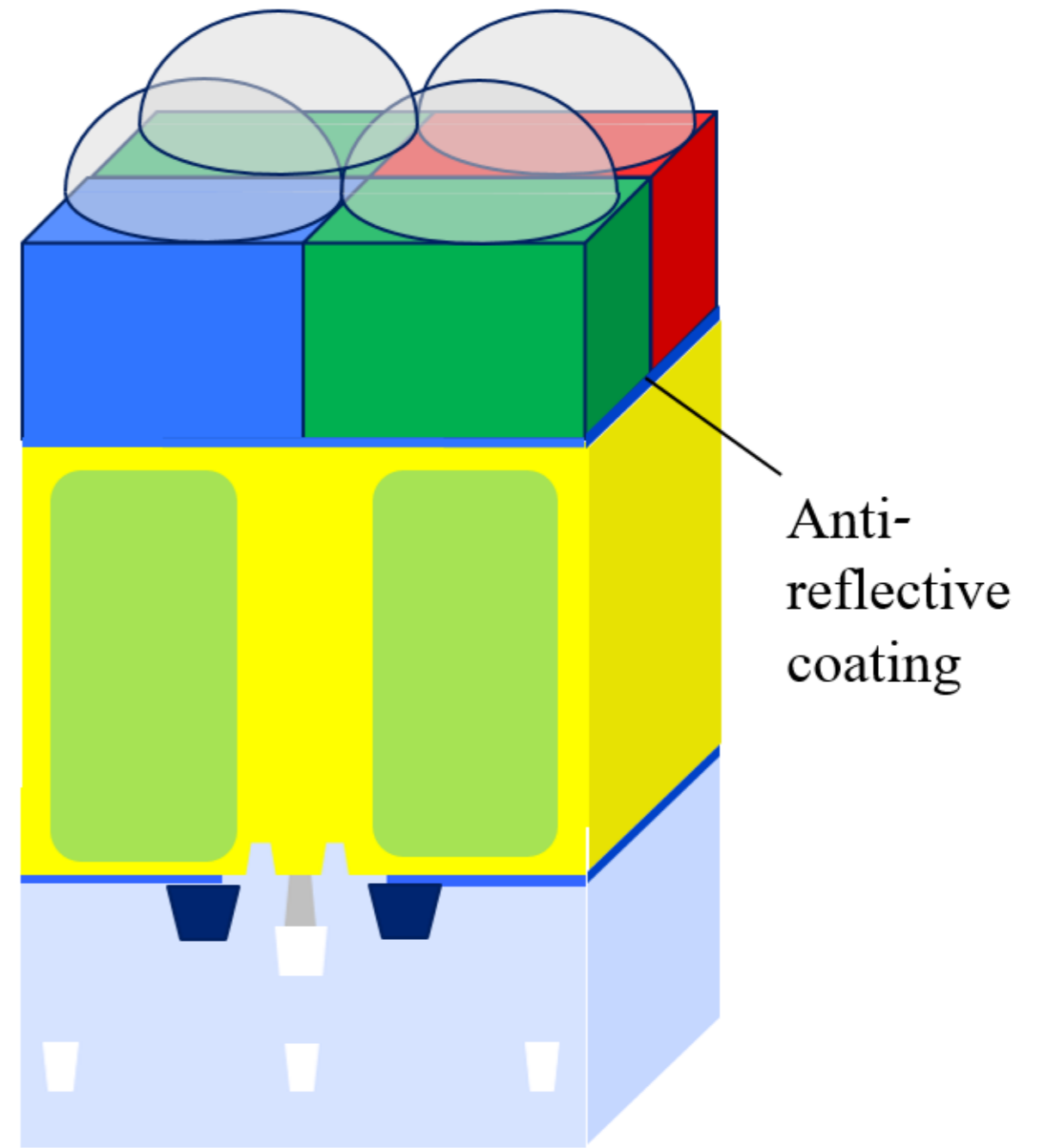
Introduction of anti-reflective coatings with proper thicknesses and refractive indexes

Optimization of the optical performance of structures present in the optical stack



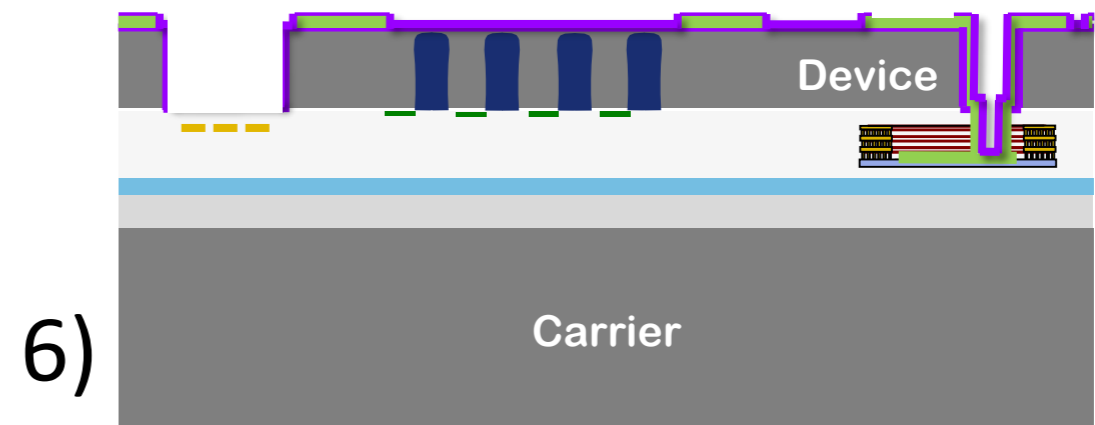
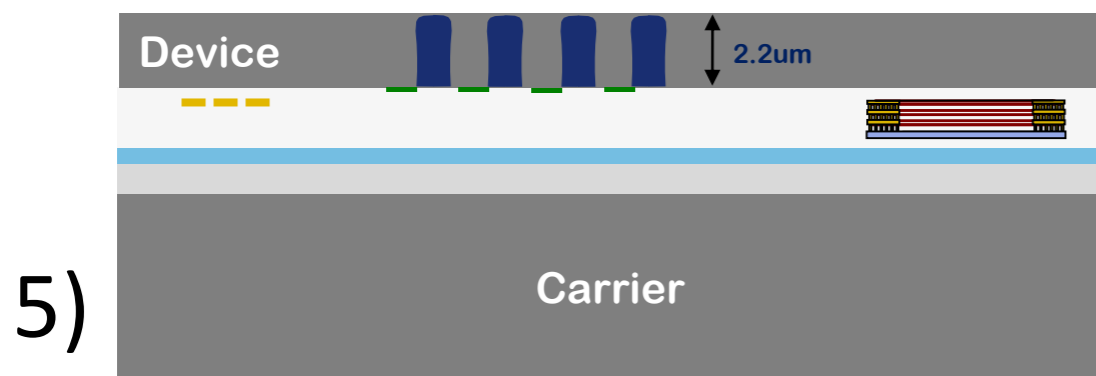
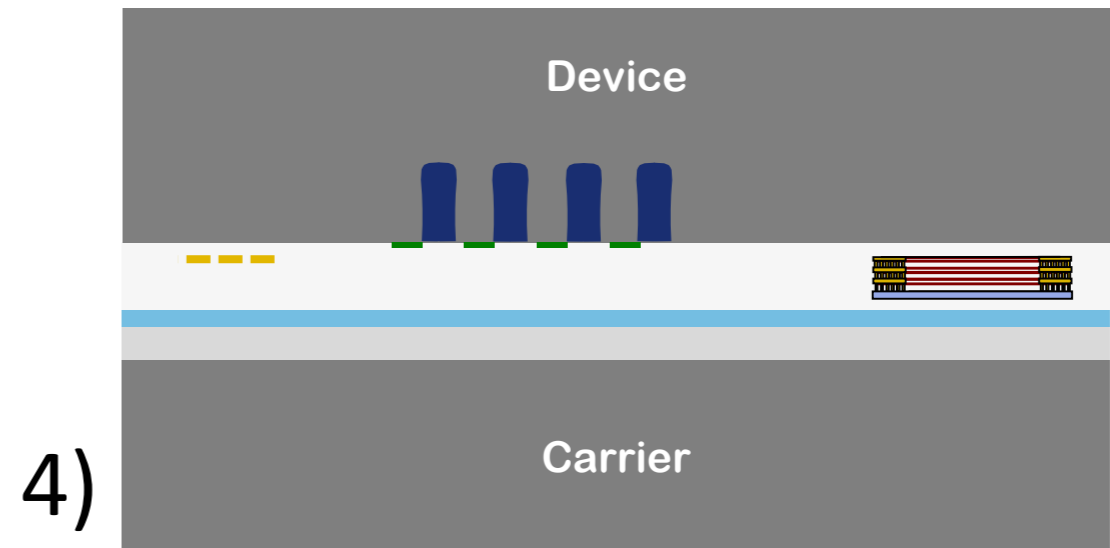
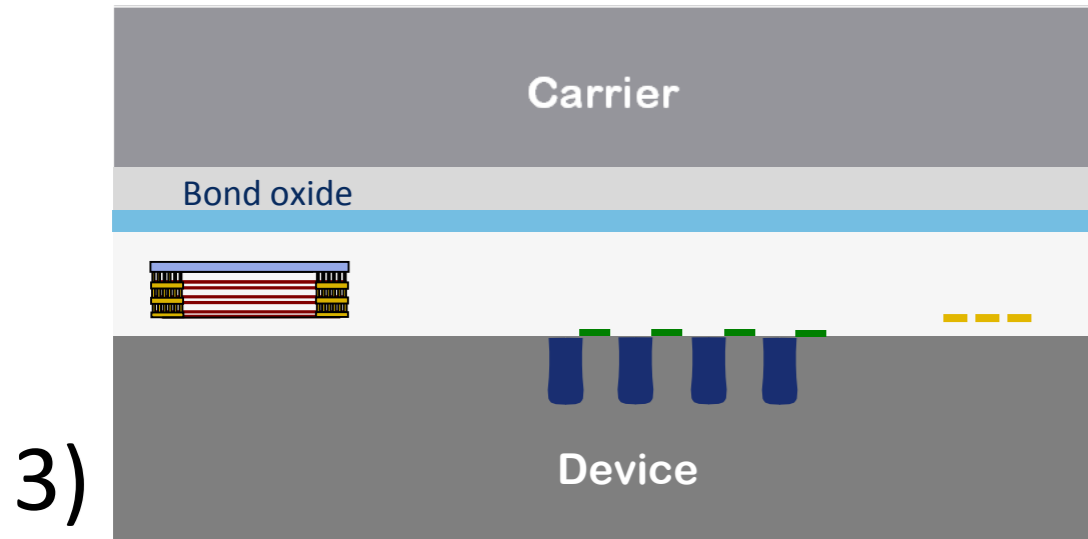
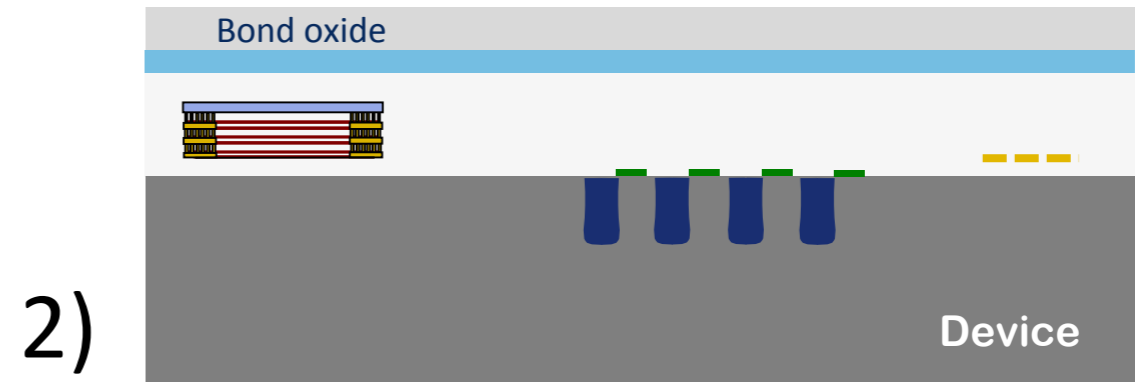
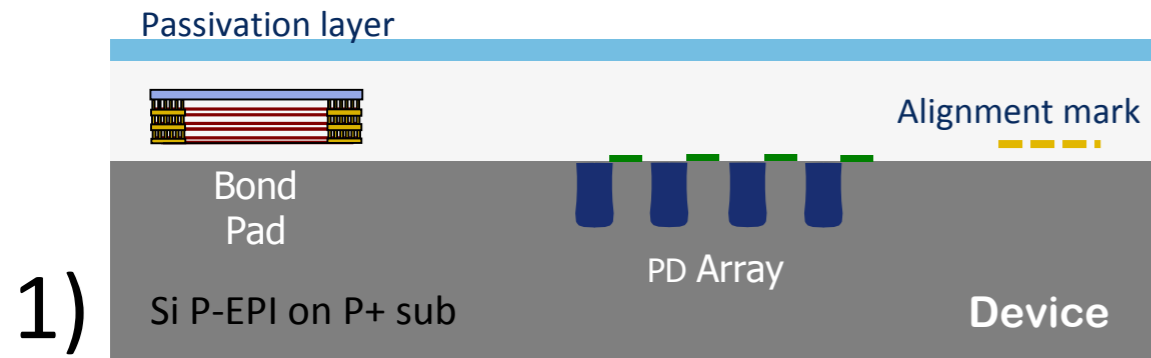


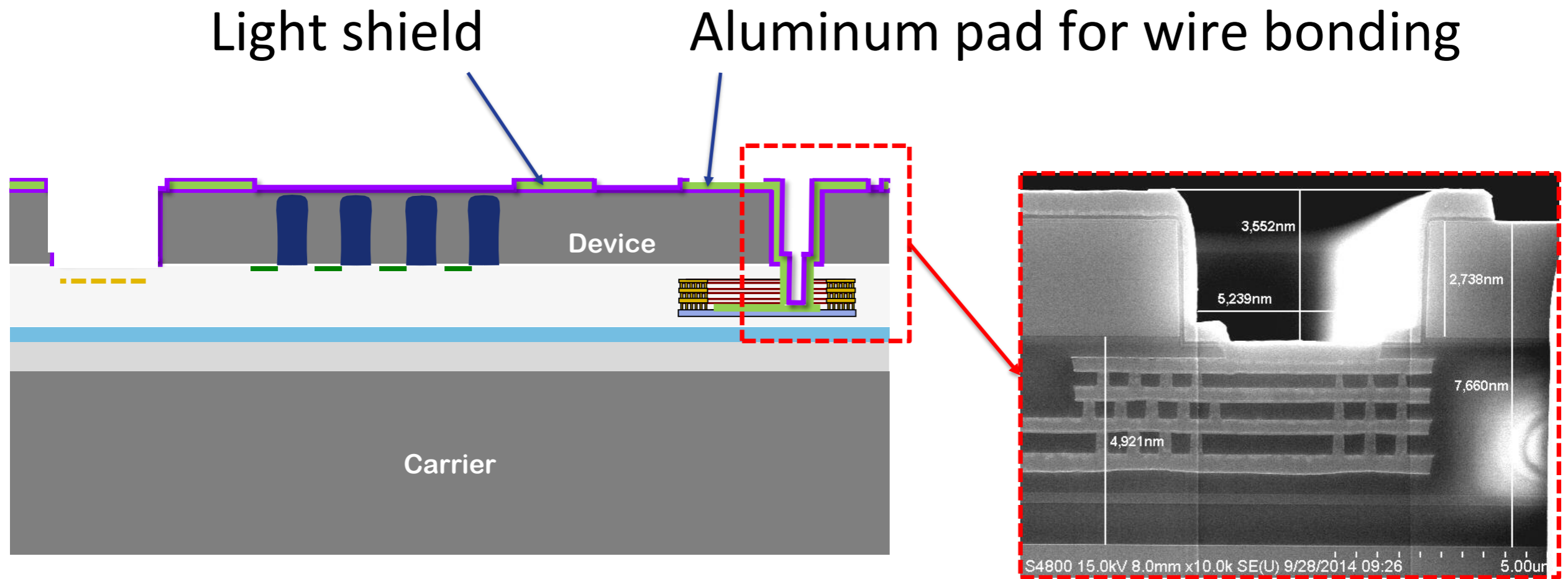
FSI

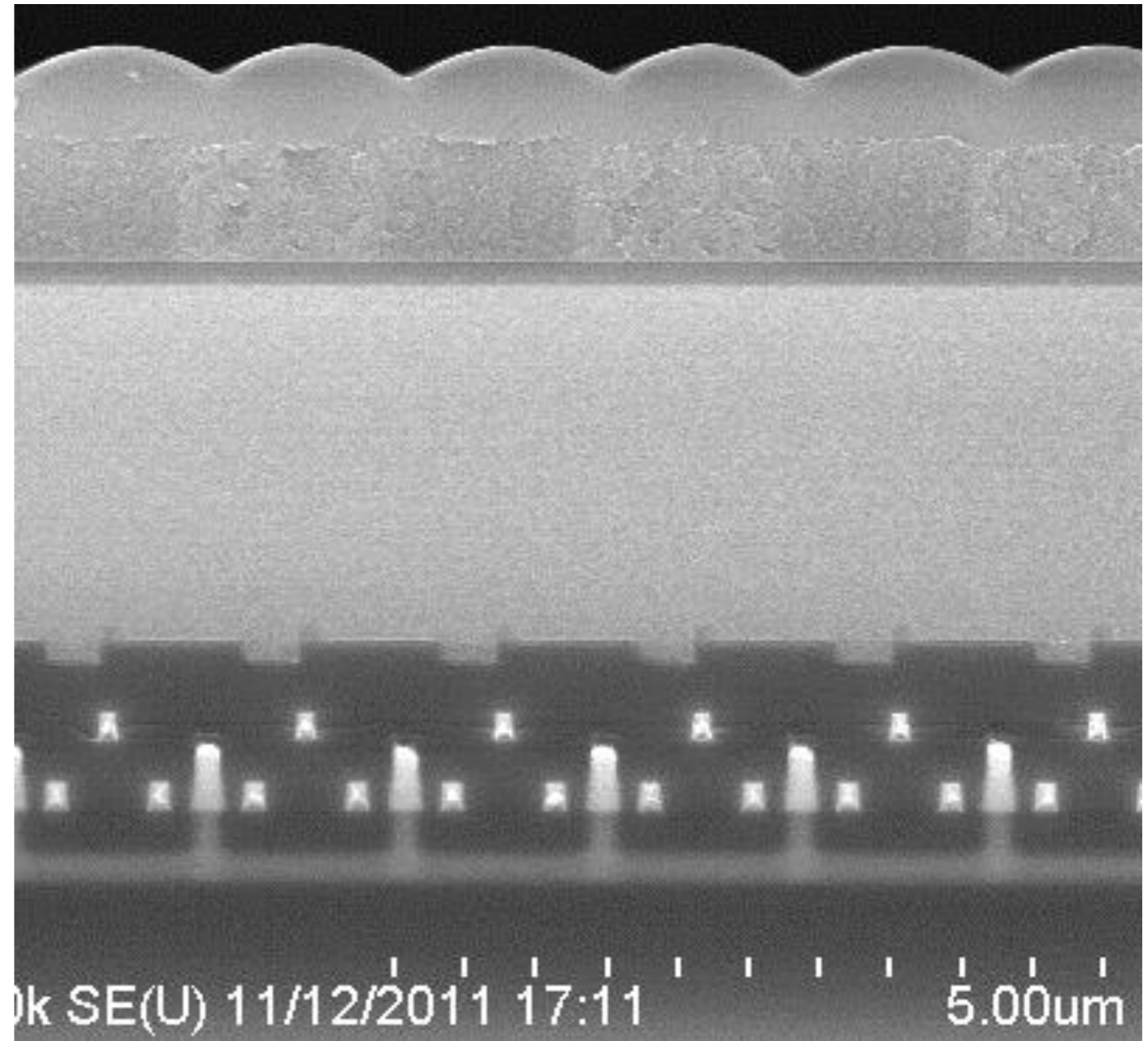
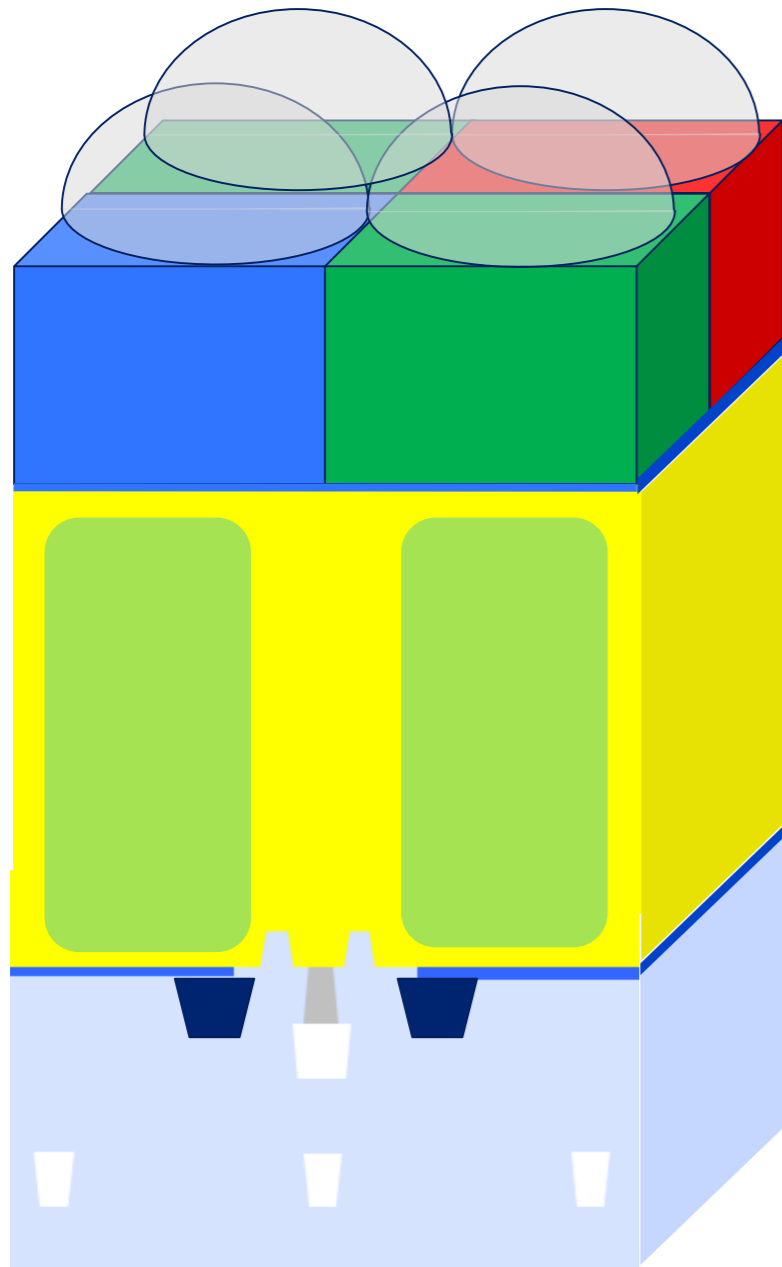


BSI

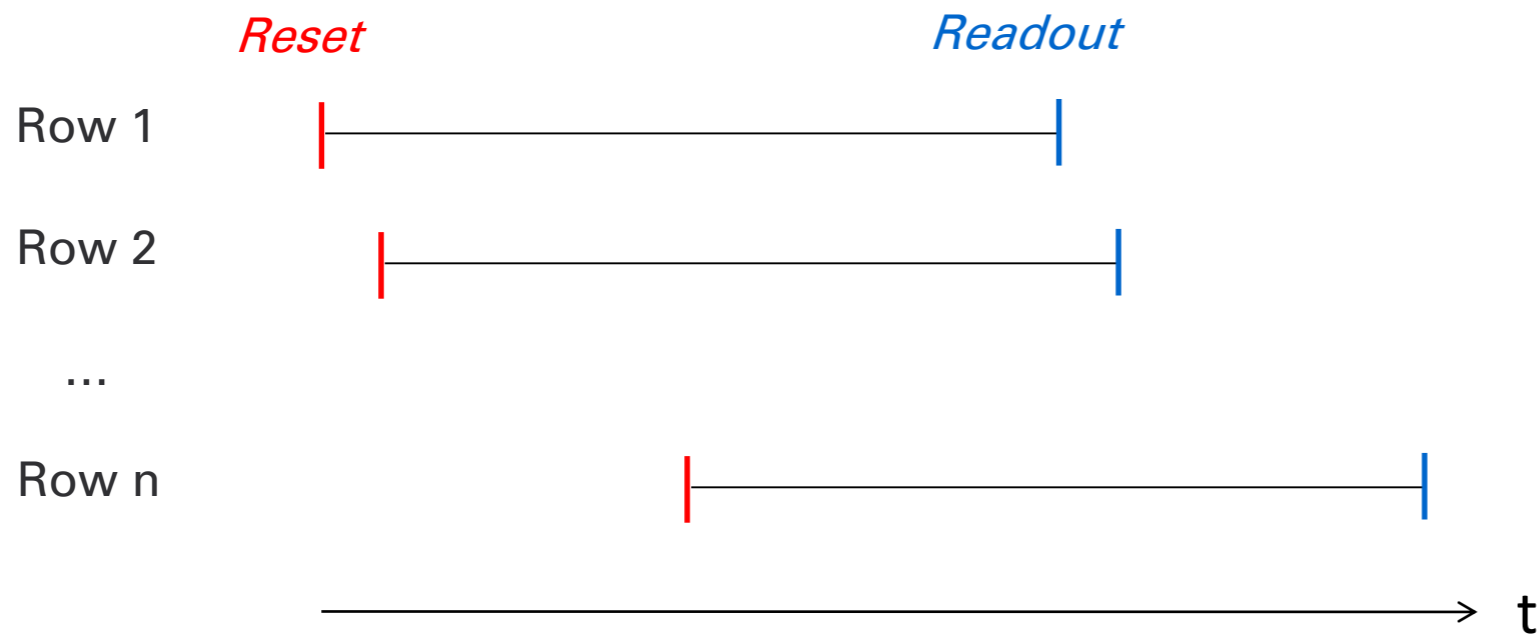
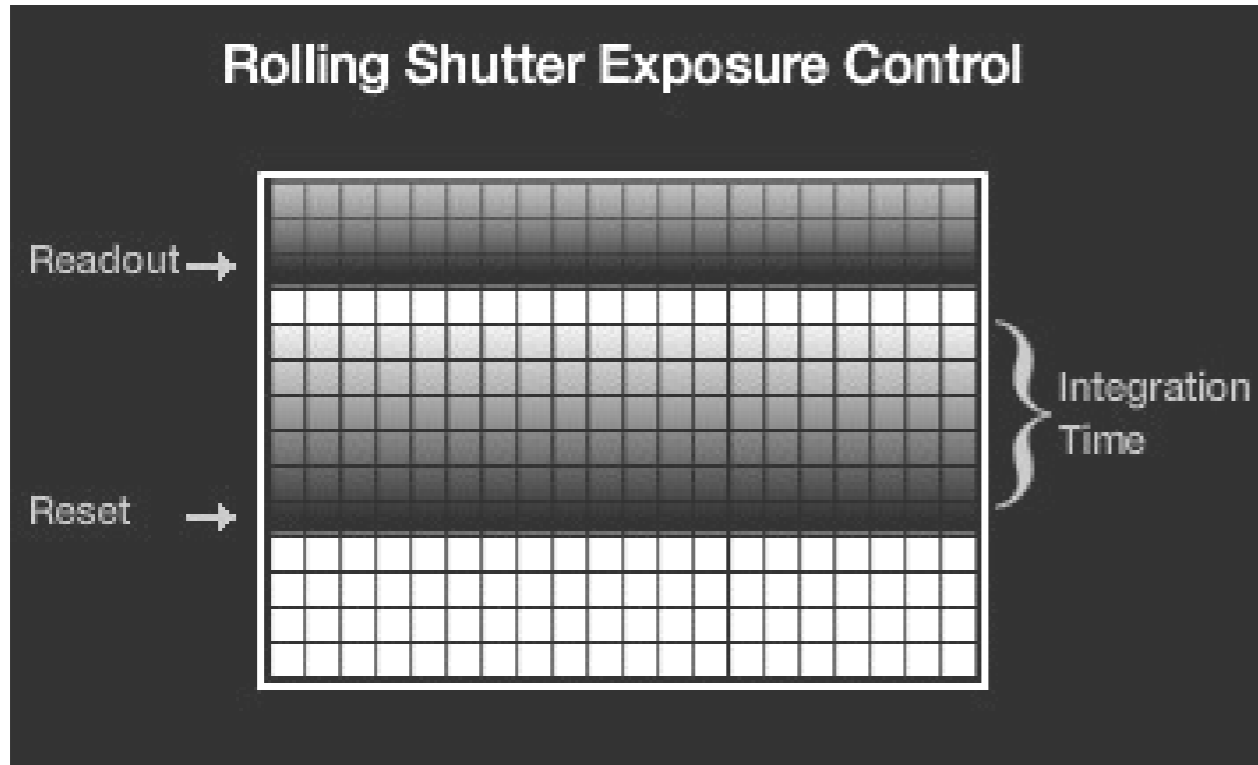
(100% fill factor)





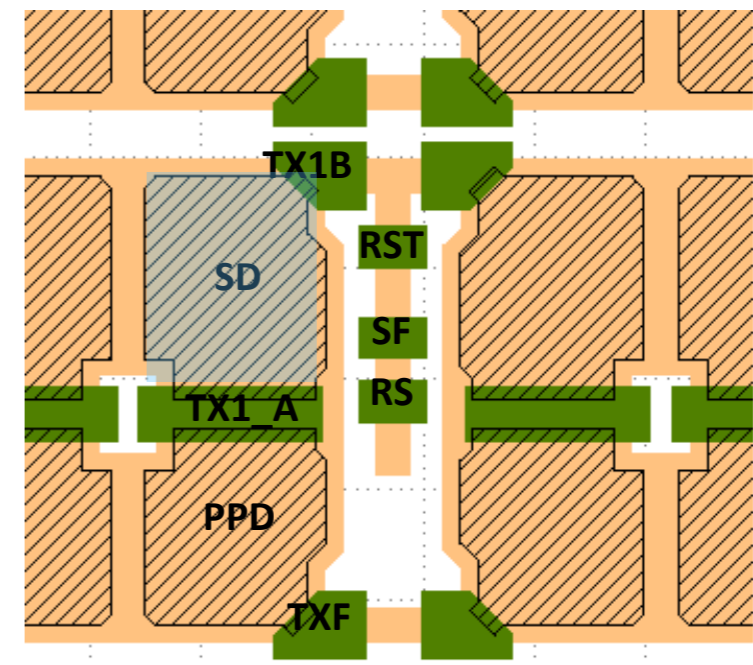
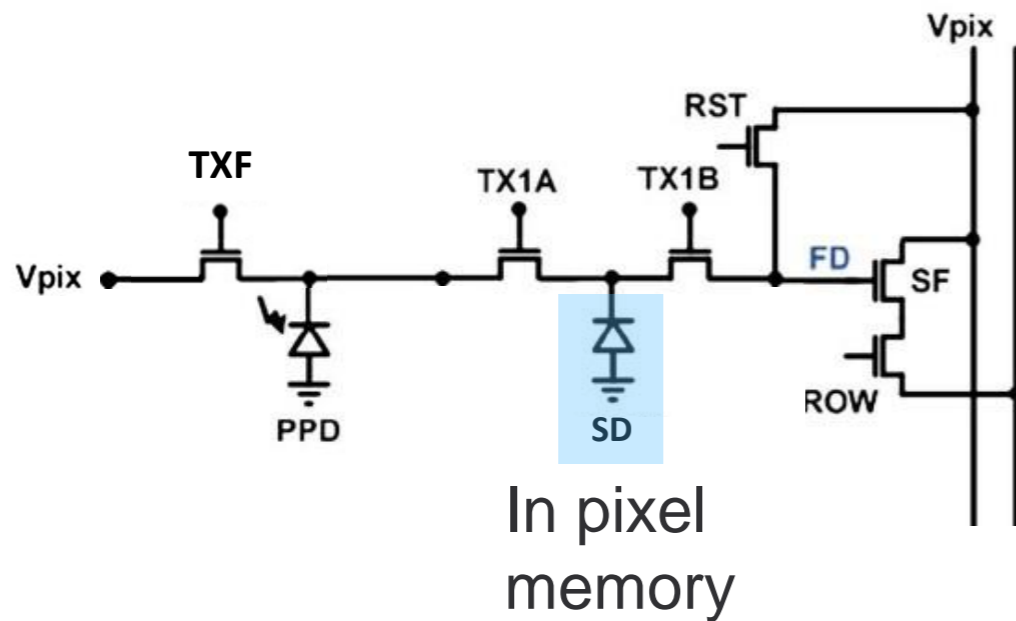


100% fill factor, stack height reduced decreasing crosstalk and improving sensor angular response



The integration time of different rows starts and ends in a different time, causing the artifacts

Introducing the “in pixel memory” all the rows start and end the integration time at the same time, while the in-pixel memories can be read row by row.



Rolling shutter artifacts

Global shutter capture

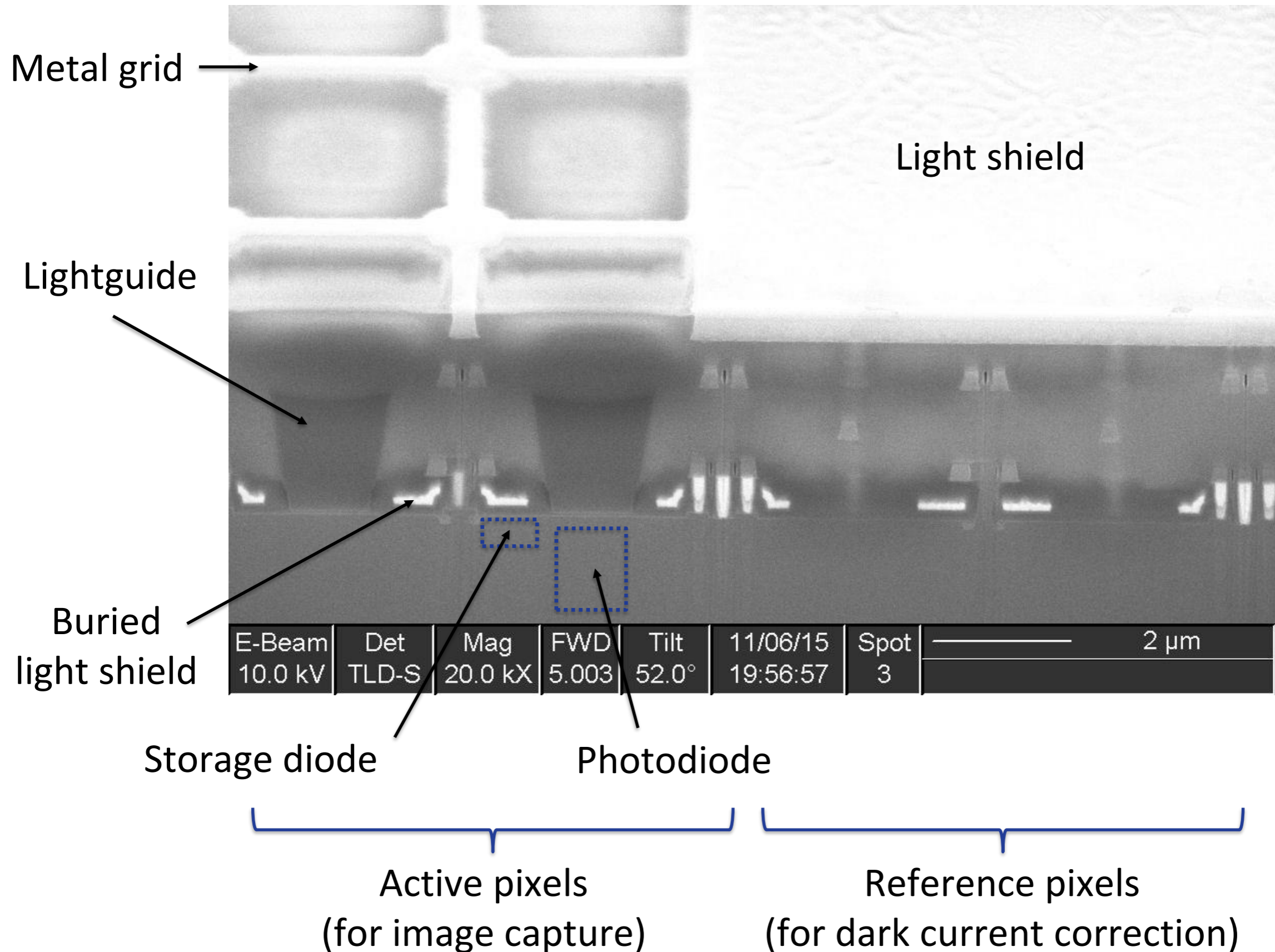
**No distortion!**

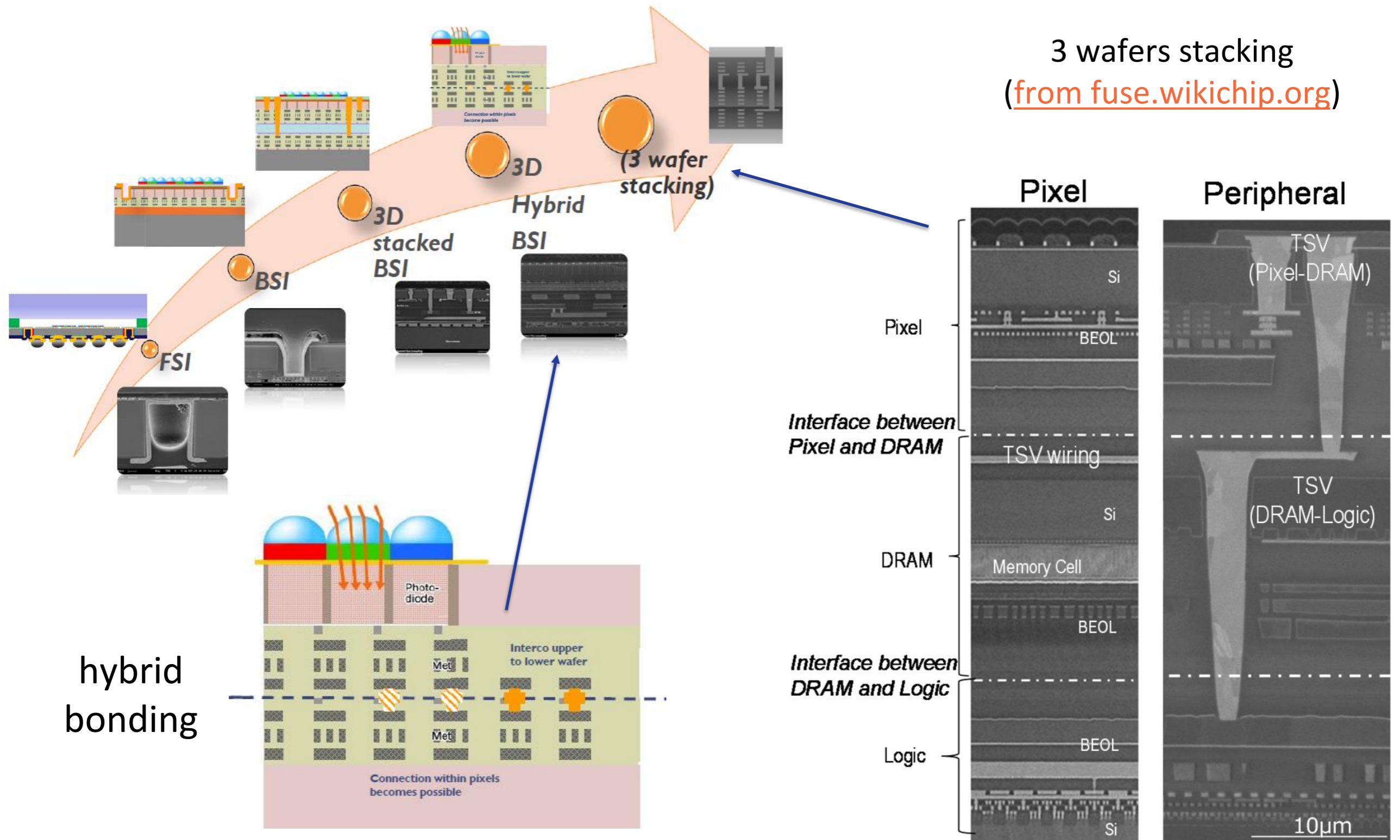
But the “In pixel memory” needs an effective shield from light!





# SEM tilted view of a state-of-art global shutter CMOS Image sensor (without filters and microlenses)





3 wafers stacking  
([from fuse.wikichip.org](http://fuse.wikichip.org))

hybrid bonding

Reduced chip size, higher speed, low power consumption

*Thanks!*