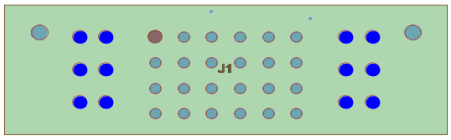
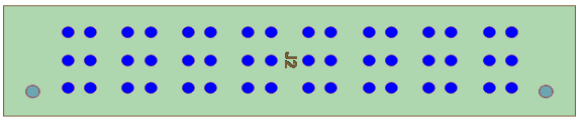
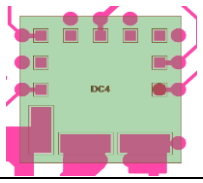
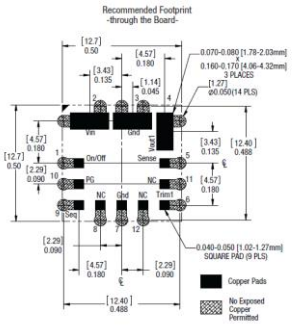
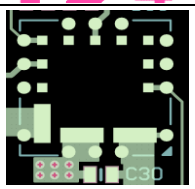
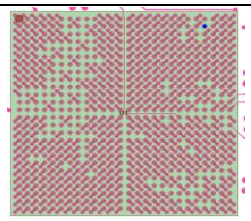
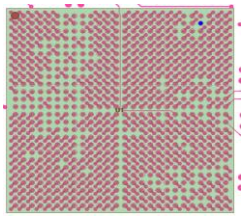
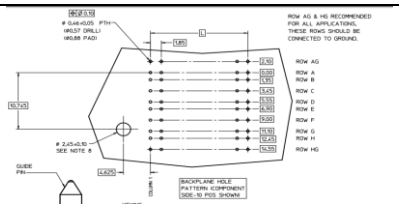
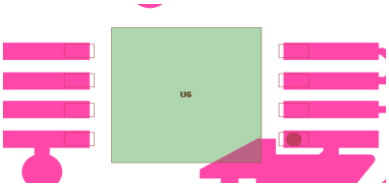
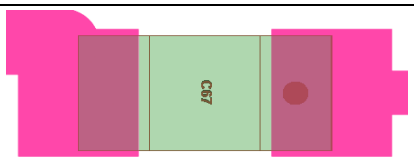
DFM issue's listed

PB Power board					
Design files = Altium, owned by KVI/NIKHEF					
Refdes	issue	Details	image	Suggested solution	Remark
J1	Incorrect drill size	12 hole sizes are 0,9906 mm. Recommended hol size is 1,04mm. Pitch should be checked		New footprint is needed with correct drill size and pitch according manufacturer datasheet	Should be corrected in source data
J2,J3	Incorrect drill size	12 hole sizes are 0,9906 mm. Recommended hol size is 1,04mm. Pitch should be checked		New footprint is needed with correct drill size and pitch according manufacturer datasheet	Should be corrected in source data
DC1,DC2, DC3,DC4, DC5,DC6	Solderpads too small	All 12 solderpads are to small of this LGA footprint	 	New footprint is needed with correct pad size and pitch according manufacturer datasheet	Should be corrected in source data
DC1,DC2, DC3,DC4, DC5,DC6	Wrong copper exposure on pads	On the additional round 14 pads on the edge of the shape should be no exposed copper.		New footprint is needed with correct soldermask sizeaccording manufacturer datasheet	Should be corrected in source data
General	Stackup file is missing	No stackup description file is in the project output.	Please provide a complete stackup file in the form of a PCB specification file. In this file items like: **layer build up, layer thickness, soldermask color and controlled Impedance specifications should be desceribed, with or without silkscreen,tolerences on thickness, copper finish (pref: ENIG), UL certification,TG value TC>150.**		-
General	No Impedance specification	No document or design layer is present where the controlled impedances are described		Please provide a document wherein the controlled impedanced nets are specified.	

DFM issue's listed

CLB board					
Design files = Allegro, owned by KVI/NIKHEF					
Refdes	issue	Details	image	Suggested solution	Remark
U1	Pad size too small	All pad sizes are too small. size = 0,508mm Recommended 0,53mm		New footprint is needed with correct pad size and pitch according manufacturer datasheet	Should be corrected in source data
U1	Soldermask wrong	Opening soldermask to small size=0,6096mm Recommended 0.63mm		New footprint is needed with correct soldermask size and pitch according manufacturer datasheet	Should be corrected in source data
J11,J12	Pitch of drill holes	Pitch of the holes are 1.8542mm (one row 1.8280mm) recommended 1.85mm		New footprint is needed with correct pitch according manufacturer datasheet	Should be corrected in source data
U6,U8	Solderpads too small	pins outside the pads, there is no heel soldering possible according IPC610		New footprint is needed with correct pad size and pitch according manufacturer datasheet	Should be corrected in source data
All 0603 and 0805 compone nts	Solderpads too small	pins outside the pads, there is no heel soldering possible according IPC610		New footprint is needed with correct pad size and pitch according manufacturer datasheet	Should be corrected in source data
General	Stackup file is missing	No stackup description file is in the project output.	Please provide a complete stackup file in the form of a PCB specification file. In this file items like: **layer build up, layer thickness, soldermask color and controlled Impedance specifications should be desceribed, with or without silkscreen,tolerences on thickness, copper finish (pref:ENIG), UL certification,TG value TC>170.**		-
General	No Impedance specification	No document or design layer is present where the controlled impedances are described		Please provide a document wherein the controlled impedanced nets are specified.	