sFGD Electronics Design Requirements – DRAFT

R. Van Berg 11 October 2019

Design requirements, in general, flow down from the physics needs and any external constraints. In addition to these specific requirements there are a number of general design principles which should also guide the detailed design:

- Maintainable for the life of the experiment
- MTBF>> expected lifetime of the experiment
- As simple and inexpensive as possible, commensurate with other requirements
- As flexible as possible, given other requirements

Physics Requirements -

- Data Rate – 10 Gb/s for entire detector – need justification (simulation and experimental) – what is available as justification – what margins should be built in?
- Time precision – the electronics should not add significantly to the inherent time uncertainty of the detector itself – an RMS result of 900 ps has been presented as the convolution of scintillator, wavelength shifting, fiber propagation and photosensor timing errors – this needs backup and justification. Note that 900 ps in quadrature with 400 ps worsens the overall timing error by 9% so that if the 900 ps is correct then the timing precision required of the electronics is probably on the order of less than 300 to 400 ps.
- Timing offsets – within a given CITIROC chip simultaneous input signals should arrive within < 200ps of each other. Chip to chip offsets can be dealt with later but those timing offsets should be known to the same 300 or 400 ps – a value large enough that such offsets can be tabulated directly from the design rather than requiring individual measurement of, say, each cable length as 300 ps is about 6 cm of cable, much cruder than the mechanical errors probable in fabricating such cables.
- Absolute time with respect to the accelerator clock ?? Need more information on the accelerator time information that is available to the sFGD via the T2K Slave Clock Module – need definition of available signals, their errors, etc.
- Charge sensitivity – a few photons minimum – needs backup and justification.
- Charge dynamic range – ~500 photons max?? – needs backup and justification.
- Charge error - ???
- What else??

Requirements – Master Clock Board

- Take clock and beam synchronization signals from T2K Slave Clock Module and distribute appropriate clocks and synchronization signals to the OCC in each crate and to the TOF system.
- Maintain timing precision, jitter and offsets in order to meet the Physics Requirements.
- Reside in on-detector crate and abide by those space and cooling restrictions.

Requirements – Optical Concentrator Card

- Take clock and synchronization signals from MCB and distribute them to the FEBs in the crate.

- Take slow control data from the slow control system and distribute it to the FEBs and the local FPGA.
- Provide a means, via slow controls, to reload the FPGA on the OCC.
- Provide a means, vis sloe controls, to reload the FPGA on any FEB.
- Provide voltage turn-on / turn-off control to each FEB in the crate.
- Take high speed detector data from each FEB in the crate and concatenate that data into a single stream to the DAQ system. Transfer that data to the DAQ via an optical link.
- Monitor the crate and data streams as needed and report errors, etc. to the DAQ and/or slow controls.

Requirements – Power System

- Provide regulated, low noise, DC power to the FEBs and the OCC in the crate.
- Derive the low voltage DC sources from a high voltage DC input (48V??) from outside the magnetic environment.
- Be able to operate properly in a magnetic field of >1T or???? Need backup and detailed field maps.
- Monitor voltages and currents and provide feedback to slow controls.

Requirements – Signal Backplane

- Provide direct LVDS connections between each FEB data source and the OCC.
- Provide direct slow control connections between the OCC and each FEB as well as the power board(s).
- Provide a signal path from the OCC capable of reloading the FPGAs on any or all FEBs.
- Provide low voltage high current DC supply paths to and from the FEBs and the power board(s).
- Provide geographic addresses for each card (?).