EDMS cover page

Super FGD / Master Clock Board

DOCUMENT INFO

EDMS Reference	
Title	Master Clock Board Specification V1.0
Brief description	
Type	Specification
Authors	Y. Favre
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Status	In Work

DOCUMENT HISTORY

Description	**Date**	**Version**
Document creation/modification date		v1.0
EDMS Upload date		

CONTENT

1 Context

The Master Clock Board (MCB) is the main organ for the synchronization of the entire Super-FGD sub-detector. It provides common clock signal and synchronization serialized bit stream signal which are feed into each FEBs crate.

The number of crates is equal to 16 (8 per detector side) and is equal to the fanout capability of the MCB.

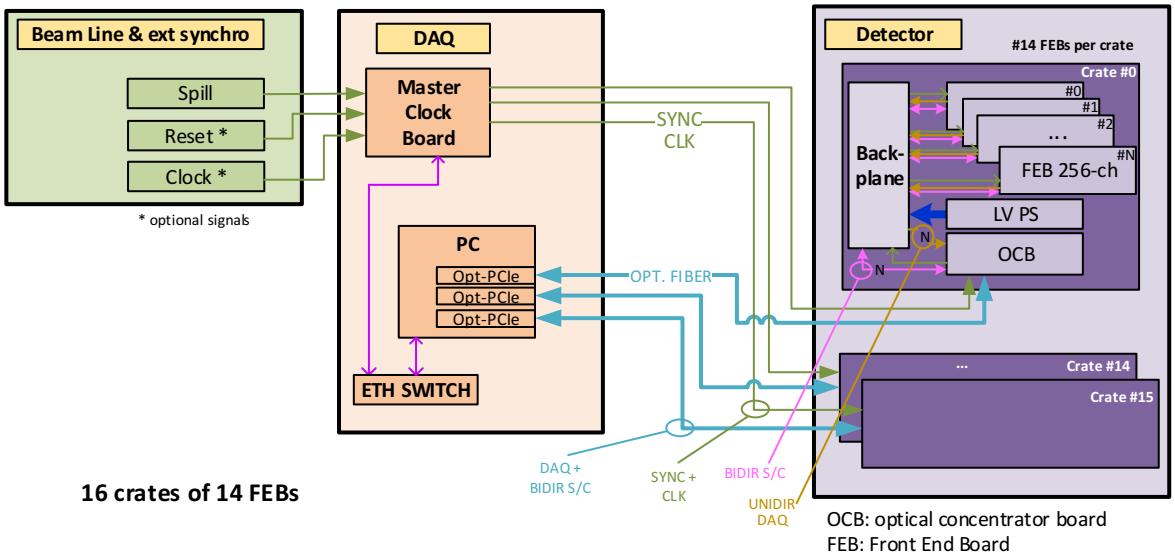


Figure 1: Super-FGD architecture

2 MCB architecture

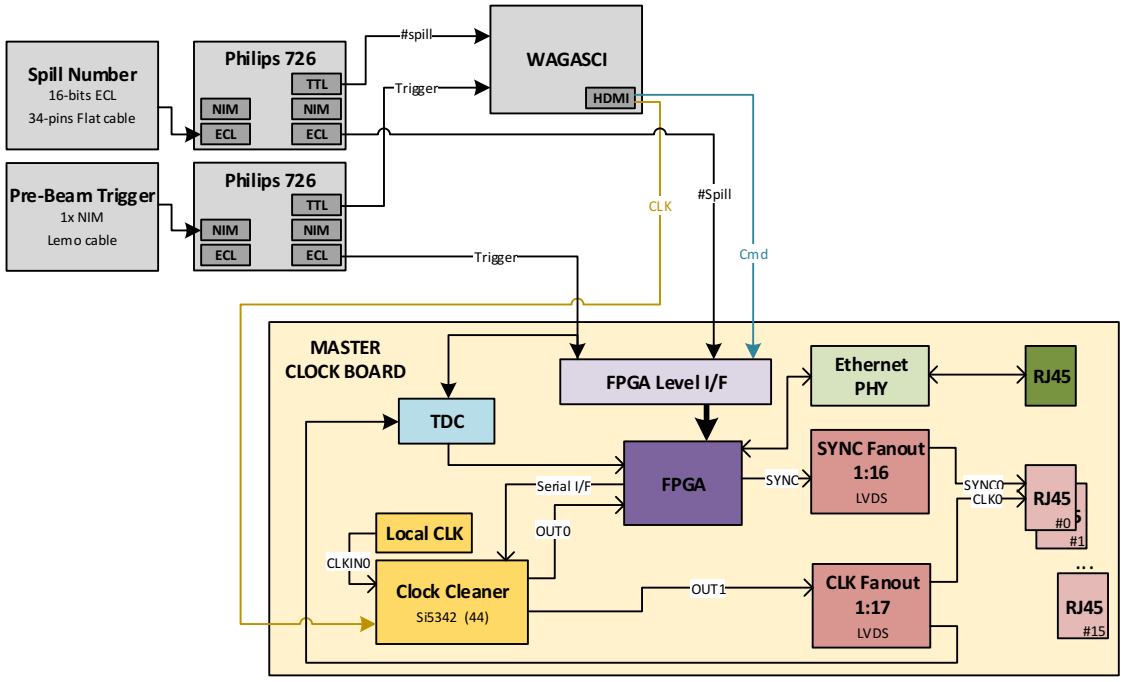


Figure 2: Master Clock Board block diagram and external signals environment

The above figure shows the Master Clock Board and the external signals connected to the board in a WAGSCI environment. This might differ for SuperFGB but this is a good starting point.

The MCB is composed of the following elements:

- **FPGA**:
  - Is driven by
  - Communicates with PC through Ethernet PHY for configuration and monitoring
  - Generates SYNC output signal from external input signals (Spill number, trigger and/or cmd signal)
  - Configures and retrieves information from TDC
  - Configures the clock cleaner
- **TDC**: measure precisely the arrival of the Trigger signal with respect to selected clock
- **Clock Cleaner**: The IC Si5342 is a good candidate. It allows ultralow jitter (90fs) and generates several outputs (2 for 42, 4 for 44). Several inputs are available for the clock selection and a switch can be done from one to another without any glitch (hitless input switching mode) when the 2 clock inputs are in phase (must have same frequency). It is configured by the FPGA
- **FPGA level I/F**: this interface changes the external levels into LVDS or Single Ended (TBD) signals acceptable by the FPGA I/O.
- **Ethernet PHY and RJ45**: this is the physical chip interface for Ethernet
- **SYNC fanout:** This chip(s) will fan-out from 1 input to 16 LVDS outputs the SYNC signal generated by the FPGA and containing all serialized information

required by the FEB for its synchronisation. The constraints on the jitter and slack are not as tight as the clock signals since the SYNC will be latched in the FEB wrt clock signal

- **SYNC clock:** this chip(s) will fan-out from 1 input to 17 LVDS outputs the CLK signal generated by the clock cleaner. The output signals should have a low jitter (TBD) and eventually a way to be phase shifted precisely in order to compensate any cable length difference from crate to crate
- **RJ45 for crate:** 16 synchronisation connectors, 1 for each crate providing SYNC + CLOCK LVDS signals

3 Synchronization principle

1.1.1 FEB synchronisation principle with MASTER CLOCK board

The following paragraph and its figures are copied from Baby Mind specification and should be updated for Super-FGD but this is a good starting point.

In order to synchronize precisely multiple boards, dedicated synchronisation signals are available and driven by a master clock board. Every FEB is connected to this master board in a star network having the same cable length between the master board and its own synchronisation connector(s).

The required signals are CLOCK, GTRIG, FS, RESET and SPILL GATE:

- CLOCK signal (typical 50 or 100 MHz) is used in order to synchronize precisely the TIMING block of all FEB. All FEB will sample the timing information of the signal at the same time. **The Master clock board is responsible of global clock precision (jitter, shift…) for a proper timing measurement of the overall system**
- GTRIG signal is synchronous with the CLOCK and provide the typical 10 µs (100 KHz) time stamp in order to avoid 10.24us overflow of the Timing counters (12-bits counter running at 400MHz). This will lead to GTRIG header/trailer data encapsulation
- FS (Frame Synchronisation) is used to work in TDM when FEB are chained (see §**Error! Reference source not found.**)
- SPILL GATE and SPILL number is not compulsory but can be used in order to stop the data flow when the window is closed rather than having GTRIG header/trailer without events. It can also be used to switch to calibration mode when the window is closed, allowing dark noise and/or cosmic measurement.
- GRESET is not compulsory but can be used to assert a signal allowing a synchronous reset of FIFO and/or counters.

In order to save cabling and use the 4 pairs of the RJ45 'SYNC' connector (see **Error! Reference source not found.**) 3 pairs are used:

- 1 pair is dedicated to the CLOCK signal (typically 100MHz) from a GPS or MCM (Master Clock Module) of ND280 or local quartz on the board itself
- 1 pair (SYNC) is dedicated to the GTRIG + GRESET + FS + SPILL GATE signals which are multiplexed where different pulse width carries the information. All the signals are synchronous with the CLOCK and the GTRIG signals i.e. an update at the GTRIG period for RESET/FS/BEAM :
    - 1 bit for GTRIG
    - 2 for FS (FS is always synchronous with GTRIG)
    - 3 bit for GRESET (GRESET is always synchronous with GTRIG)
    - 16-bits for SPILL number which is encoded serially from a parallel 16-bits information (ECL on flat cable or 16 NIM signals) coming from the beam line synchronously with the PRE-BEAM trigger
- the 2 other pair remains unused (one is reserved as an auxiliary pair in parallel of SYNC, i.e. form MCB to FEBS, and the other as a upstream pair if the FEBs wants to send back information to MCB)

Error! Reference source not found. shows the synchronization scheme.

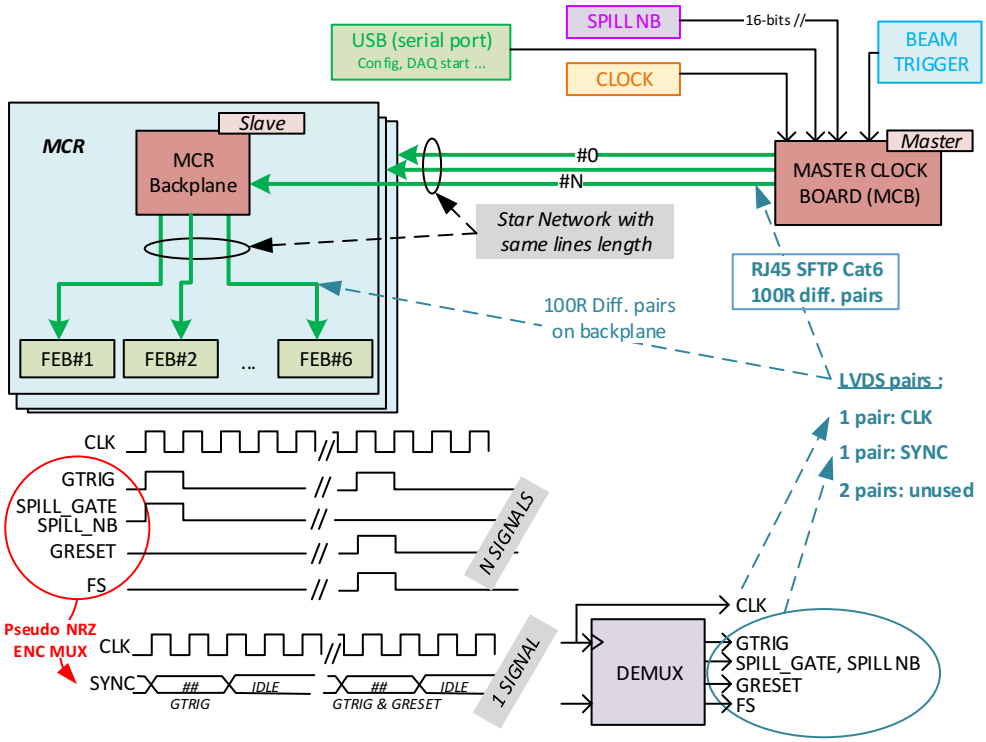


Figure 3: Synchronisation scheme in baby-mind experiment architecture with 1 Master Clock Board (MCB) shaping SPILL+RESET+CLOCK+SPILL GATE (pseudo-NRZ encoder and multiplexer) and propagating signals over 4-pairs RJ45 LVDS over all MCR FEBS (1 to 9 star fanout n)

1.1.2 FEB synchronisation protocol with MASTER CLOCK board

The following paragraph is copied from Baby Mind specification and should be updated for Super-FGD but this is a good starting point.

The data are encoded with a pseudo NRZ code.
If no data are to be sent then the SYNC signal is oscillating at 1MHz i.e. IDLE state.
If data are to be sent i.e. upon GTRIG or SPILL event then the frame is sent and the SOF word is set depending of the previous level of the SYNC signal : if previous value = 0 then SOF = 1011, else SOF = 0100. This ensures a unique recognition of the start of frame whatever the IDLE state is.

The frame is composed of 5x8-bits (including SOF) + 2-bits of EOF (00) and details are described below:

	8	7	6	5	4	3	2	1	0
0	SOF 1011/0100				GTRIG	FSYNC	READOUT_EI	DAQ_TYPE M	ODD parity
	17	16	15	14	13	12	11	10	9
1	DAQ_TYPE LSB		DAQ TYPE COMPENSATION DELAY						ODD parity
	26	25	24	23	22	21	20	19	18
2	NA: 1	NA:0	NA: 1	NA:1	NA: 0	LED SYNC	GRESET	SPILL_NB_AV	ODD parity
	35	34	33	32	31	30	29	28	27
3	SPILL_NB MSB								ODD parity
	44	43	42	41	40	39	38	37	36
4	SPILL_NB LSB								ODD parity
	46	45							
5	EOF 00								
Frame nb.									

5 frames of 9 bits + 2-bits EOF => 47 bits sent

DAQ_TYPE:		DAQ TYPE COMPENSATION DELAY:
0	NONE	Compensate the delay of the TX frame in order to restore it correctly at the decoder side
1	BEAM	64 values fit with 45 bits frame and up to eventual upgrade to 7 frames (63 bits)
2	COSMIC	
3	BEAM+COSMIC	
4	FULL	**SPILL_NB_AV:**
5	WG	If =1 then Spill number is available and can be used
6	NA	Else The value iis not usable at decoder side, encoder fills it with 0xCCCC (balanced word)

SOF pattern recognition:

IDLE			PATERN				0	1
0	0	0	1	0	1	1	y	n
0	0	1	0	1	0	0	n	y
0	1	0	1	0	1	1	y	n
0	1	1	0	1	0	0	n	y
1	0	0	1	0	1	1	y	n
1	0	1	0	1	0	0	n	y
1	1	0	1	0	1	1	y	n
1	1	1	0	1	0	0	n	y
IDLE								
0	0	1	1	1	1	1	n	n
0	1	1	1	1	1	1	n	n
1	0	0	0	0	0	0	n	n
1	1	0	0	0	0	0	n	n

0 pattern = 01011

1 pattern = 10100

1.1.3 FEB synchronization modes & parameters

The following paragraph and its figures are copied from Baby Mind specification and should be updated for Super-FGD but this is a good starting point.

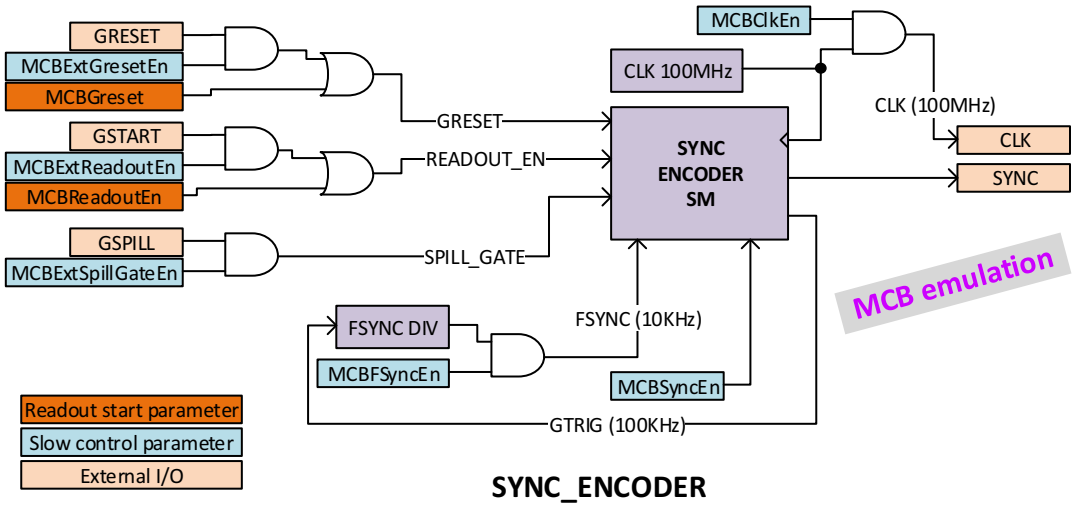


Figure 4: FEB SYNC Encoder modes and parameters when used as master clock board emulation

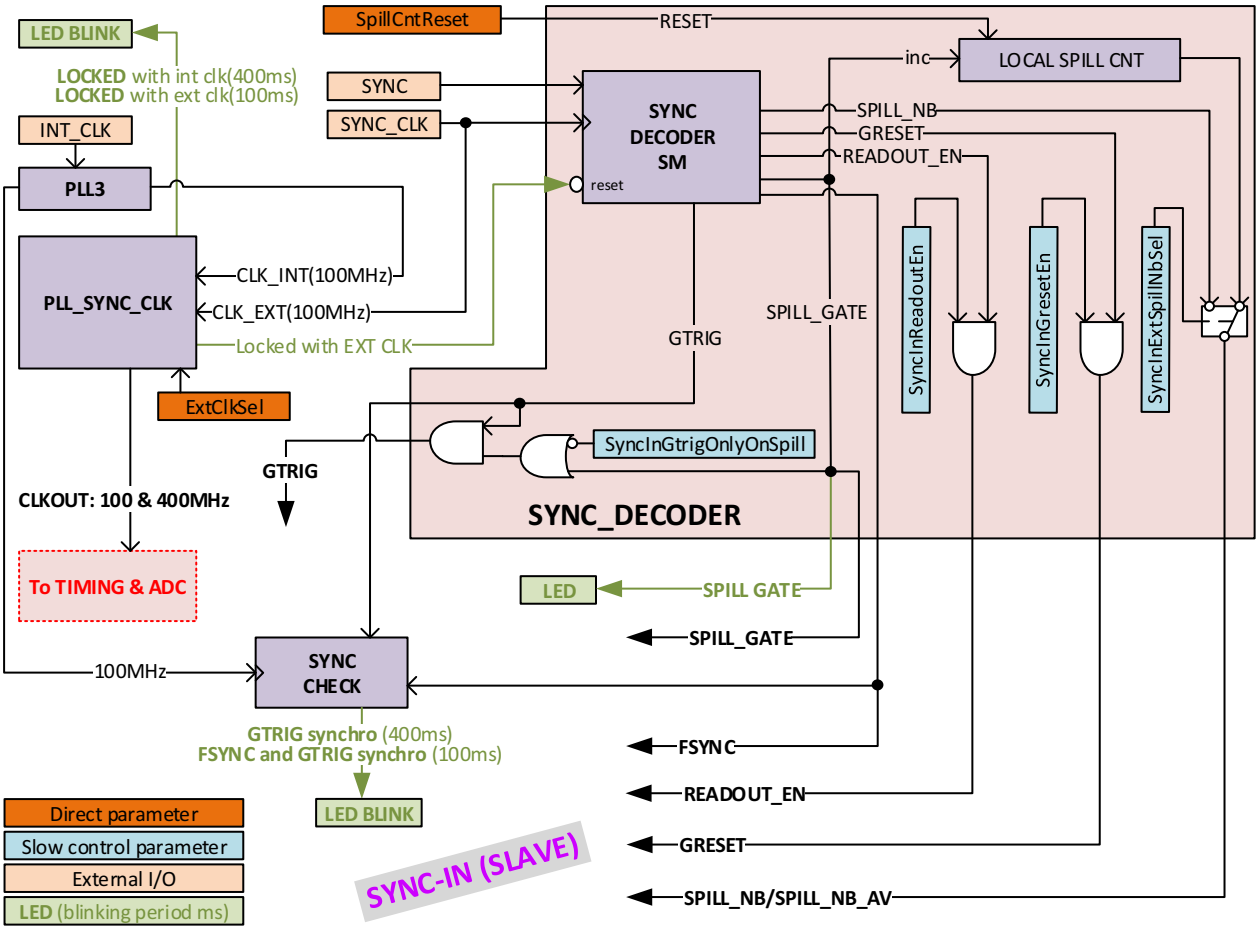
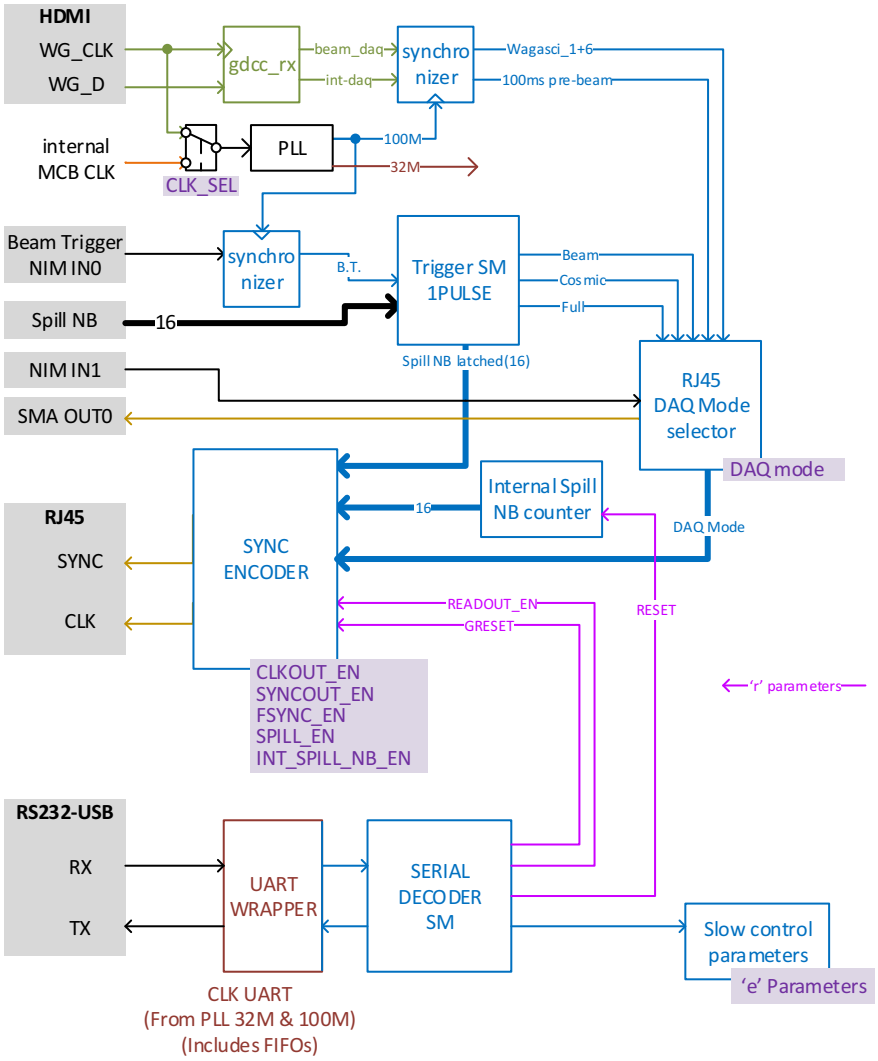


Figure 5: FEB SYNC Decoder modes and parameters

4 Firmware Architecture

The following paragraph and its figures are copied from Baby Mind specification and should be updated for Super-FGD but this is a good starting point.



Trigger SM 1 pulse : similar to wagashi ext_trig_in state machine
After rising edge on pulse on EXT_TRIG_IN (i.e. beam trigger) :
- Assert BEAM_DAQ for 60µs
- Assert FULL_DAQ for 1.986µs
- Wait 4 µs and latch the Spill number
- Wait 20ms and assert COSIC_DAQ for 1.966µs

NB: Spill NB is not synchronized since supposed to be stable @ 4µs after pulse on EXT_TRIG_IN

Synchronizer
To pass signals from 1 clock domain to another

Figure 6: FW architecture

5 Protocol

The following paragraphs are copied from Baby Mind specification and should be updated for Super-FGD but this is a good starting point.

5.1 Communication

5.1.1 RESET UART communication “x”

To be sent in case of communication failure, timeout or wrong answer. It has the n°1 priority over all other commands.
TX request: “x”
RX answer: “x”

5.2 Slow control parameters commands

5.2.1 SYNC Encoder "e"

TX request: "e" + xx
RX answer: "e" + xx or "y" + error code
xx = ASCII char corresponding of the following byte:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPILL GATE MODE on OUT0 (always) & RJ45 (only if bit3=1)			Enable Internal Spill NB inc. else Ext. SP IN	Enable Spill Gate & Spill NB **on RJ45**	Enable FSYNC **on RJ45**	Enable Sync CLK OUT **on RJ45**	Enable Sync Data OUT **on RJ45**
***000**: None* ***001**: 60us Beam DAQ pulse on NIM 0 input* ***010**: Internal DAQ (20ms after Beam DAQ, duration=1.966s)* ***011**: 001 OR 010 (i.e. 2 pulses)* ***100**: 1.986s full pulse* ***101**: Wagasci HDMI input* ***110:** External NIM 1 input*			*From SP IN else internal counter (no usage of ECL flat cable)*	*To FEBs on RJ45* *From trig 0 IN on mode = 1-4* *From WG IN on mode = 5* *From trig 1 IN on mode = 6*	*To FEBs on RJ45* *Internal 10KHz*	*To FEBs on RJ45*	*To FEBs on RJ45* *GTRIG auto. enabled*

Example:

- All bit set to 0 : "e00"
- Enable Sync + Sync Clk : "e03"
- Enable Sync + Sync Clk + FSYNC + 60us DAQ pulse on OUT0 : "e27"
- Enable Sync + Sync Clk + FSYNC + Internal DAQ pulse on OUT0 & RJ45: "e4F"
- Enable Sync + Sync Clk + FSYNC + External NIM1 input to OUT0 & RJ45: "eCF"
- Enable Sync + Sync Clk + FSYNC + External NIM1 input to OUT0 & RJ45 and internal spill number increment (not using flat cable) : "eDF"

5.2.2 Spill NB "s"

TX request: "s00"
RX answer: "s" + xxxx or "y" + error code
xxxx = ASCII char corresponding of the spill number in HEX format
Example:

- "s", answer "s010A" for spill number 0x010A = 266

5.3 Readout commands

5.3.1 Readout “R”

TX request: “r” + xx
RX answer: “r” + xx or “y” + error code
xx = ASCII char corresponding of the following byte:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
			Reset internal spill counter			Send GRESET pulse	Enable READOUT

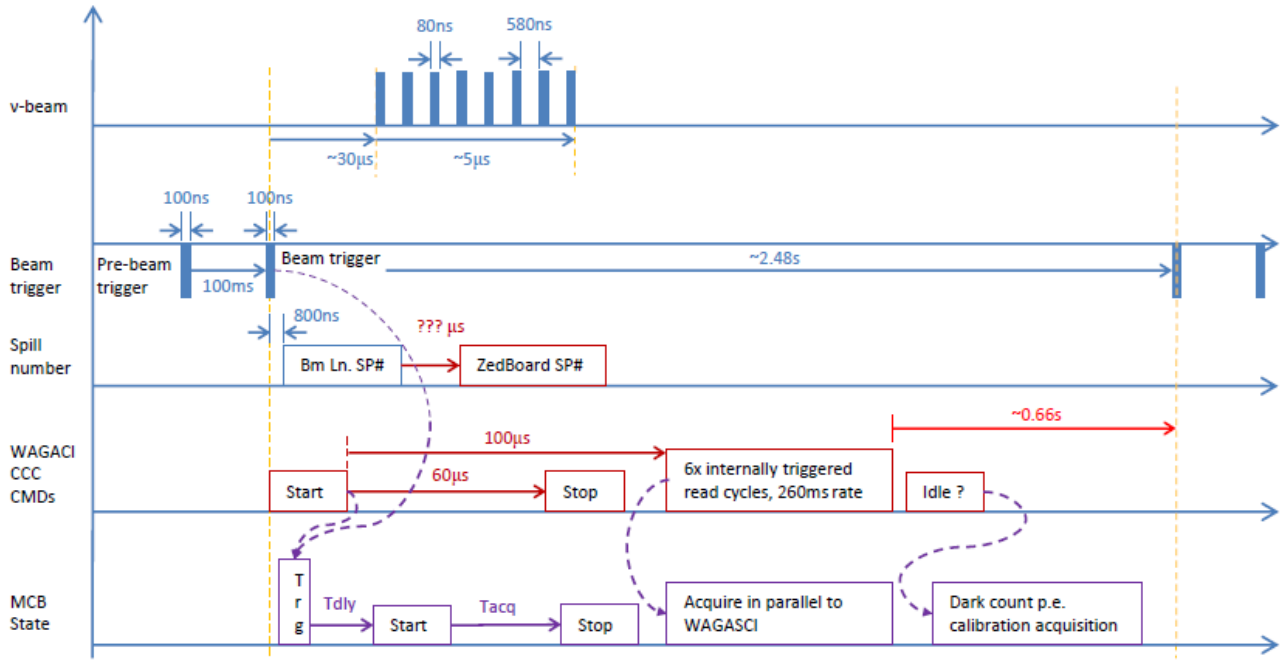
Example:

- Stop readout : “r00”
- Enable Readout : “r01”
- Enable Readout with GRESET: “r03”
- Reset Internal Spill Counter: “r10”

6 Appendixes

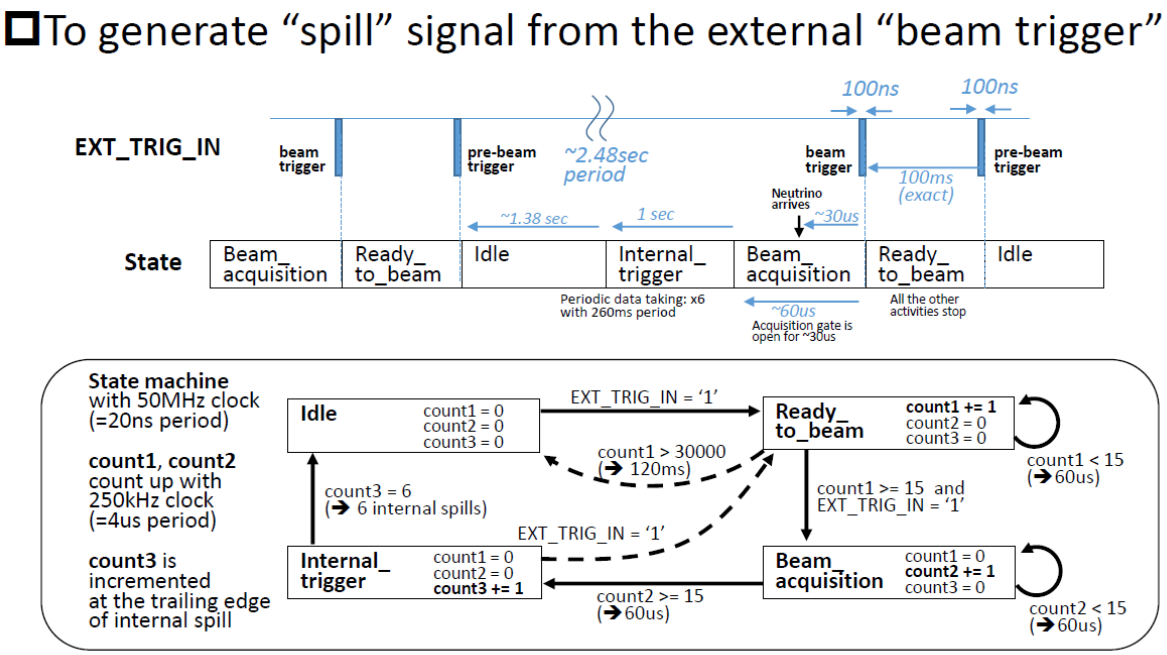
The following paragraphs and its figures are copied from Baby Mind specification and should be updated for Super-FGD but this is a good starting point.

6.1 Beam triggering from J-PARK



6.2 J-PARK CCC triggering state machine

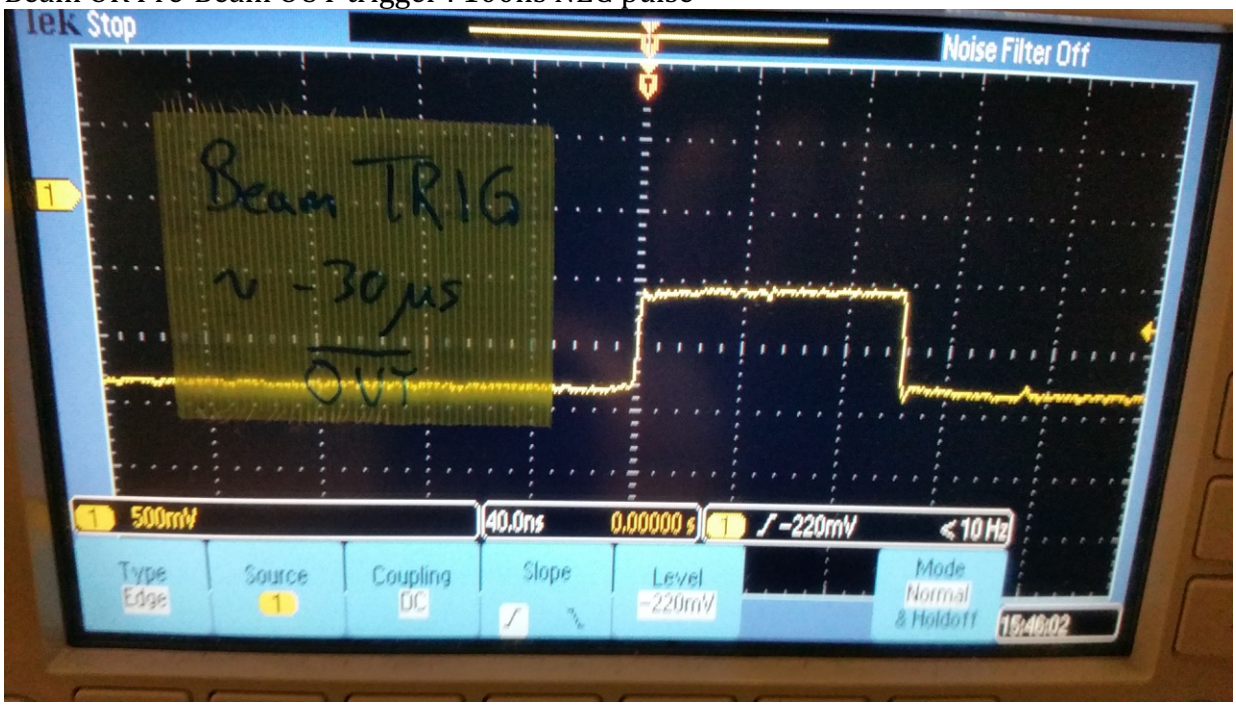
Something similar will be used for the 'trigger state machine' of the MCB firmware



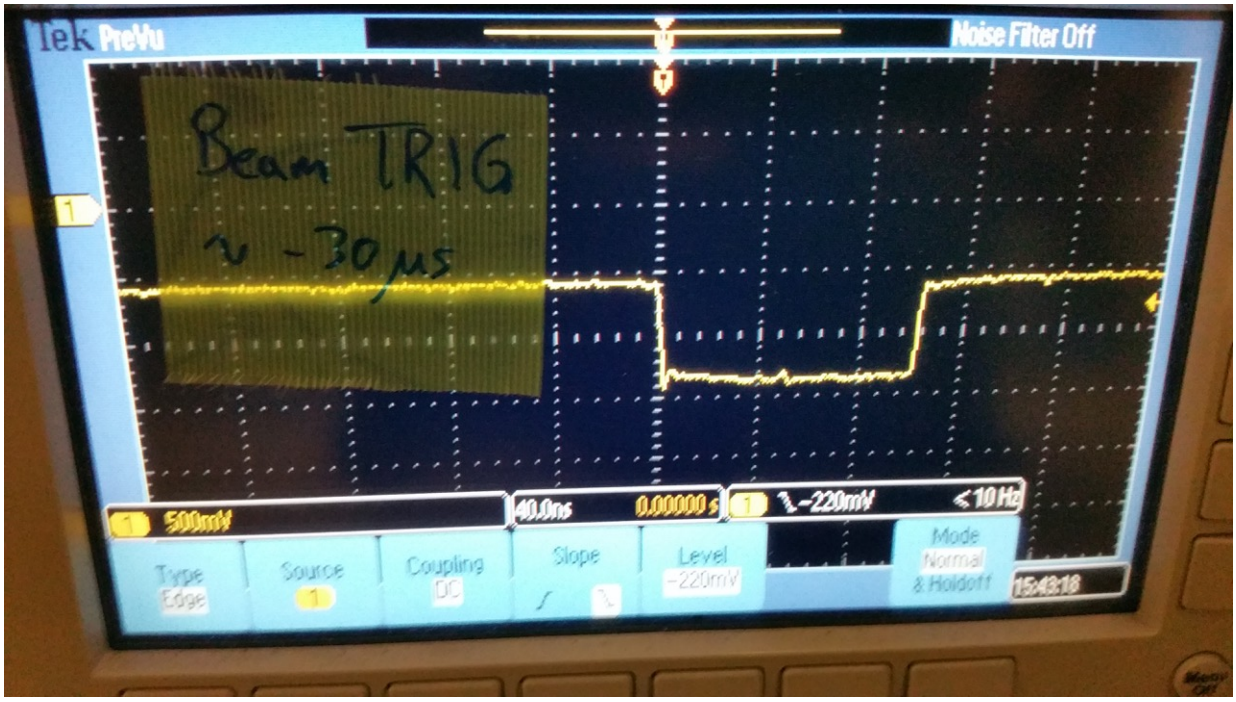
*In the case where one of "pre-beam trigger" and "beam trigger" fails to arrive.
➔ It may stay at "Ready_to_beam". ➔ The state is back to "Idle" state after 150ms.
*In the case of "unexpected procedure"(▬▬), error messages would be sent to the DAQ PC via TCP socket.

6.3 BEAM signals

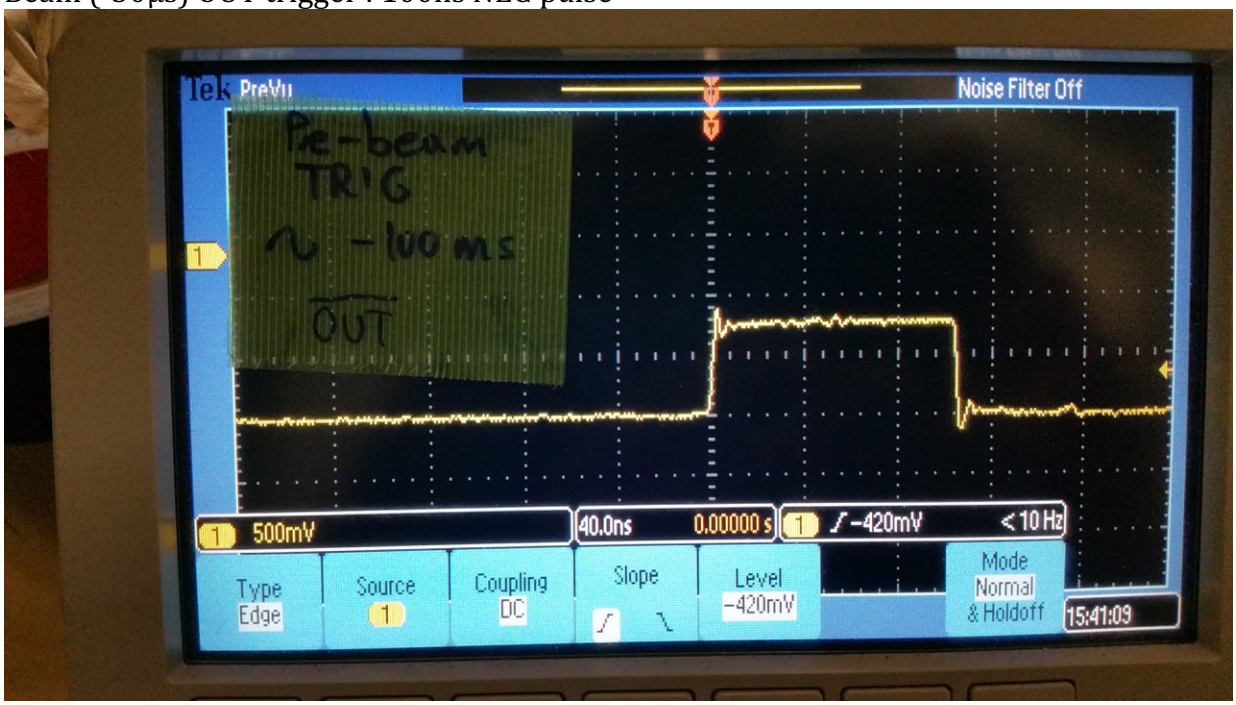
Beam OR Pre-Beam OUT trigger : 100ns NEG pulse



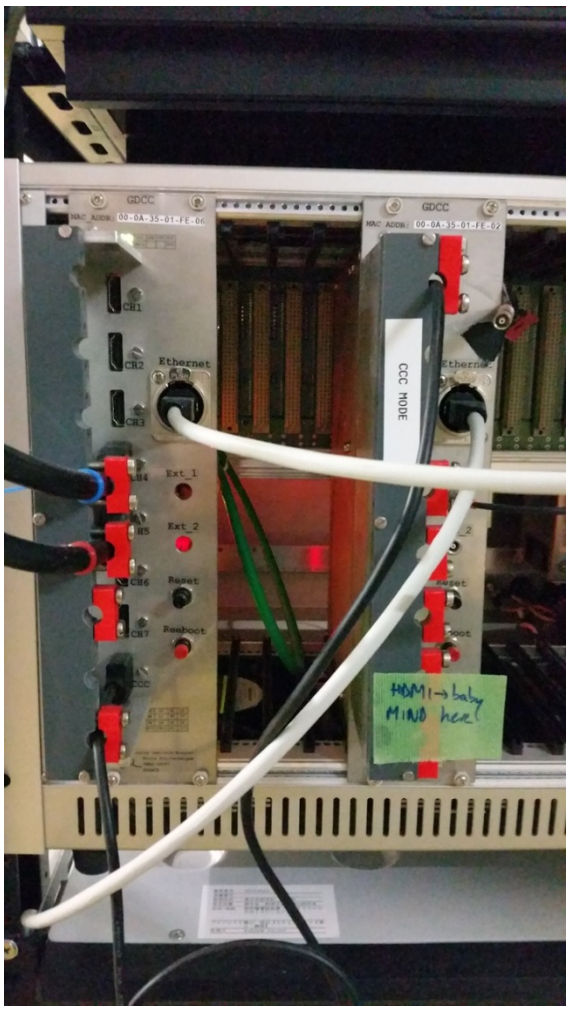
Beam (-30µs) /OUT trigger : 100ns POS pulse



Beam (-30µs) OUT trigger : 100ns NEG pulse



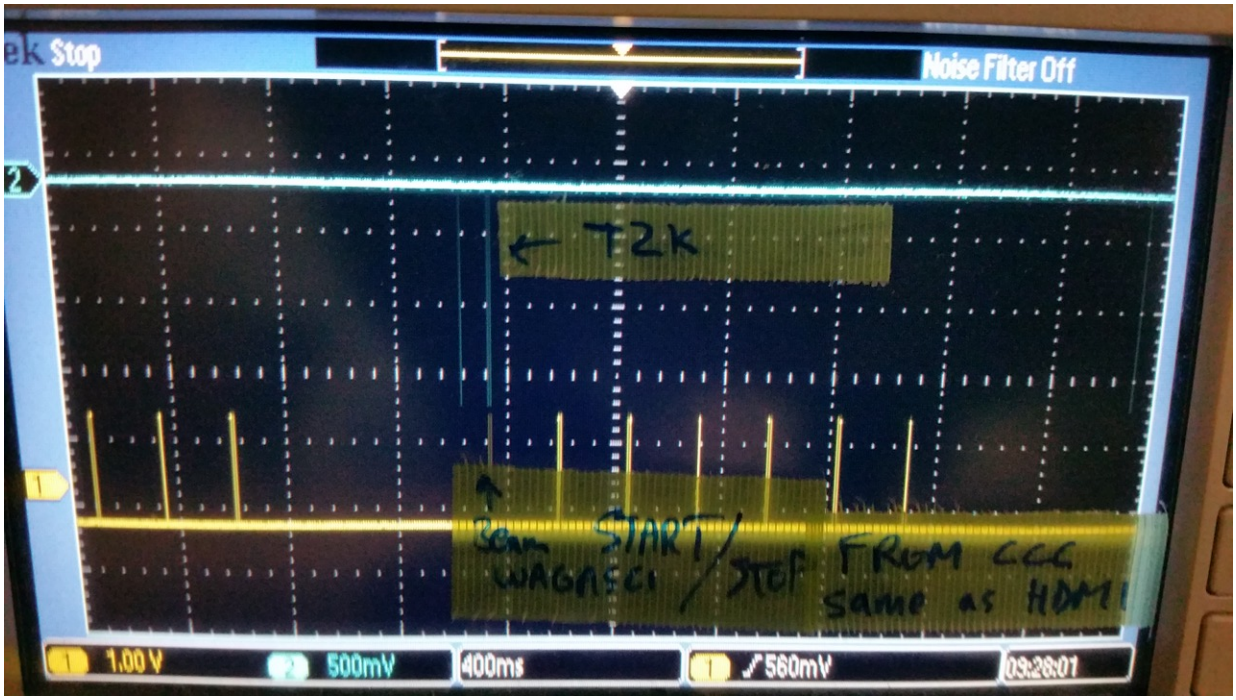
Pre-Beam (-100ms) /OUT trigger : 100ns POS pulse



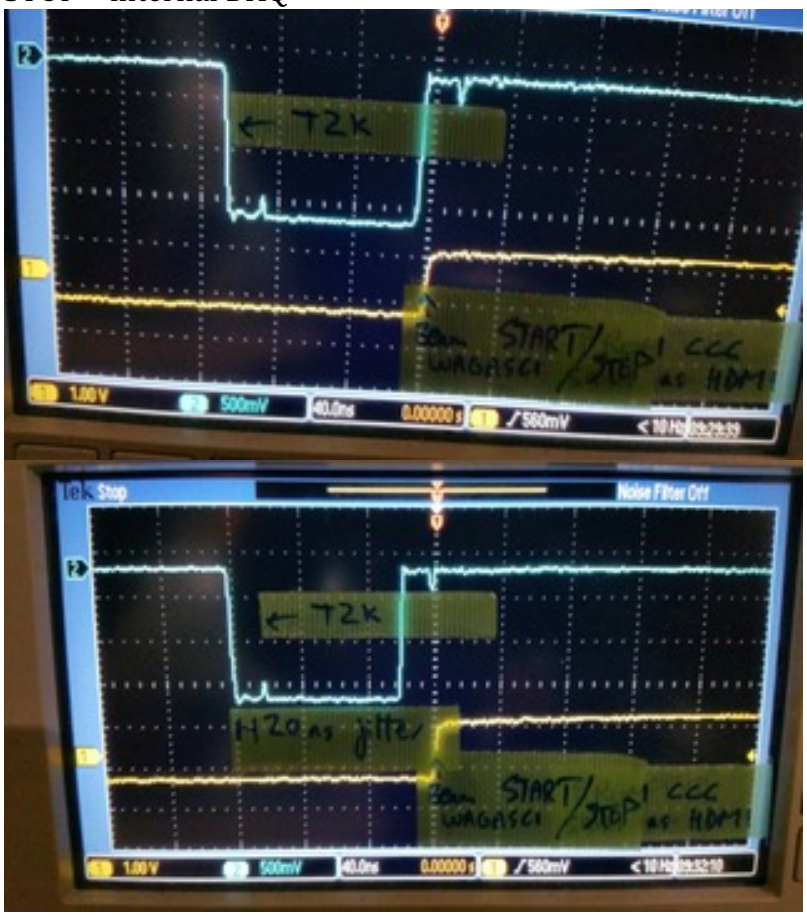
HDMI CCC connections

Beam/Pre-Beam NIM connections

6.4 CCC signals



T2K & START/STOP overview with 1st START-STOP = µBEAM, 2nd to 7th START-STOP = internal DAQ



20 ns jitter from T2K beam to START rising edge

START-STOP duration = 60μs