Simple Pattern Matching Algorithm for DAQ using FPGA

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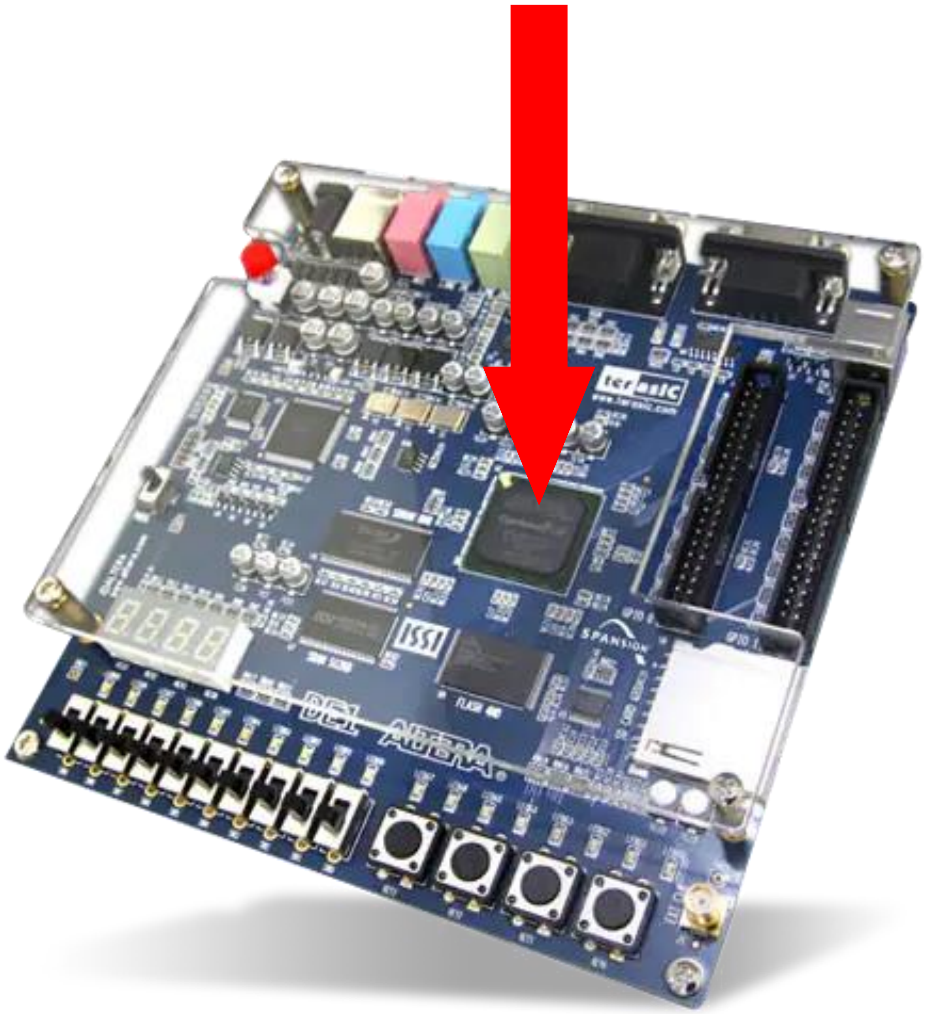
What we did

- Combinatorial Logics (Logic Gates: OR, AND, etc…)
- Boolean Algebra
  - Adding
  - Subtraction
  - Negative Number Representation
- Sequential Logics (Flip-Flops)
  - Shift Registers
  - Counters, Clock speed division
  - Zig-Zag
- FPGA internals
- Pattern Matching Algorithms

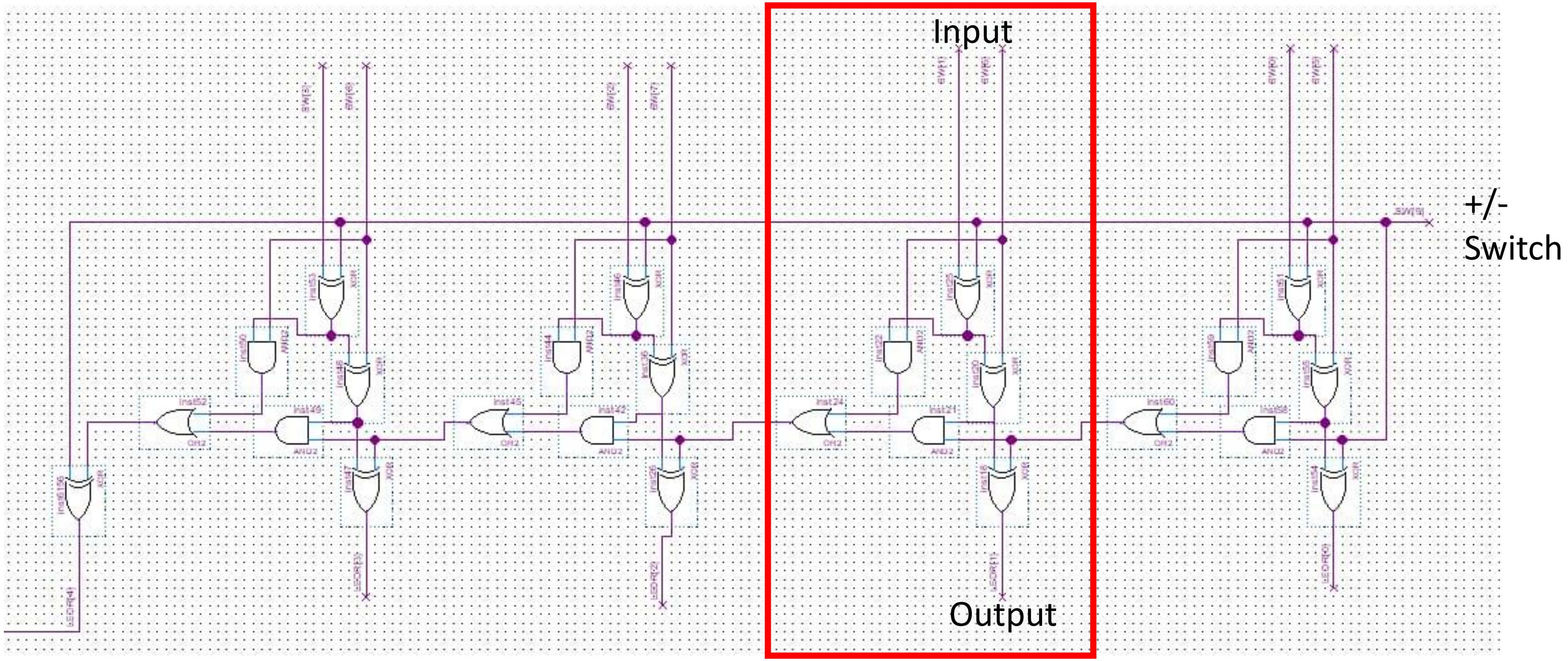
FPGA

Field Programmable Gate Array:

- integrated circuit (IC) to which a logic circuit can be uploaded
- wide range of applications
- fast signal processing
- easy to make subsequent adjustments to implemented functionalities
- prototyping for application-specific integrated circuit (ASIC) development



Binary Adder & Subtractor



Input

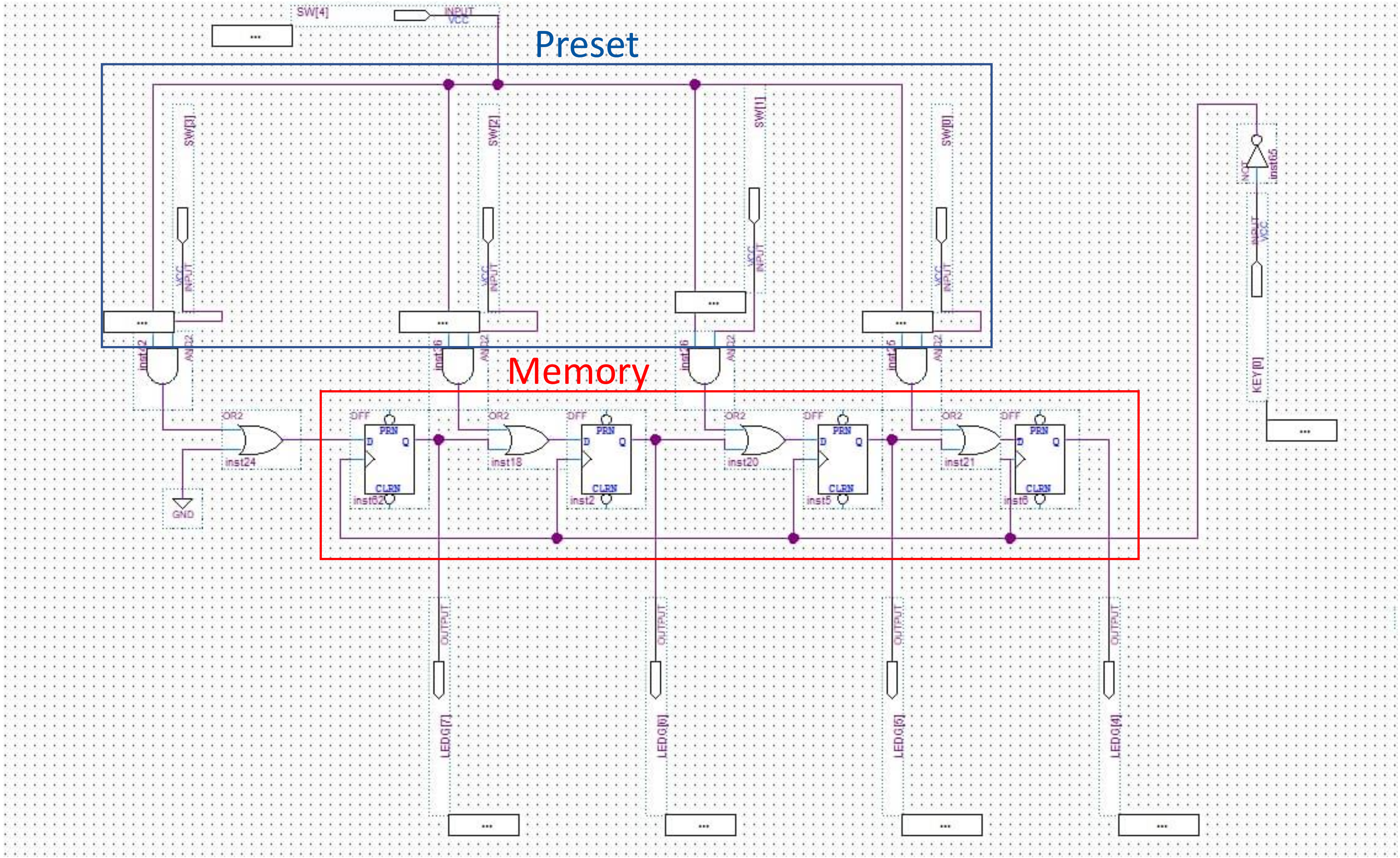
+/-
Switch

Output

Shift Register

Integer Multiplication and Integer Division by 2

Example for right shift



Output

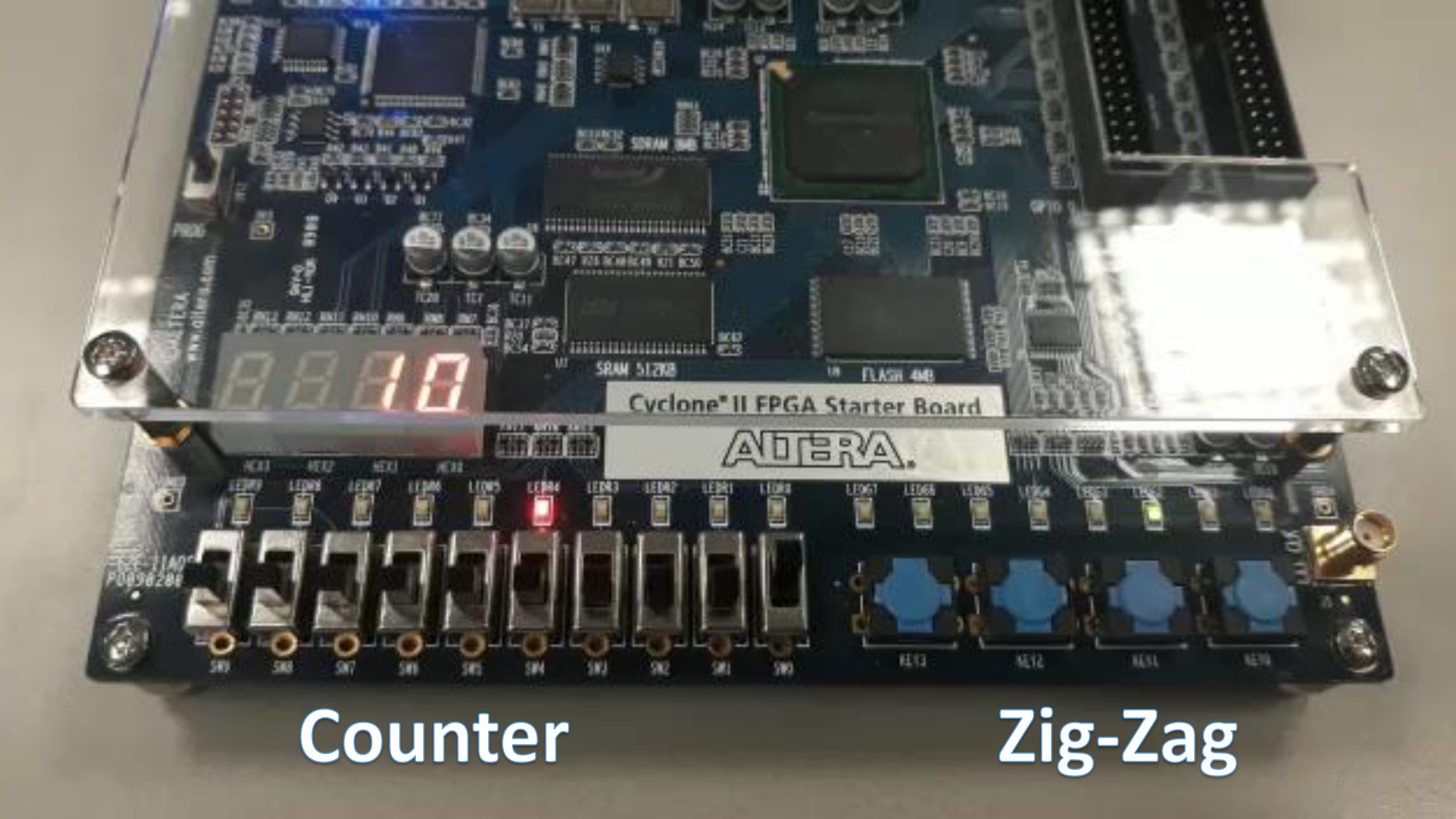
1010 (10)

0101 (5)

0010 (2)

0001 (1)

0000 (0)

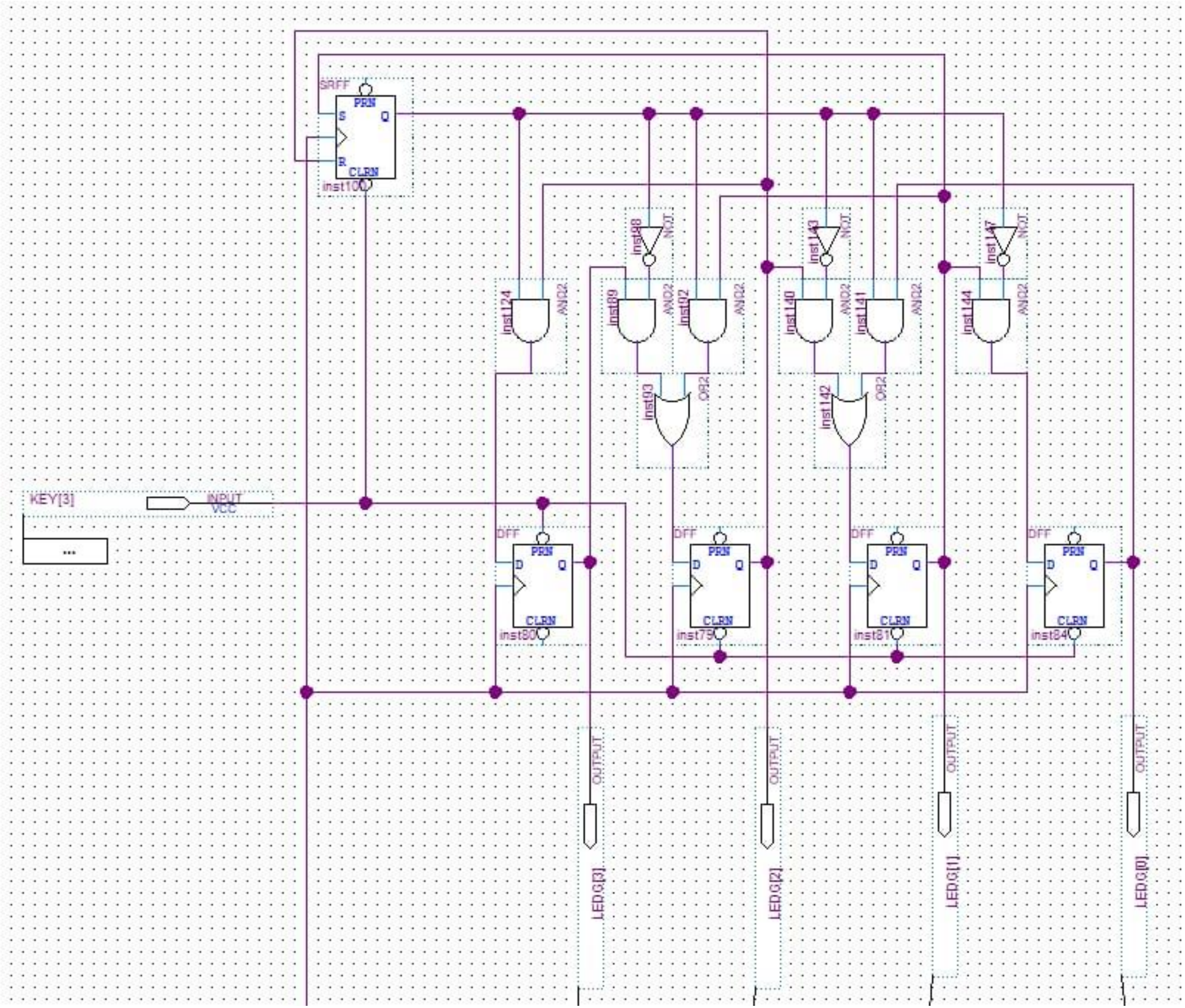


Counter

Zig-Zag

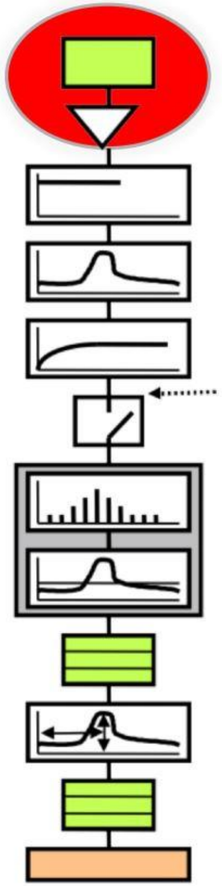
Zig-Zag

Advanced left and right shifter



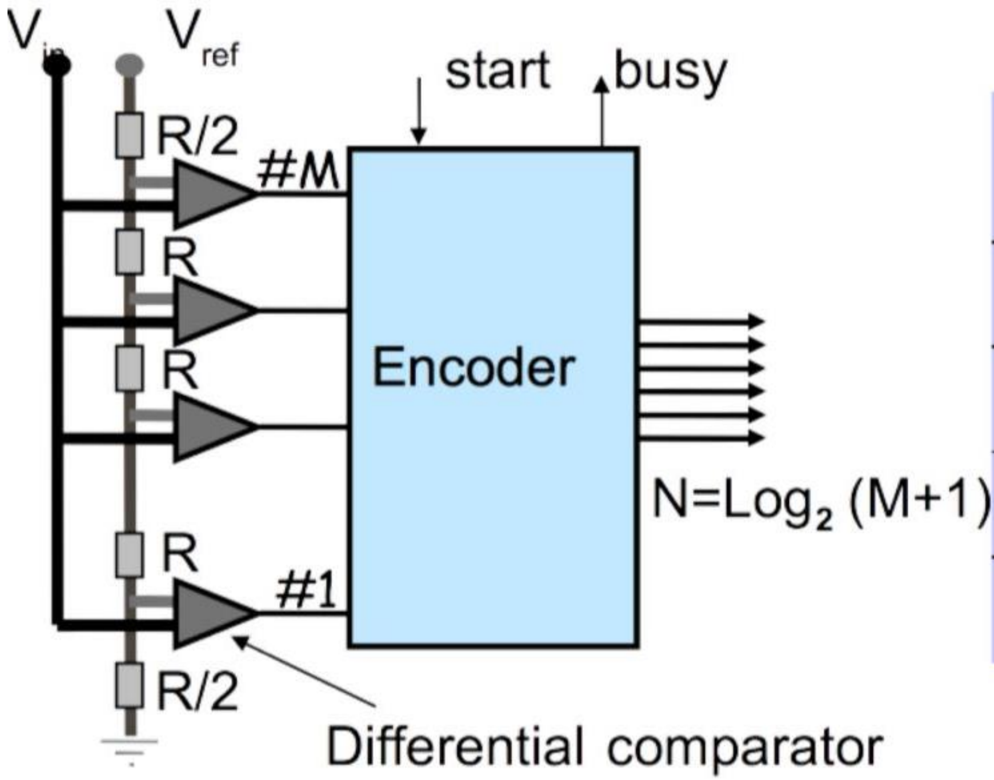
Designing a Pattern Matching Algorithm using FPGA

Quick Introduction to Data Acquisition

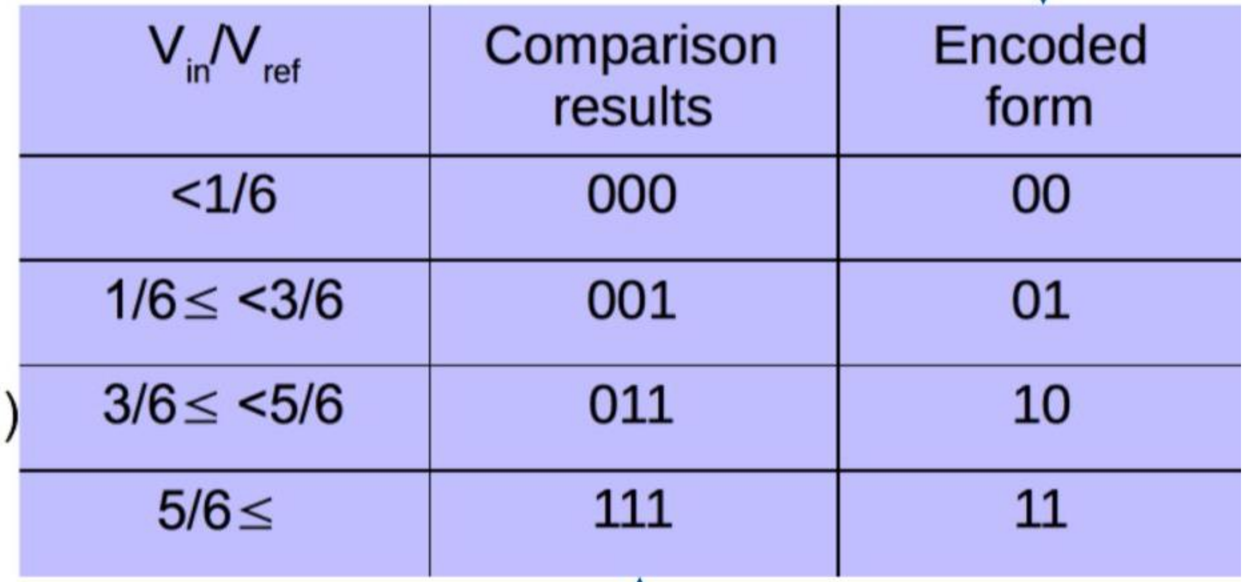


- Signal from a detector which is captured whenever it exceeds a certain threshold
- Amplification of the signal
- Analog to digital conversion
- Additional digital processing
  (digital filters: e.g. **pattern matching**)
- Storing

Flash Analog to Digital Conversion



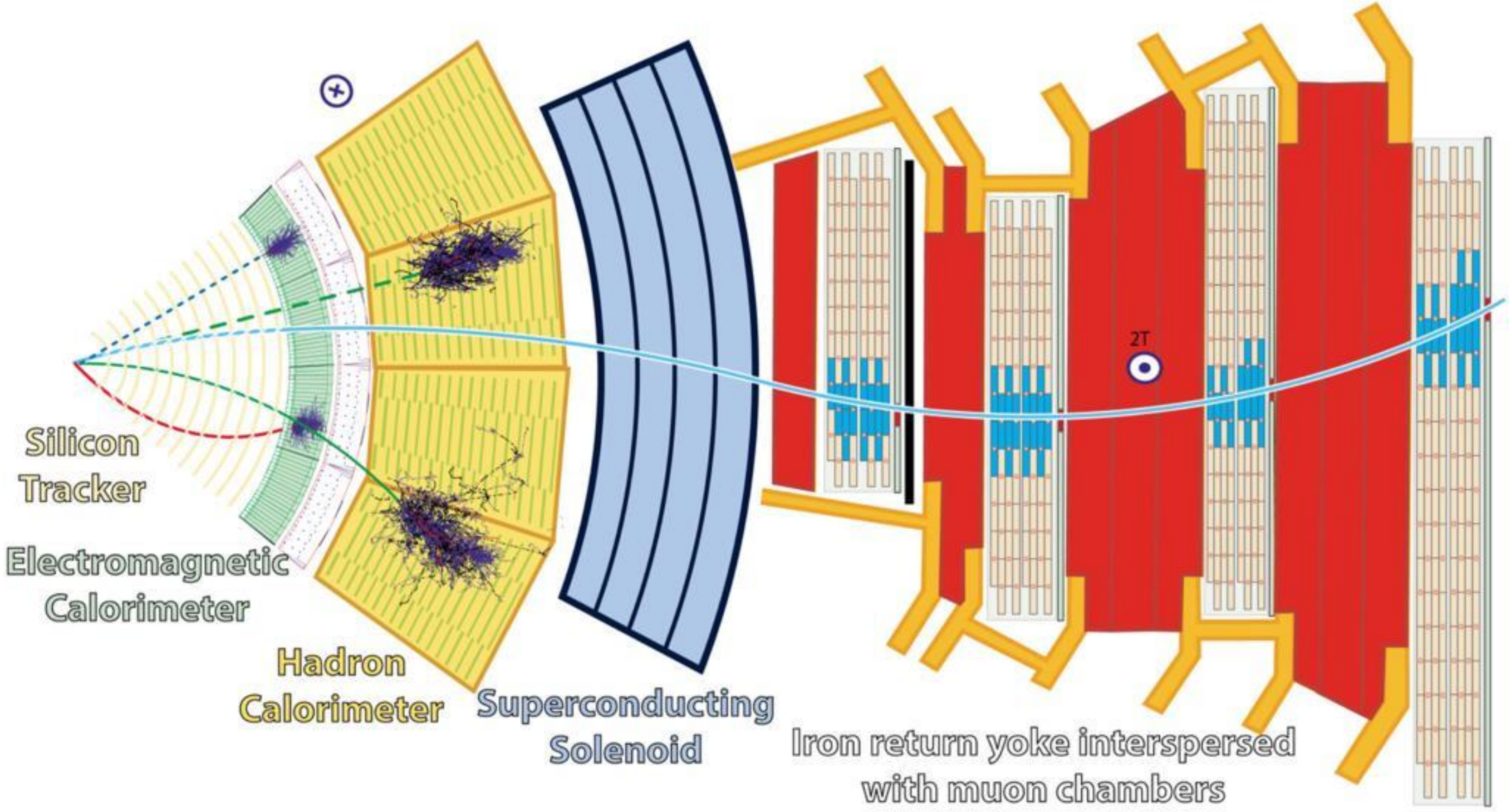
binary code



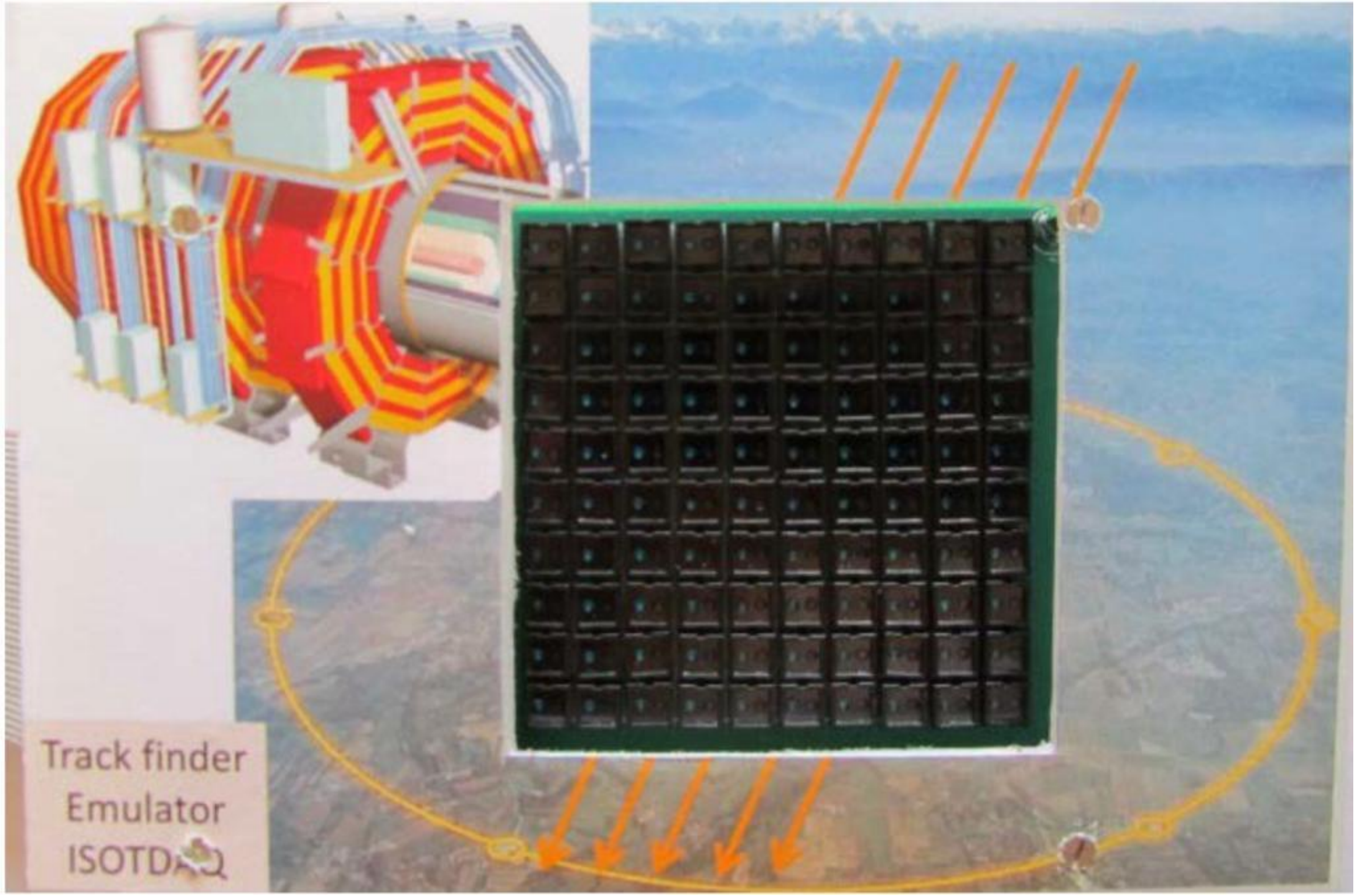
V_{in}/V_{ref}	Comparison results	Encoded form
<1/6	000	00
1/6≤ <3/6	001	01
3/6≤ <5/6	011	10
5/6≤	111	11

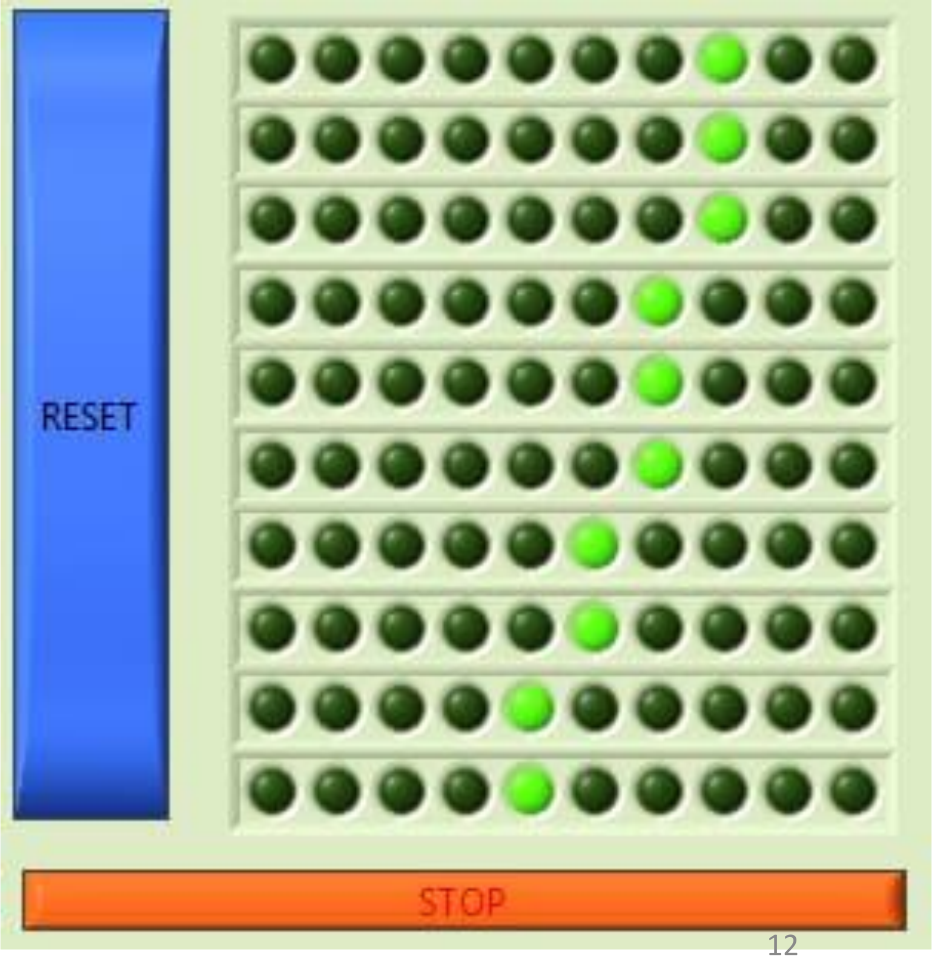
Encoder Input

CMS Particle Trajectory Detection


2T
Silicon Tracker
Electromagnetic Calorimeter
Hadron Calorimeter
Superconducting Solenoid
Iron return yoke interspersed with muon chambers

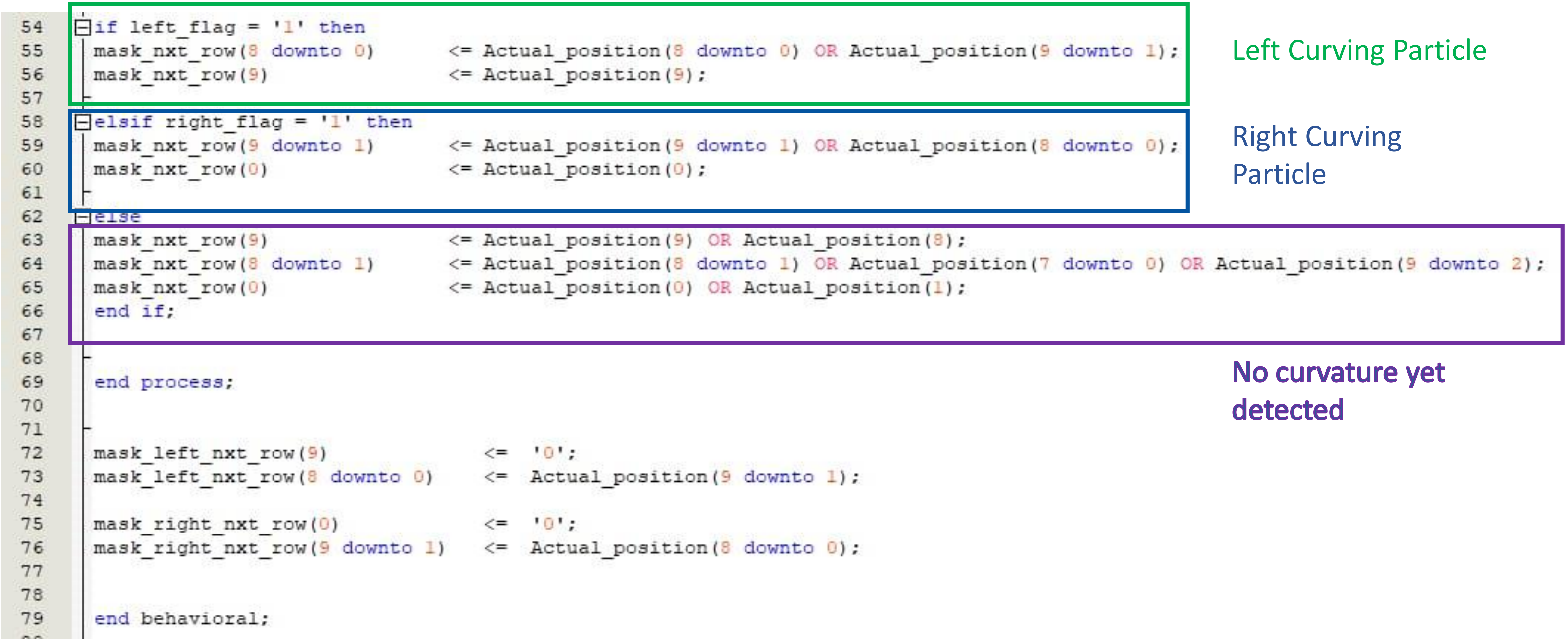
Track finder Emulator





Concept of the final Algorithm

Expected Position of Particle **Actual Position of Particle**



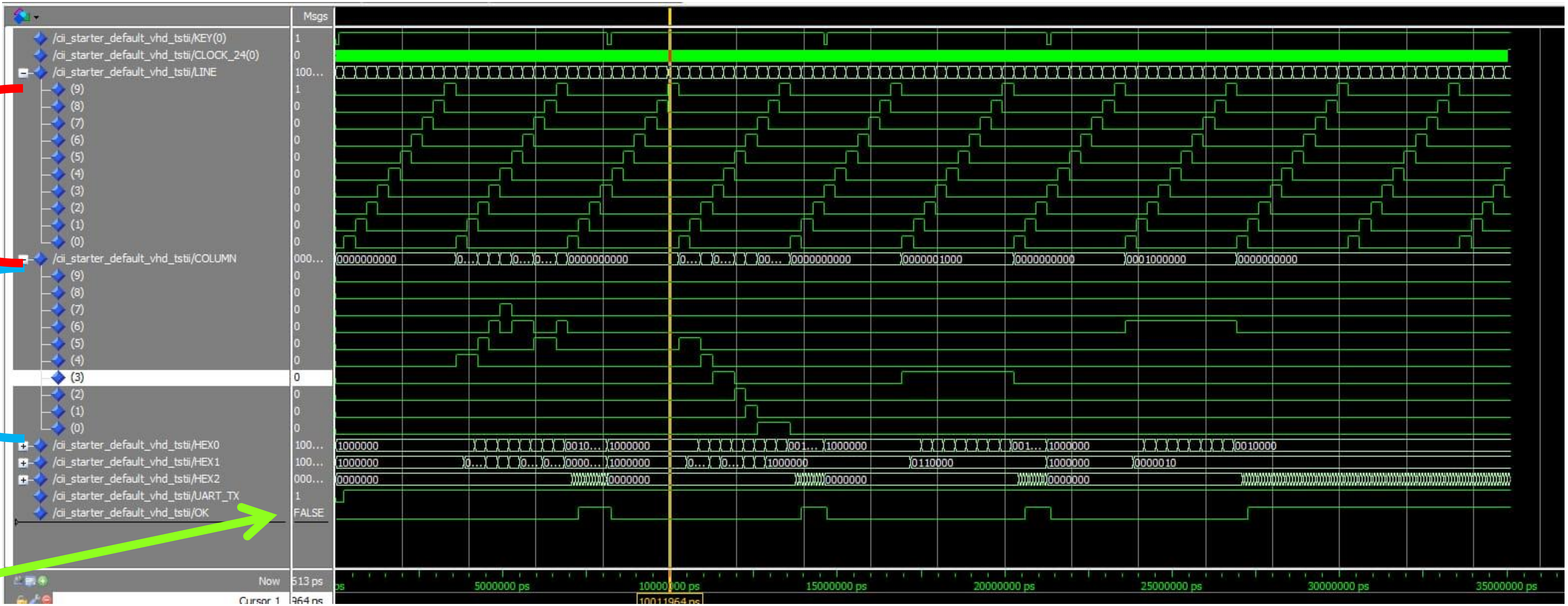
```
if left_flag = '1' then
mask_nxt_row(8 downto 0)      <= Actual_position(8 downto 0) OR Actual_position(9 downto 1);
mask_nxt_row(9)               <= Actual_position(9);

elsif right_flag = '1' then
mask_nxt_row(9 downto 1)      <= Actual_position(9 downto 1) OR Actual_position(8 downto 0);
mask_nxt_row(0)               <= Actual_position(0);

else
mask_nxt_row(9)               <= Actual_position(9) OR Actual_position(8);
mask_nxt_row(8 downto 1)      <= Actual_position(8 downto 1) OR Actual_position(7 downto 0) OR Actual_position(9 downto 2);
mask_nxt_row(0)               <= Actual_position(0) OR Actual_position(1);
end if;


end process;


mask_left_nxt_row(9)            <=  '0';
mask_left_nxt_row(8 downto 0)   <=  Actual_position(9 downto 1);

mask_right_nxt_row(0)           <=  '0';
mask_right_nxt_row(9 downto 1)  <=  Actual_position(8 downto 0);


end behavioral;
```

Left Curving Particle

Right Curving Particle

No curvature yet detected

PMA Simulation



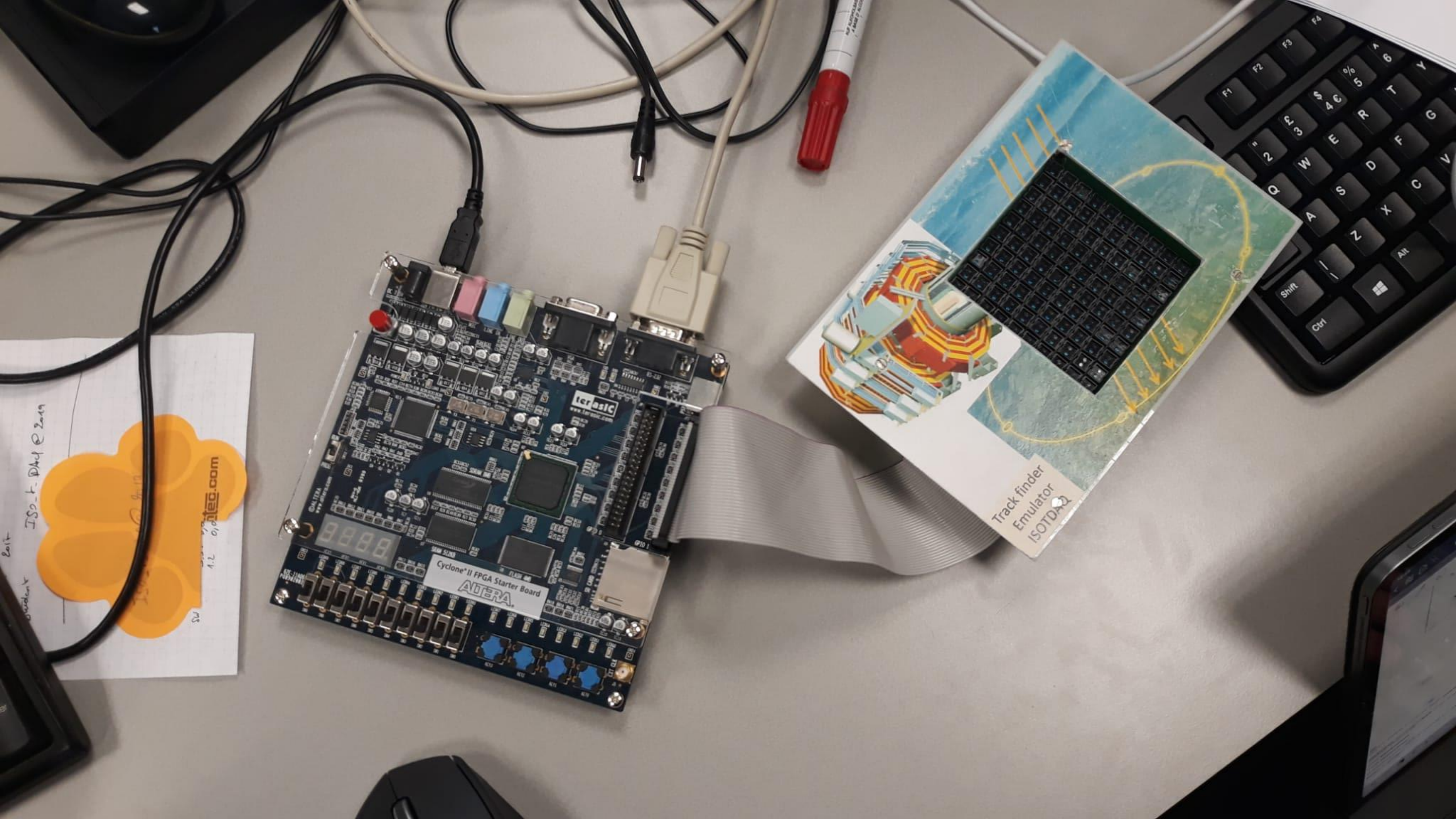
```
                                              Msgs
/cii_starter_default_vhd_tstii/KEY(0)         1
/cii_starter_default_vhd_tstii/CLOCK_24(0)    0
/cii_starter_default_vhd_tstii/LINE           100...
   (9)                                        1
   (8)                                        0
   (7)                                        0
   (6)                                        0
   (5)                                        0
   (4)                                        0
   (3)                                        0
   (2)                                        0
   (1)                                        0
   (0)                                        0
/cii_starter_default_vhd_tstii/COLUMN         000...
   (9)                                        0
   (8)                                        0
   (7)                                        0
   (6)                                        0
   (5)                                        0
   (4)                                        0
   (3)                                        0
   (2)                                        0
   (1)                                        0
   (0)                                        0
/cii_starter_default_vhd_tstii/HEX0           100...
/cii_starter_default_vhd_tstii/HEX1           100...
/cii_starter_default_vhd_tstii/HEX2           000...
/cii_starter_default_vhd_tstii/UART_TX        1
/cii_starter_default_vhd_tstii/OK             FALSE
                                       Now    613 ps
                                  Cursor 1    964 ps
```

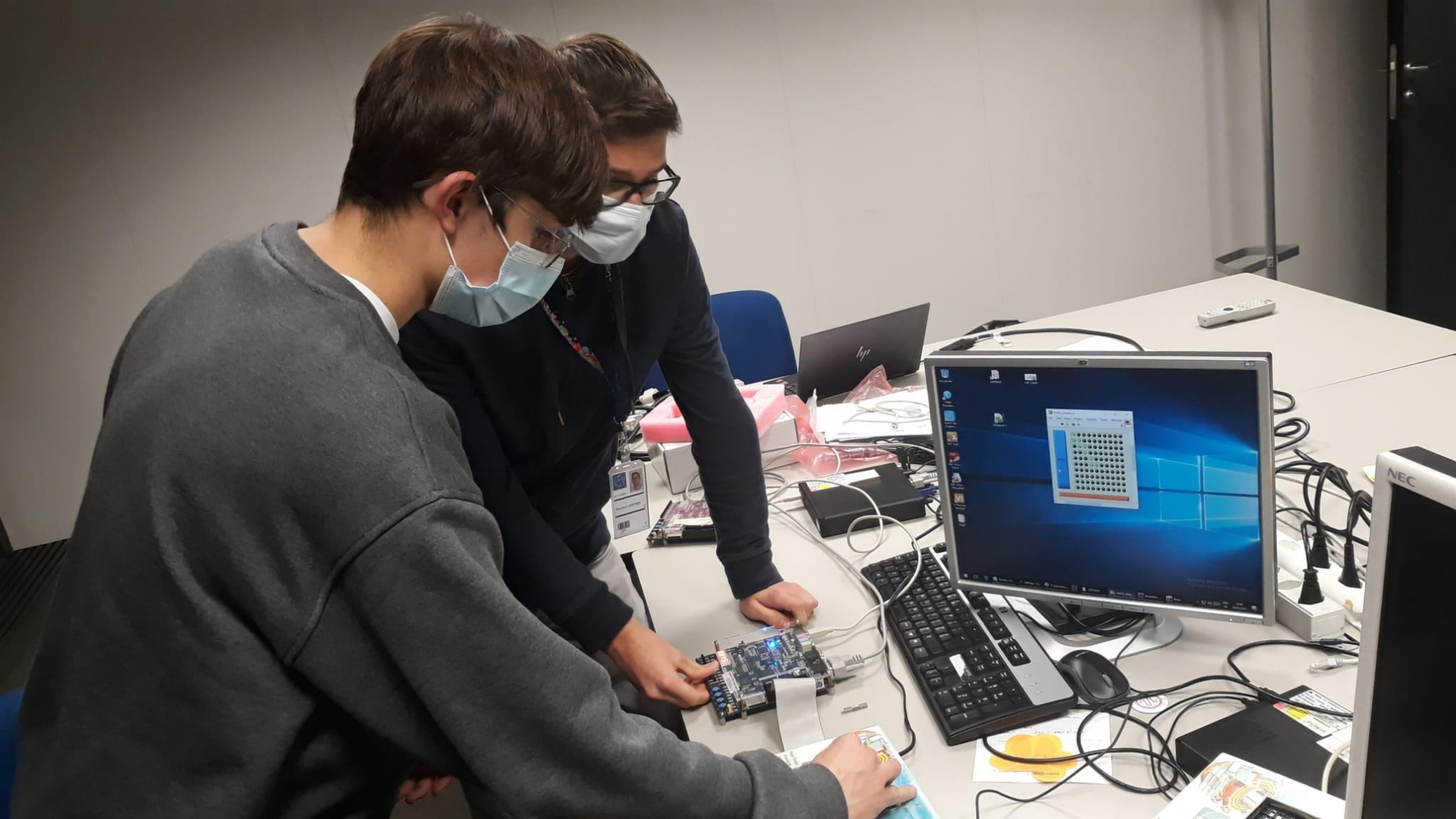
Row

Column

Pattern Recognition Output Signal

Time


Track finder
Emulator
ISOTDAQ
terasic
Cyclone® II FPGA Starter Board
ALTERA
ISO_t_DAQ @ 2019


NEC