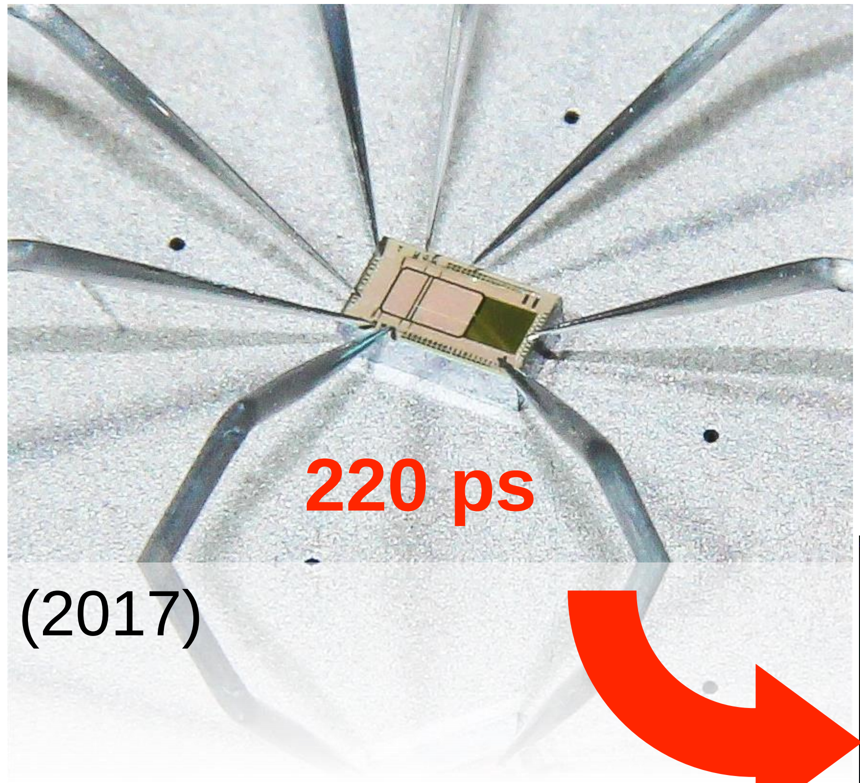
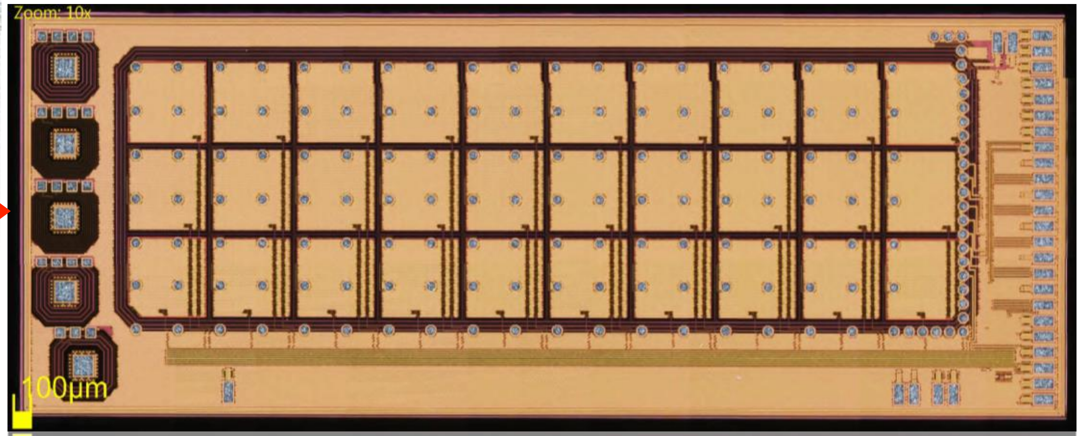
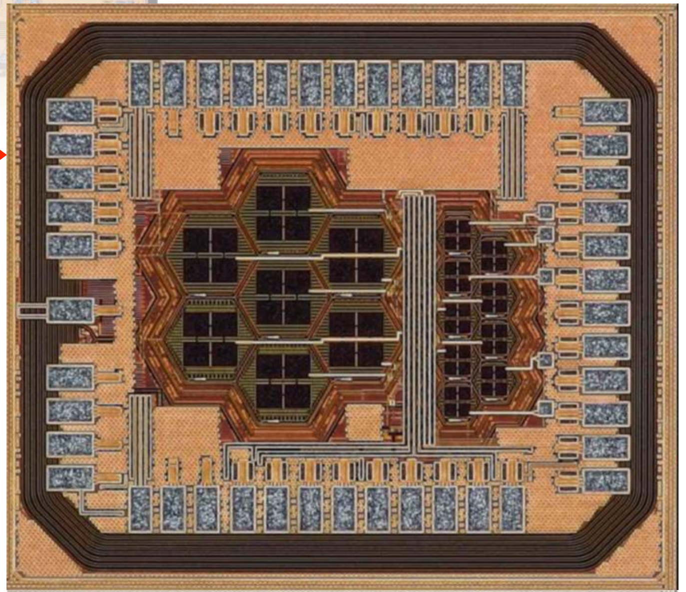
Design of SiGe BiCMOS monolithic pixel sensors with picosecond-level time resolution





(2018) **110 ps**



(2019) **50 ps**

?

Lorenzo Paolozzi
Université de Genève

Heidelberg
November 13, 2019

- Back in **2014** G. Iacobucci, R. Cardarelli and M. Nessi proposed a strategy to use SiGe HBTs for ultra-fast, low noise signal amplification in particle detectors.

- The goal was to produce a monolithic pixelated silicon detector with 100 ps time resolution.

  - L. Paolozzi and P. Valerio joined shortly later as chip designers.

Today collaboration of:

UNIVERSITÉ DE GENÈVE – FACULTÉ DES SCIENCES

ihp – innovations for high performance microelectronics – Leibniz-Institut für innovative Mikroelektronik

INFN Sezione di Roma Tor Vergata

CERN Ideas

EPFL

Funded by:

FNSNF – FONDS NATIONAL SUISSE DE LA RECHERCHE SCIENTIFIQUE

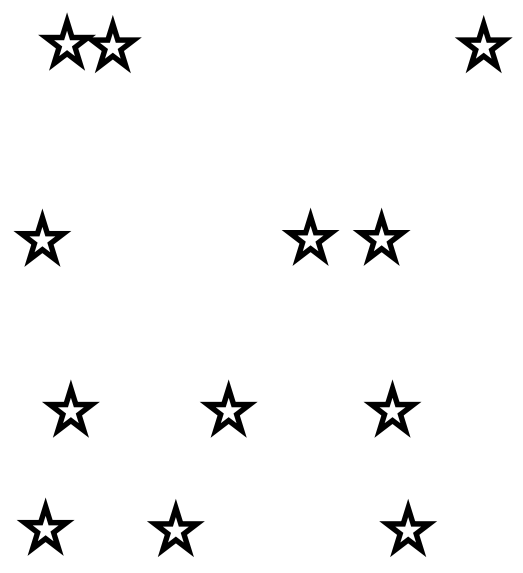
ATTRACT

Five years of (hard) R&D

Timing for high-energy physics experiments

Hartmut F-W Sadrozinski *et al* 2018 *Rep. Prog. Phys.* **81** 026101

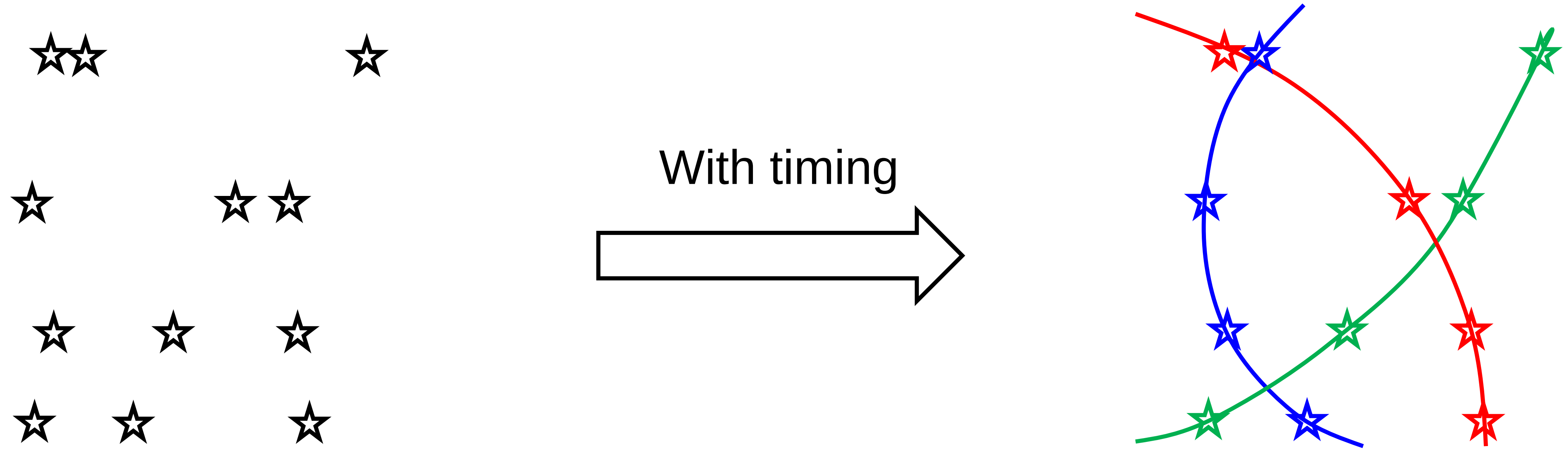
Advanced track reconstruction



Timing for high-energy physics experiments

Hartmut F-W Sadrozinski *et al* 2018 *Rep. Prog. Phys.* **81** 026101

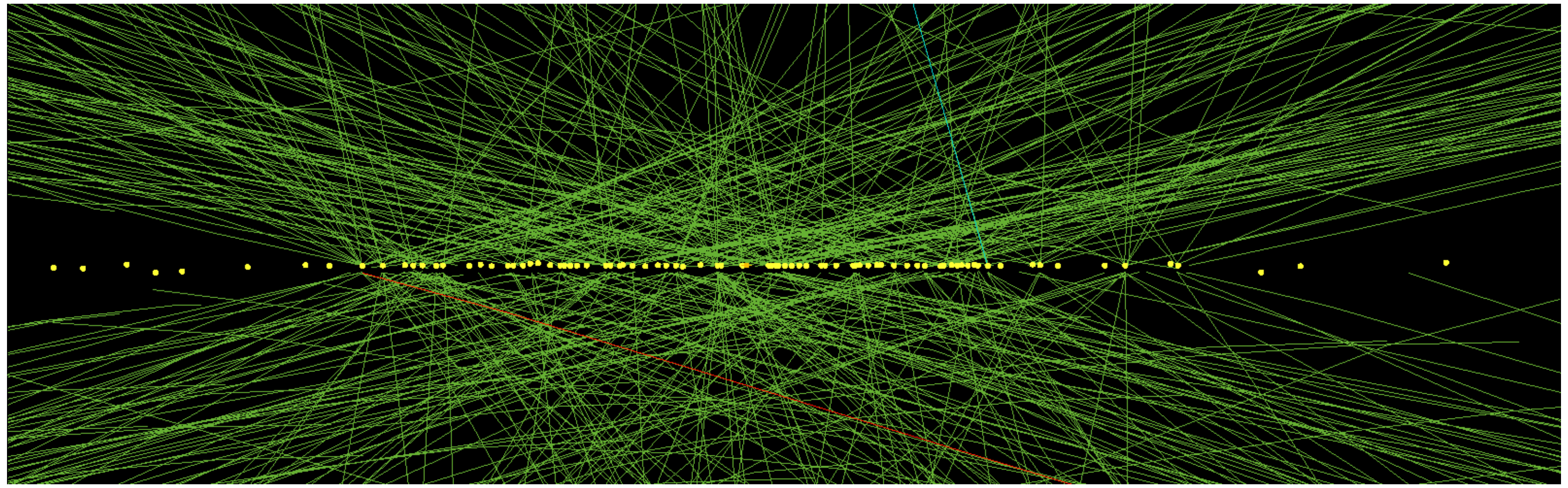
Advanced track reconstruction



Timing for high-energy physics experiments

Hartmut F-W Sadrozinski *et al* 2018 *Rep. Prog. Phys.* **81** 026101

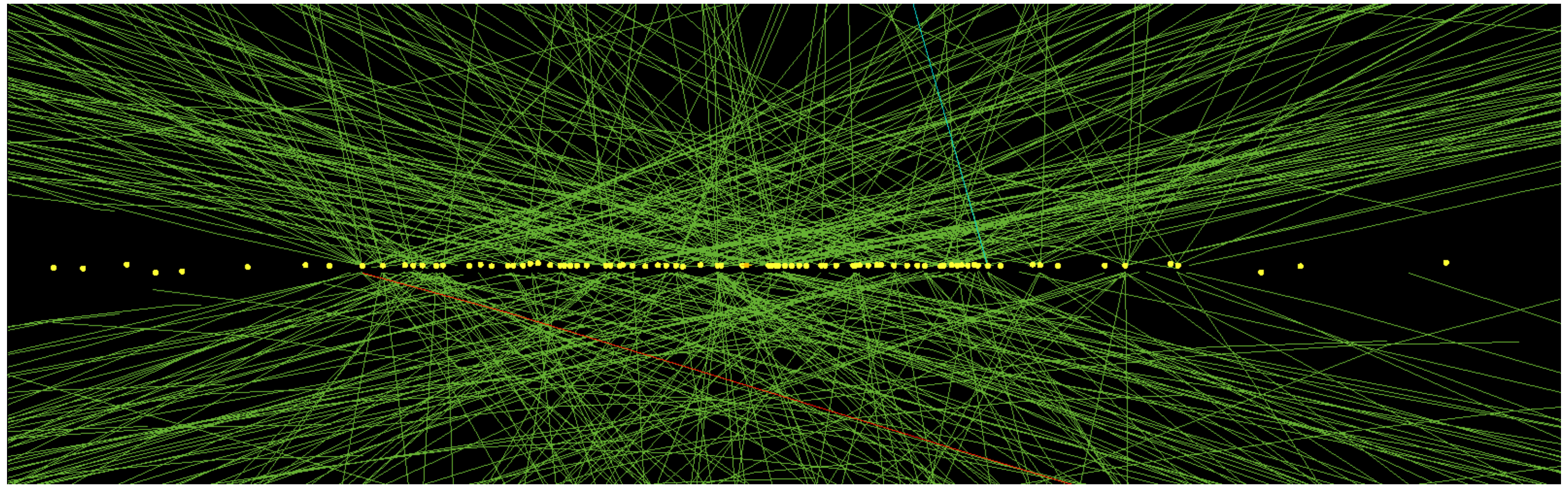
Pile-up suppression

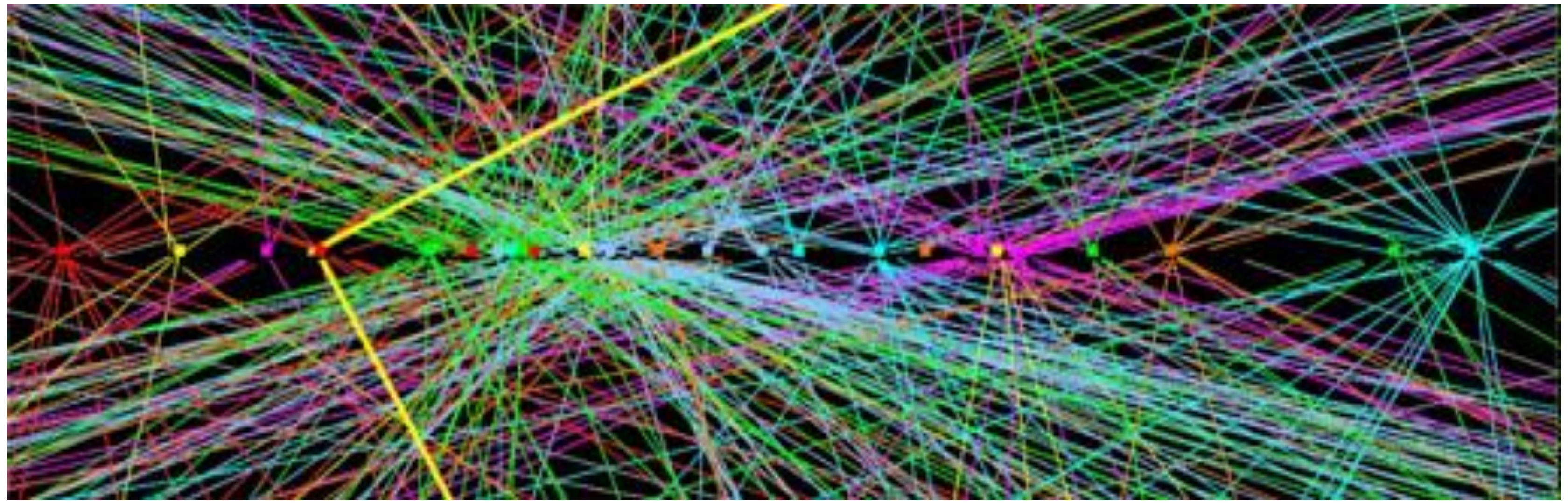


Timing for high-energy physics experiments

Hartmut F-W Sadrozinski *et al* 2018 *Rep. Prog. Phys.* **81** 026101

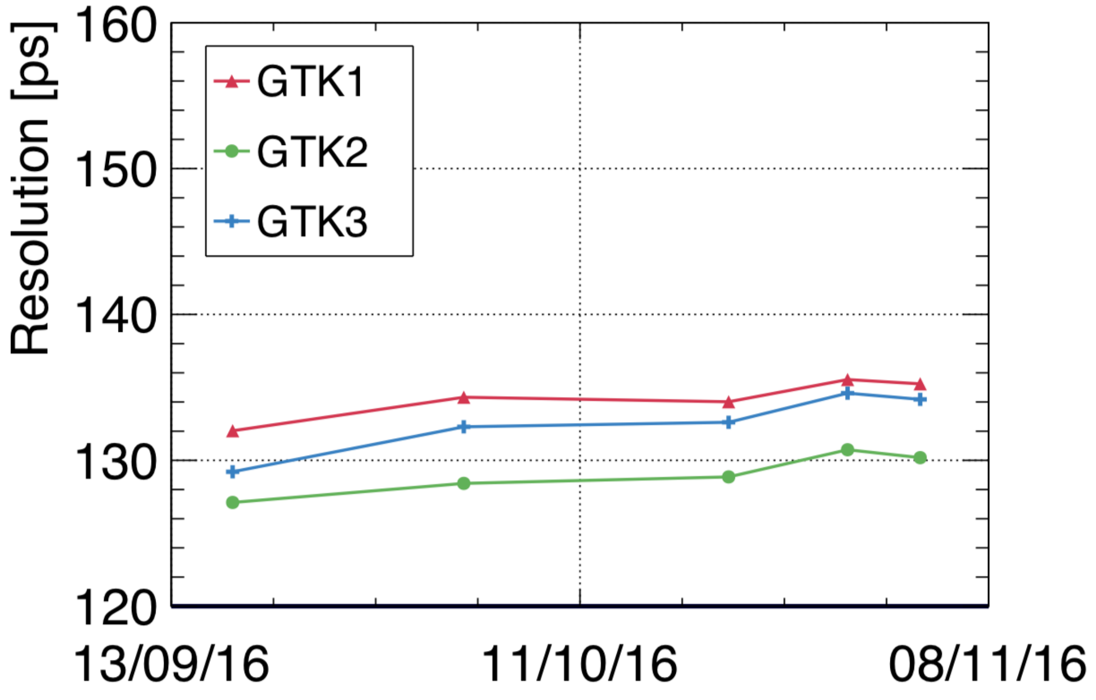
Pile-up suppression



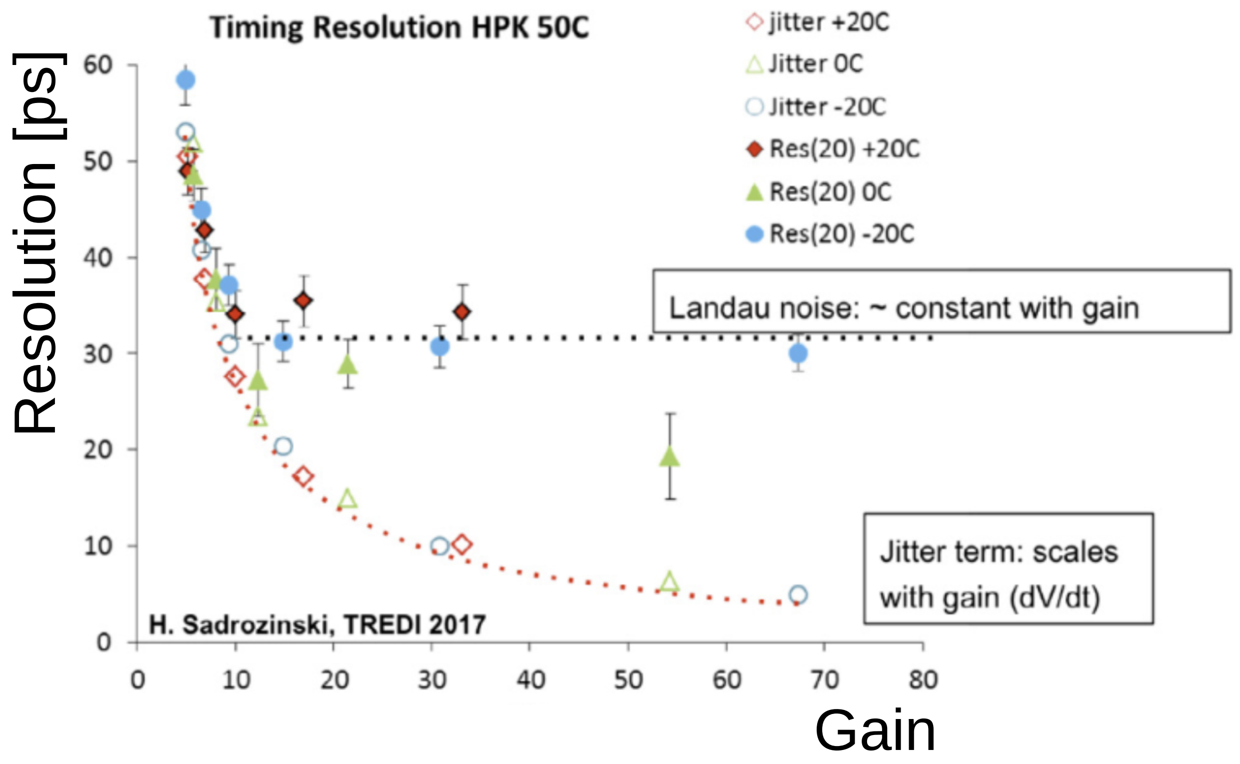


Situation today: technologies in HEP experiments

NA62 GigaTracKer:
hybrid pixels 300x300 μm^2
no internal gain
130 ps time resolution
G. Aglieri Rinella et al., JINST 14 (2019) P07010



Low Gain Avalanche Detectors:
hybrid pads 1x1 mm^2
internal gain (10-100)
30 ps time resolution
N. Cartiglia et al., NIM A 924 (2019) 350-354



Excellent results.

Is timing performance of silicon **fully exploited** ?

How far are we from producing a monolithic 4D sensor with small pixels ?

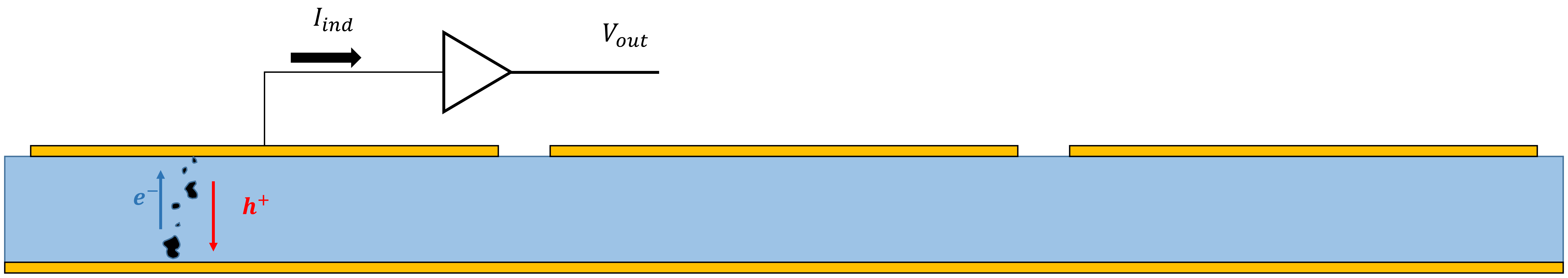
Timing with silicon detectors

Time resolution of silicon pixel detectors

(Recommended reading W. Riegler and G. Aglieri Rinella, Time resolution of silicon pixel sensors, JINST 12 (2017) P11017)

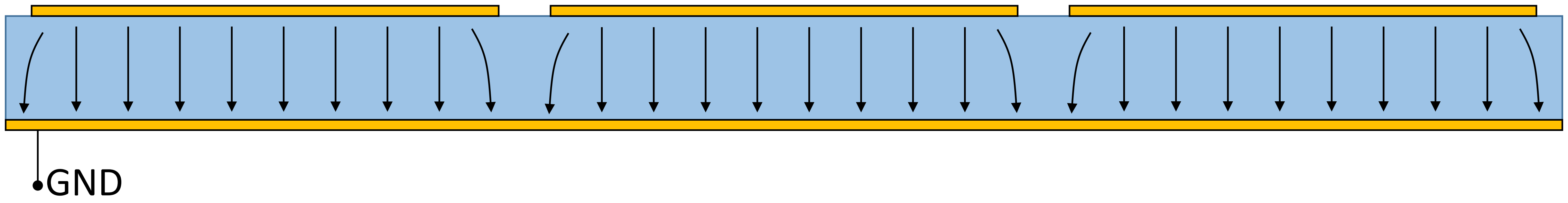
What are the main parameters that control the time resolution of semiconductor detectors?

1. Geometry & fields
2. Charge collection (or Landau) noise
3. Electronics noise



1. Geometry and fields

Sensor optimization for time measurement means:
sensor time response **independent** from the particle trajectory



$\Longrightarrow$ **"Parallel plate"** read out: wide pixel w.r.t. depletion depth

Induced current for a parallel plate readout from Shockley-Ramo's theorem:

$$I_{ind} = \sum_i q_i \bar{v}_{drift,i} \cdot \bar{E}_{w,i} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

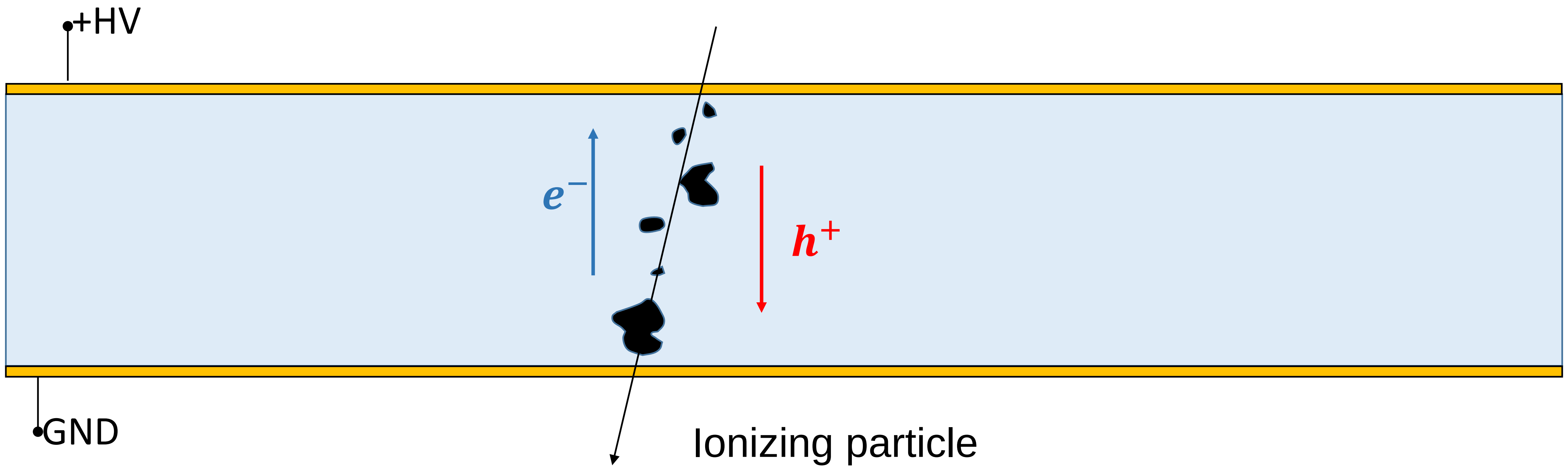
Scalar, saturated

Scalar, uniform

Desired features:

- **Uniform** Ramo field (signal induction)
- **Uniform** electric field (charge transport)
- **Saturated** charge drift velocity

2. Charge-collection (or Landau) noise

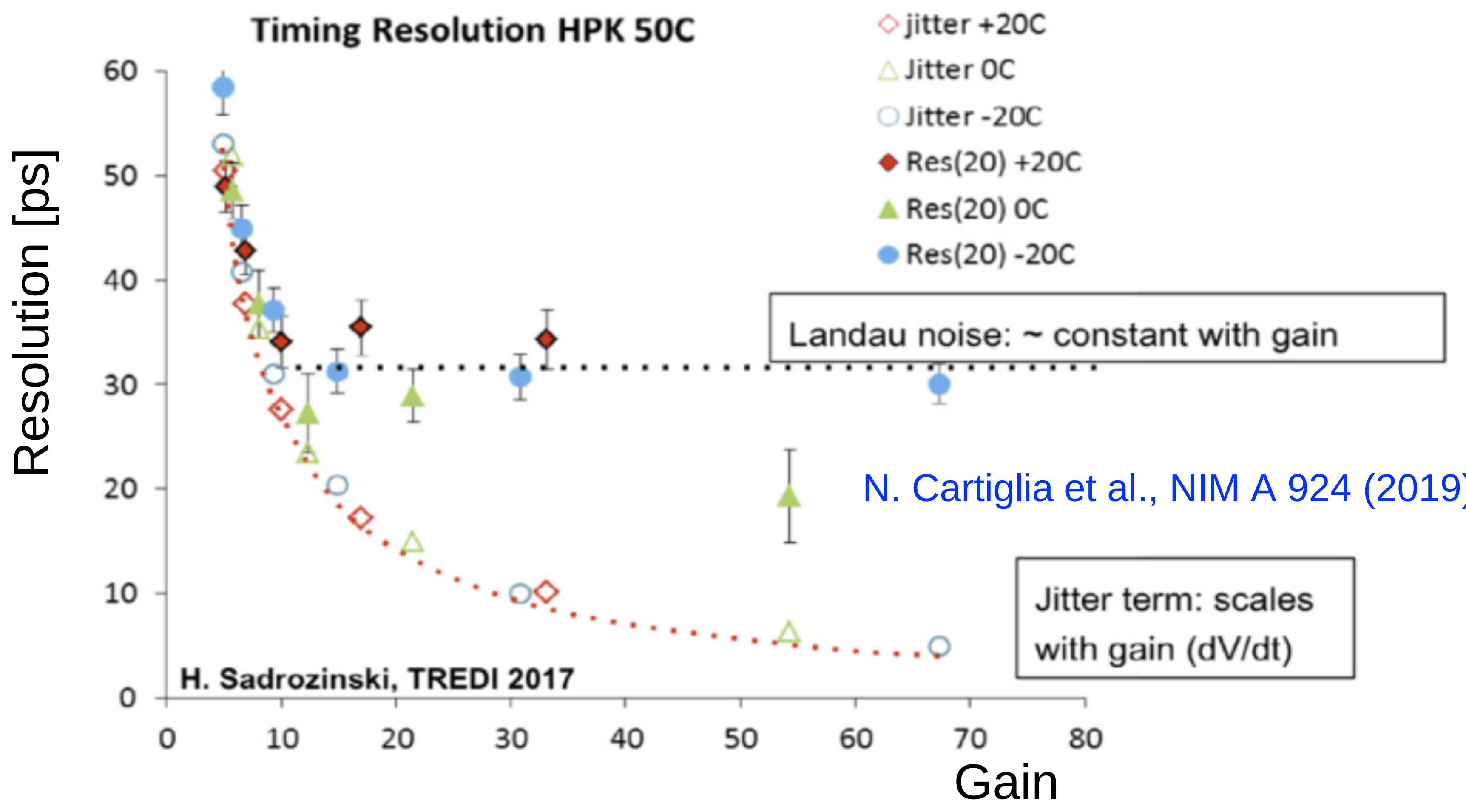


is produced by the **non uniformity of the charge deposition** in the sensor:

$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

When **large clusters** are absorbed at the electrodes, their contribution is removed from the induced current. The **statistical origin** of this variability of I_{ind} makes this effect irreducible in PN-junction sensors.

2. Charge-collection (or Landau) noise



N. Cartiglia et al., NIM A 924 (2019) 350-354

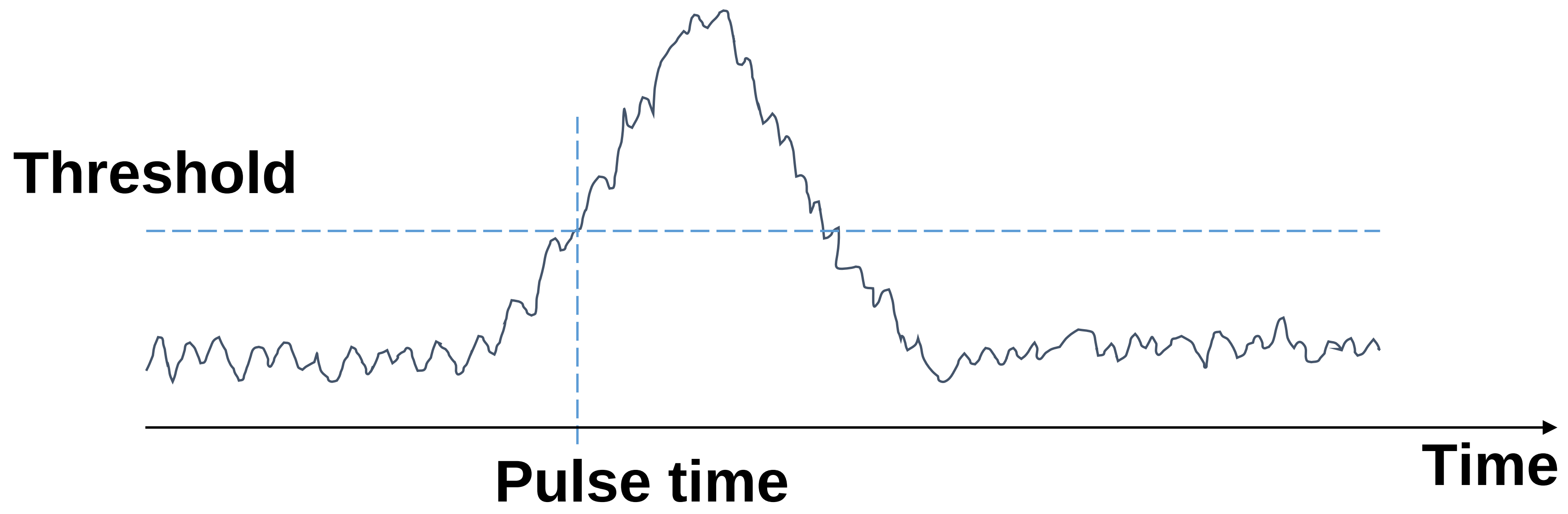
Charge collection noise represents an intrinsic limit to the time resolution for a semiconductor PN-junction detector.

~30 ps reached by present LGAD sensors.

Lower contribution from sensors without internal gain

3. Electronics noise

Once the geometry has been fixed, the time resolution depends mostly on the amplifier performance.

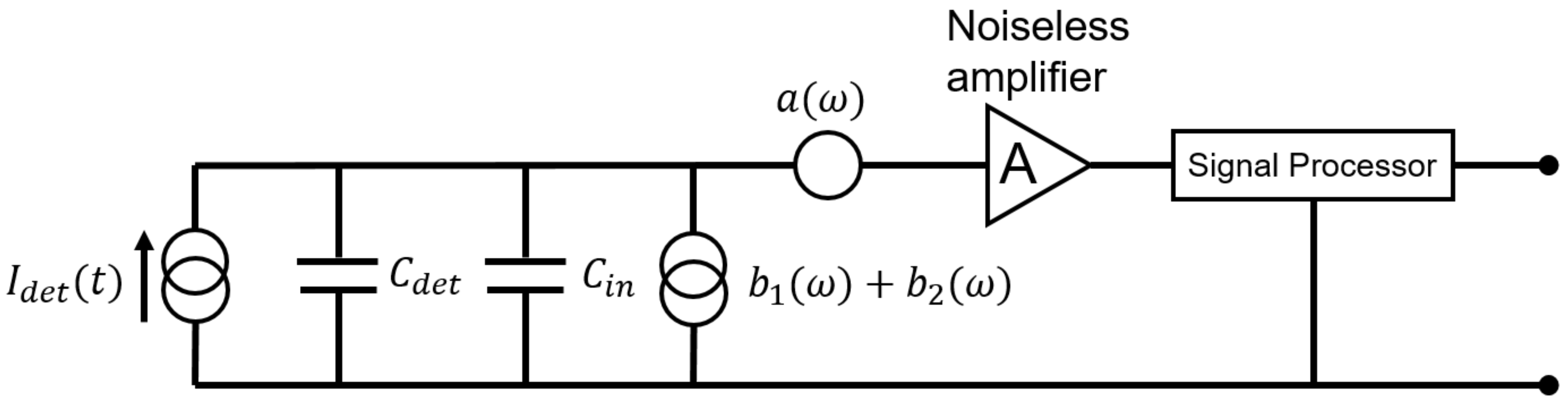


$$\sigma_t = \frac{\sigma_V}{\frac{dV}{dt}} \cong \frac{ENC}{I_{ind}}$$

Need an ultra-fast, low noise, low power-consumption electronics with fast rise time and small capacitance. Our solution:

High f_t, single transistor preamplifier.

Equivalent Noise Charge: device comparison

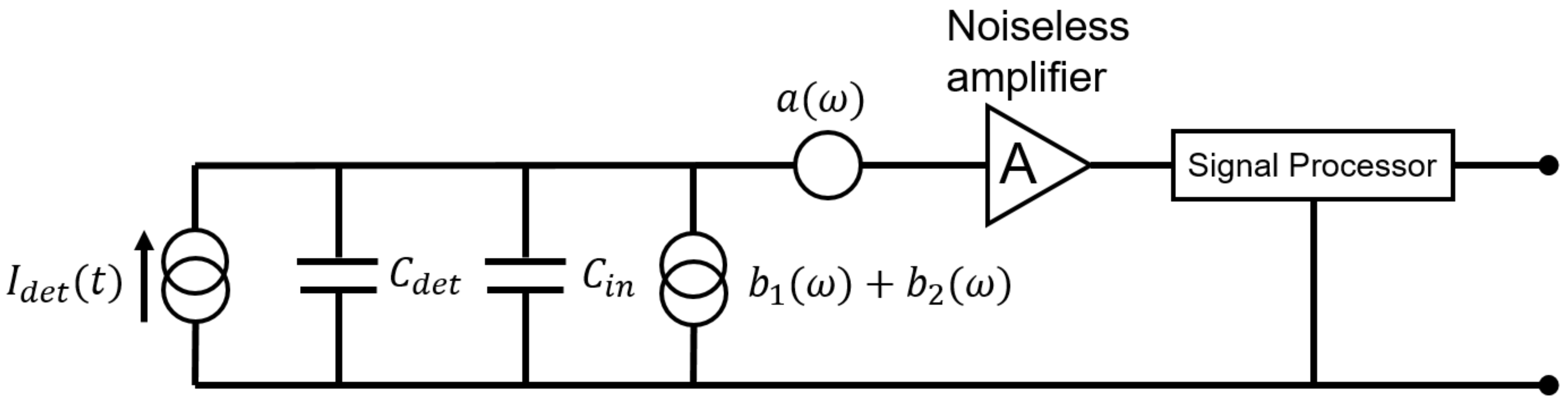


$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + \cancel{A_3(b_1 + b_2)\tau_M}$$

$$\boldsymbol{\tau_M \sim 1\, ns}$$

How do MOS-FET and BJT compare in terms of noise?

Equivalent Noise Charge: device comparison



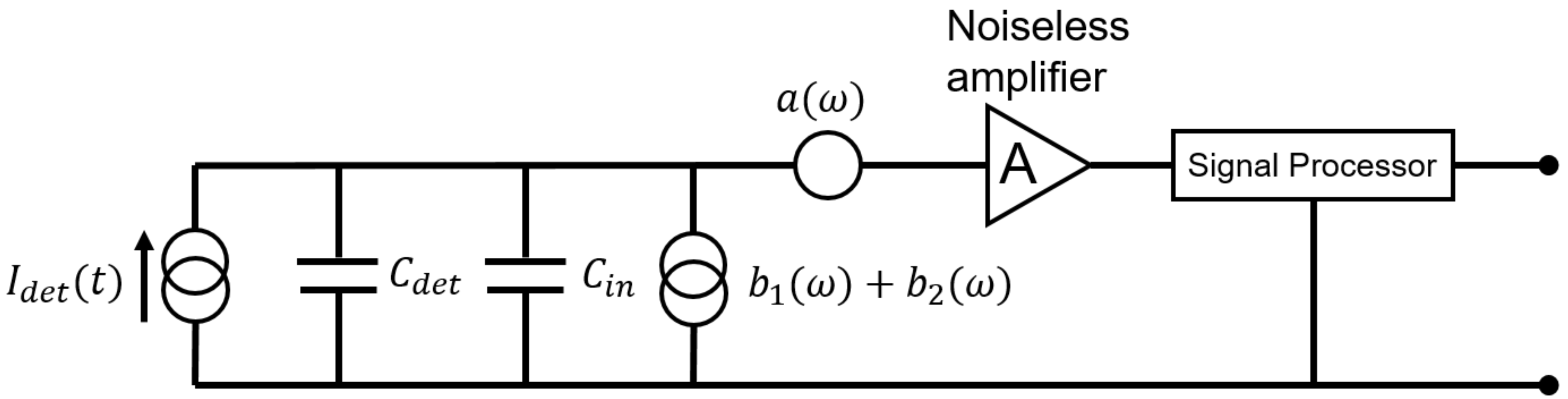
$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + A_3(b_1 + b_2)\tau_M$$

CMOS based amplifier

$$2kT \frac{h}{g_m}$$

Large $^1/_f$ contribution

Equivalent Noise Charge: device comparison



$$ENC^2 = A_1 \frac{a_W}{\tau_M}(C_{det} + C_{in})^2 + A_2 \frac{ln2}{\pi} c(C_{det} + C_{in})^2 + A_3(b_1 + b_2)\tau_M$$

BJT based amplifier

$$ENC_{\text{series noise}} \propto \sqrt{k_1 \cdot \frac{C_{tot}^2}{\beta} + k_2 \cdot R_b C_{tot}^2}$$

Goal: maximize the current gain β at high frequencies while keeping a low base resistance R_b

Equivalent Noise Charge

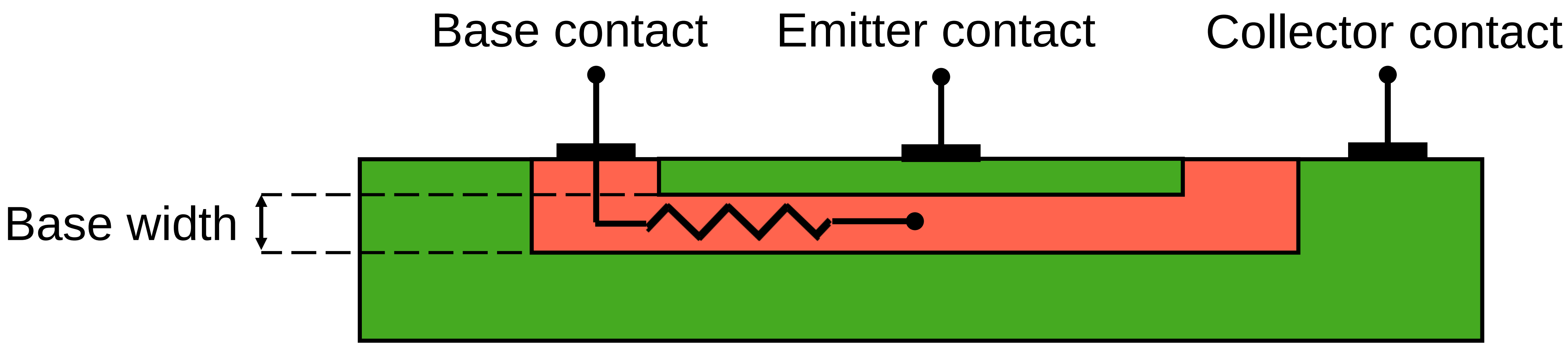
For a NPN BJT, the amplifier current gain β can be expressed as:

$$\beta = \frac{i_C}{i_B} = \frac{\tau_p}{\tau_t}$$

τ_p = hole recombination time in Base

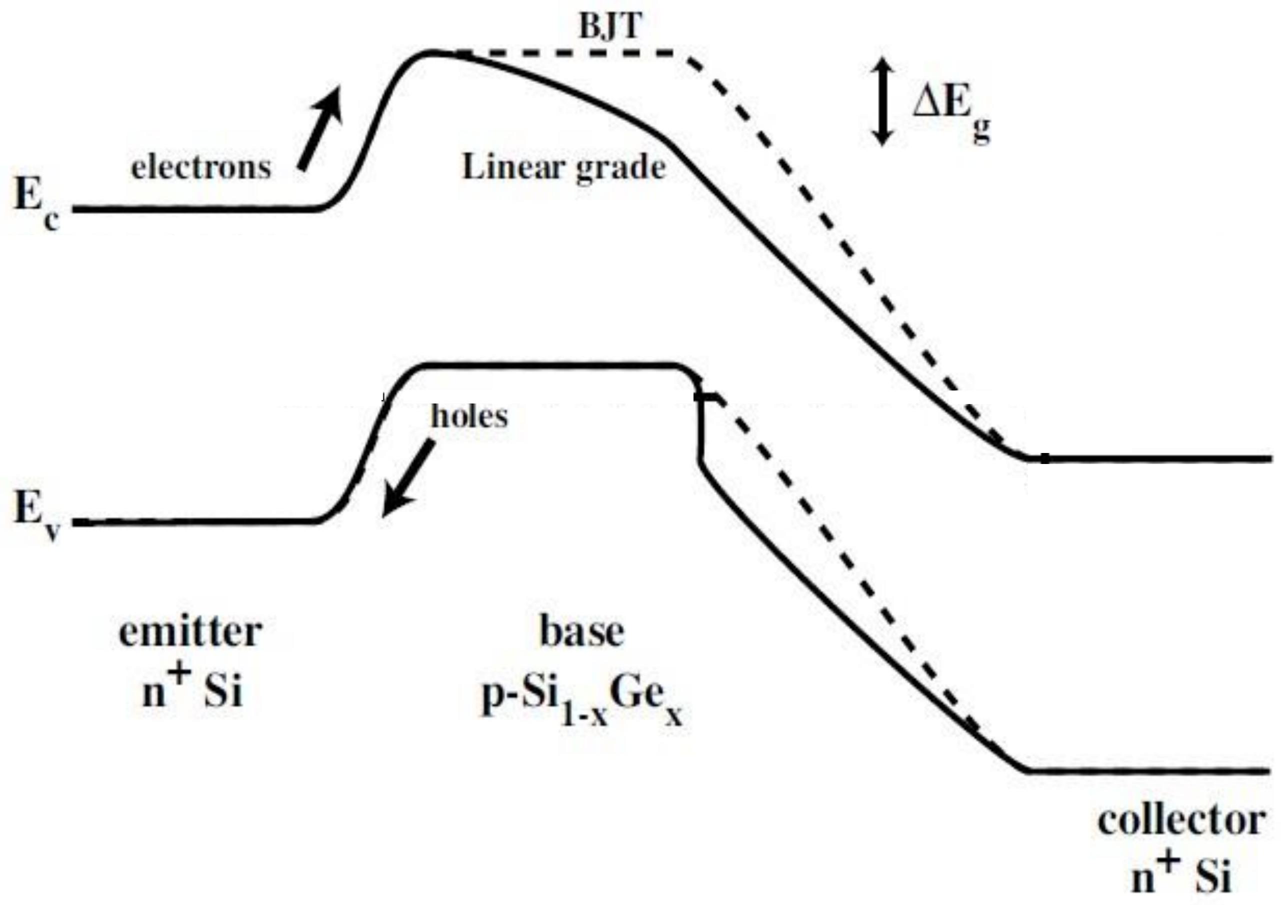
τ_t = electron transit time (Emitter to Collector)

Large $\beta \Longrightarrow$ Minimize the electron transit time



SiGe HBT technology for low-noise, fast amplifiers

In SiGe Heterojunction Bipolar Transistors (HBT) the **grading** of the bandgap in the Base changes the **charge-transport mechanism** in the Base from **diffusion** to **drift**:



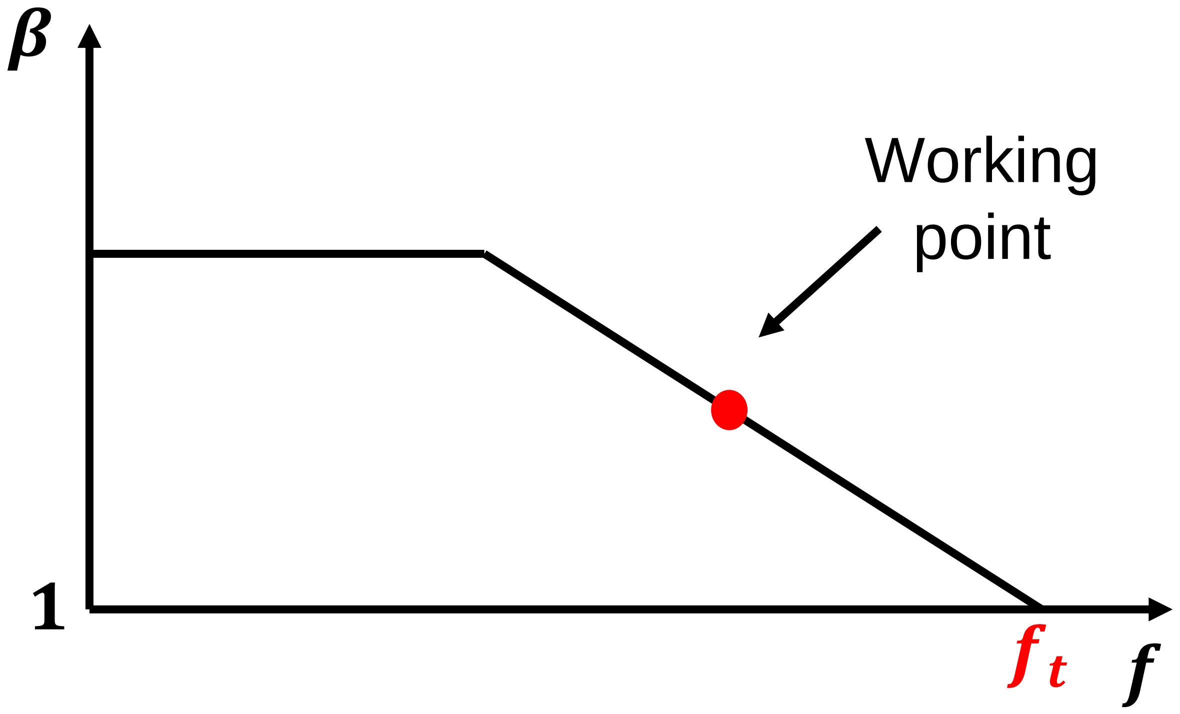
Grading of germanium in the base:
field-assisted charge transport in the Base,
equivalent to introducing an electric field in the Base

$\Longrightarrow$ short e^- transit time in Base $\Longrightarrow$ very high β

$\Longrightarrow$ smaller size $\Longrightarrow$ reduction of R_b and very high f_t

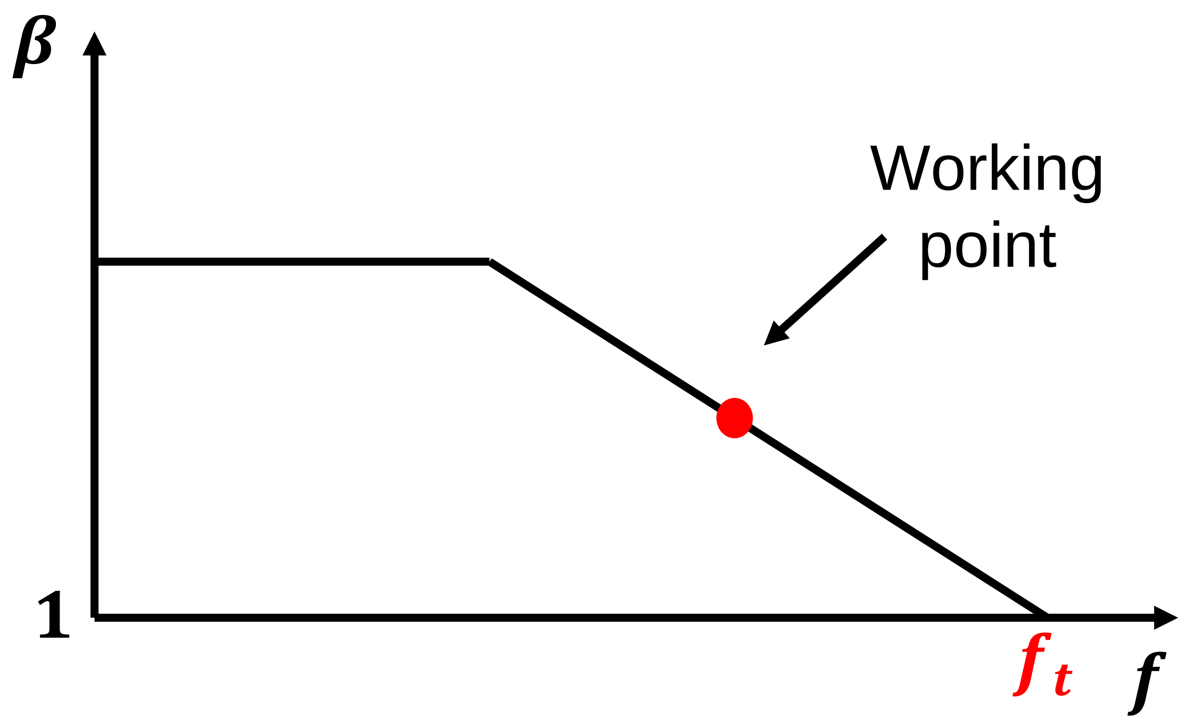
Hundreds of GHz

Current gain and power consumption: f_t is the key



	$f_t = 10\ GHz$	$f_t = 50\ GHz$	$f_t = 100\ GHz$
β_{max} at $200\ MHz$	50	250	500
β_{max} at $1\ GHz$	10	50	100
β_{max} at $5\ GHz$	2	10	20

Current gain and power consumption: f_t is the key



	$f_t = 10\ GHz$	$f_t = 50\ GHz$	$f_t = 100\ GHz$
$\beta_{max}\ at\ 200\ MHz$	50	250	500
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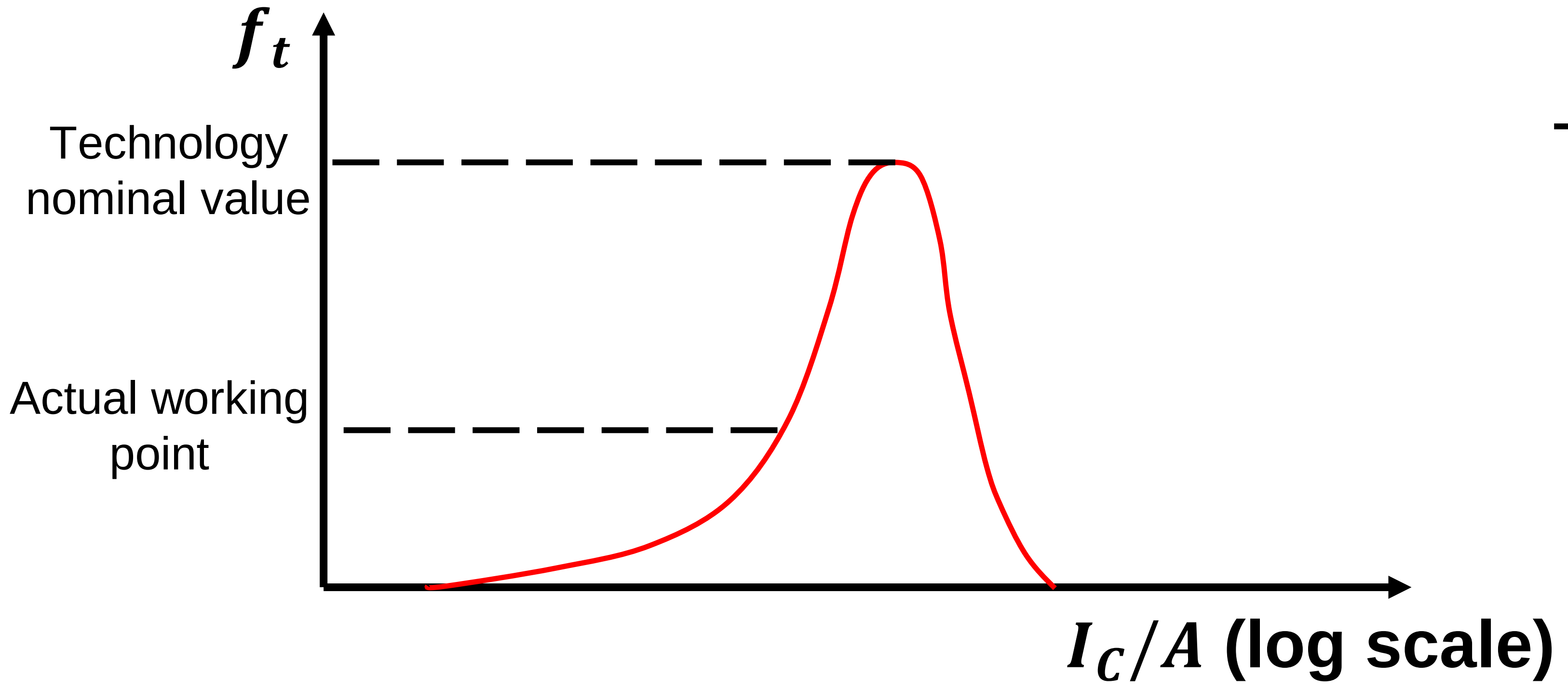


Trade-off: **ENC** ⇔ **Power Consumption**

$f_t > 100\ GHz$ technologies are necessary for a fast amplification of silicon pixel signals.

SiGe BiCMOS applications

Commercial VLSI CMOS foundry processes available

source: https://towerjazz.com/technology/rf-and-hpa/sige-bicmos-platform/

Applications:
- Automotive radars (27/77 GHz)
- Satellite communications
- LAN RF transceivers (60 GHz)
- Point-to-point radio (V-band, E-band)
- Defense
- Security
- Instrumentation

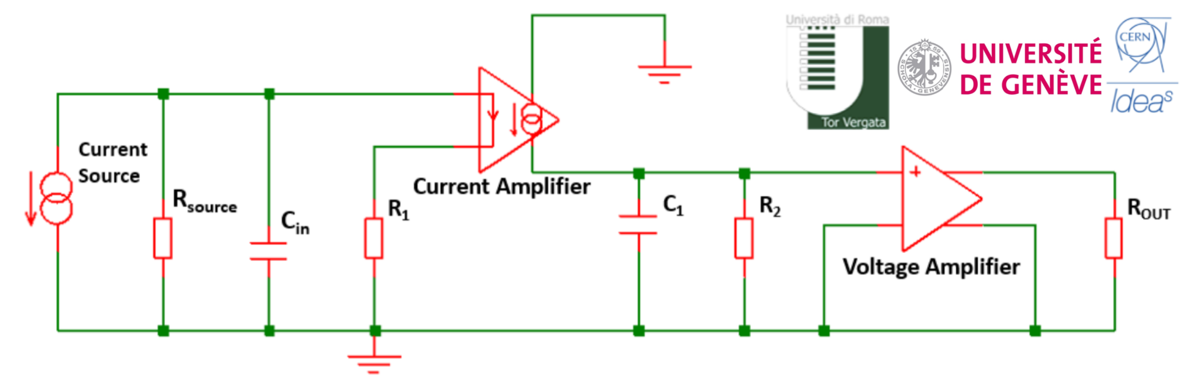
Foundries offering SiGe process:
- IHP Mikroelektronik (→ Research Inst.)
- TowerJazz
- Globafoundries
- TSMC
- STM
- AMS
- ...

A **fast growing technology: f_t = 700 GHz** transistor under development

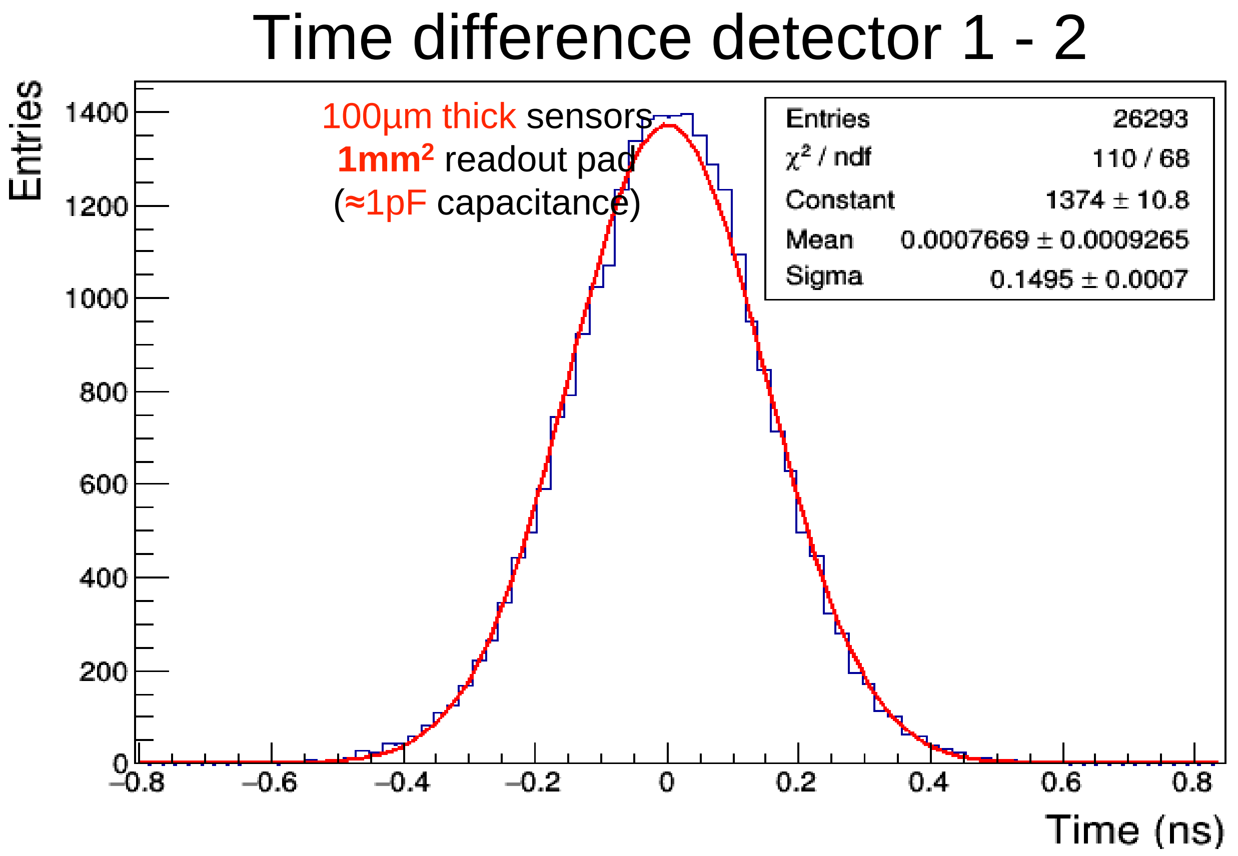
Discrete-component SiGe HBT amplifier

In 2015:

- **Proof-of-concept SiGe amplifier** and produced it with **discrete components**
- This amplifier was coupled to a 100µm thick n-on-p silicon sensor with readout pad of **1mm^2** area (~1pF capacitance)



JINST 11 (2016) P03011: https://doi.org/10.1088/1748-0221/11/03/P03011



$$\sigma_T = \frac{(150 \pm 1)\text{ps}}{\sqrt{2}} = (106 \pm 1)\text{ps}$$

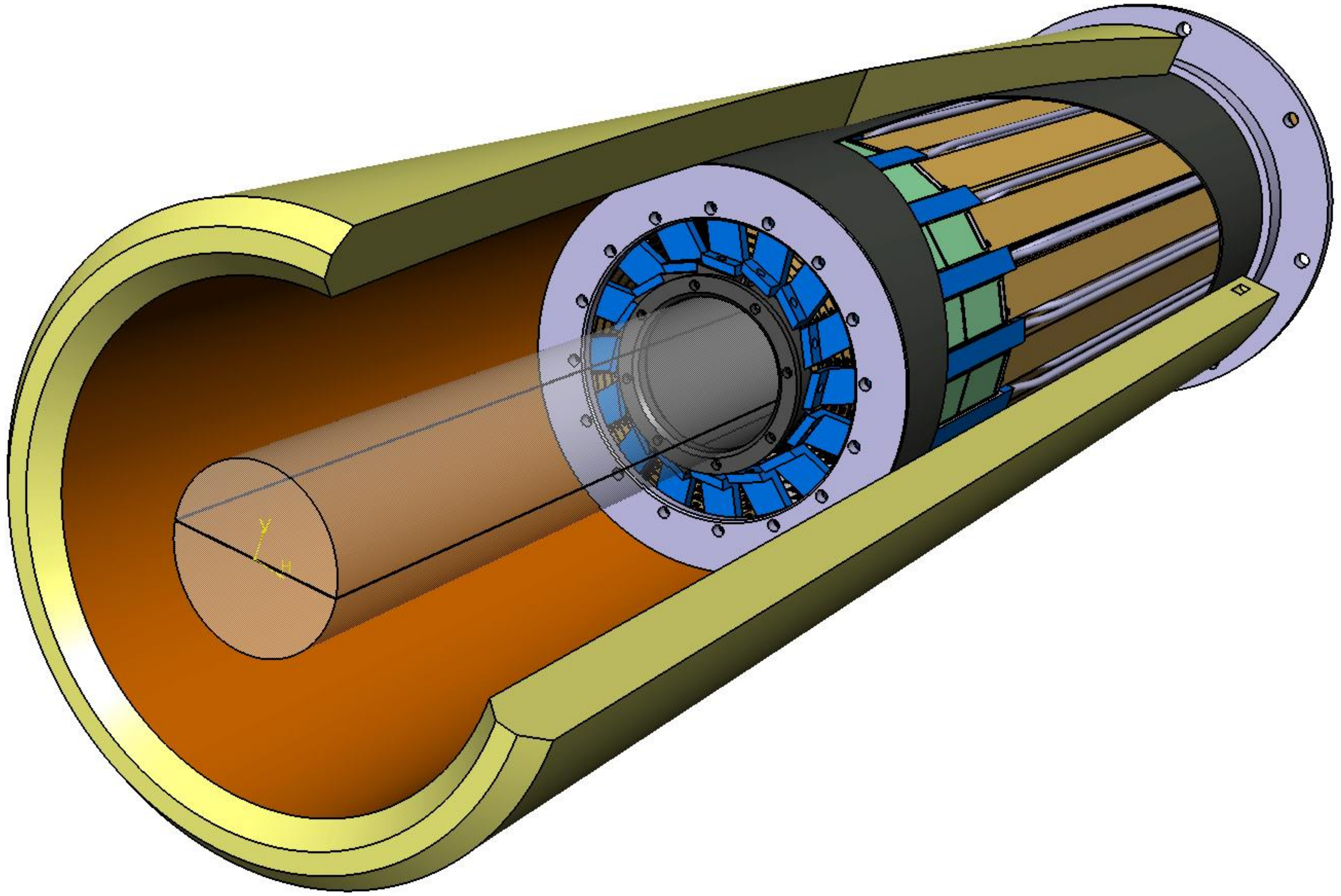
measured with MIPs

Remarkable result for a 1mm^2 silicon pad (1pF capacitance) **without internal gain**

Published in JINST 11 (2016) P03011: https://doi.org/10.1088/1748-0221/11/03/P03011

The TT-PET project: a 30 ps[+] Time-of-Flight PET scanner with monolithic SiGe silicon pixels

TT-PET



([+] GEANT4 simulation shows that 100 ps for MIPs corresponds to ~30 ps in case of the 511 keV photons of a PET)

Time-Of-Flight PET

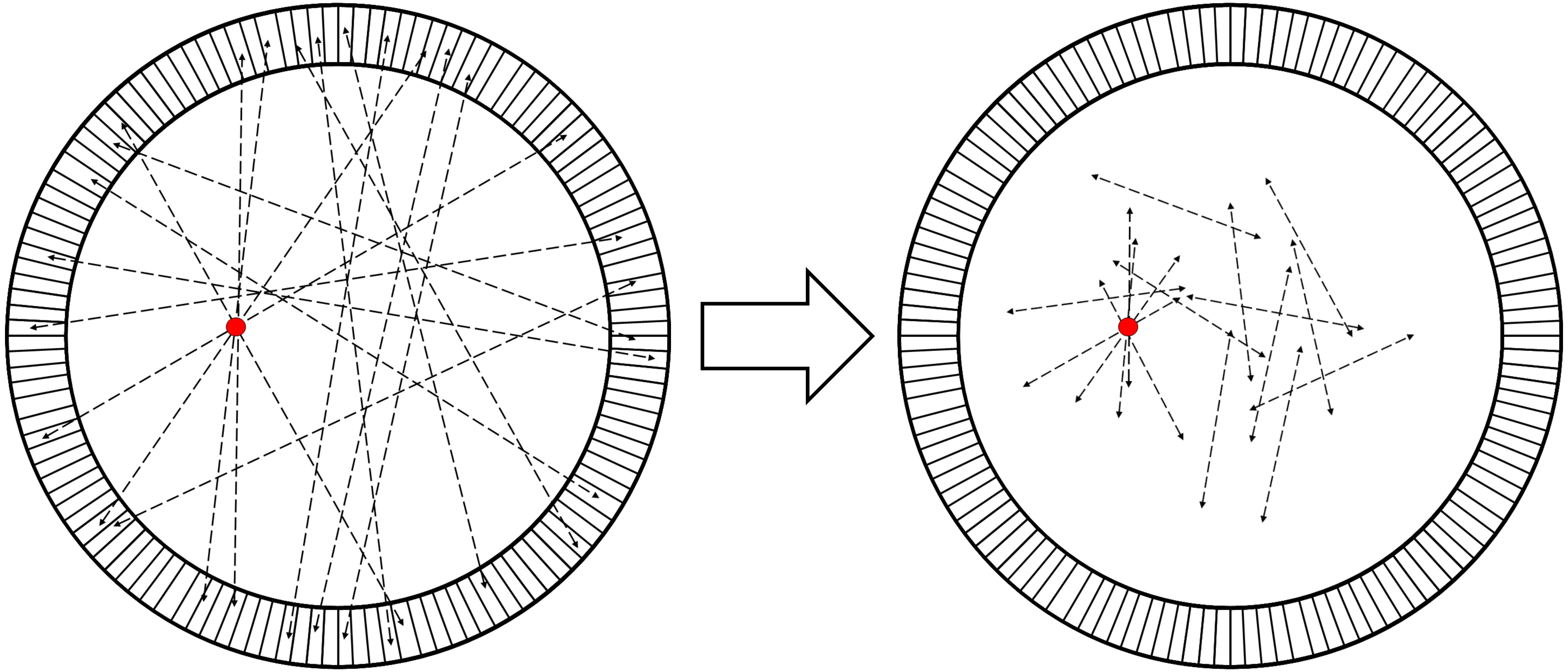
TT-PET

Improved background rejection by measurement of difference in arrival time of the two photons.

Goal:

30 ps time resolution for
1 cm spatial measurement

FLASH SLIDE



The TT-PET team funded by

SWISS NATIONAL SCIENCE FOUNDATION

TT-PET

DPNC Geneva:

Giuseppe Iacobucci
- P. I.
- Scanner design

Lorenzo Paolozzi
- Sensor design
- Analogue electronics design

Pierpaolo Valerio
- Electronics design
- Chip design

HUG Geneva:

Osman Ratib
- Scanner operation

Emanuele Ripiccini
- Scanner simulation
- Image reconstruction

Daiki Hayakawa
- Sensor simulation
- Image reconstruction

LHEP Bern:

Michele Weber
- Scanner assembly

A. Miucci/D. Forshaw
- Readout system
- Scanner assembly

Yves Bandi
- Readout system

Collaboration with:
- **Roberto Cardarelli (INFN Roma Tor Vergata)**
- **Holger Ruecker (IHP Microelectronics)**
- **Marzio Nessi (CERN & UNIGE)**

and their research teams

Frank Cadoux
- Mechanics design and assembly, thermal management

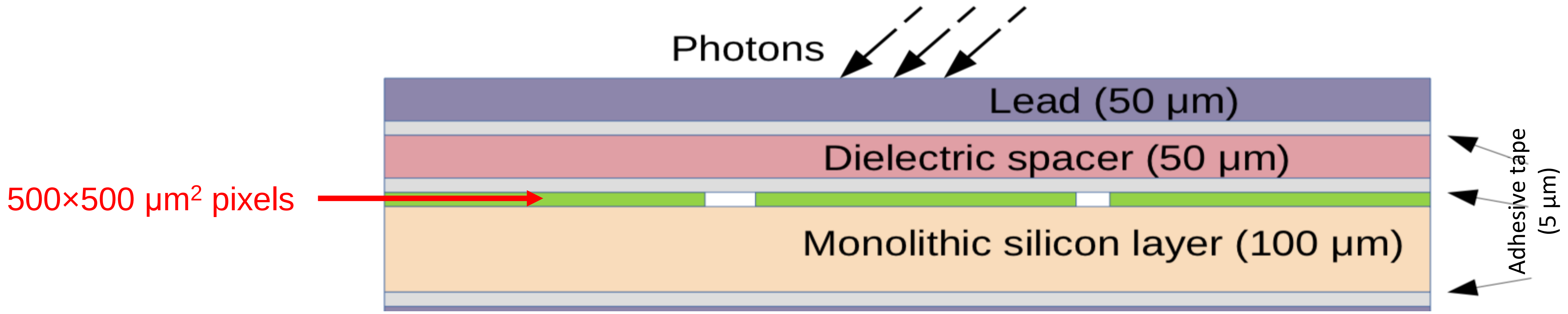
Stéphane Debieux
- Board design, system-level electronics

Yannick Favre
- Readout system

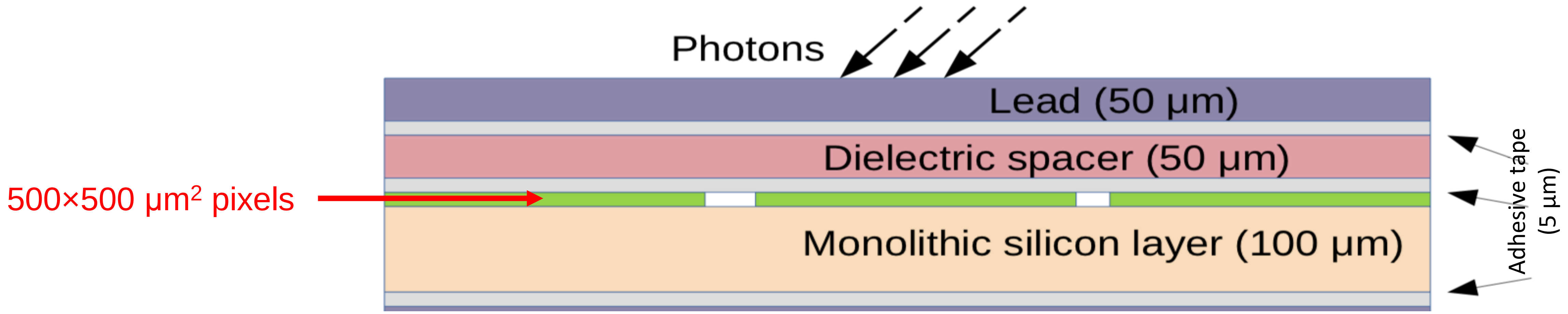
Mathieu Benoit
- Sensor and guard ring simulation

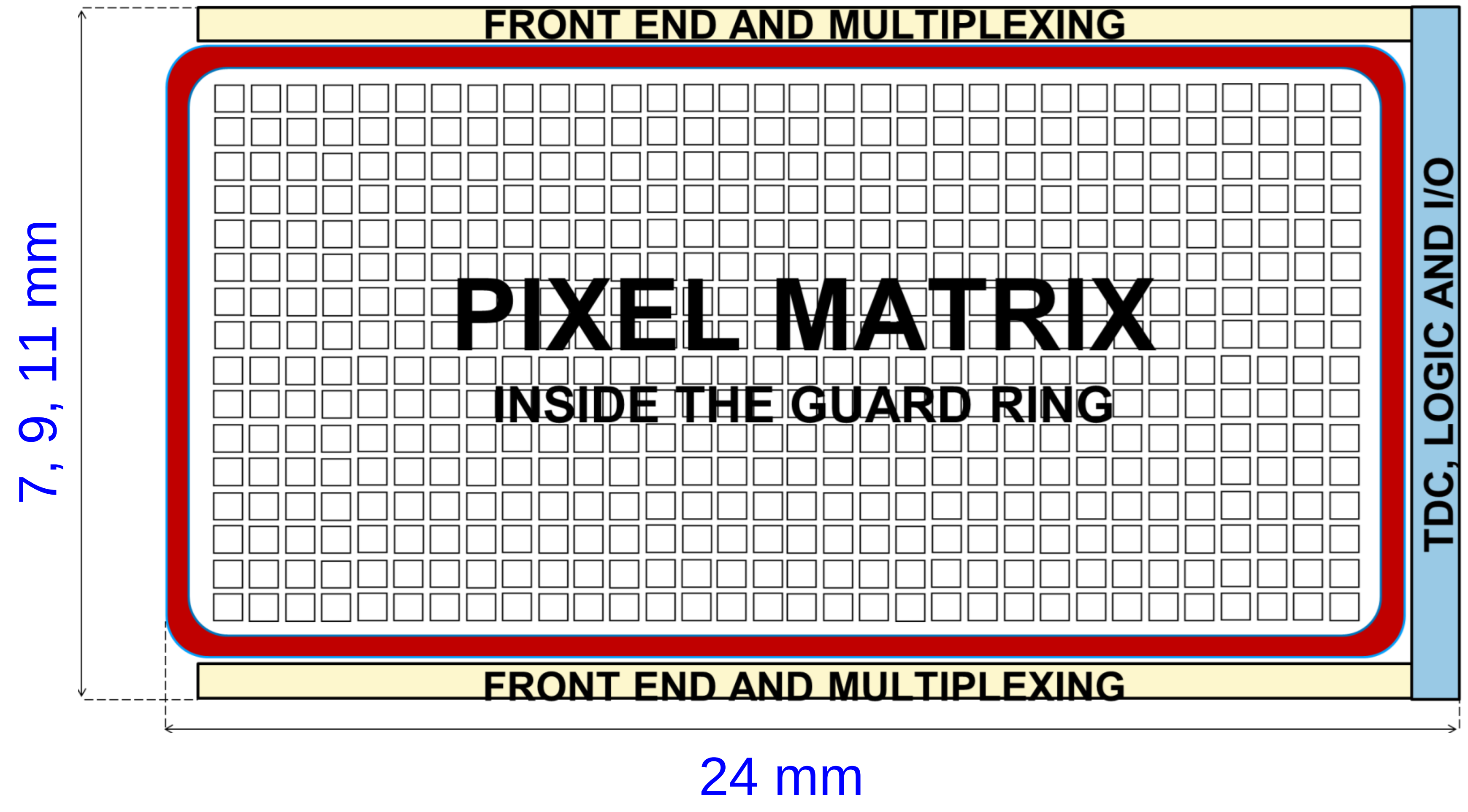
Didier Ferrere
- Scanner assembly support

TT-PET: Basic detection unit

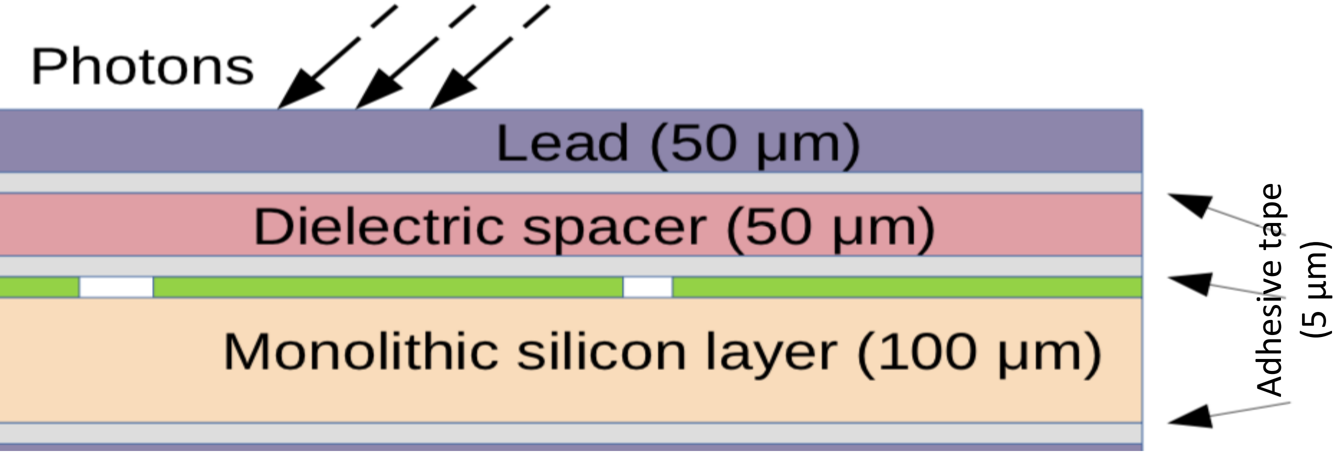


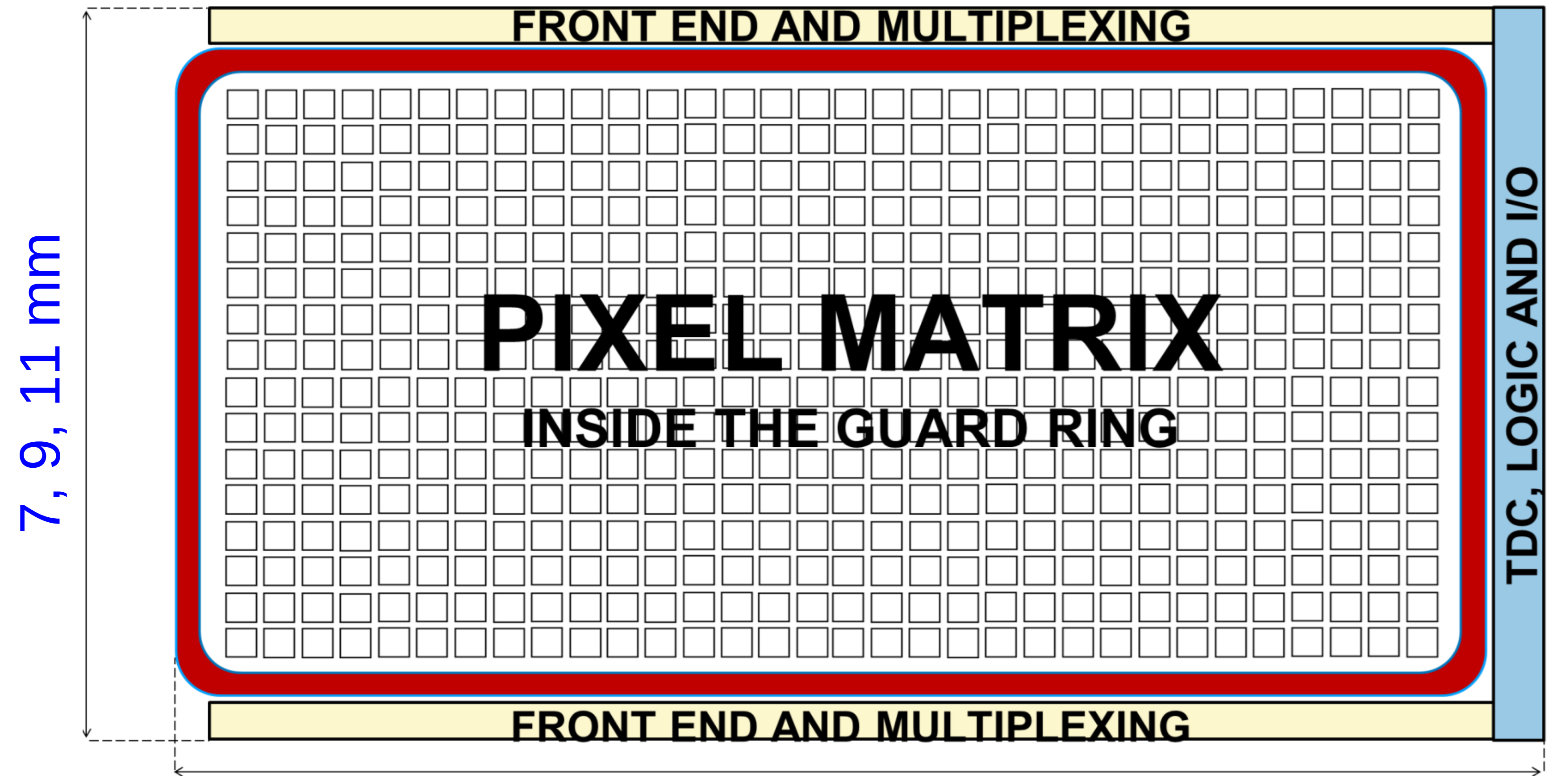
TT-PET: Basic detection unit





TT-PET: Basic detection unit





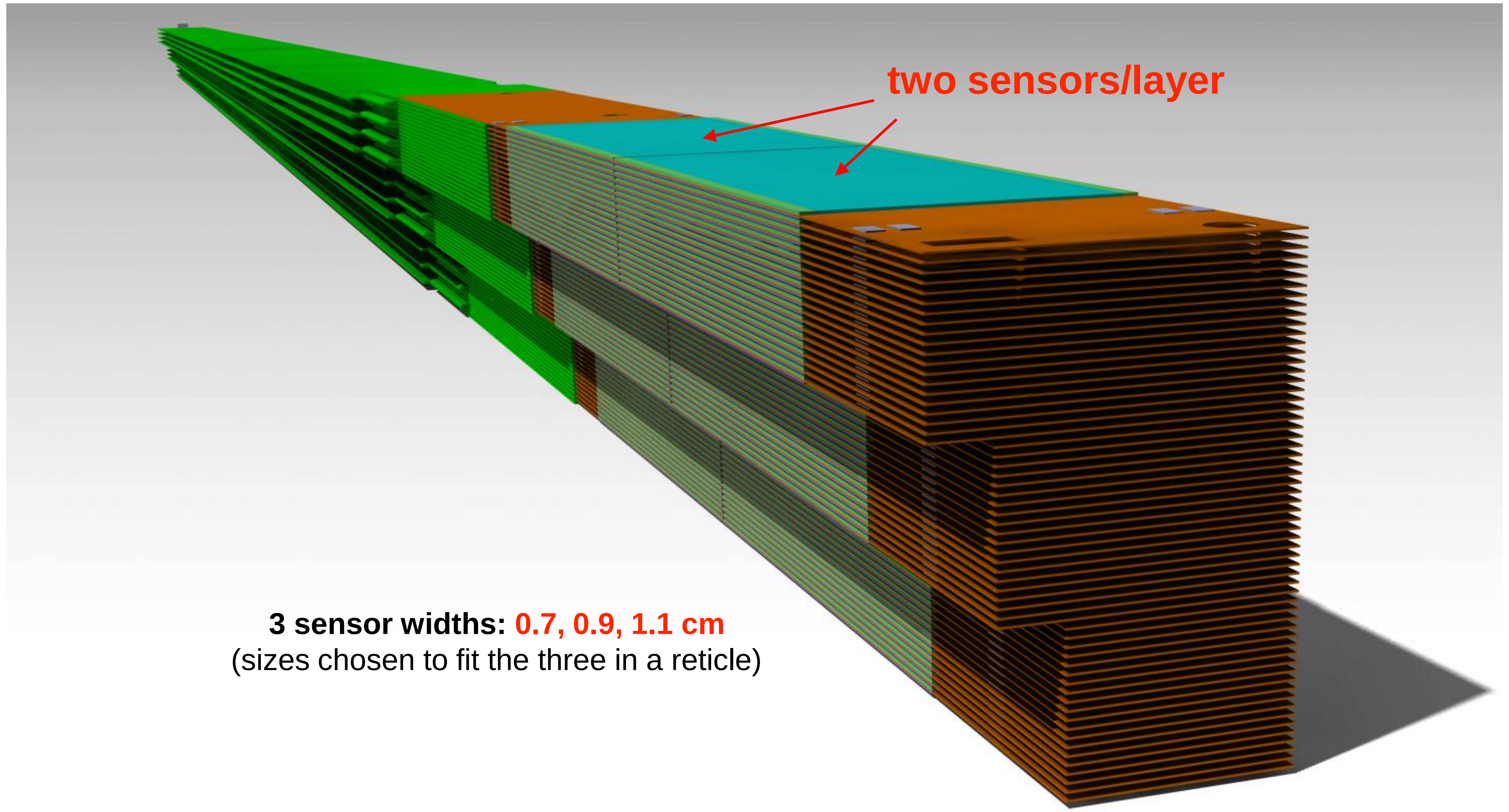
ASIC length	$24\ mm$
ASIC width	$7, 9, 11\ mm$
Pixel Size	$500 \times 500\ \mu m^2$
Pixel Capacitance (comprised routing)	$750\ fF$
Preamplifier power consumption	$80\ mW/cm^2$
Preamplifier Equivalent Noise Charge	$600\ e^-\ RMS$
Preamplifier Rise time (10% - 90%)	$800\ ps$
Time resolution for MIPs	$100\ ps\ RMS$
TDC time binning*	$50\ ps$
TDC power consumption	$< 1\ mW/ch$

*** NOTE: 1920 chips synchronized at $\mathcal{O}(10)\ ps$ precision.**
A new TDC synchronization technique developed for this project patented.

Patent EP18181123

TT-PET: Scanner Tower

TT-PET



- A tower is a stack of **60 detection units**, tightly coupled.
- Total tower thickness: **1.5 cm**
- Two sensors/layer: **4.8 cm length**
- Wedge-shaped: **three sensor widths**
- Tower assembly will be done with the SET Accµra100 DPNC flip-chip machine.

Results of GEANT and FLUKA simulations:

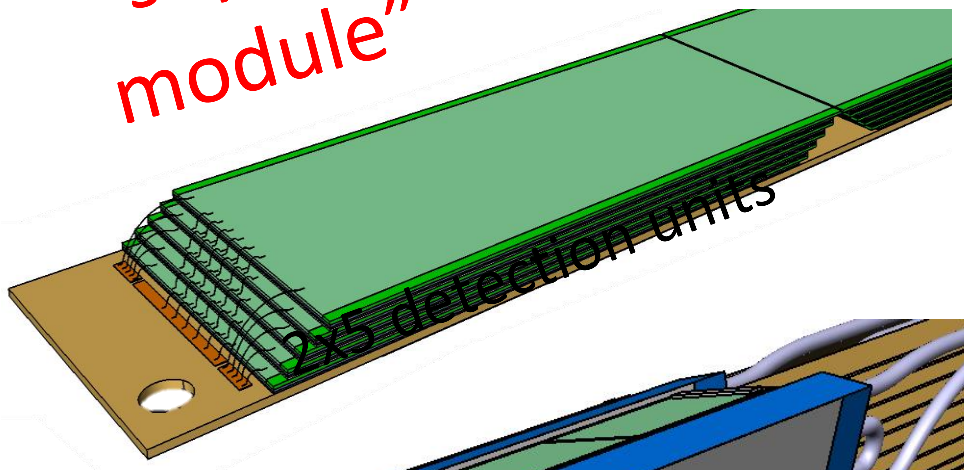
Tower efficiency for 511 keV photons: 27%

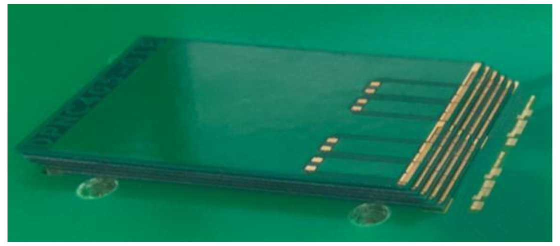
Scanner sensitivity: 4.1%

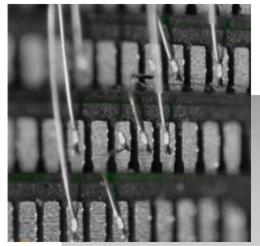
The TT-PET small-animal scanner

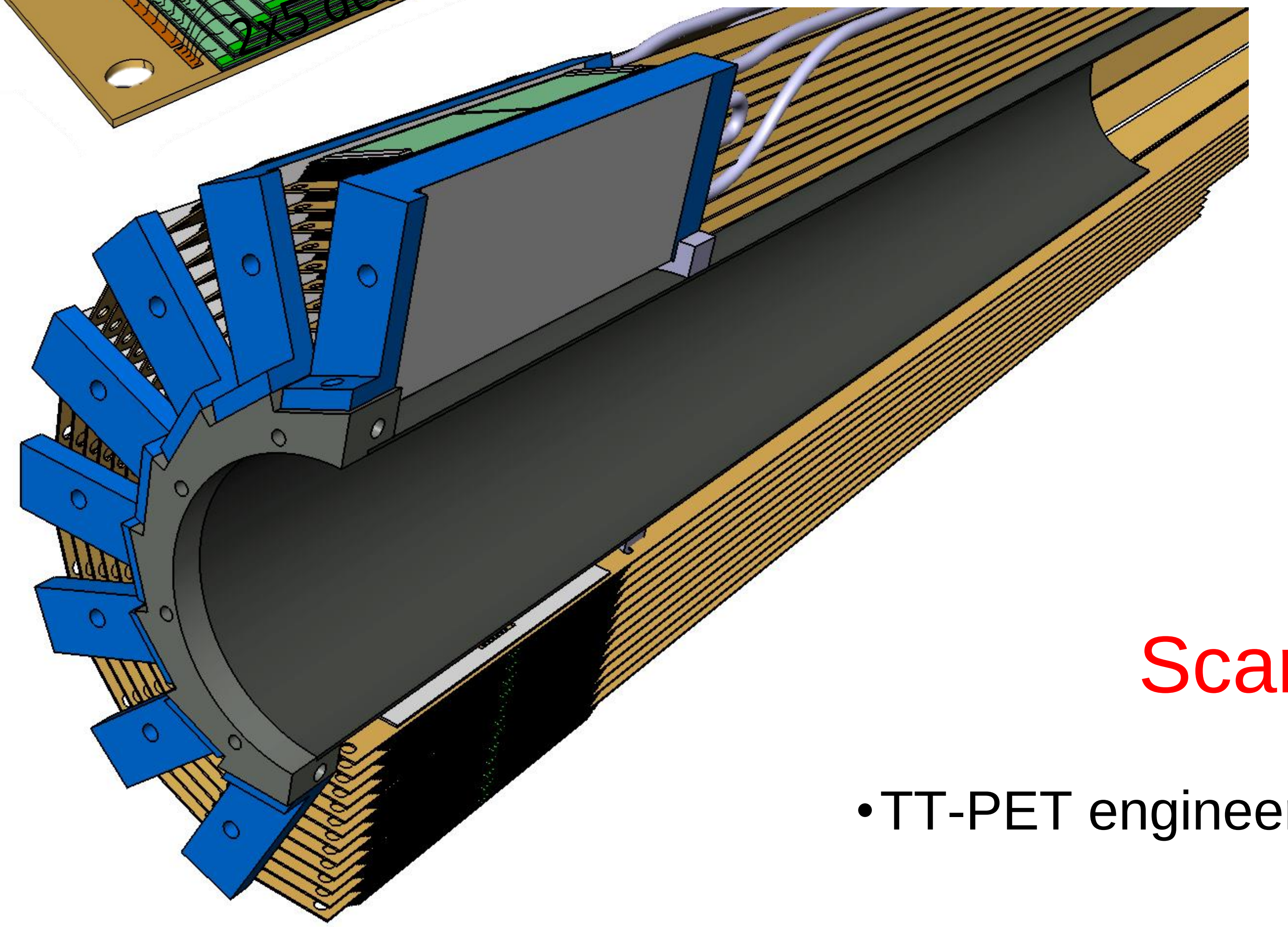
TT-PET

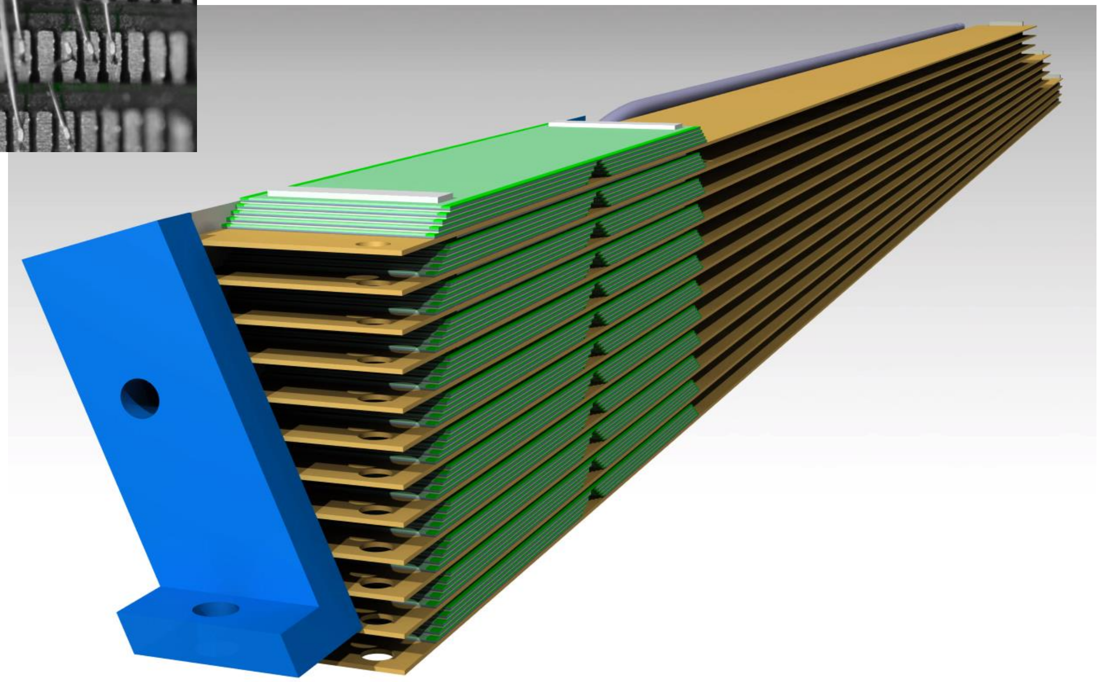
“super-module”











“Tower”

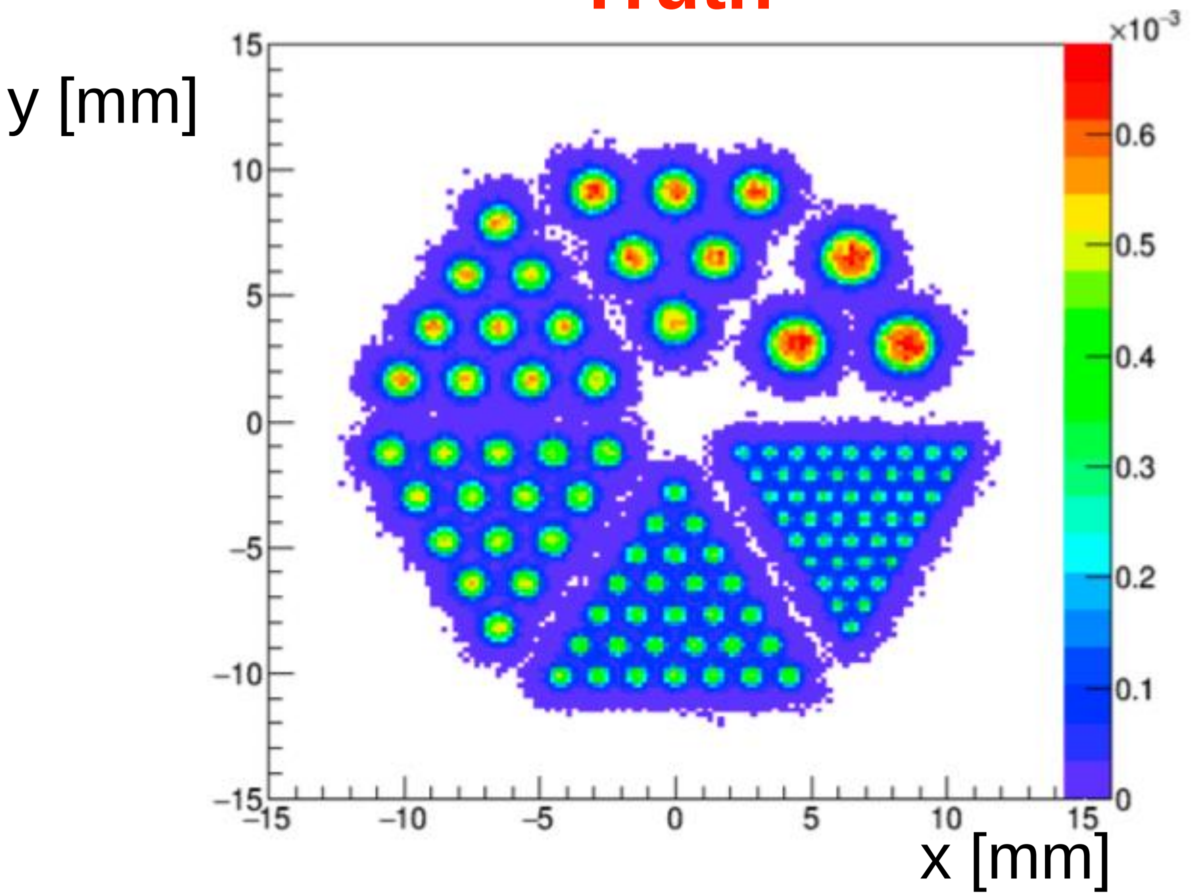
Scanner fully engineered

- TT-PET engineering and cooling system preprint: arxiv:1812.00788

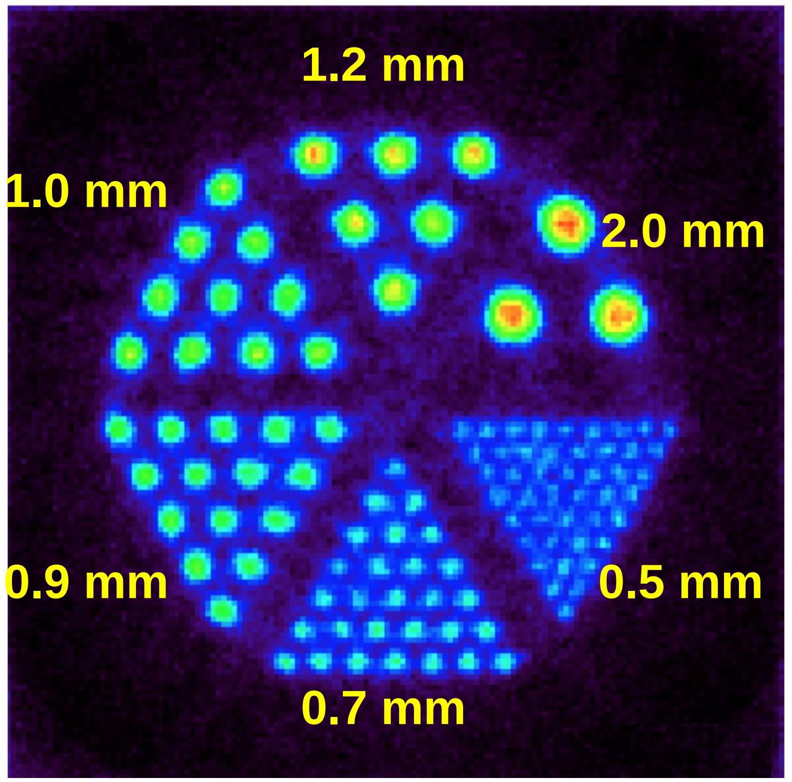
The TT-PET small-animal scanner

Excellent performance expected.
MLEM iterative reconstruction of Derenzo phantom:

Truth



Reconstructed



High FWHM resolutions in entire Field-Of-View:

Z position [mm]		0				12.5			
X position [mm]		0	5	10	15	0	5	10	15
FWHM [mm]	Radial	0.59	0.57	0.56	0.52	0.65	0.61	0.60	0.56
	Tangential	0.60	0.60	0.67	0.71	0.64	0.65	0.65	0.70
	Axial	0.50	0.49	0.50	0.51	0.45	0.45	0.45	0.45

TT-PET **simulation & performance preprint**: https://arxiv.org/abs/1811.12381

Challenges towards a monolithic ASIC

Time resolution of 30 ps for Eγ = 511 keV: ultra-fast electronics

Achieved in discrete SiGe components, but need to implement it in ASIC. Need to **identify technology** that allows for it.

Power consumption

Proof-of-concept results were obtained with a power consumption of ≈1.4W/cm^2. The target for the chip power is **80mW/cm^2**

Synchronization of a thousand chips at few ps precision

Given the low power budget, we needed a **new concept** for the TDC and synchronisation system

Monolithic integration

Requires to define a strategy for the sensor design to have a simple and effective structure, a detailed simulation and possibly a **collaboration with the foundry**

Technology choice

Exploit the properties of state-of-the-art SiGe Bi-CMOS transistors to produce an **ultra-fast, low-noise, low-power consumption amplifier**

Leading-edge technology: **IHP SG13G2**

130 nm process featuring **SiGe HBT** with

- Transistor transition frequency: $f_t = 0.3\, THz$
- DC Current gain: $\beta = 900$

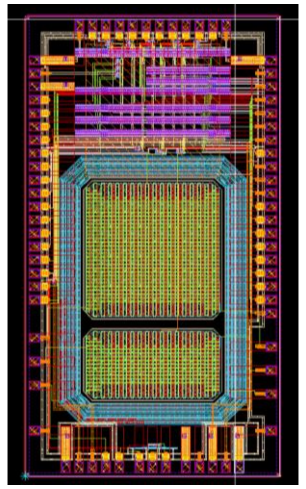
innovations for high performance microelectronics
Leibniz-Institut für innovative Mikroelektronik

Time digitization:

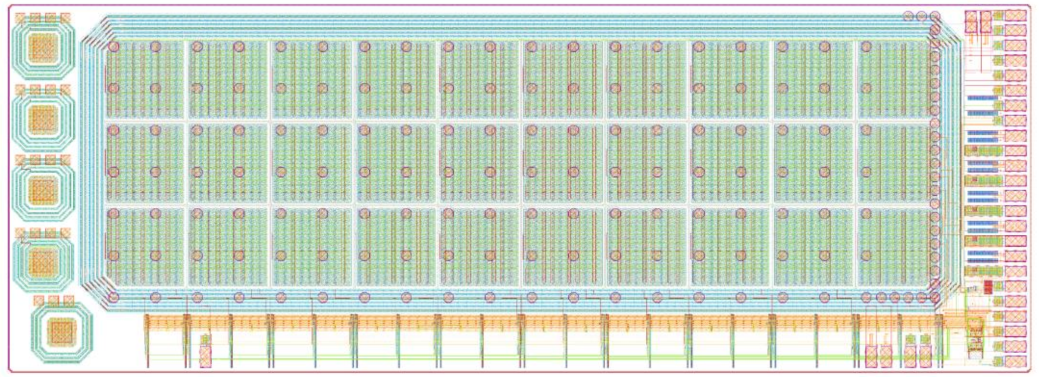
- 4 ps inverter; delay precision ~100 fs
- > 40GHz oscillation frequency achievable with purely digital schematics

We were able to design a TDCs with a time binning down to 4ps and power consumption of **few tens mW/ch** with simple architecture

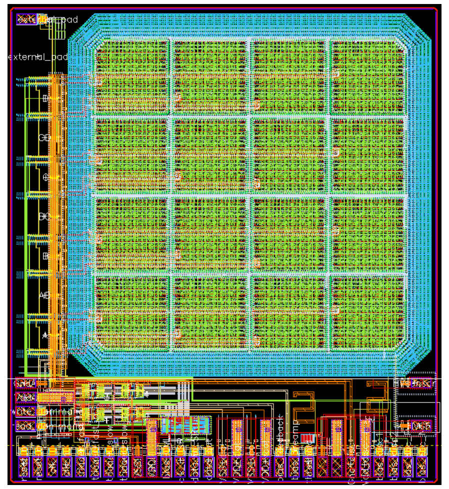
2016



2017



2019

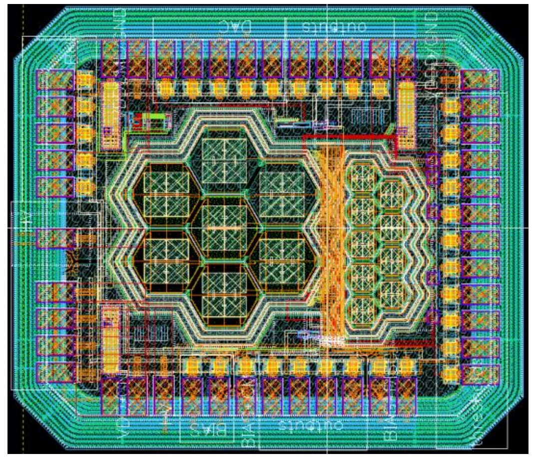


TT-PET

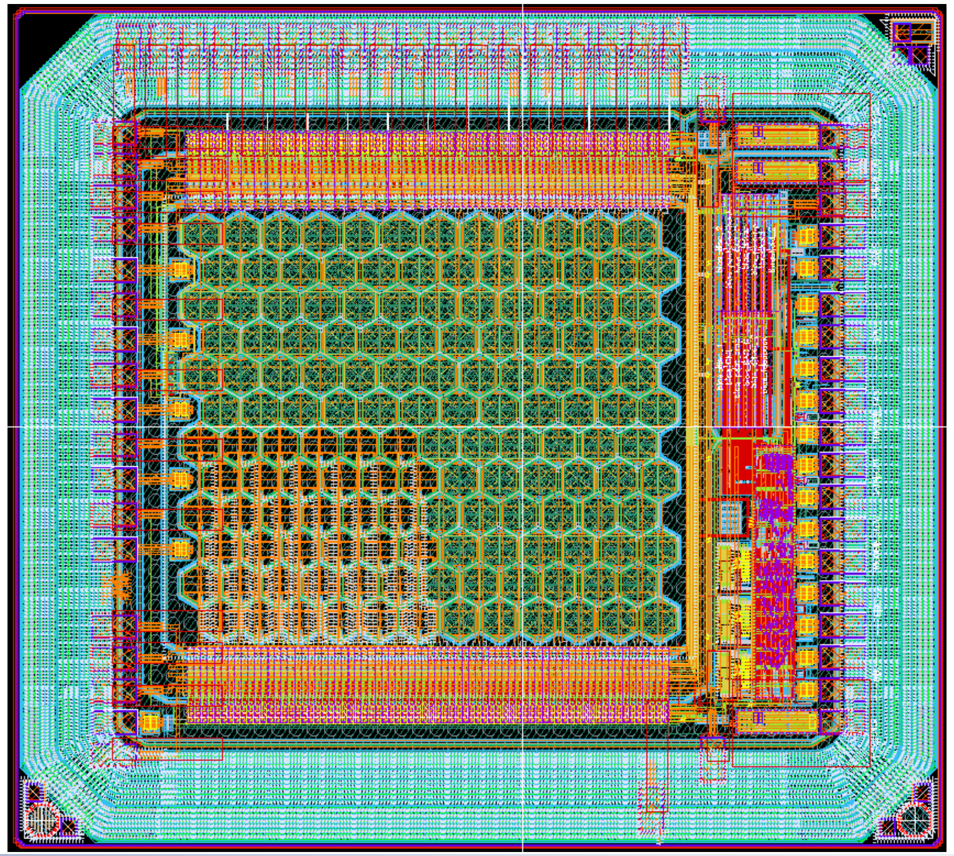
For the TT-PET Project

The prototype chips

2018



2019

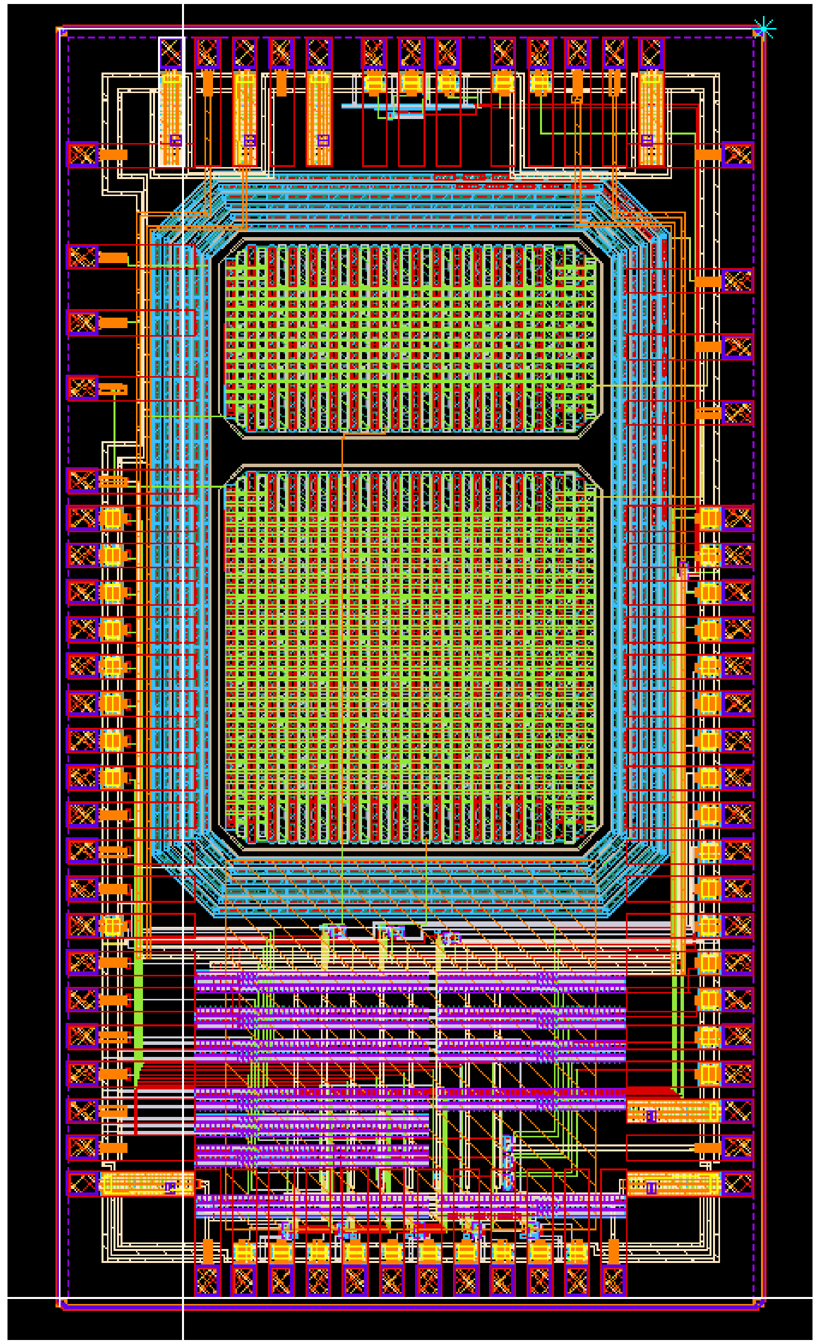


ATTRACT

unitec

For generic timing sensor R&D

Analogue ASIC prototype submission

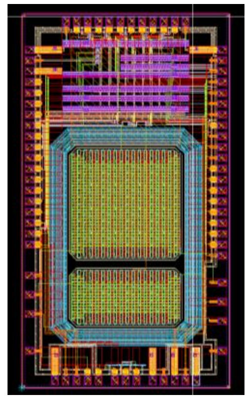


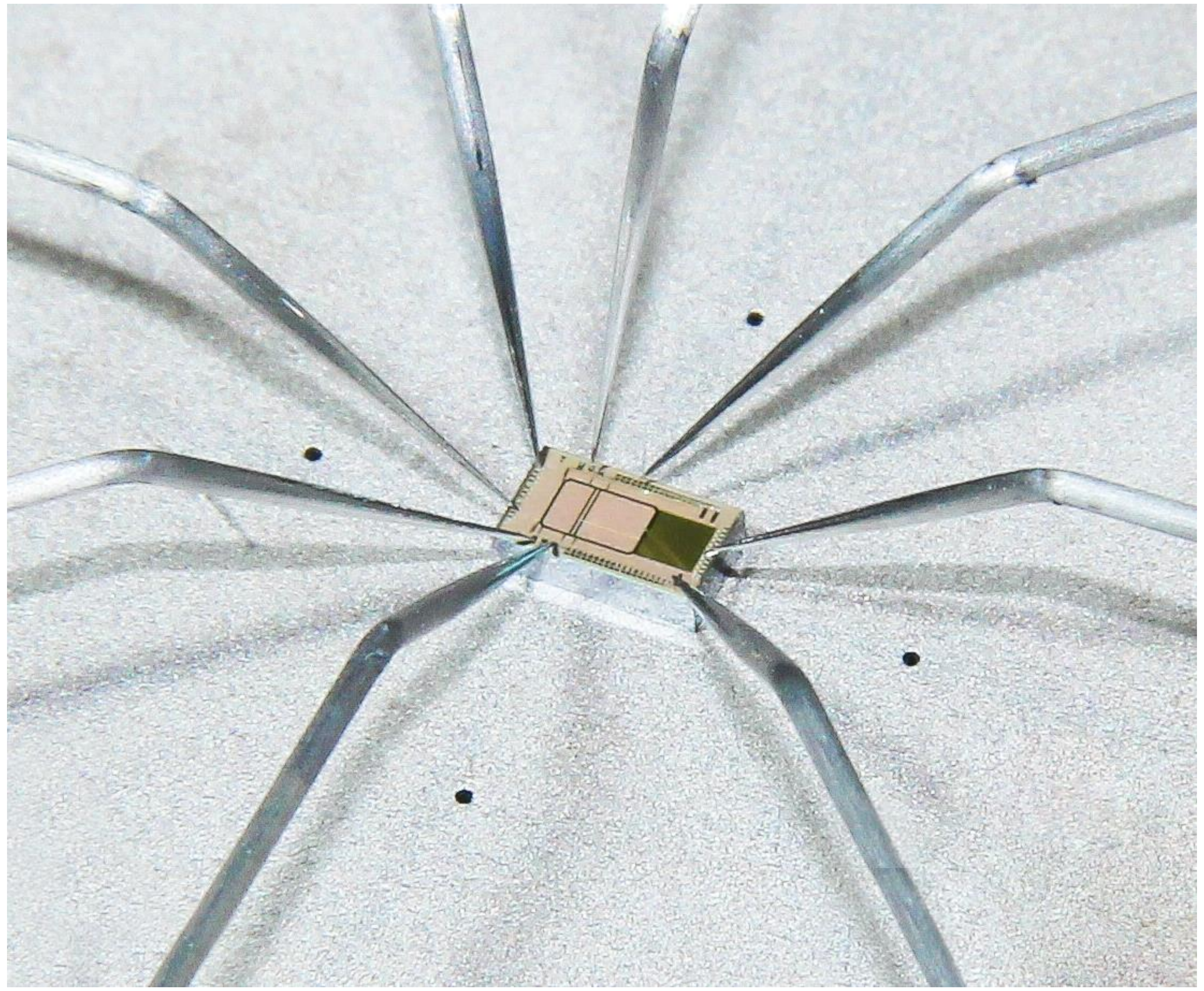
- Monolithic sensor with **two n-on-p pads:**

  900×900 µm^2 and 900×450 µm^2, spaced by 100 µm.

- Inside a **guard ring**.
- SiGe HBT **amplifier** and MOSFET **discriminator** with TOT capability, placed outside the guard ring

Operation of the ASIC

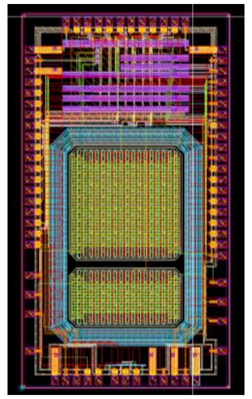




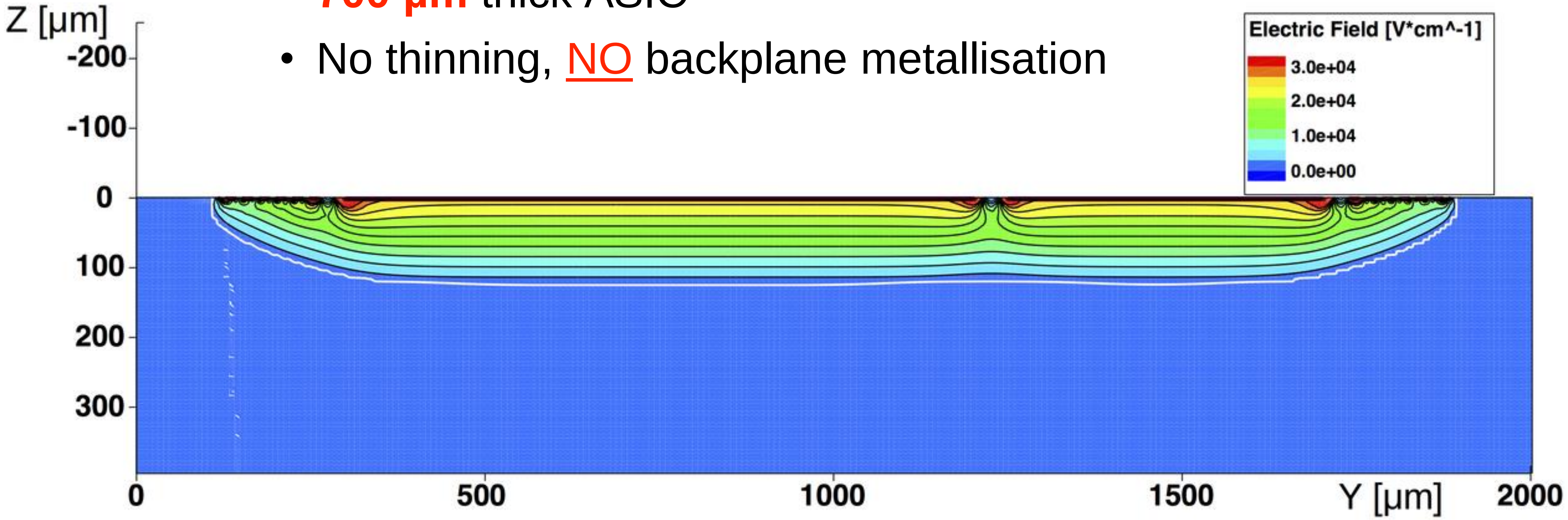
Prototype ASIC under test in the DPNC probe station

- Estimated pixel **capacitance**:
  0.8 pF for the small pixel
  1.2 pF for the large pixel
- **ENC** (CADENCE estimation):
  600 e^- RMS (small pixel)
  750 e^- RMS (large pixel)
- +ve bias voltage applied to pixels using poly-silicon biasing resistors
- **Breakdown** voltage: **165 V**
- **Power** consumption ≈ **350 µW/ch**

TCAD simulation of the ASIC



- Substrate resistivity of **1 kΩcm**.
- **700 µm** thick ASIC
- No thinning, NO backplane metallisation



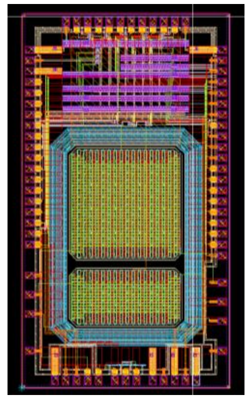
Depletion depth **≈ 130 µm**.

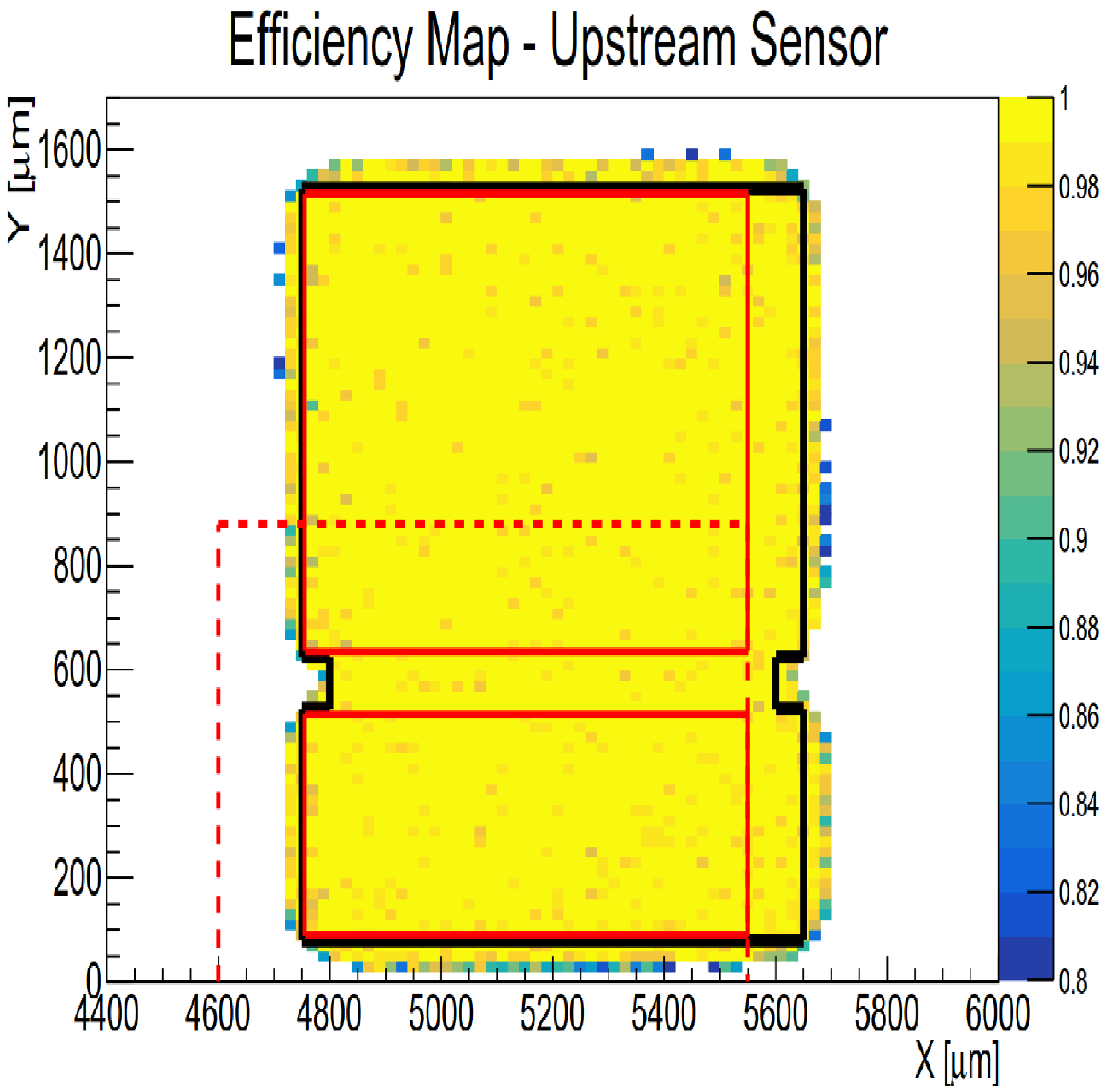
Due to the **absence of thinning and backplane metallisation**:

- **electric field non-uniform** in depth and well below 2-3 V/µm
- the **drift velocity** of the charge carriers was **NOT saturated**

⇒ **sensor NON optimal for time resolution**

Testbeam results: efficiency



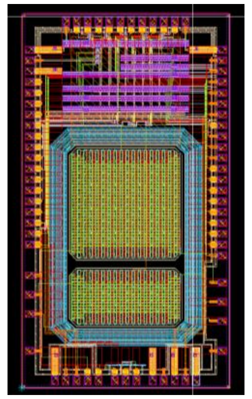


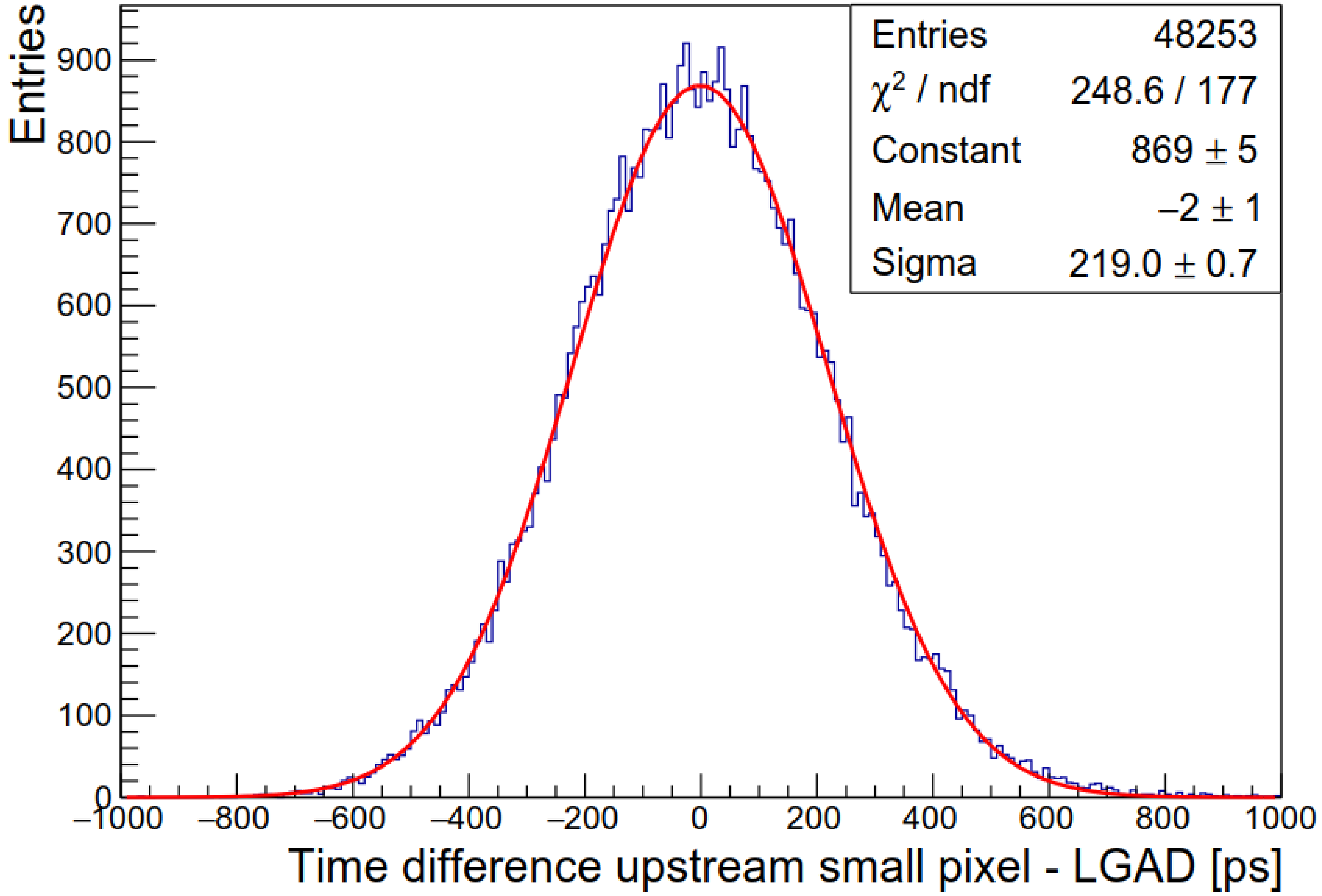
Published in JINST 13 (2018) P04015: https://doi.org/10.1088/1748-0221/13/04/P04015

Efficiency = 99.8 %

even in the **inter-pixel region**

Testbeam results: time resolution





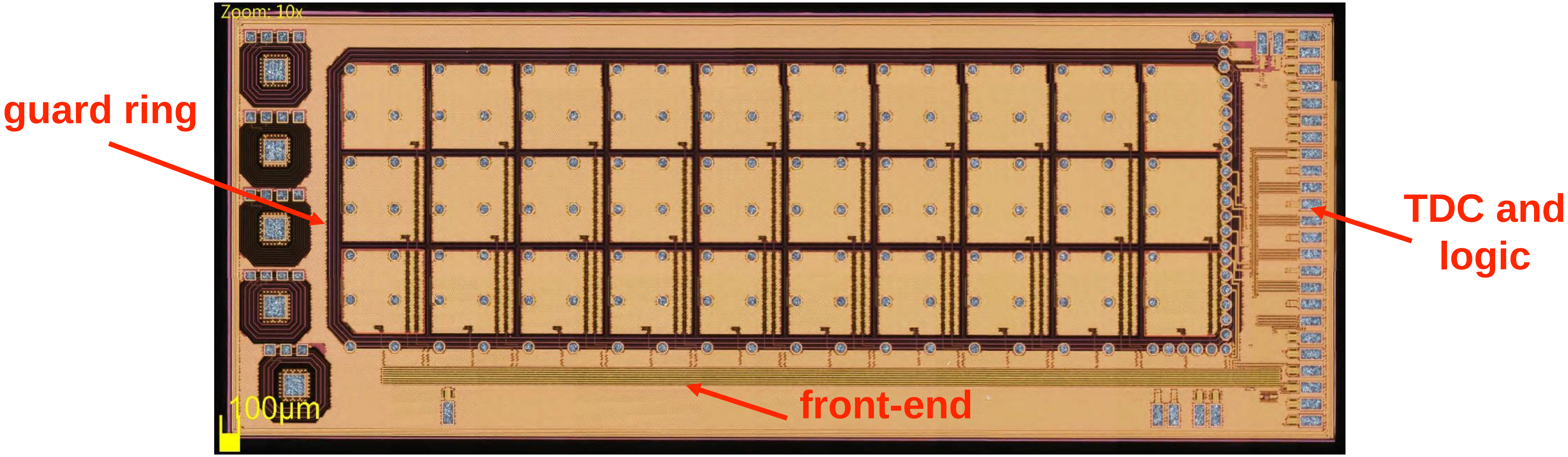
Very nice Gaussian distribution

Time resolution:
(220 ± 1) ps

Published in JINST 13 (2018) P04015: https://doi.org/10.1088/1748-0221/13/04/P04015

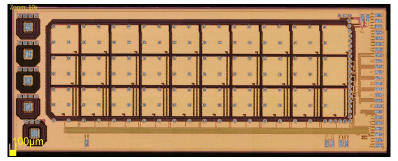
The TT-PET “demonstrator” chip

Matrix of **3×10** n-on-p pixels, of **470×470 μm²** (C_{tot} = 750 fF) spaced by **30 μm**.



- SiGe HBT **preamplifier**
- CMOS-based open-loop tri-stage **discriminator** (adjustable threshold with an 8-bit DAC), that preserves the **TOA** and the **TOT** of the pixel
- Discriminator output sent to **fast-OR chain**
- **50ps binning TDC**, R/O logic, serializer

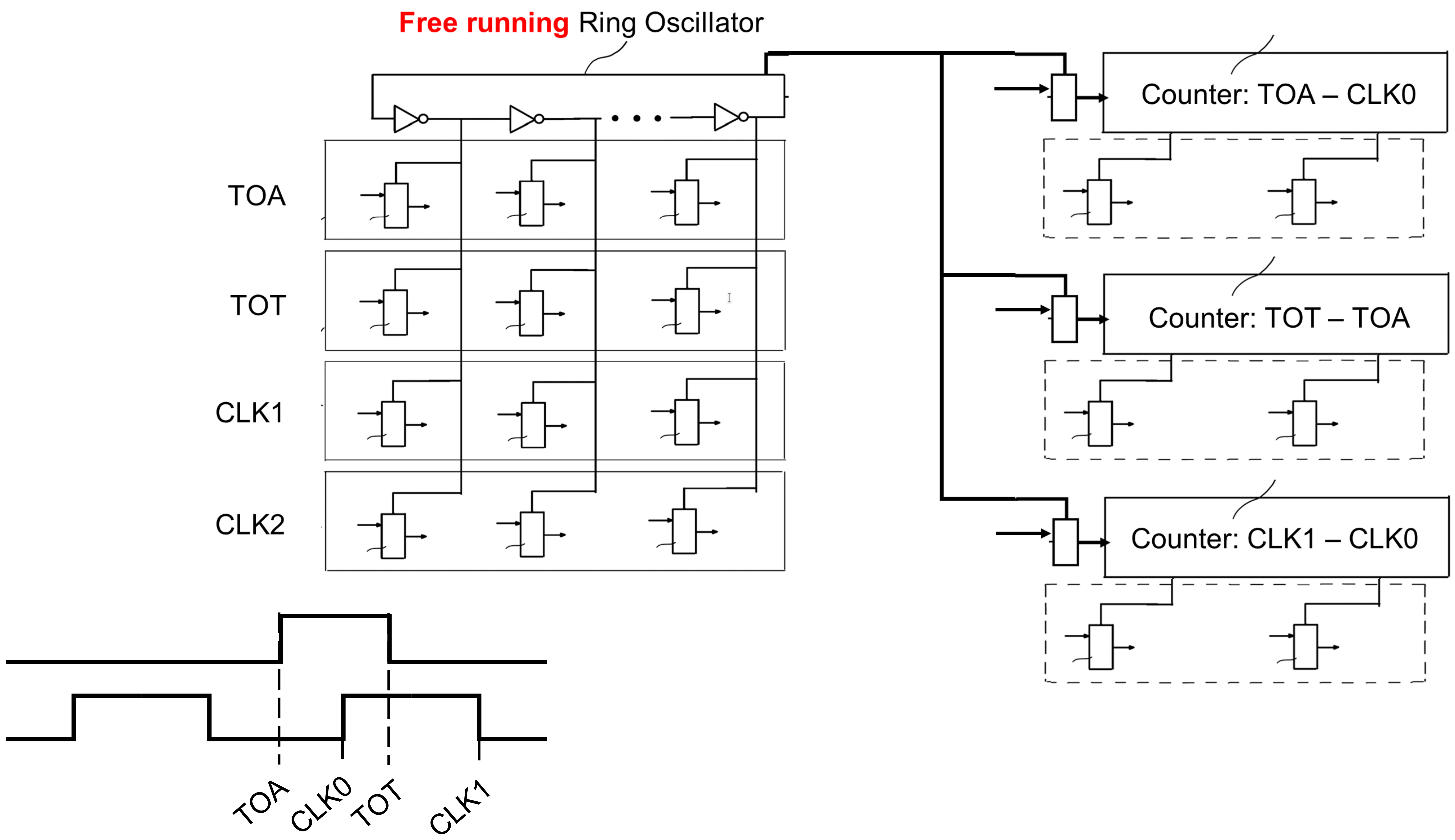
The frontend



Main specifications of the simulated front-end for C_{TOT} = 500 fF

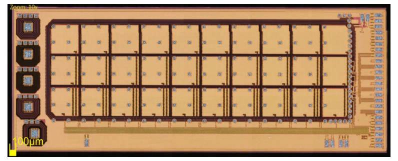
Power supply	1.8 V
Gain	90 mV/fC
ENC	300 e^- RMS
Minimum threshold	0.4 fC
Power consumption	135 μW/ch
Peaking time	1.3 ns
Simulated ToA jitter (for 1 fC signal)	82 ps

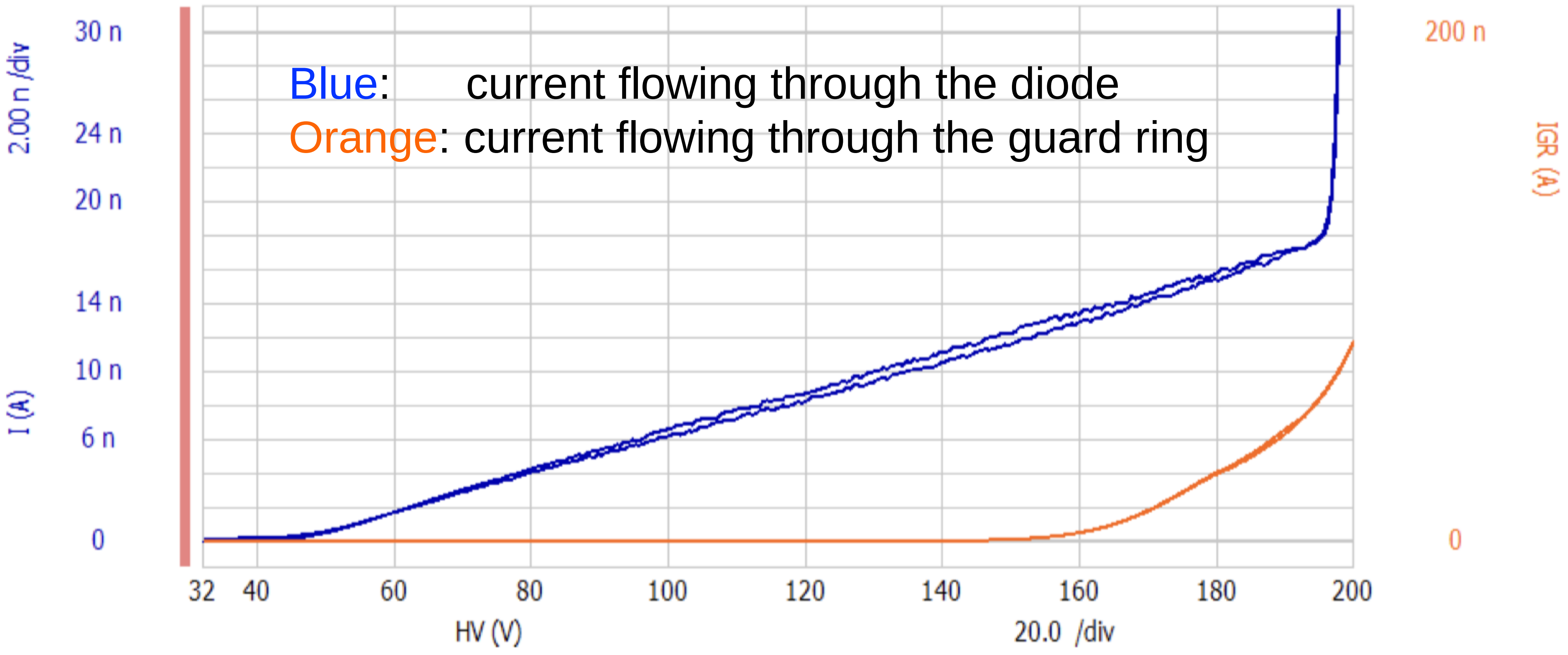
The TDC



Free running Ring Oscillator
TOA
TOT
CLK1
CLK2
Counter: TOA – CLK0
Counter: TOT – TOA
Counter: CLK1 – CLK0
TOA
CLK0
TOT
CLK1

Sensor I-V curve

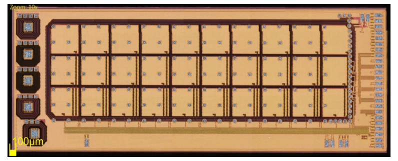


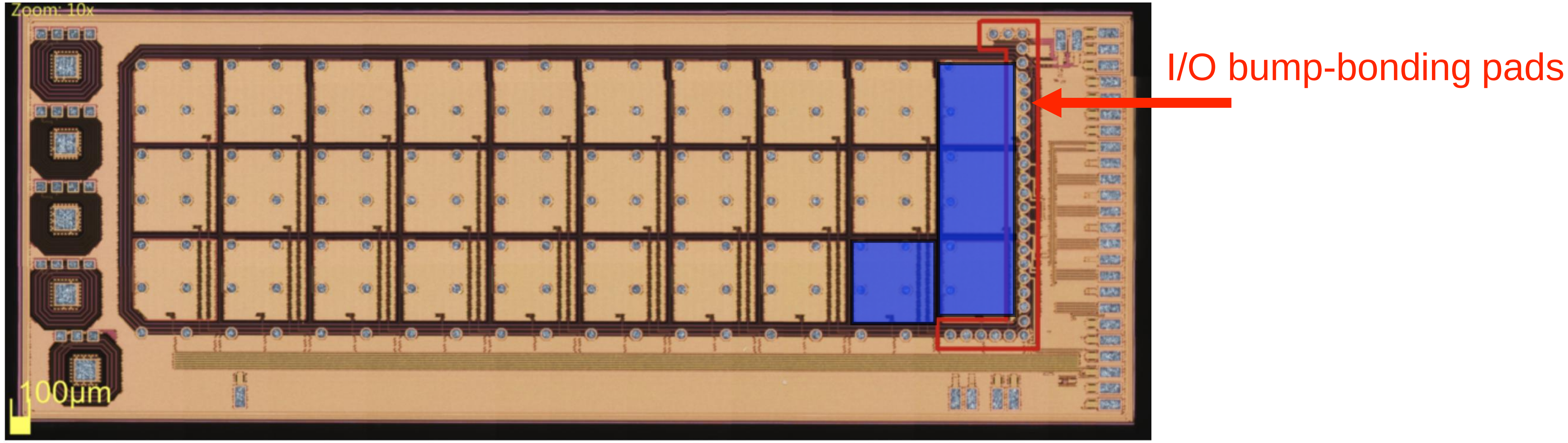


Breakdown at ≈ **200 V**

Resistive behaviour produced by non-ideal ground contact through the backplane

TT-PET "demonstrator" chip

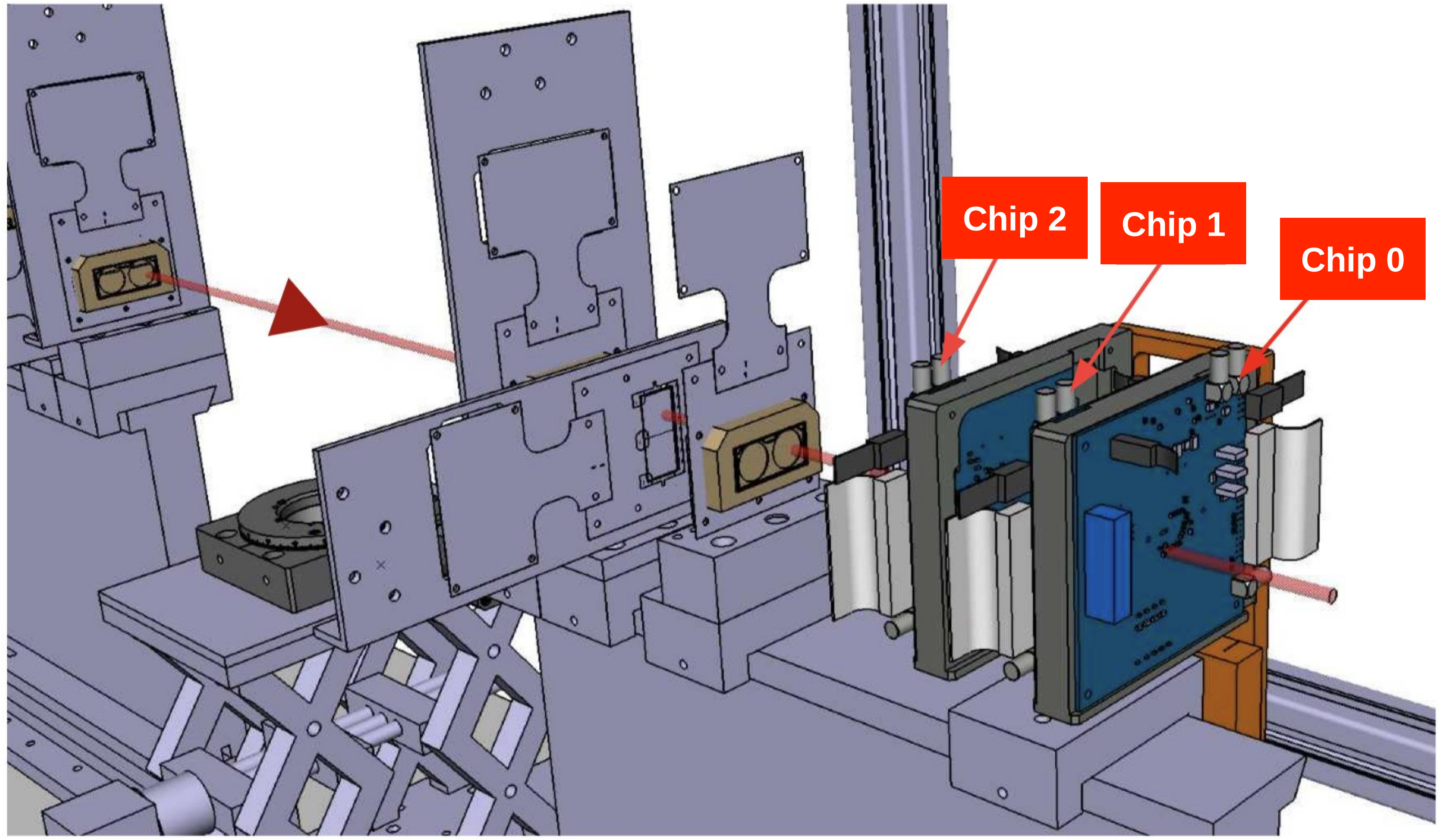




The four pixels (in blue) closer to the I/O pads were masked on hardware, due to **noise induced by the single-ended clock line** by the I/O bump-bonding pads (inside the red lines), which were not used but still connected.
(These pads will be removed and the clock distributed using differential lines.)

- Front-end **ENC = 350 e^- RMS** (on a capacitance of ≈ 750 fF).
- Therefore the nominal threshold was set to to **1750 e^-** (5σ above noise).
- Noise hit rate per chip of **4.3×10^{-3} Hz** measured at the nominal threshold.

Testbeam experiment with MIPs

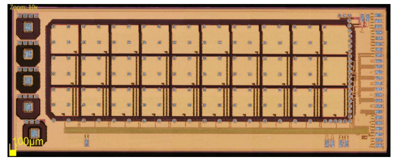


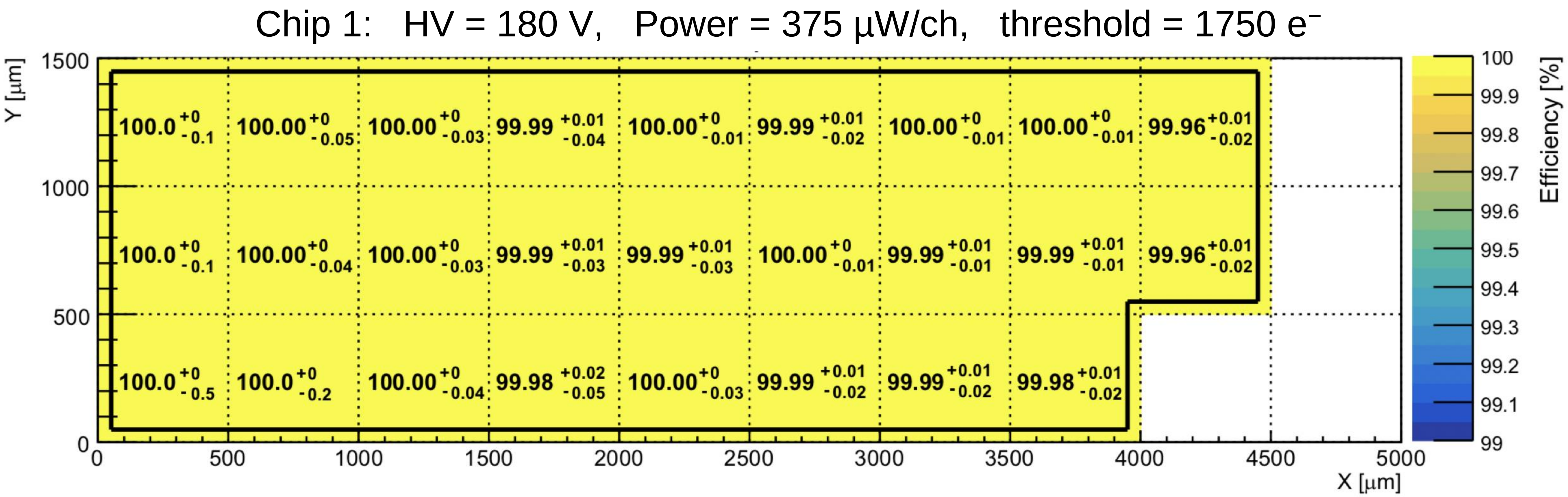
Three chips were installed downstream our beam telescope.

Chips operated at two preamplifier power-consumption working points:

- **160 μW/channel**, compliant with the TT-PET power requirements
- **375 μW/channel**, expected to perform better in terms of gain and noise (larger $I_c \Rightarrow$ larger transistor $f_T \Rightarrow$ better matching of the pixel capacitance)

Test beam results: efficiency

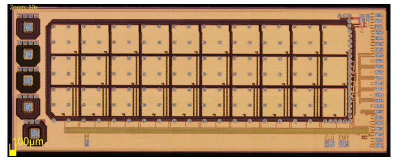




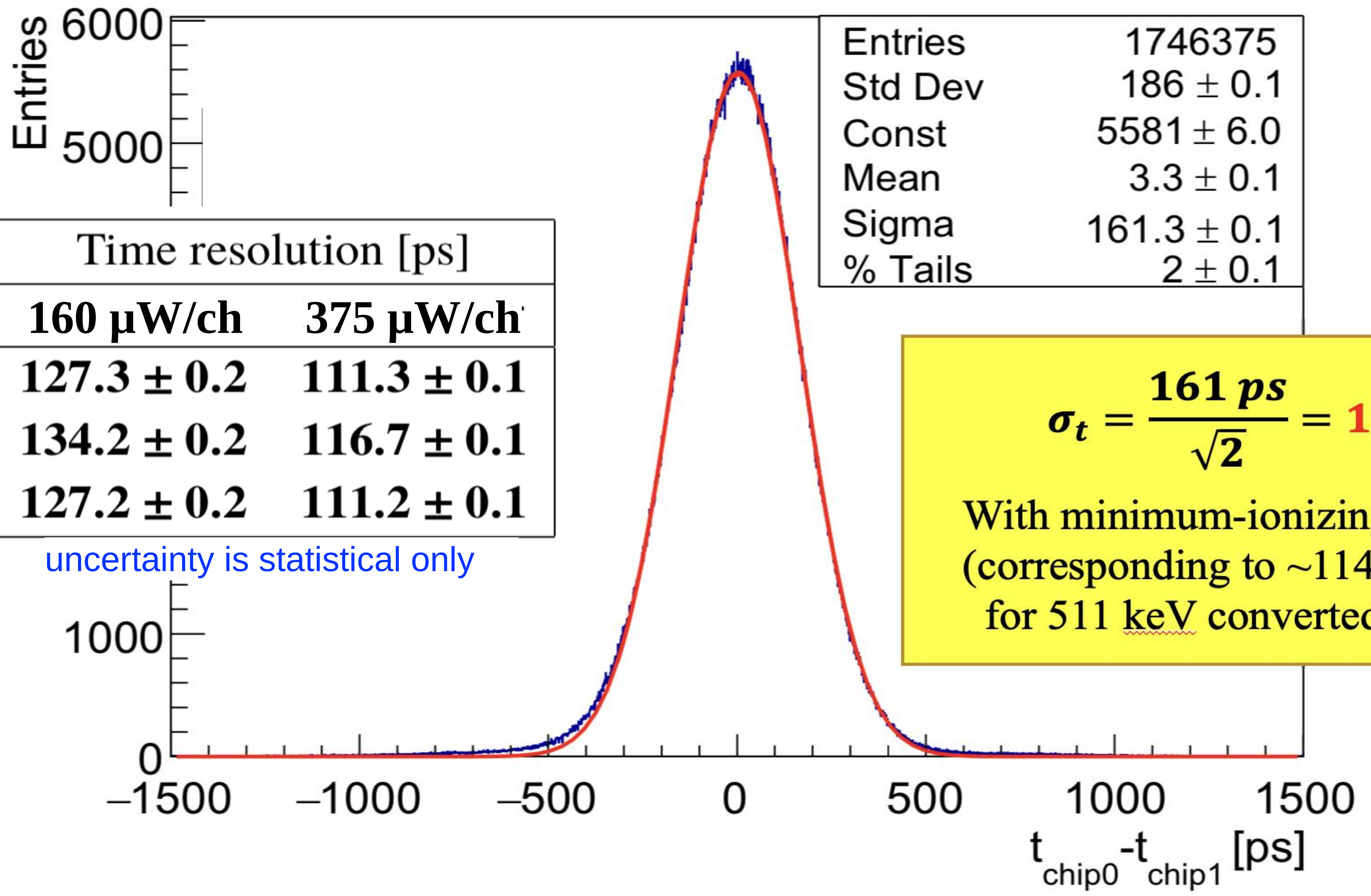
Full efficiency, even in the inter-pixel region.

L. Paolozzi *et al.*, 2019 JINST **14** P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
P. Valerio *et al.*, 2019 JINST **14** P07013, https://doi.org/10.1088/1748-0221/14/07/P07013

Test beam results: time resolution



Chip 1: HV = 180 V, Power = 375 µW/ch, threshold = 1750 e⁻



	Time resolution [ps]	
	160 µW/ch	375 µW/ch
$\sigma_{t,\ \text{chip 0}}$	127.3 ± 0.2	111.3 ± 0.1
$\sigma_{t,\ \text{chip 1}}$	134.2 ± 0.2	116.7 ± 0.1
$\sigma_{t,\ \text{chip 2}}$	127.2 ± 0.2	111.2 ± 0.1

uncertainty is statistical only

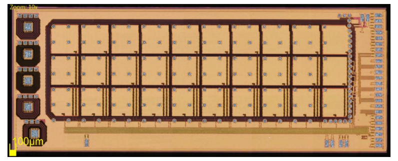
$$\sigma_t = \frac{161\ ps}{\sqrt{2}} = 114\ ps$$

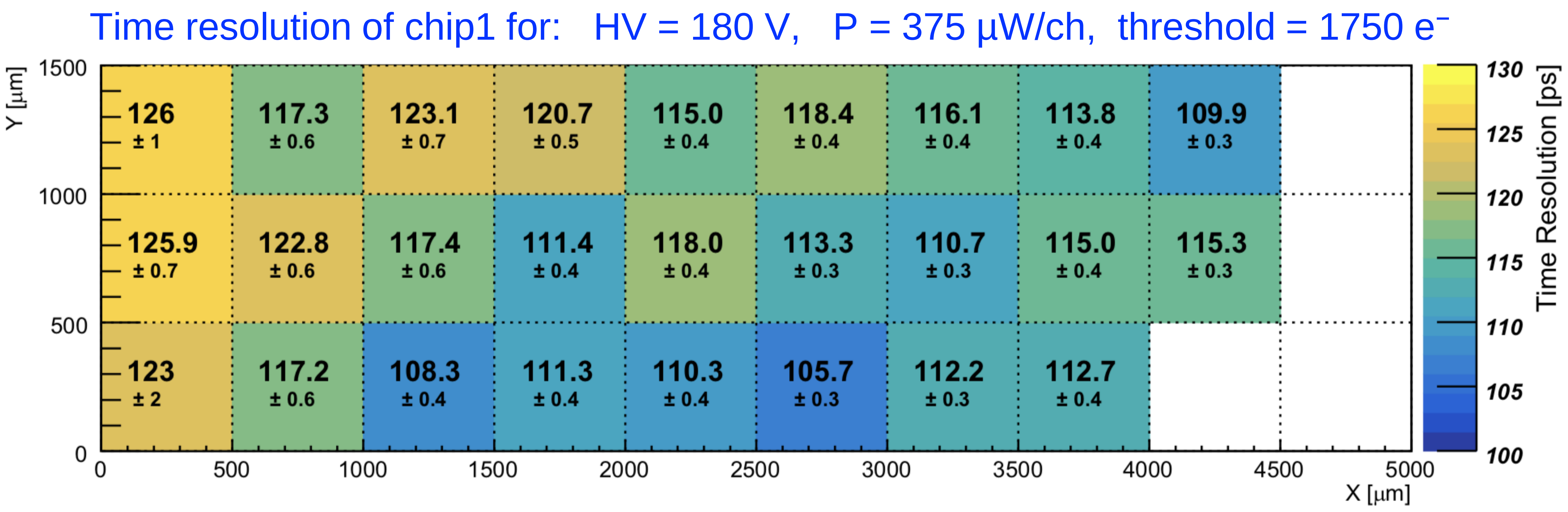
With minimum-ionizing particles (corresponding to ~114/4 ~ 30ps for 511 keV converted photons)

Excellent result for a silicon pixel detector without internal gain, **obtained on a large capacitance (750 fF) and power consumption of 150 mW/cm^2.**

L. Paolozzi *et al.*, 2019 JINST **14** P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
P. Valerio *et al.*, 2019 JINST **14** P07013, https://doi.org/10.1088/1748-0221/14/07/P07013

CAVEAT 1: Uniformity of response



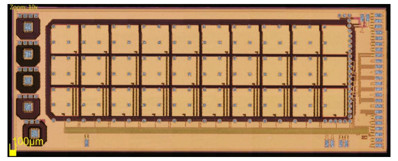


The map of pixels shows a steady small **worsening** towards the left.
Hypothesis: larger impedance of the ground line for the front-end channels far from the chip ground connection that is done in the right side of the chip

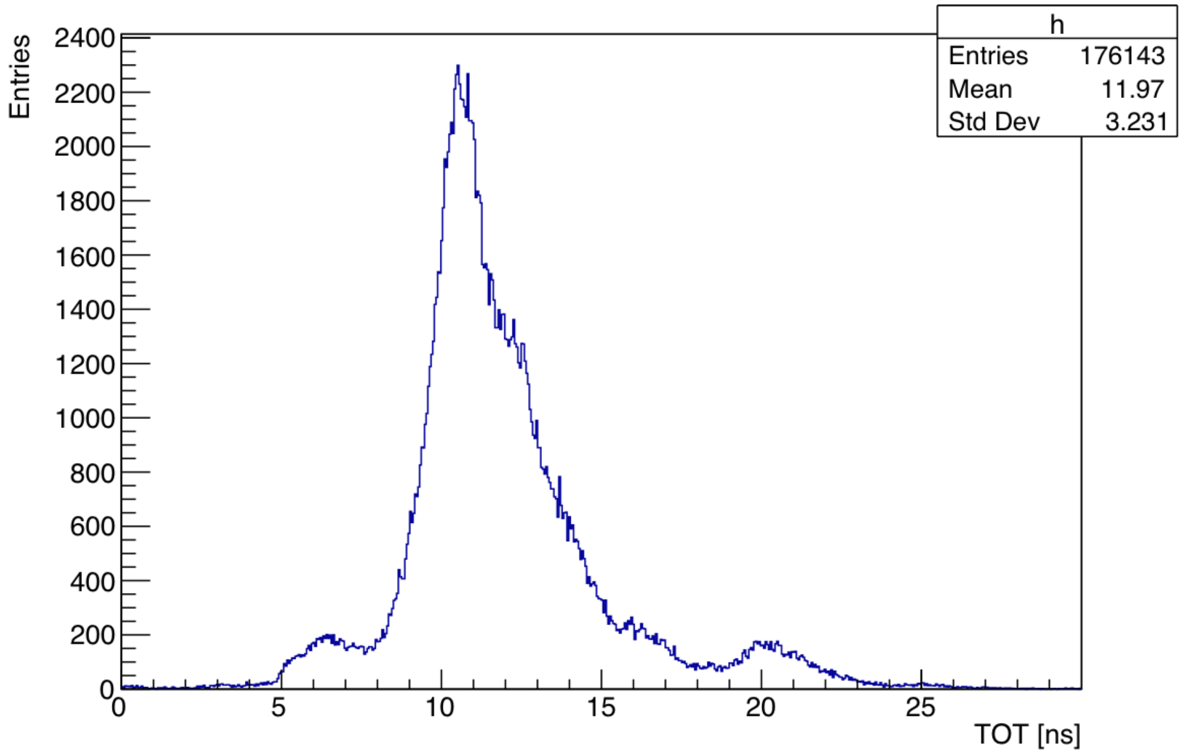
(“IR drop” of the supply voltage).

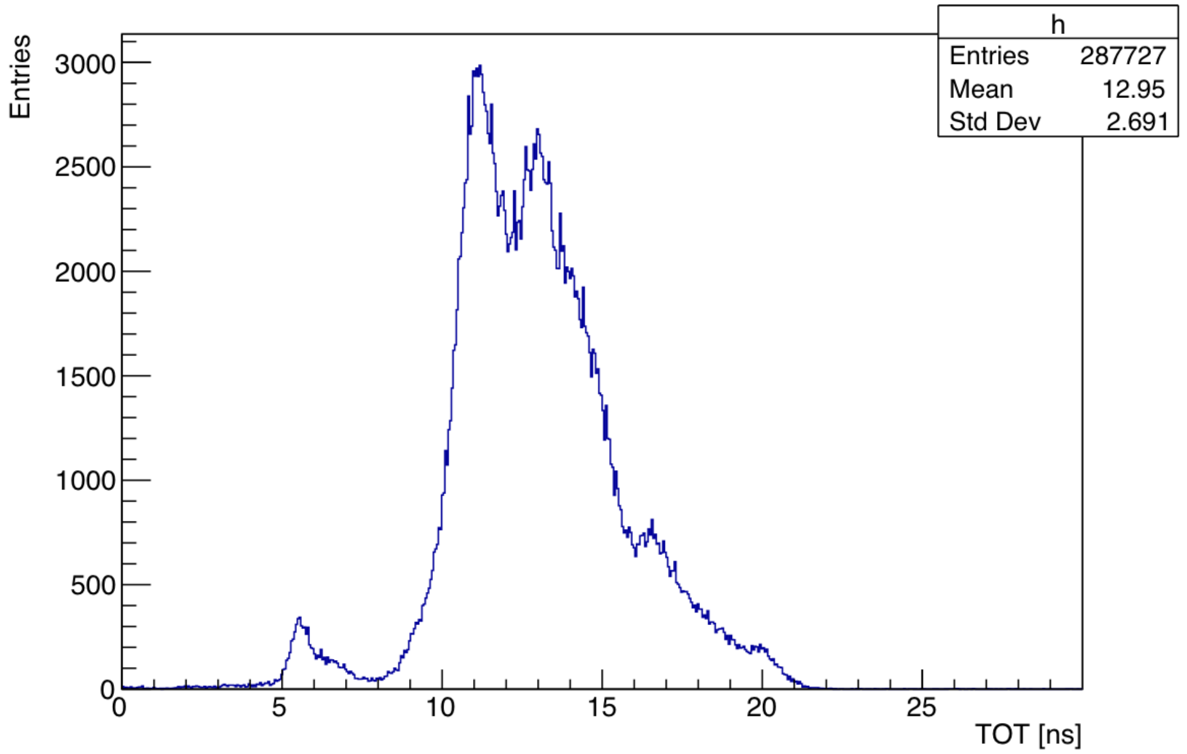
Mitigation measures implemented: improvement of the power-distribution network (larger distribution lines & power pads at the corners of the chip)

CAVEAT 2:   TOT distribution



It was found that **the single-ended digital trigger signal** affected the grounding of the pixel matrix and induced a small residual noise.
Consequence: the TOT distributions show **peaks**, with time difference between peaks caused by the delay of the fast-OR line.





This modulation of the TOT distribution **degrades** the time-walk correction, and therefore **the time resolution**

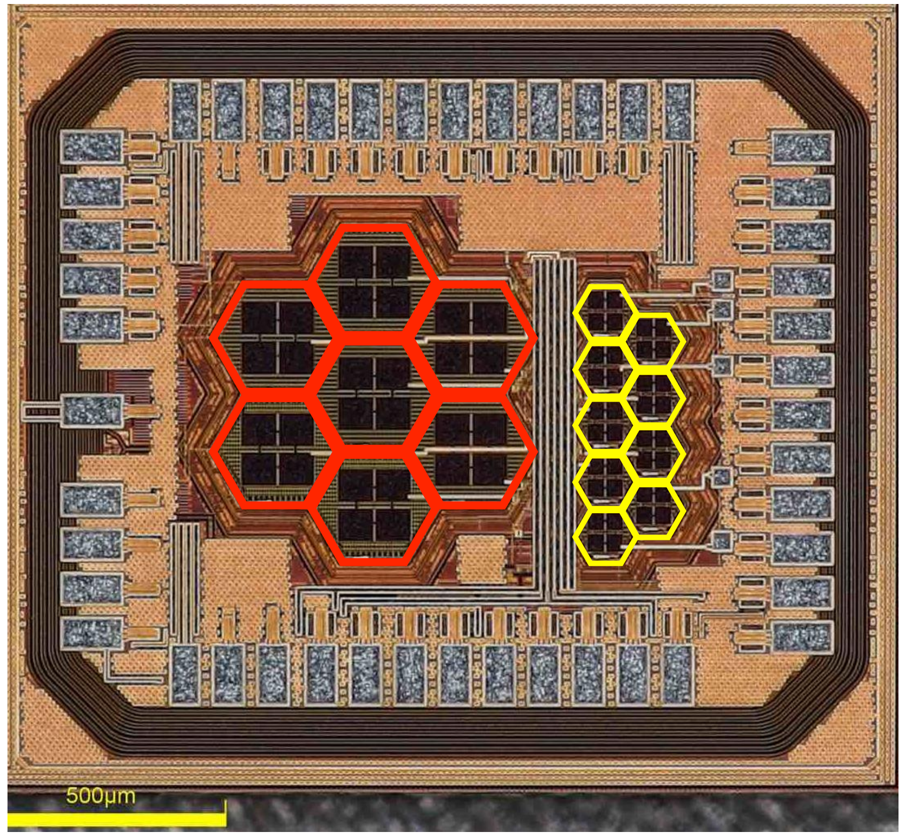
Mitigation measure: introduction of **trigger signals in a differential configuration**

The “hexagonal” prototype sensor

Developed in IHP **SG13G2** technology (130nm).

Matrices with hexagons of two sizes:

- ➞ hexagon side 130µm and 65µm, with 10µm inter-pixel spacing
- ➞ C_{TOT} = 220 and 70 fF

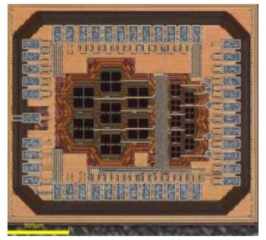


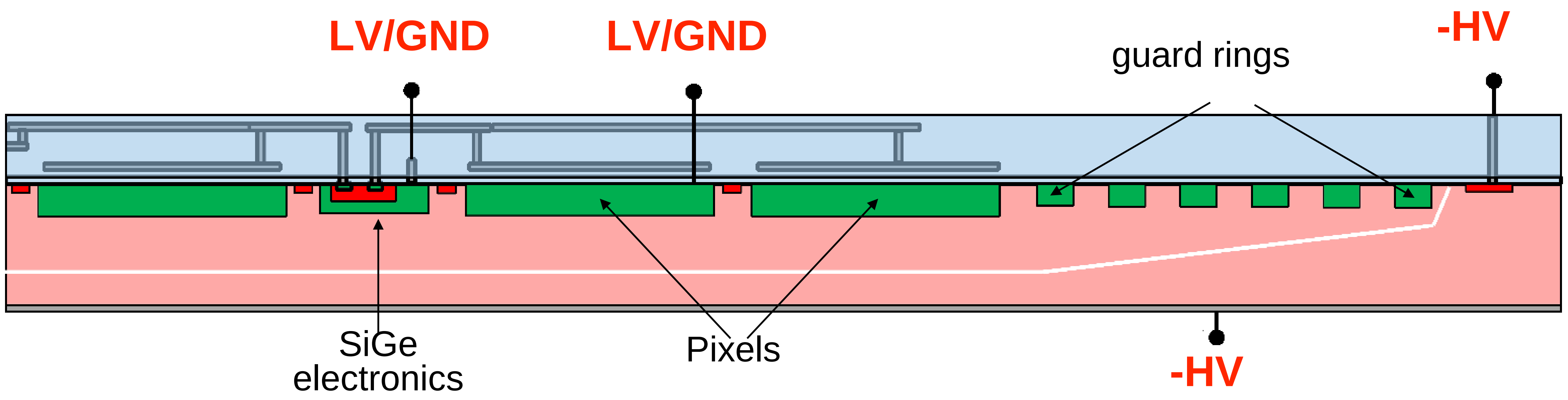
Exploits:

- ➞ New dedicated custom components developed together with foundry
- ➞ New guard-ring structure

Collaboration of: Université de Genève, Faculté des Sciences, Département de physique nucléaire et corpusculaire; IHP innovations for high performance microelectronics, Leibniz-Institut für innovative Mikroelektronik; INFN Sezione di Roma Tor Vergata; CERN Ideas

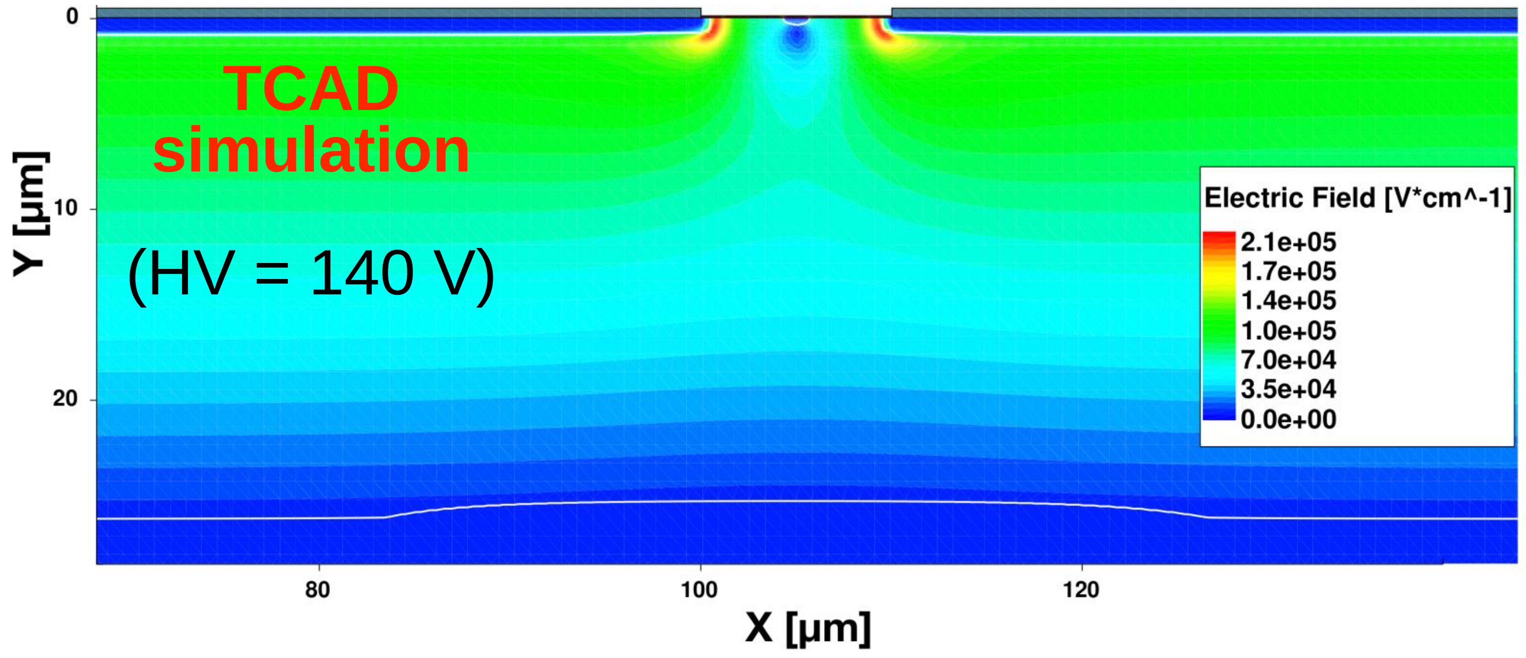
The “hexagonal” prototype sensor





Standard substrate resistivity ρ = 50 Ωcm
No backside metallisation ⟹ **not fully depleted**
PRO: much easier **production**, but

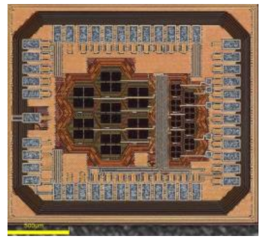
- ➞ slightly degraded performance because of regions where drift velocity is not saturated

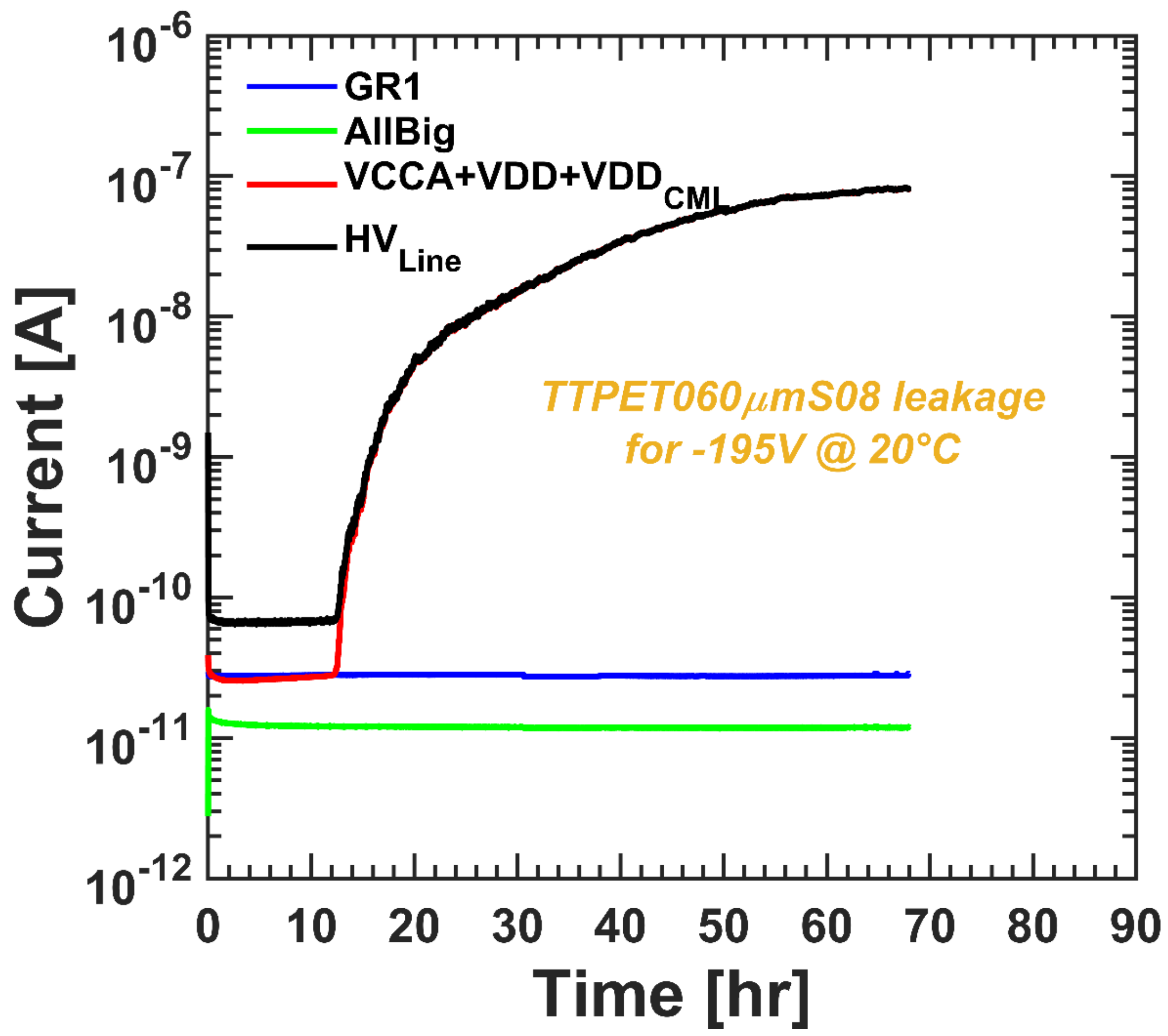


Depletion depth is **26µm** at HV = 140 V

- ➞ Most probable deposited charge for a MIP **≈ 1600 electrons**
- ➞ CADENCE Spectre simulation for 1600e⁻ (0.25 fC): ideally, **ToA jitter = 22 ps**

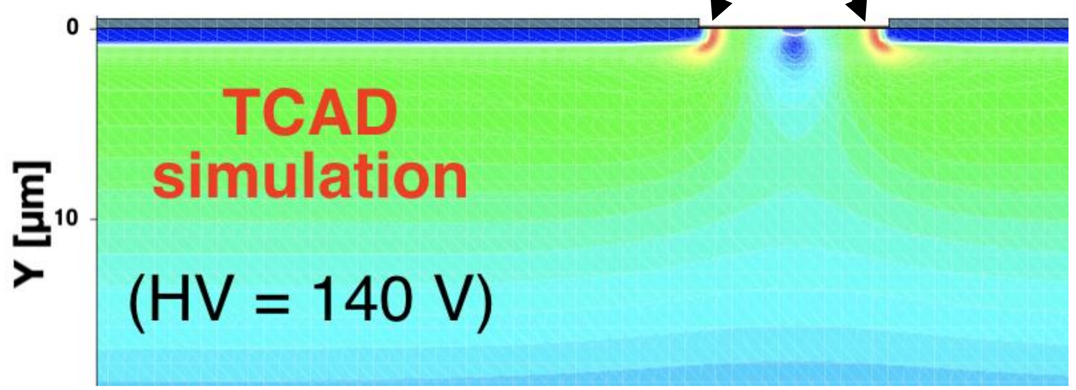
CAVEAT:





- ➞ Current drift up to ~100nA after two days of continuous operation.
- ➞ reversible.
- ➞ under investigation

maybe this high field is responsible for it

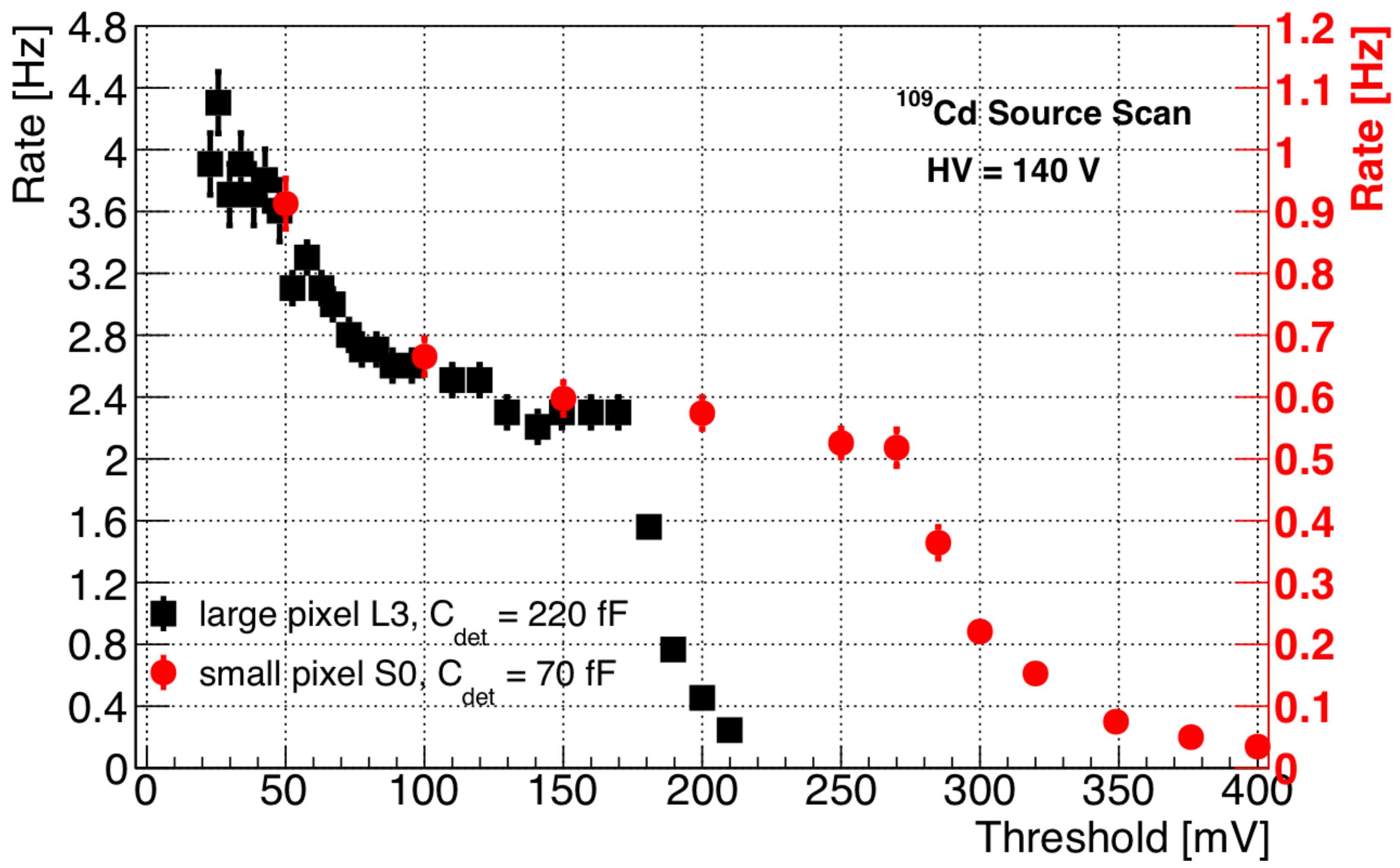


This behavior does not compromise the chip performance.

Therefore, we made measurements with a source and at a testbeam

^{109}Cd radioactive source calibrations

JINST 14 (2019) P11008, https://doi.org/10.1088/1748-0221/14/11/P11008

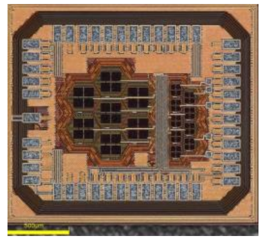


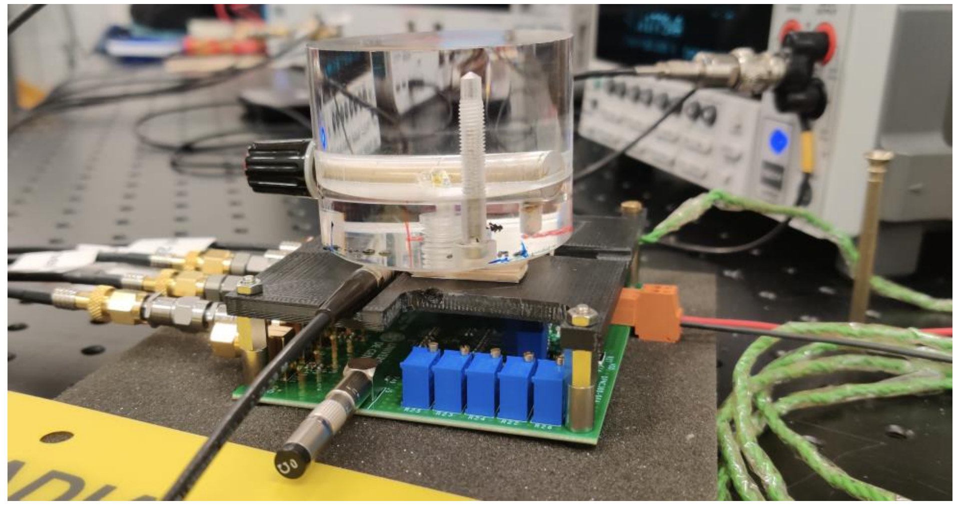
Rate ≈constant for low thresh. values ⟹ good discrimination of γ peak.

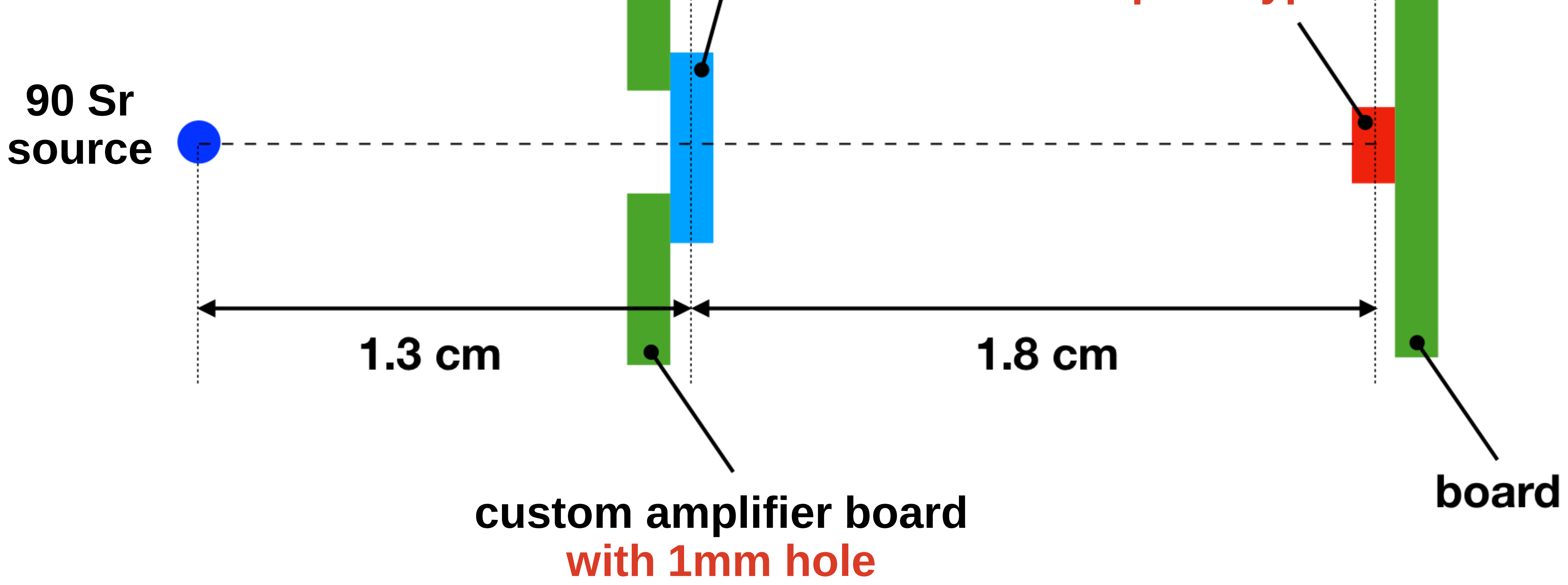
^{109}Cd photons (~22 keV) energetic enough for measurement of the gain:

- A_Q = 290 mV fC^{-1} for the small pixel ⟹ ENC = σ_V/A_Q = 90 electrons
- A_Q = 185 mV fC^{-1} for the large pixel ⟹ ENC = σ_V/A_Q = 160 electrons

^{90}Sr source experimental setup



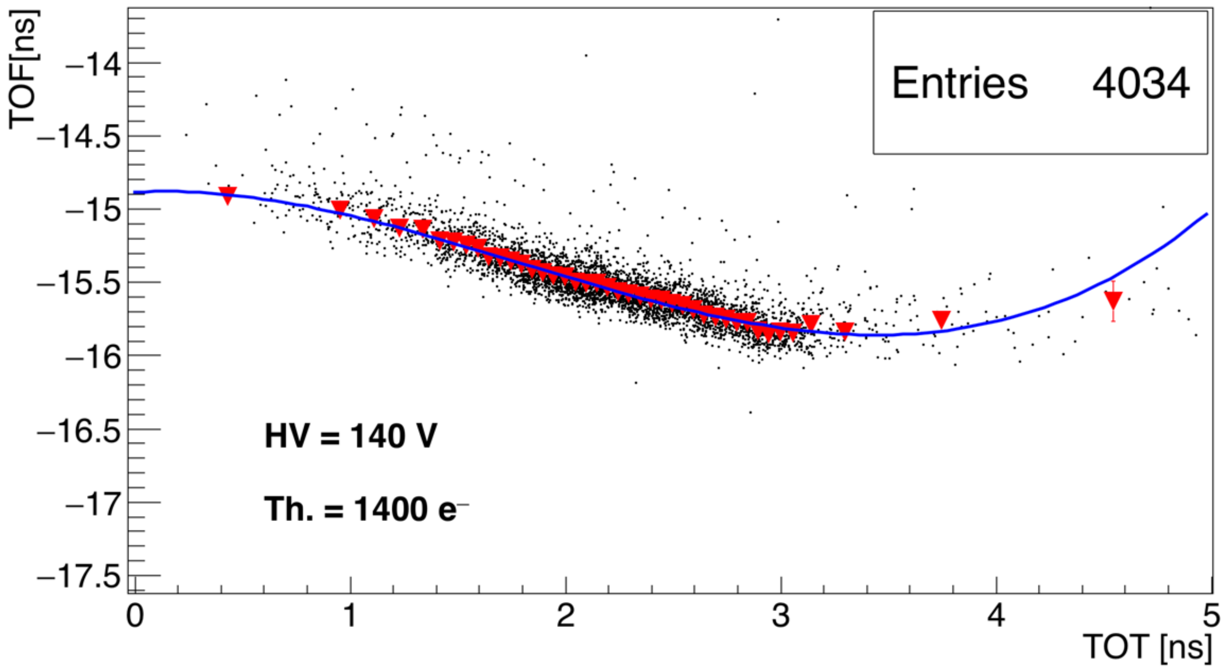




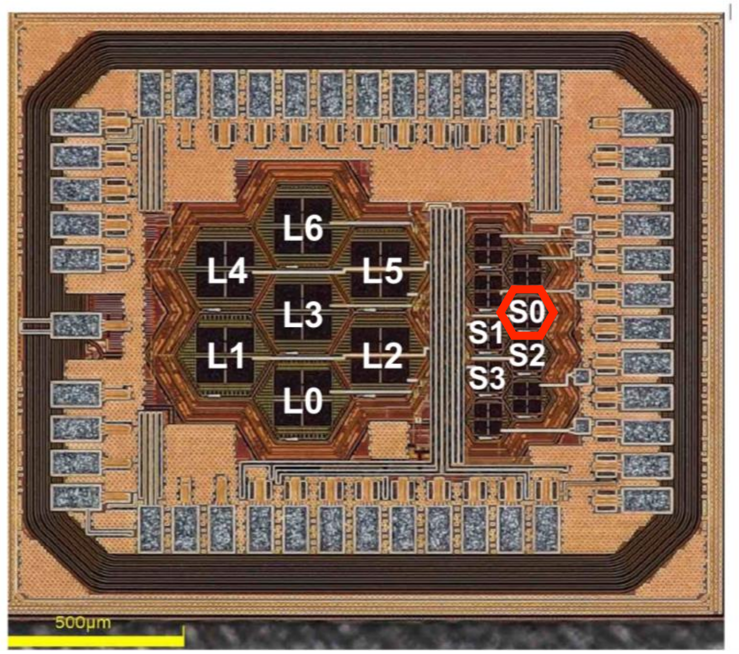
No analysis selection applied to the events in our monolithic SiGe prototype

Time-walk correction and TOF

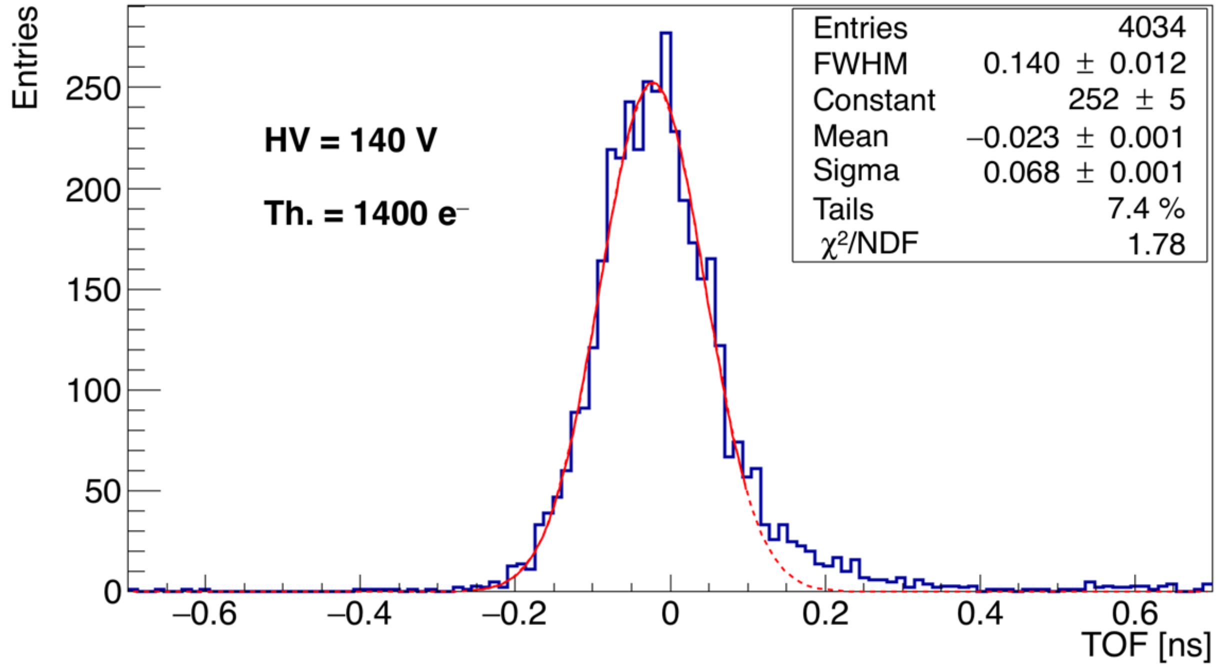
Time-walk correction



Small pixel S0, C = 70 fF



Time of Flight (time-walk corrected)



non-Gaussian tail (≈10%) for TOF ≥ 100ps, maybe due to e⁻ from the ^{90}Sr source

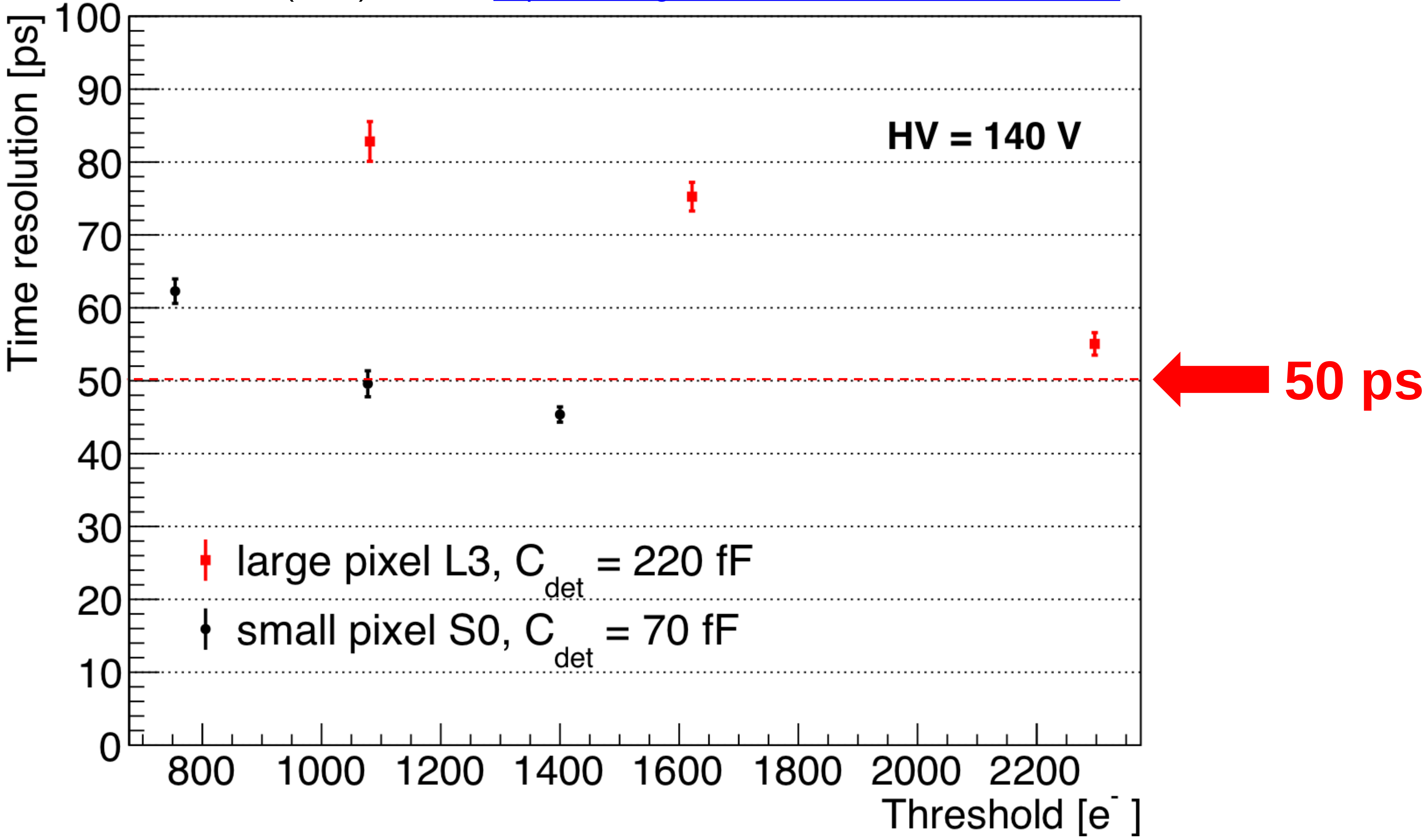
crossing the 10µm region between two pixels. Requires to be investigated in a testbeam.

Time resolution of Gaussian part:

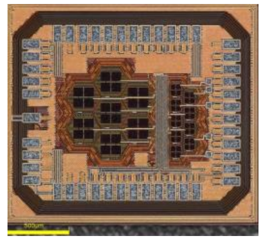
$$\sqrt{68^2 - 50^2} \simeq (46 \pm 2)\mathrm{ps}$$

Time resolution vs. threshold

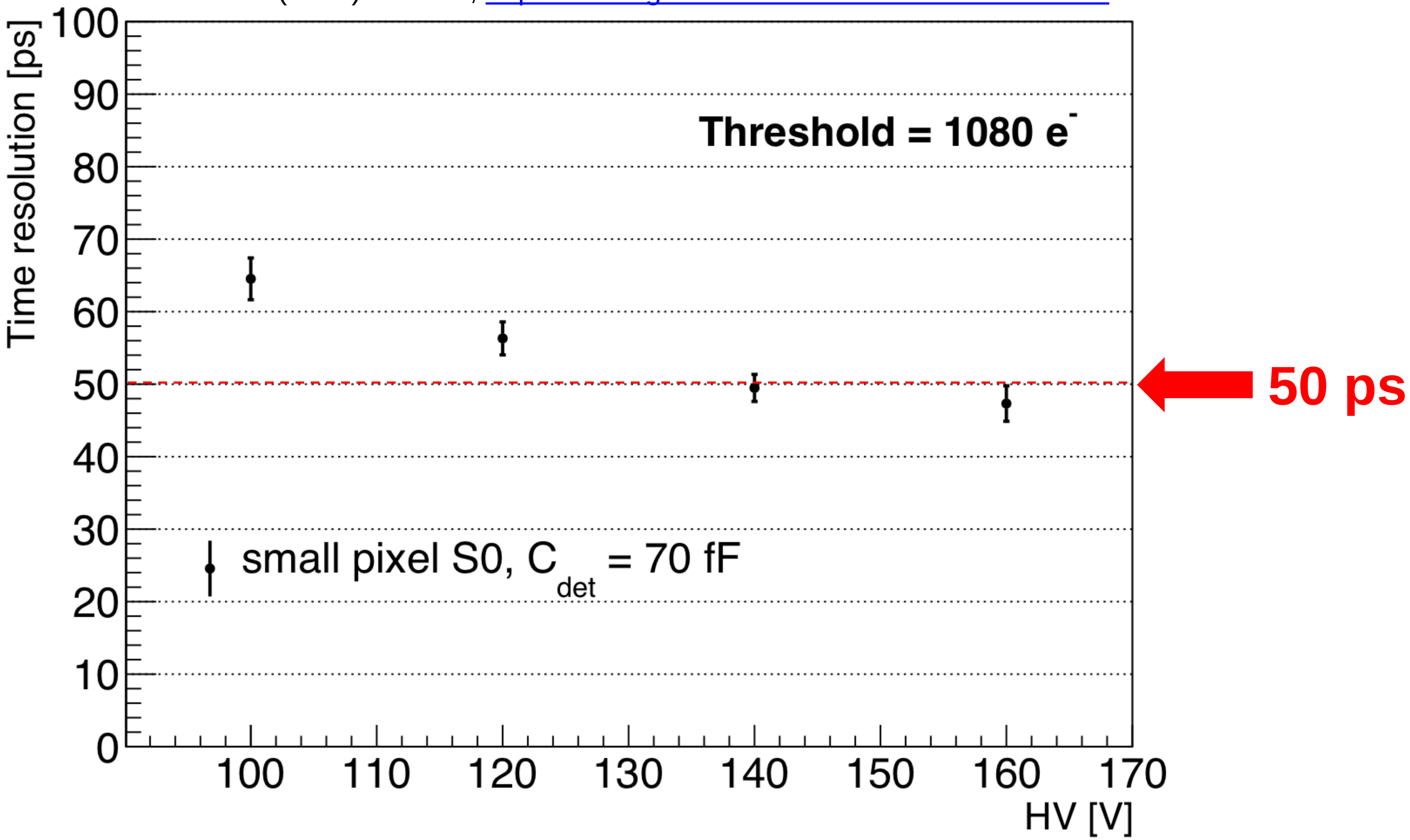
JINST 14 (2019) P11008, https://doi.org/10.1088/1748-0221/14/11/P11008



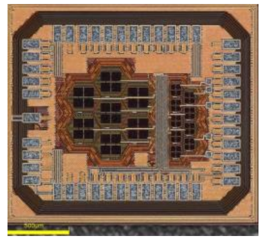
Time resolution vs. HV

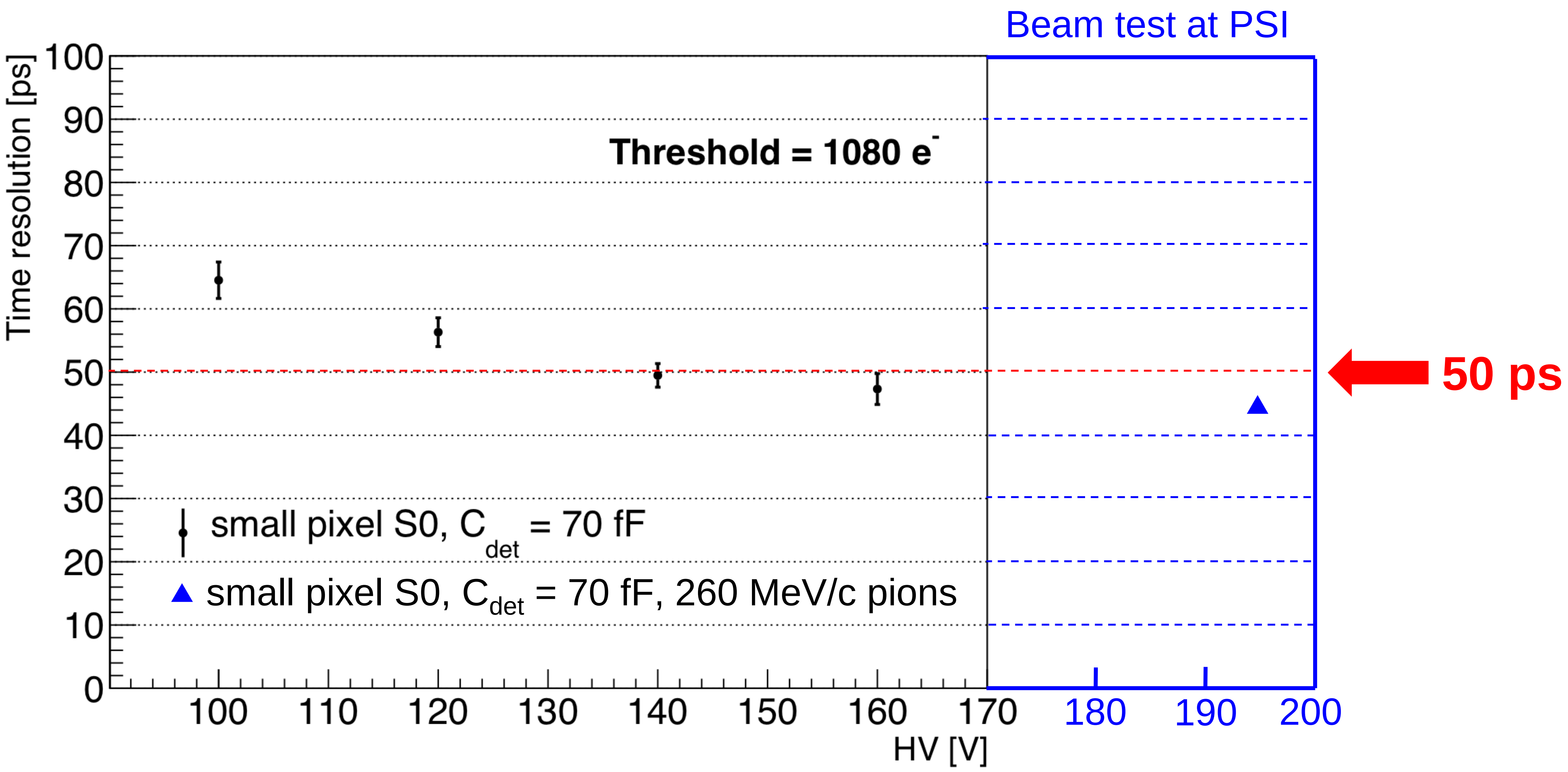


JINST 14 (2019) P11008, https://doi.org/10.1088/1748-0221/14/11/P11008

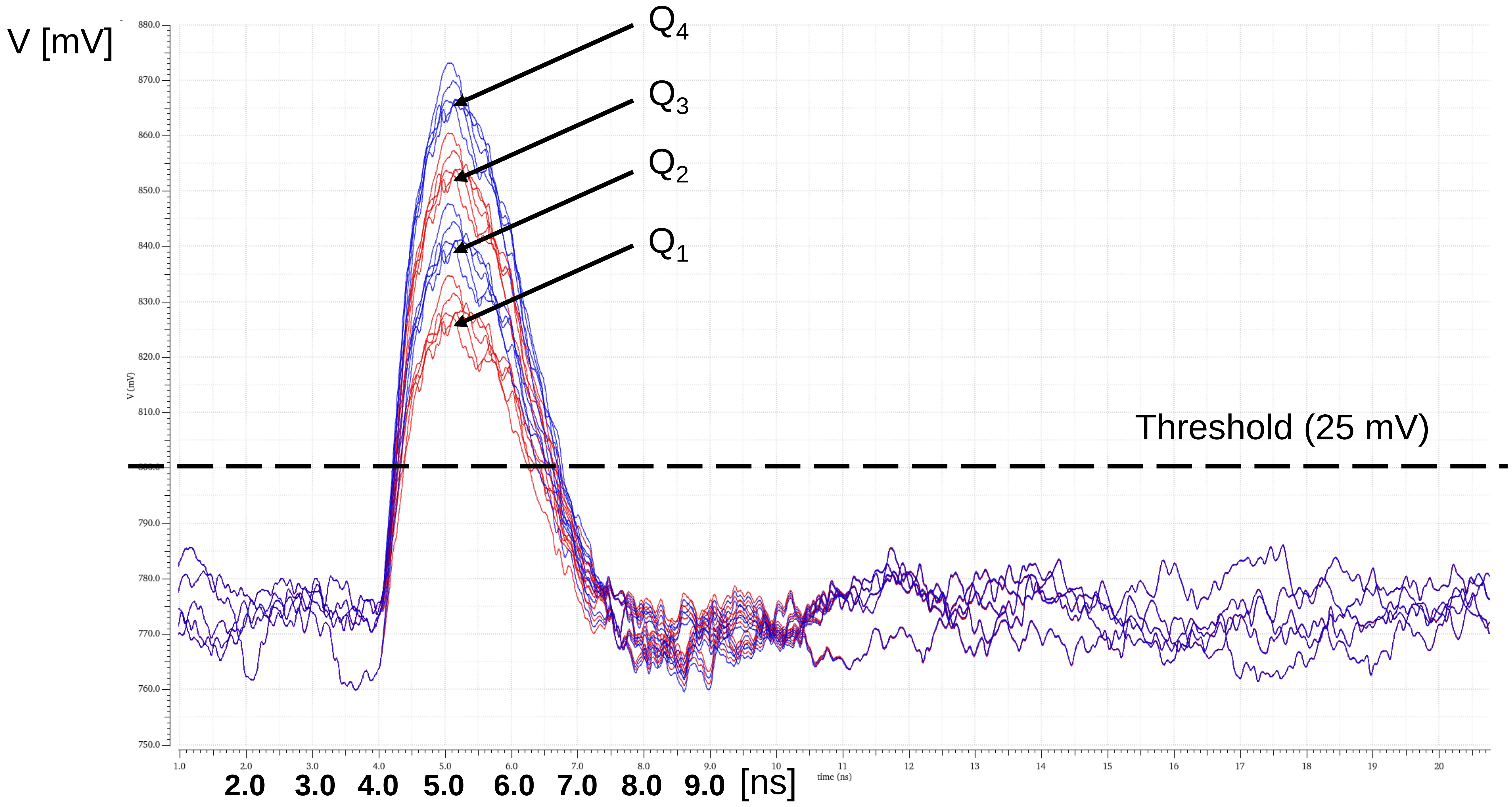


Time resolution vs. HV





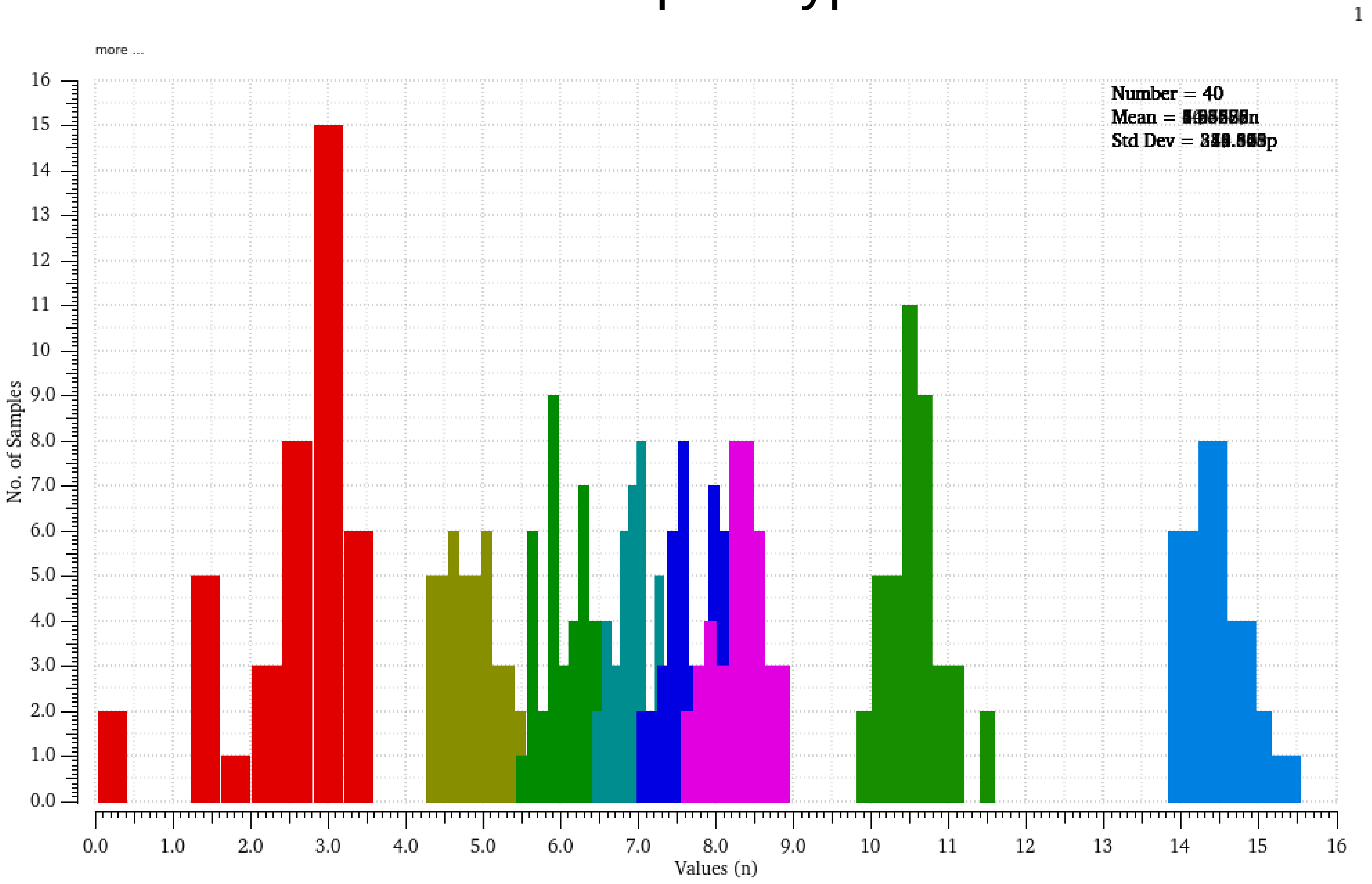
Time walk correction



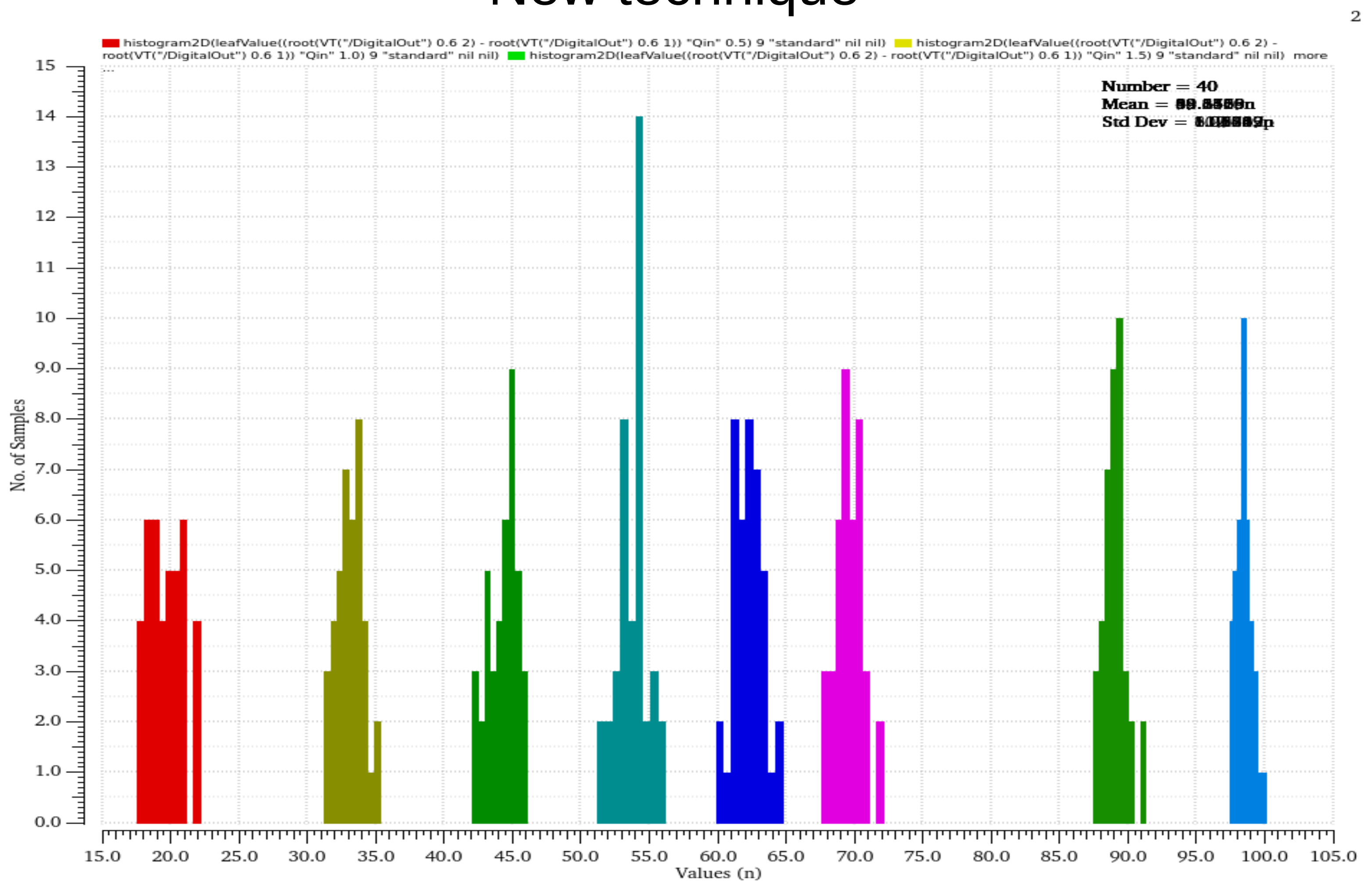
Improved time walk correction

Charge resolution (Cadence spectre simulation)

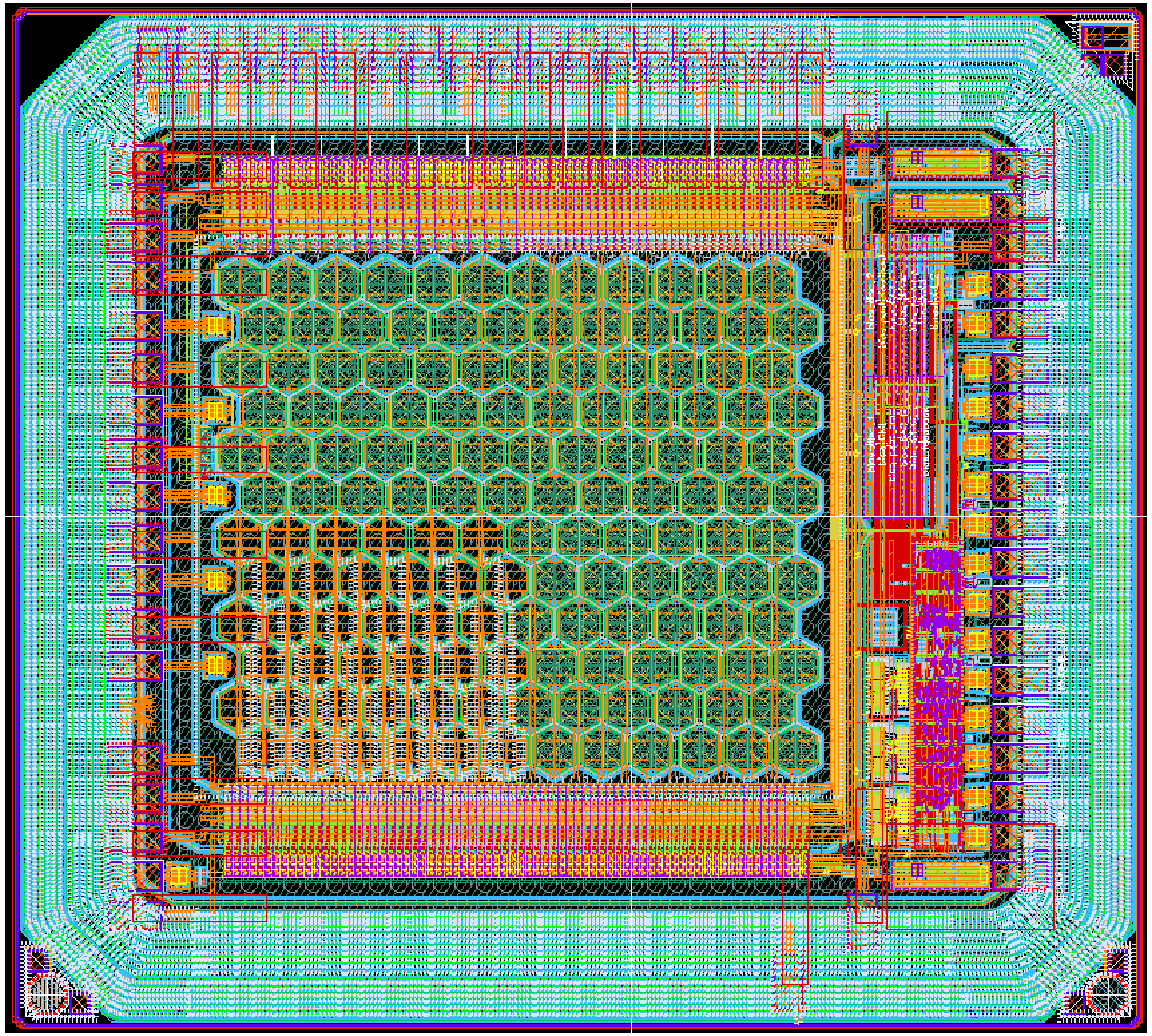
Present prototypes



New technique



Next steps



CONCLUSIONS

- **Timing** capability of silicon still to be fully exploited
- **SiGe HBT** allows for low-noise and fast amplifiers and picosecond readout
- **Monolithic** ASICs in IHP 130nm SiGe processes without internal gain provided
  - **full efficiency**
  - **excellent time resolution**: 220 → 115 → 50 ps RMS ⟶ ???

Publications and patents

Articles:

- Hexagonal small-area pixels — JINST 14 (2019) P11008, https://doi.org/10.1088/1748-0221/14/11/P11008
- TT-PET demonstrator chip testbeam: — JINST 14 (2019) P02009, https://doi.org/10.1088/1748-0221/14/02/P02009
- TT-PET demonstrator chip design: — JINST 14 (2019) P07013, https://doi.org/10.1088/1748-0221/14/07/P07013
- First TT-PET prototype — JINST 13 (2017) P02015, https://doi.org/10.1088/1748-0221/13/04/P04015
- Proof-of-concept amplifier — JINST 11 (2016) P03011, https://doi.org/10.1088/1748-0221/11/03/P03011

- TT-PET engineering: — arxiv:1812.00788
- TT-PET simulation & performance: — arxiv:1811.12381

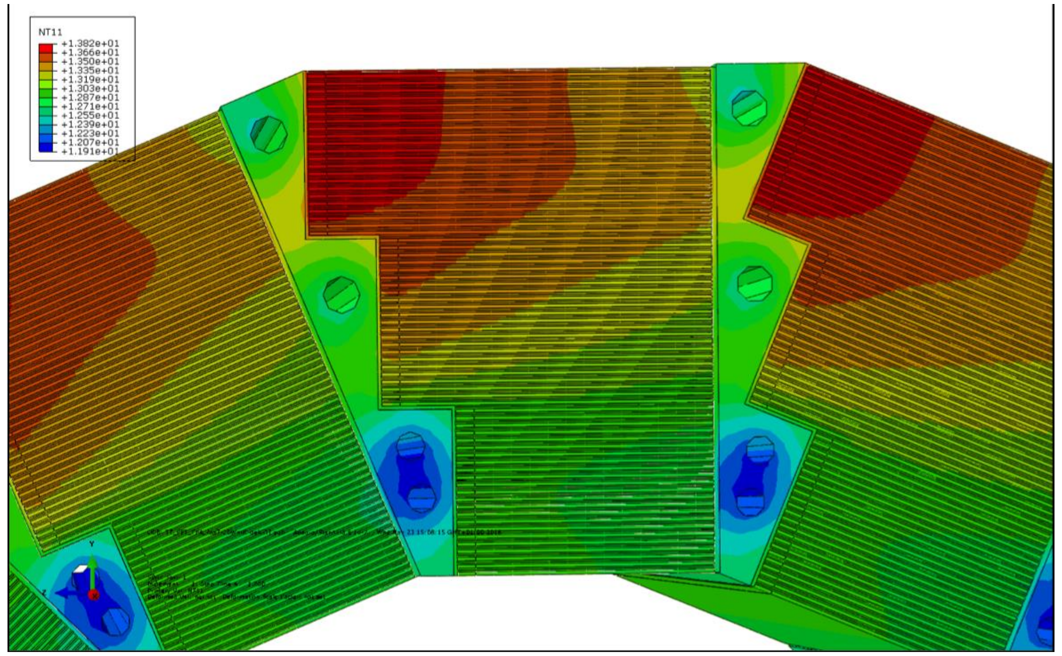
Patents:

- PLL-less TDC & synchronisation System: — EU Patent EP18181123.3
- Picosecond Avalanche Detector (pending): — EU Patent Application EP18207008.6

Extra Material

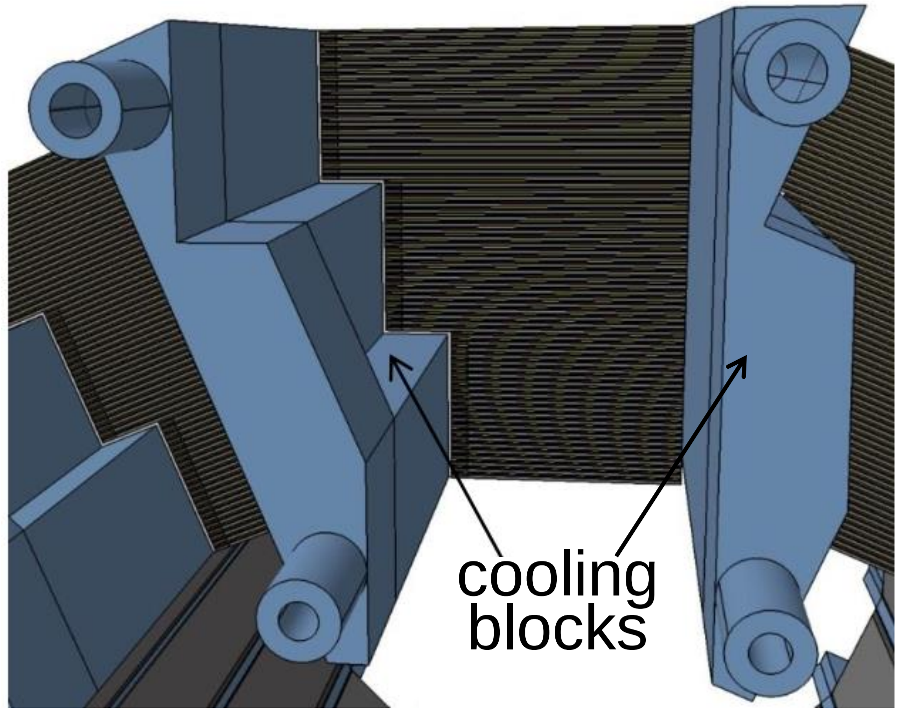
The TT-PET small-animal scanner

TT-PET



Thermal studies:

- High density of silicon pixel sensors
- Sensor power budget < $80 mW/cm^2$
- Finite-Element Analysis performed
- Active cooling: **ΔT < 1˚C** in the sensitive volume
- Cooling block produced and tests made

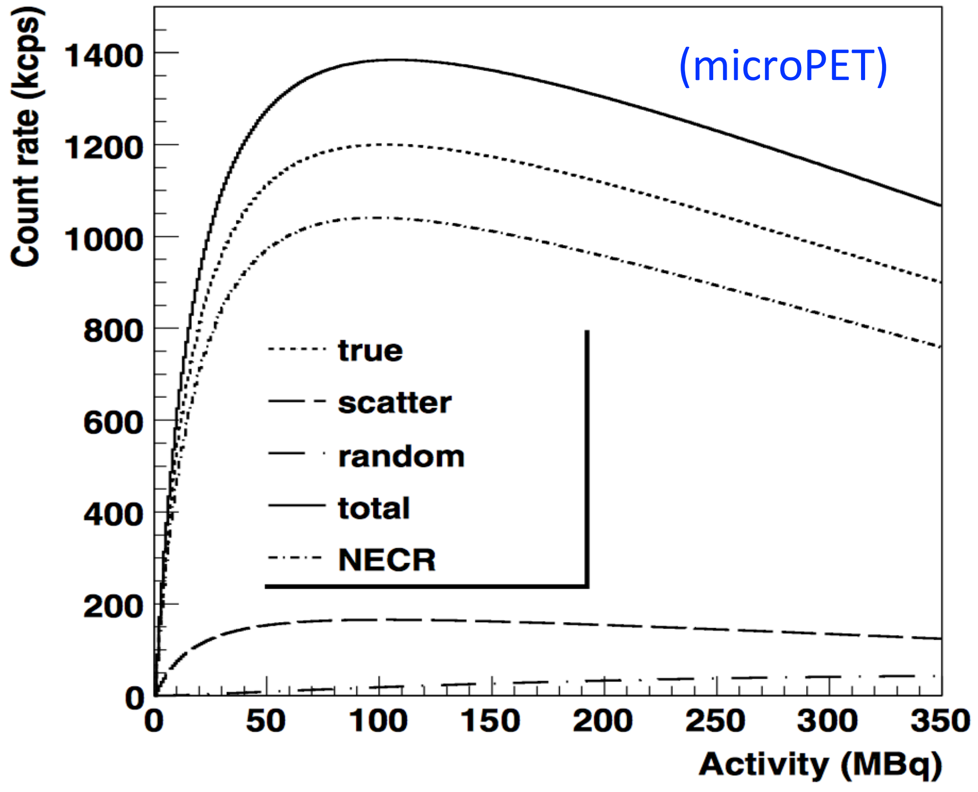


The TT-PET scanner performance

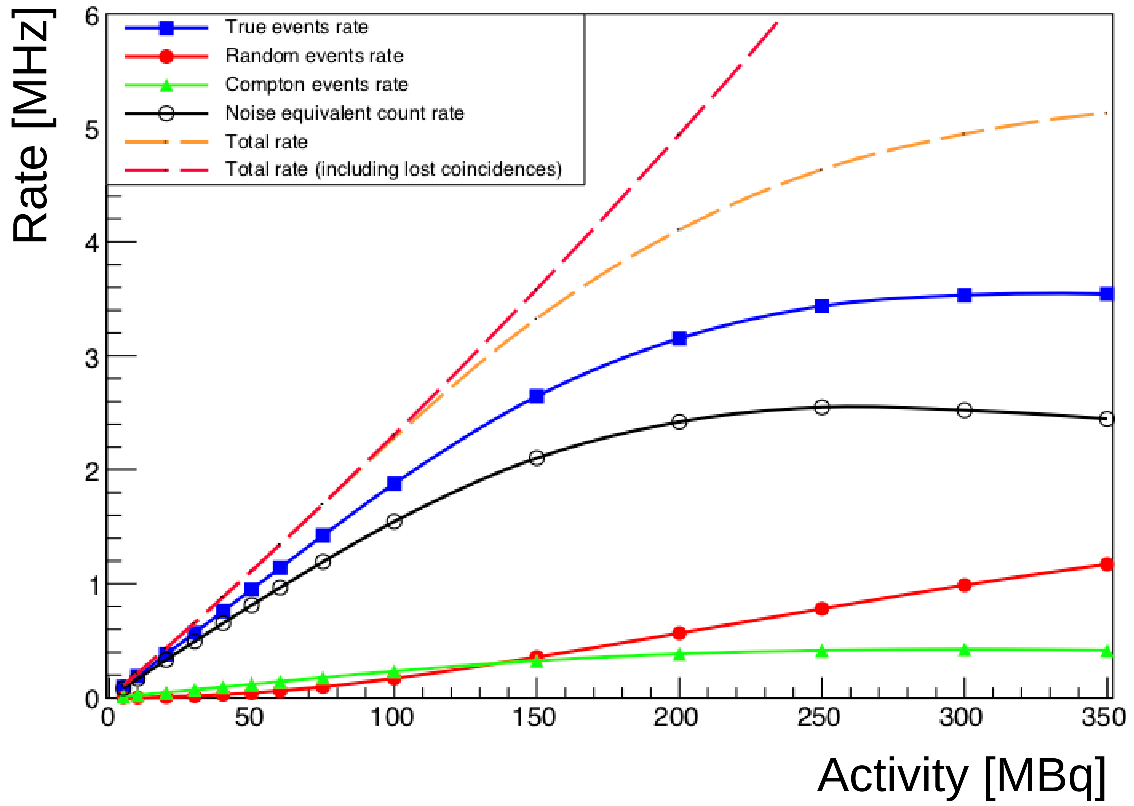
TT-PET

The high segmentation of the scanner and fast response of the silicon pixel detector allow for a very high counting rate.

Typical performance of a small animal TOF-PET

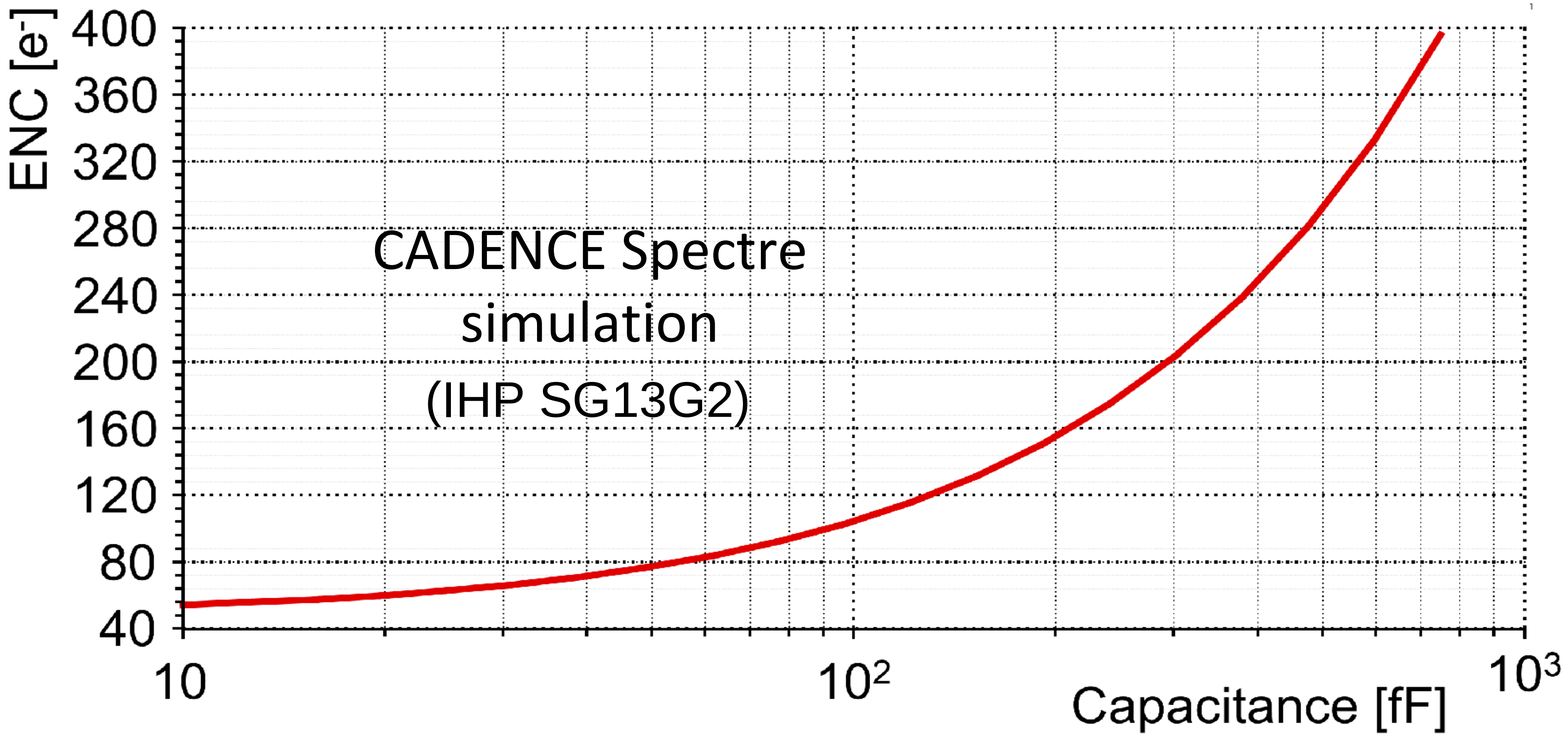


TT-PET scanner counting rates – GEANT4 simulation



Towards **1 ps** time resolution: SiGe electronics

Performance of our **present** electronics

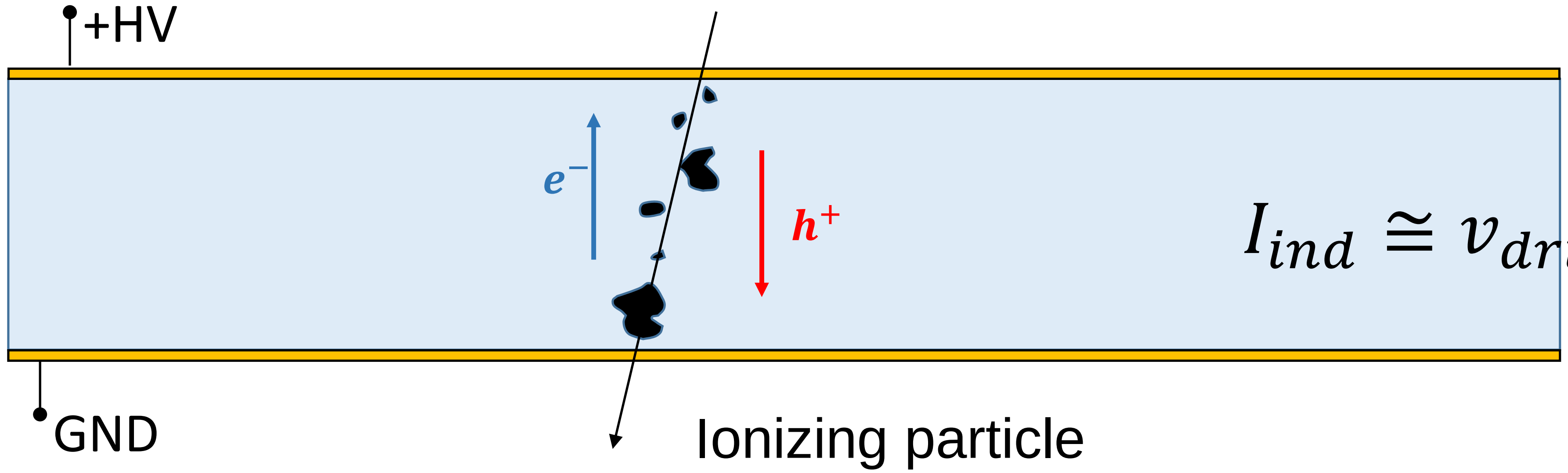


Frontend ENC (CADENCE simulation):

80 e^- RMS for C_{in} = 50 fF and Gain = 30 $\Longrightarrow$ σ_{time} = 4 ps

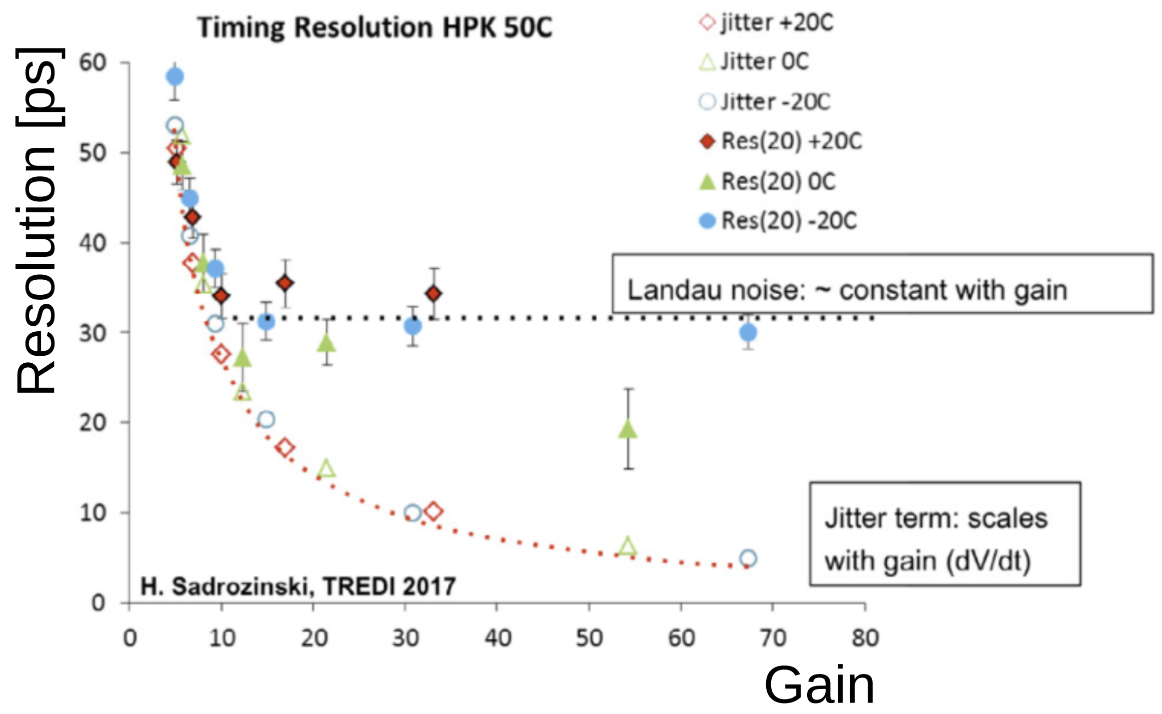
We are working on new version of FE electronics and on a ps TDC

Towards **1 ps** time resolution: Landau noise



$$I_{ind} \cong v_{drift} \frac{1}{D} \sum_i q_i$$

Landau fluctuations of the charge deposition constitute an irreducible effect of standard PN-junction sensors



N. Cartiglia et al., NIM A 924 (2019) 350-354

Need for a **novel** silicon sensor to go beyond this ⟹

Towards **1 ps** time resolution

We designed a new sensor, the

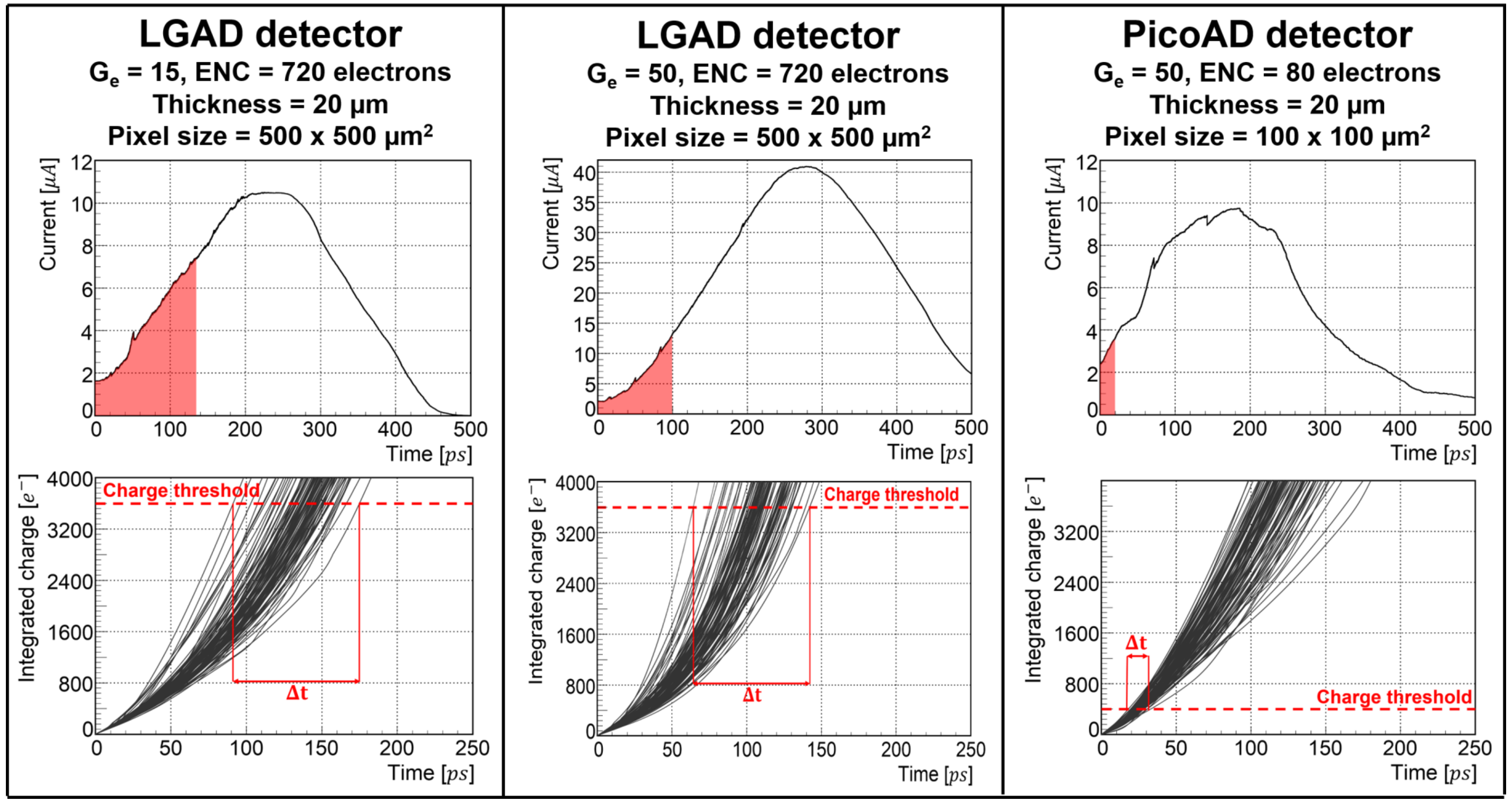
PicoAD: Picosecond Avalanche Detector

Patent pending (EP 18207008.6)

The PicoAD time resolution

One order of magnitude better than present best results

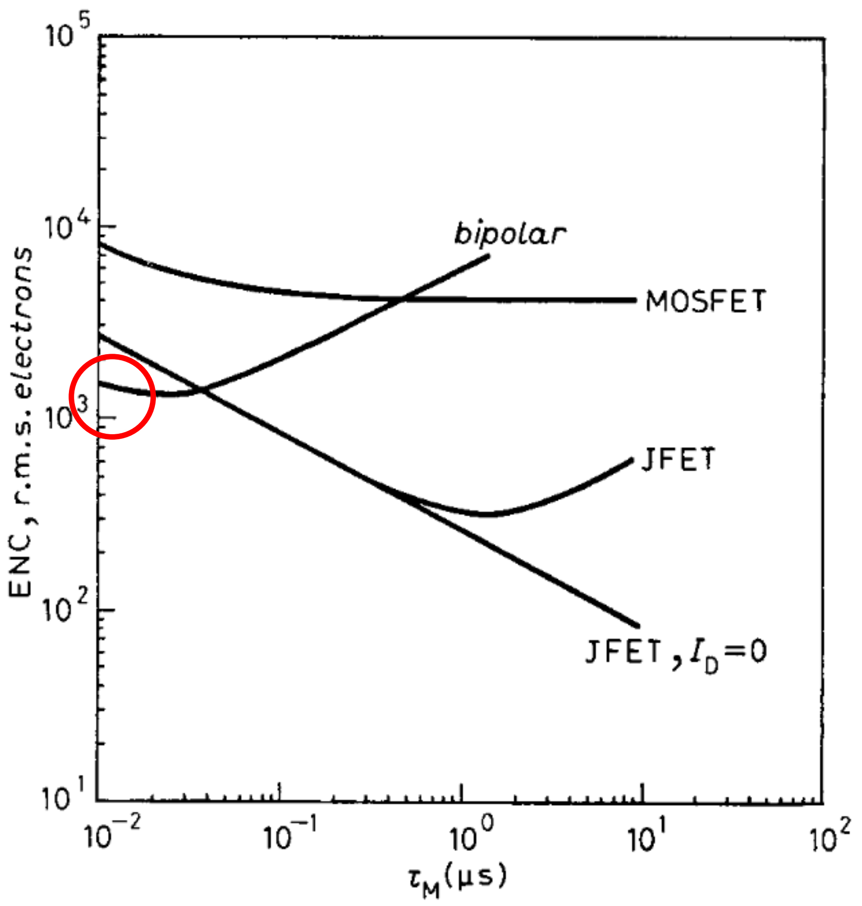
GEANT4 + TCAD + CADENCE Spectre **simulation**



LGAD read out by our SiGe HBT ultra-fast low-noise electronics

PicoAD

Bipolar transistors for fast low-noise amplifiers



E. Gatti, P. F. Manfredi, *Processing the Signals from Solid-State Detectors in Elementary-Particle Physics*, rivista del Nuovo Cimento Vol. 9, No. 1 (1986).

It is known since a long time that for BJT technology the Equivalent Noise Charge (ENC) depends on the capacitance C_{tot} and the integration time τ as follows:

$$ENC = \sqrt{k_1 \cdot \tau + k_2 \cdot \frac{C_{tot}^2}{\tau} + k_3 C_{tot}^2}$$

parallel noise

dominating term: series noise

1/f (series) noise

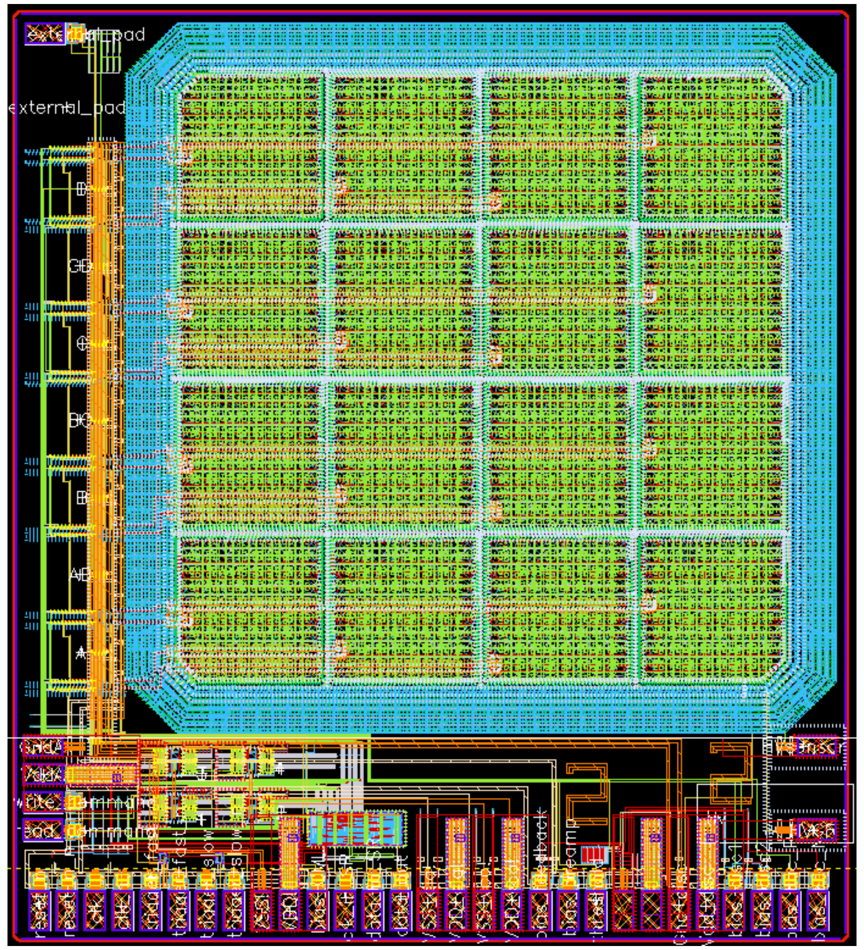
BJT technology: can provide a fast integrator that minimises series noise

⬇

to produce fast and low-noise amplifiers

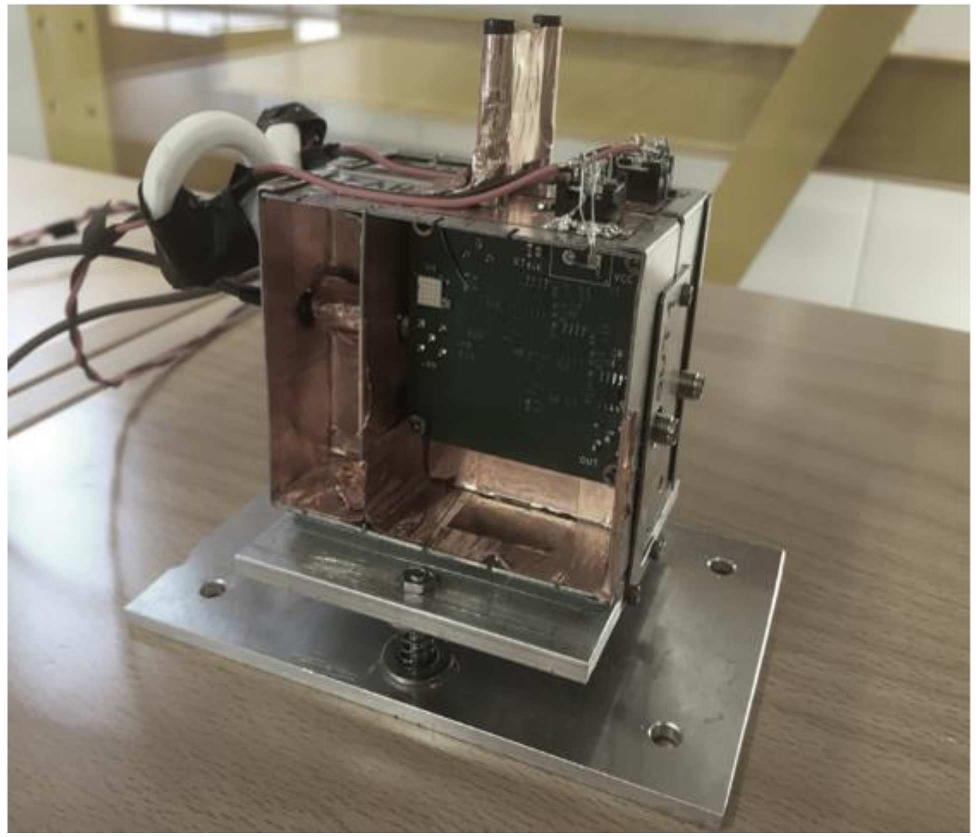
- These two caveats are fixed in a new chip, that we just received back from IHP.

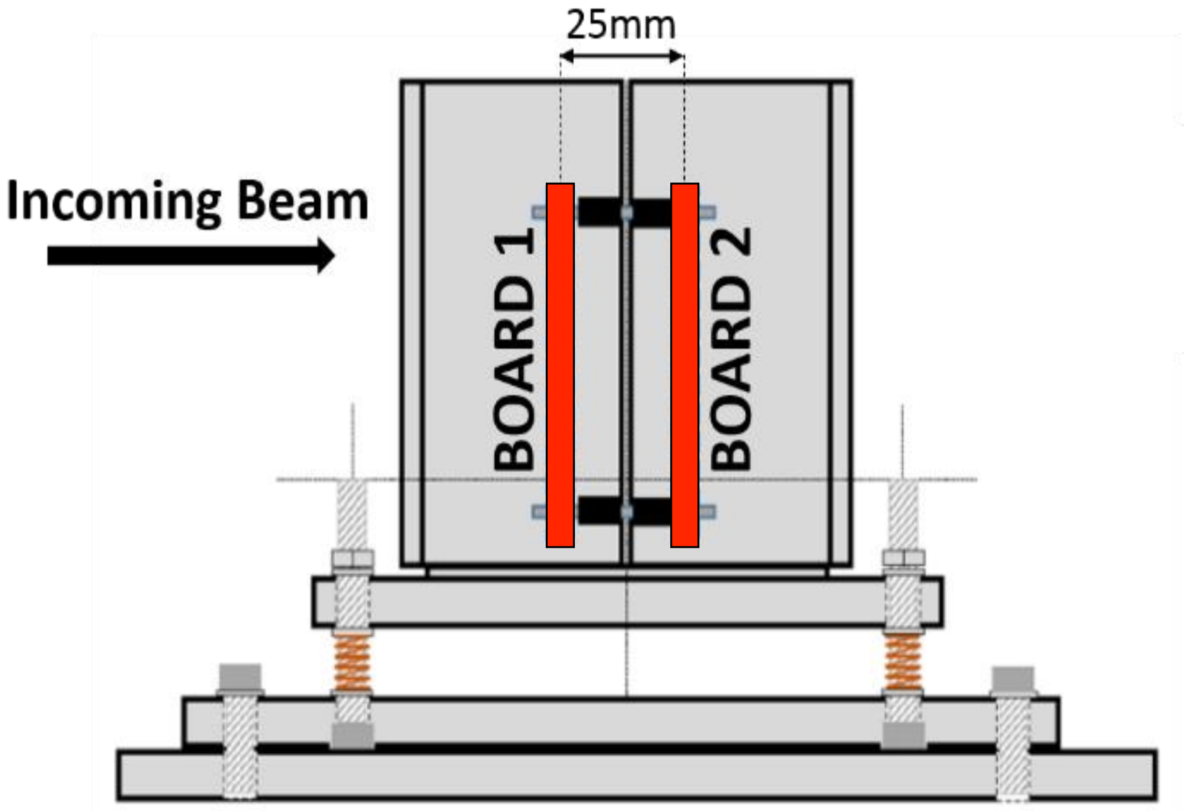
- The chip contains also front-end test structures:
  - peak-sensing fast ADC
  - higher gain pre-amp
  - new differential driver

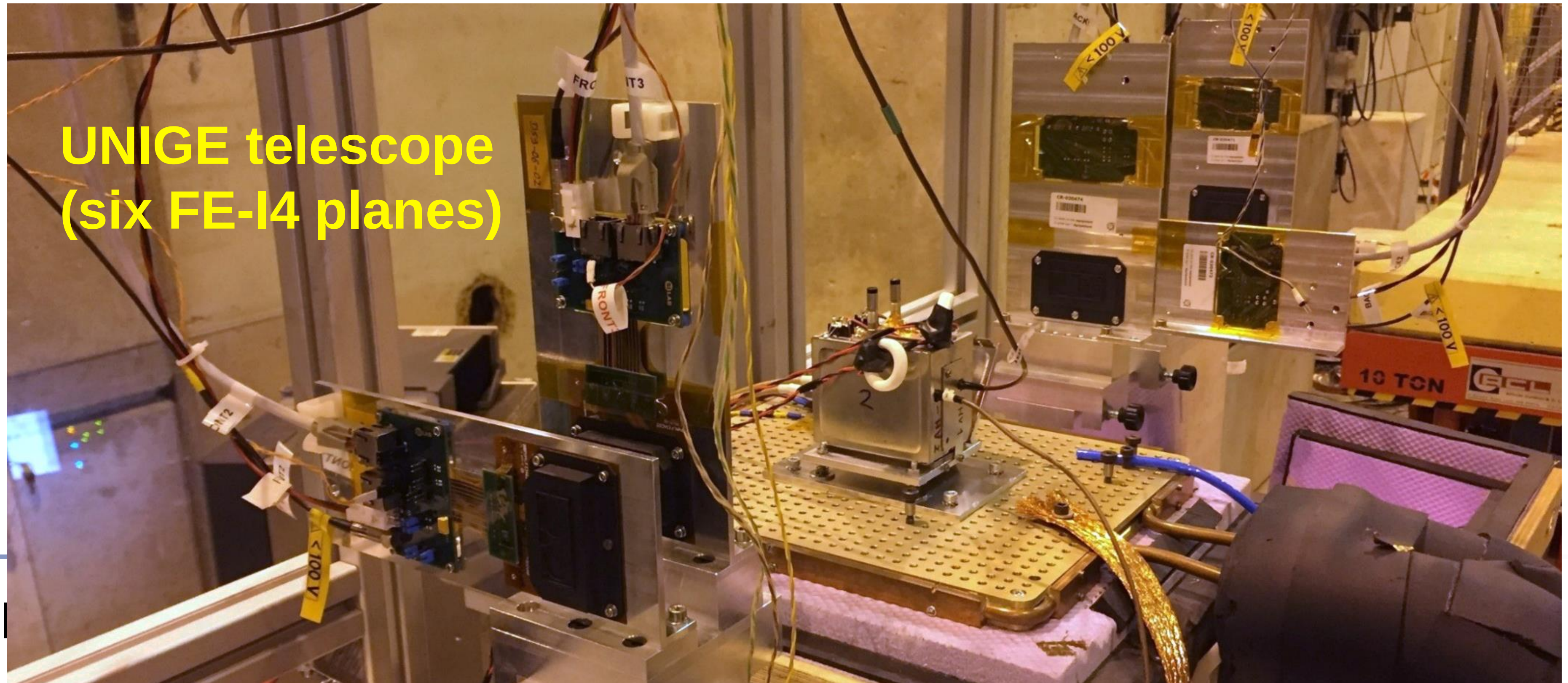


CERN testbeam experimental setup

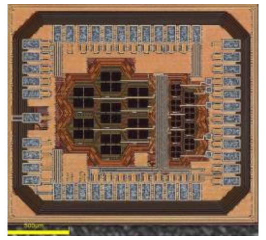
Mechanical support



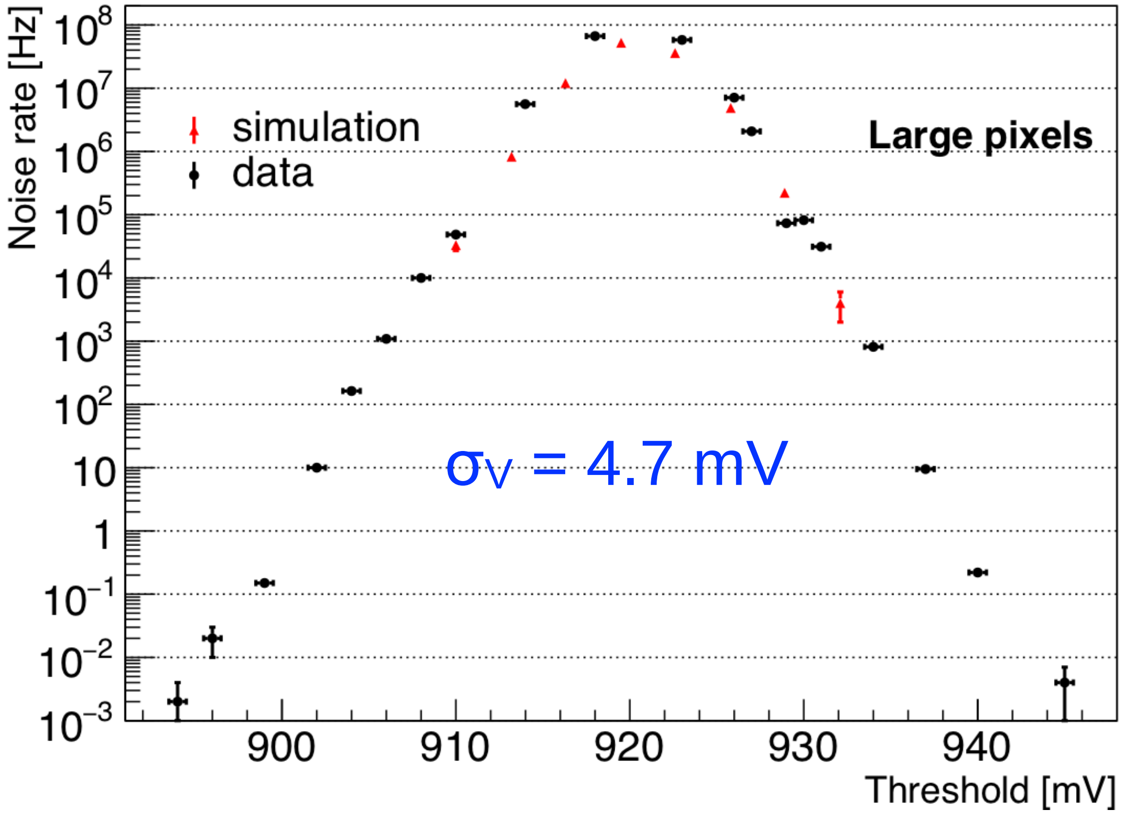




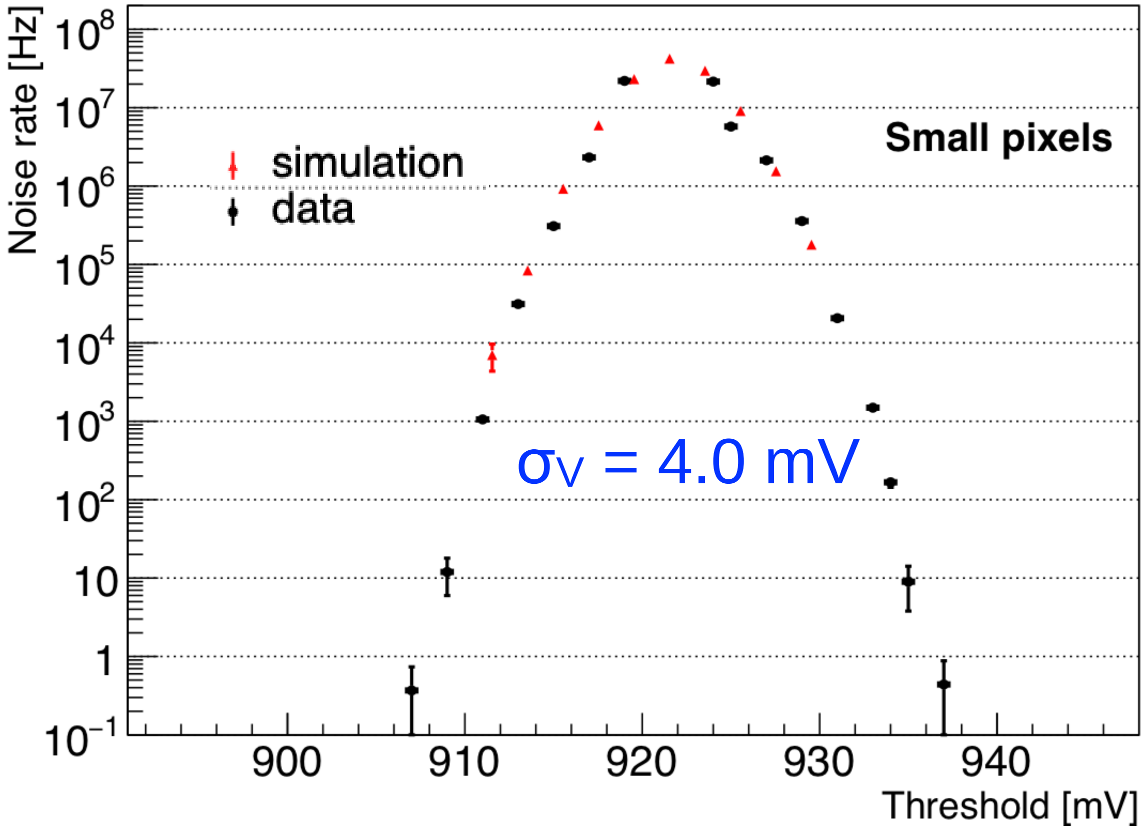
Noise rates



Large pixels (220 fF)

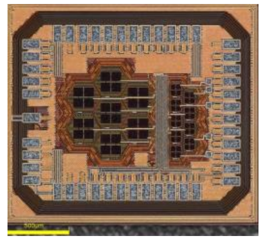


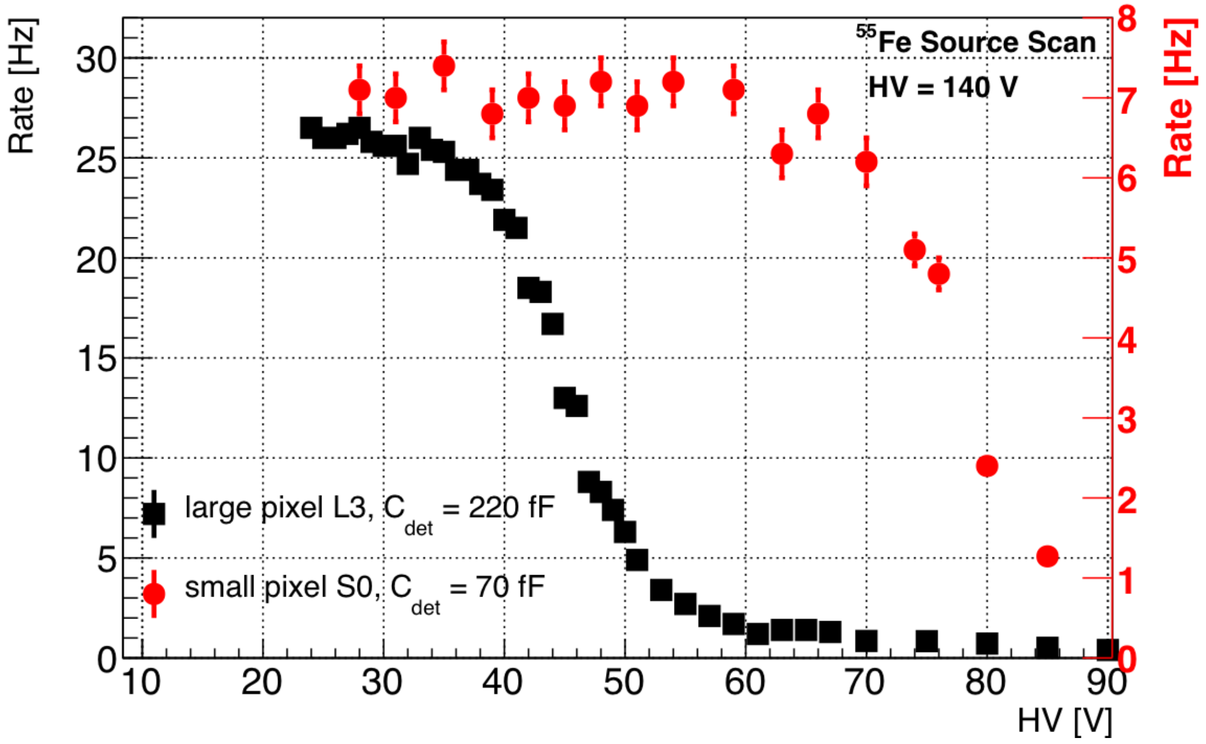
Small pixels (70 fF)

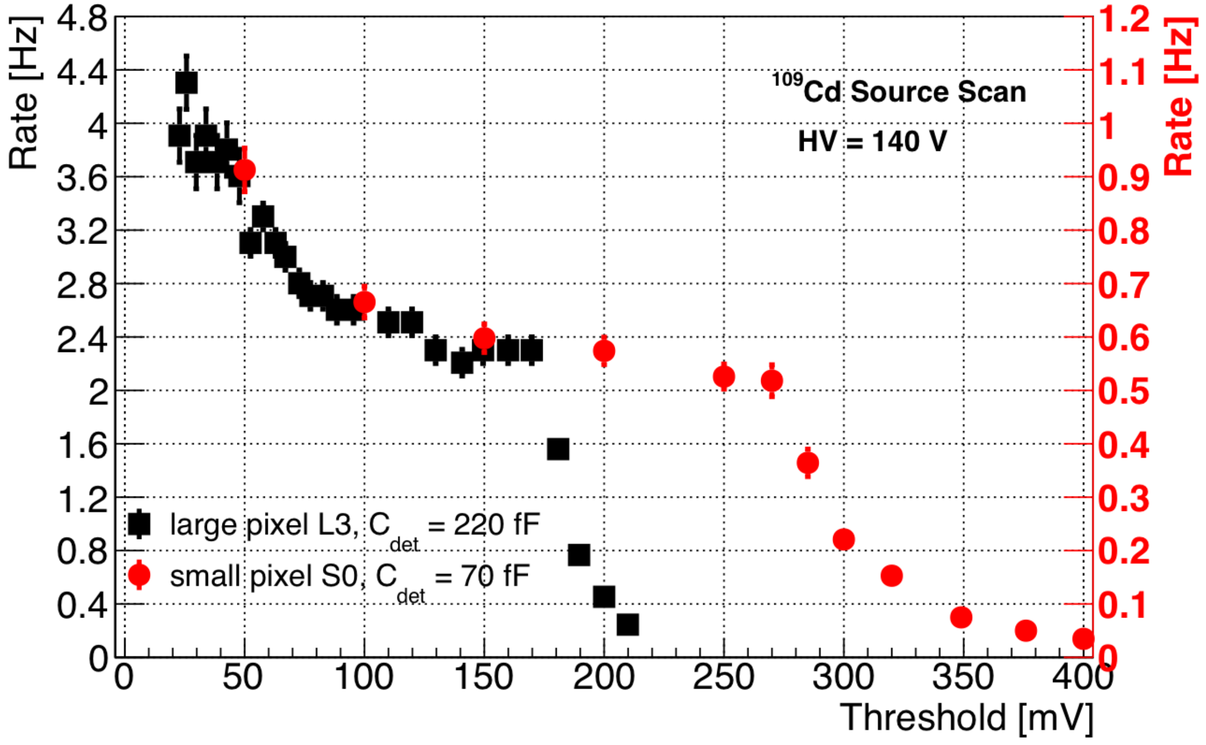


Measured noise rates agree well with CADENCE Spectre simulation

^{55}Fe and ^{109}Cd source calibrations



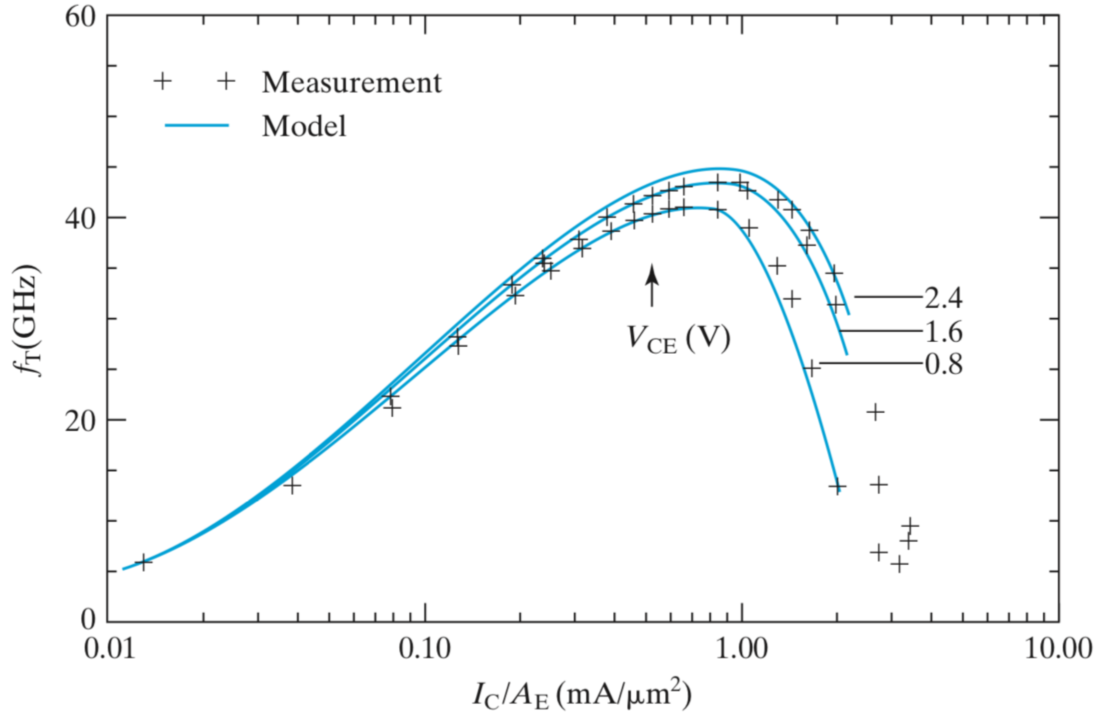




Time resolution vs. power consumption

f_T depends on the collector current I_c
(that is proportional to the power: $P = I_c \cdot V_{cc}$)

From Chenming Hu: Modern Semiconductor Devices for Integrated Circuits, Pearson Ed.



The charge gain can be written as:

$$A_Q = \frac{1}{C_f + \frac{C_{det}}{|A_V|}}$$

In our case, the capacitance C_f between the Base and the Collector of the HBT is much smaller than the detector capacitance: $C_{det}/|A_V| \gg C_f$

Therefore, since A_V is proportional to f_T:
larger power $\Longrightarrow$ larger f_T $\Longrightarrow$ larger A_V $\Longrightarrow$ smaller ratio $C_{det}/|A_V|$ $\Longrightarrow$ higher A_Q

CADENCE simulation

Signal in the hexagonal small pixels: