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Latest Developments of Trench-Isolated LGADs

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CMM
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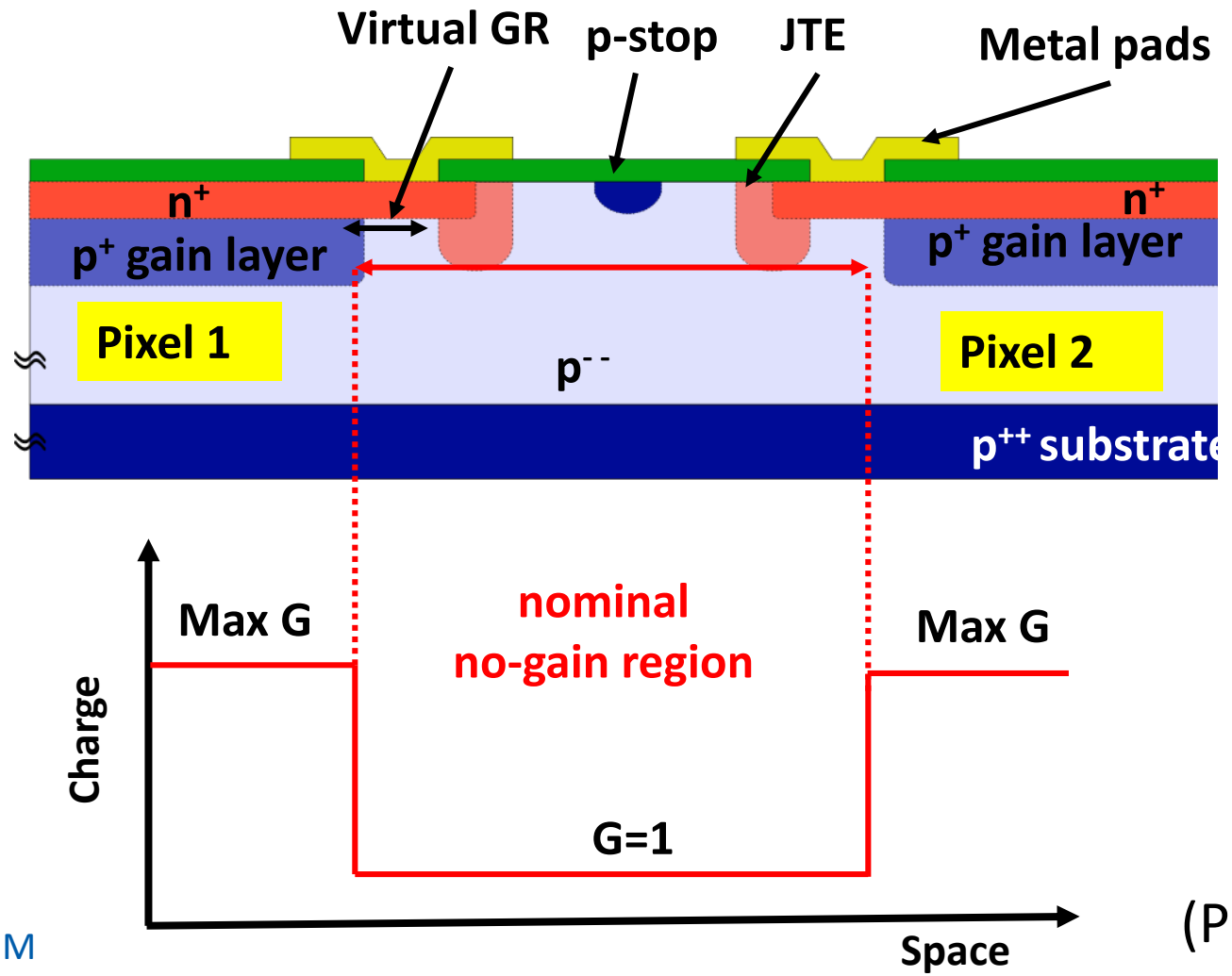
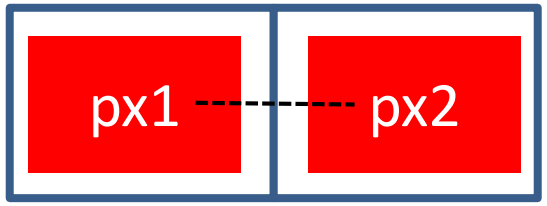
Segmentation in LGAD

Inter-pixel region in Standard LGADs



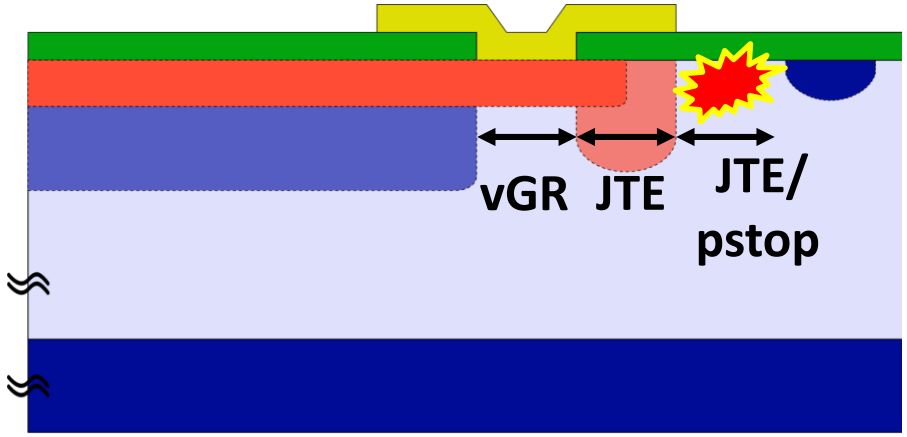


- Inter-pixel region hosts the isolation and termination structures:
  - P-stop
  - Junction Termination Extension (JTE)
  - Virtual GR
- **The pixel border is a dead-region.** The carriers generated in this area are not multiplied.

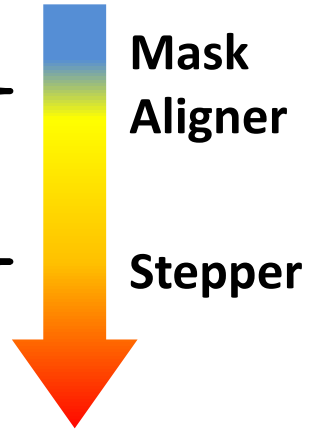
Nominal NO-GAIN region
(PGAIN-PGAIN distance defined by layout)

Segmentation in LGAD

- The nominal no-gain width depends on:
  - **technology** (photolithographic) constraints
  - **physical limits** (maximum E fields) to fulfill operational requirements (V_{BD} , etc.)



Layout	No-gain width
UFSD 2	66 um
UFSD 3 - Safe	31 um
UFSD 3 Intermediate	20.5 um
UFSD 3 Aggressive	11 um



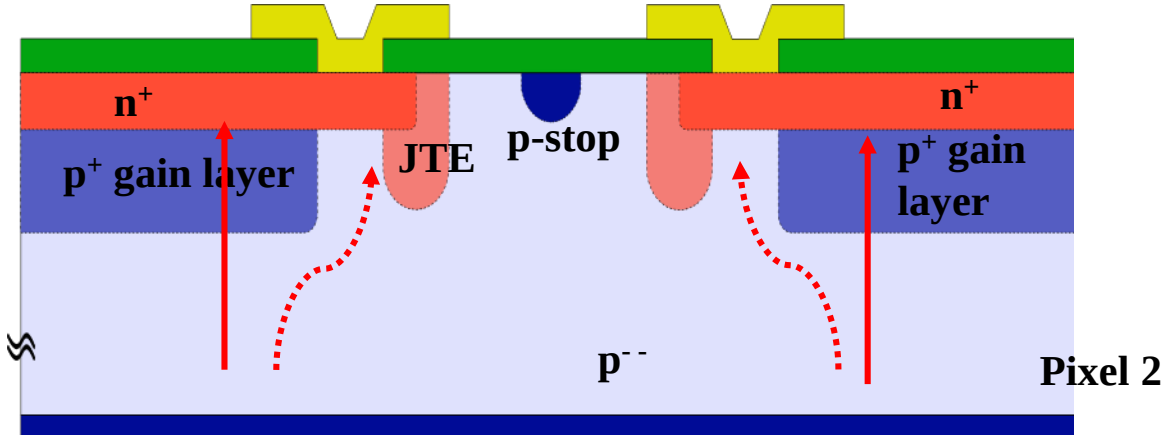
There is an **intrinsic limit in reducing the inter-pad region**. A too small distance between n-doped regions and p-stop leads to early edge-BD and pop-corn noise

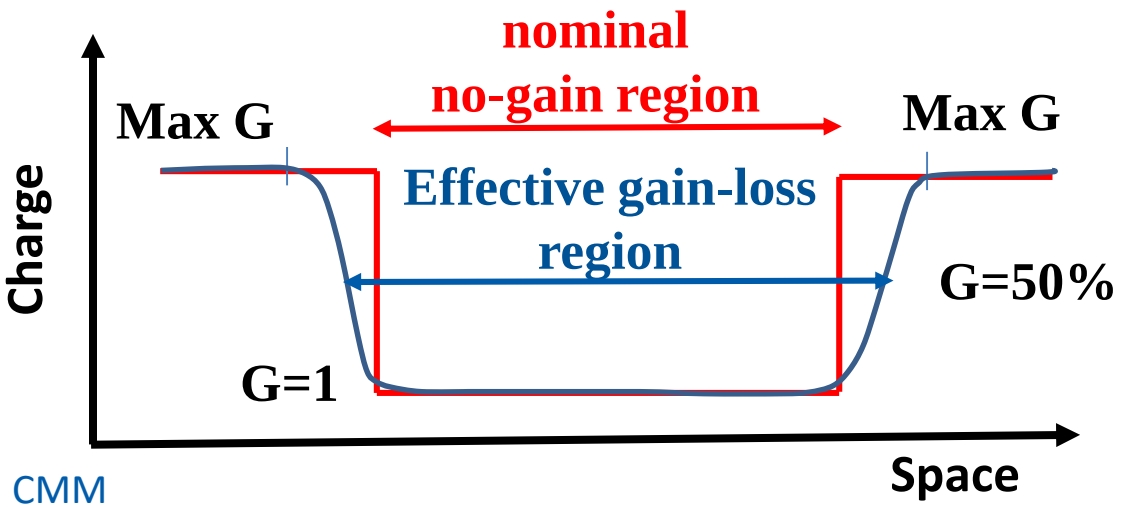
With the current design/technology 20 um can be considered the minimum safe no-gain width

(see V. Sola's Talk)

Segmentation in LGAD

The collection and drift mechanisms also play a role in the no-gain region.





- Some carriers, even if generated below the nominal gain layer, are collected by the deeper JTE and does not pass through the gain layer.
- These carriers are multiplied with reduced gain

Effective gain-loss width >= nominal no-gain

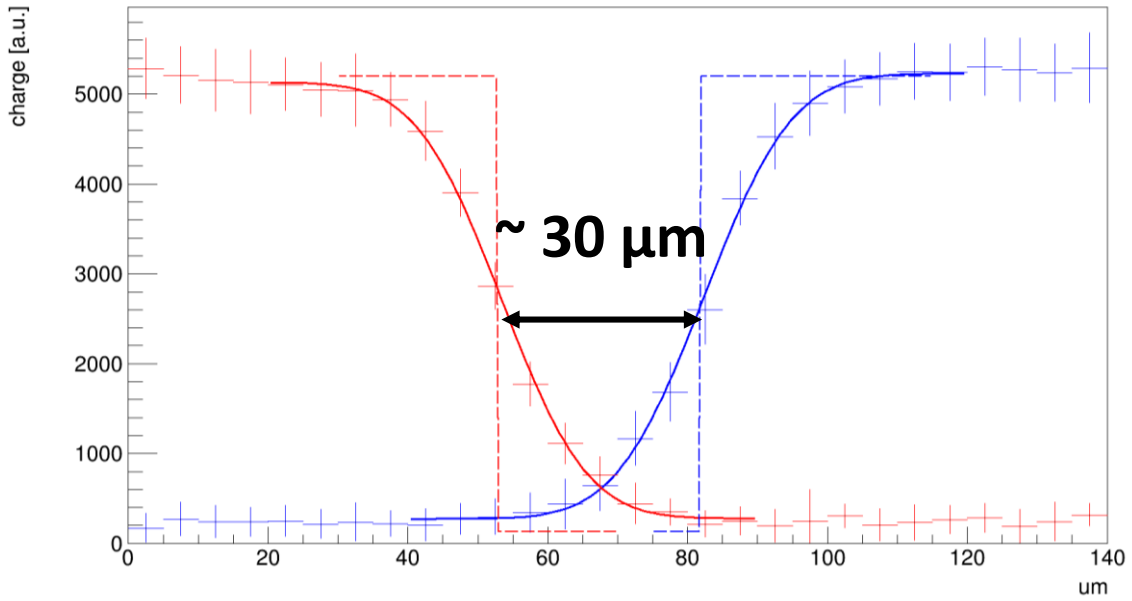
Segmentation in LGAD

UFSD3 – Intermediate

Nominal no-gain width = 20.5 µm

Measured gain-loss width = 30 µm

Measurement (laser scan)

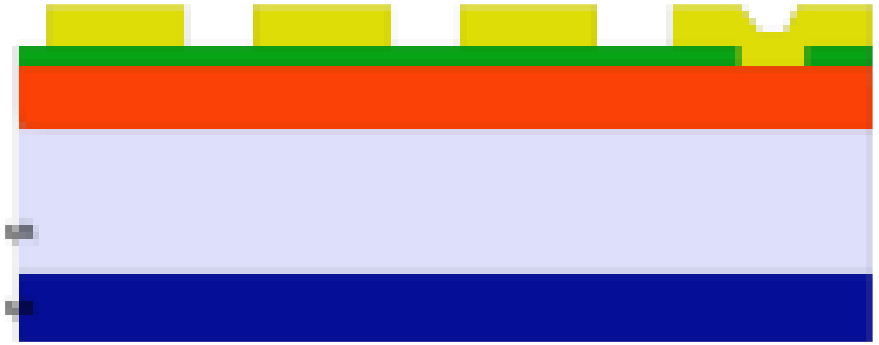


Measurements performed in Torino Silicon Lab
(University of Torino - INFN)

New Segmentation Strategies under development at FBK

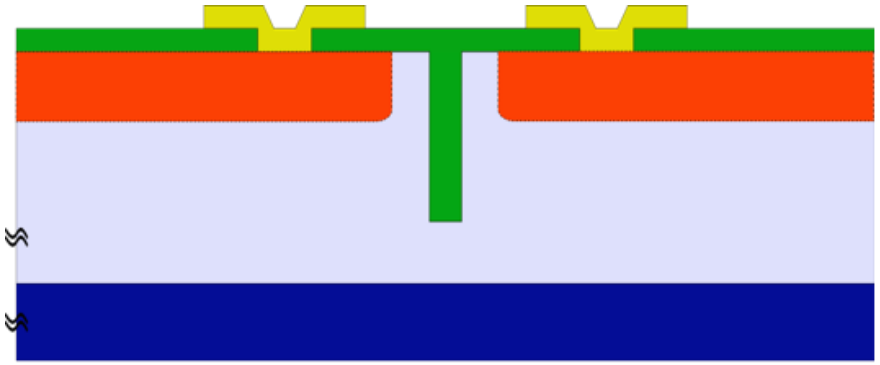
RSD Resistive Silicon Detectors

(M. Mandurrino INFN To)



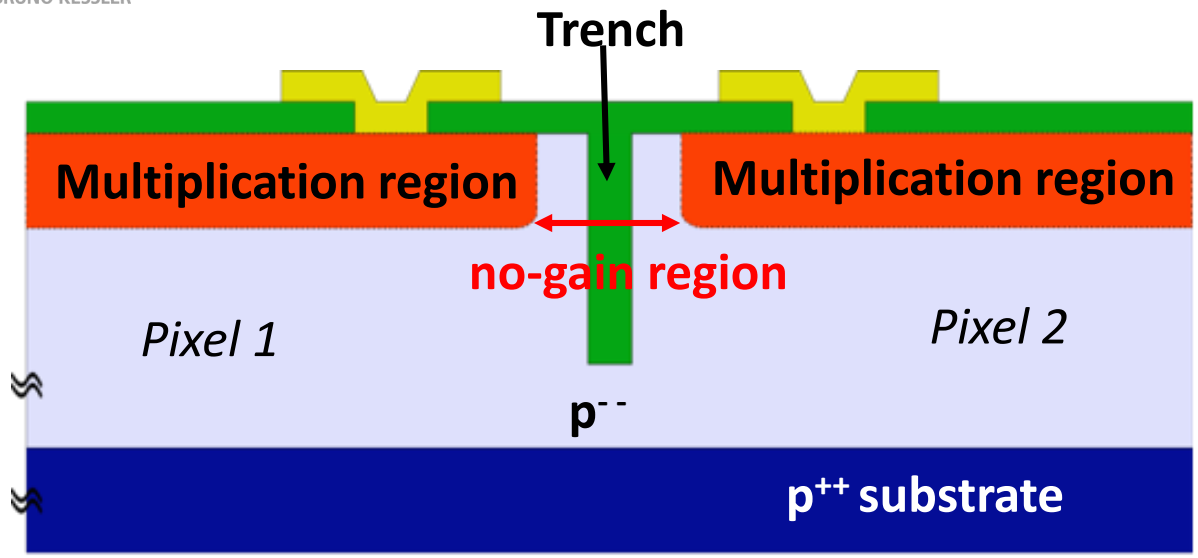
- Metal Pads AC-coupled to the resistive n+ via dielectric coupling layer
- Not-segmented PGAIN -> virtually 100% FF **(see Tornago's Talk)**

Trench-Isolated LGADs (TI-LGAD)

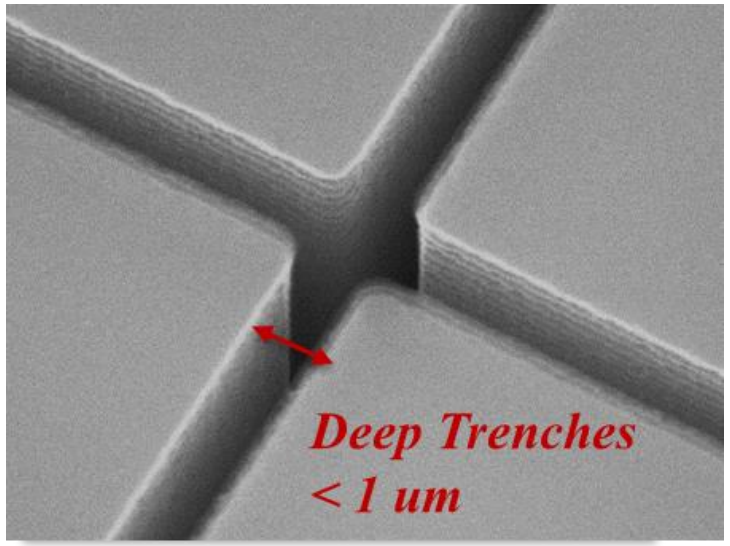


- DC readout
- Patterned p-gain
- Compact isolation structure based on Deep Trench Isolation technology

Deep Trench Isolation technology

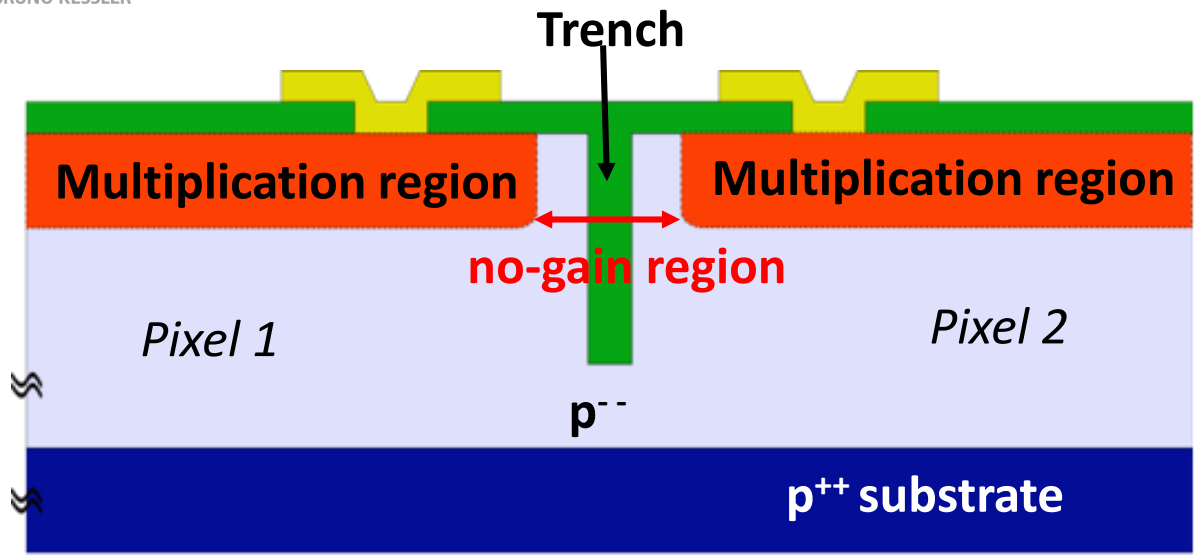


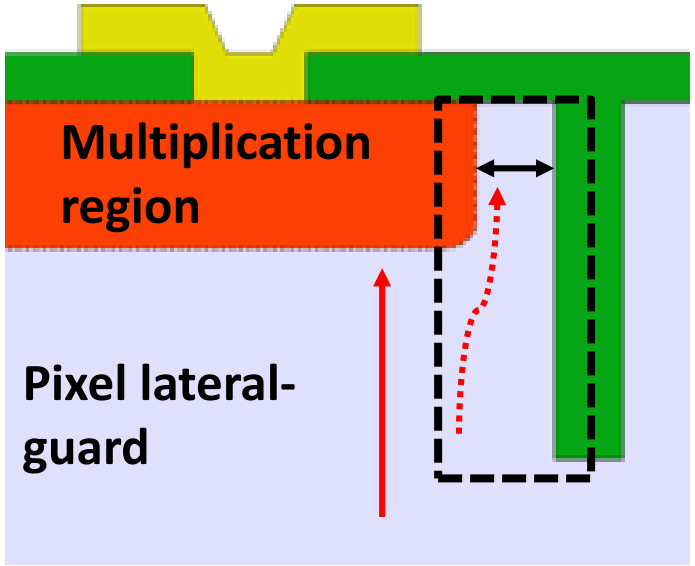
- New **LGAD** technology proposed by FBK:
  - **JTE and p-stop are replaced by a single trench.**
  - Trenches act as a drift/diffusion barrier for electrons and isolate the pixels.



- The trenches are a few microns deep and < 1um wide.
- Filled with Silicon Oxide
- The fabrication process of trenches is compatible with the standard LGAD process flow.

Deep Trench Isolation technology





Multiplication Region to Trench distance

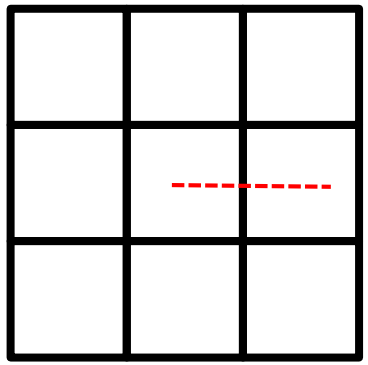
Two-fold advantage with respect to standard LGADs:

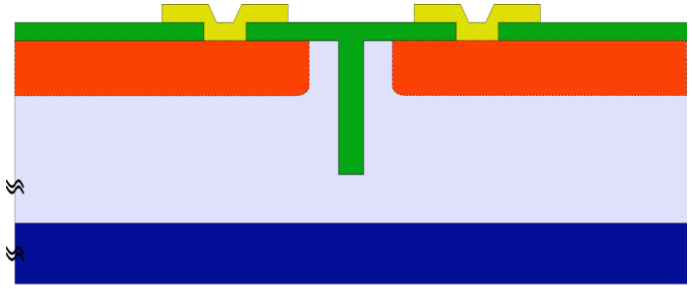
- Trenches are much smaller wrt JTE and p-stop => smaller nominal no-gain region (**from 20-60 um to 4-6um**)
- The E-field at the pixel border could be optimized to reduce the transition region width

Smaller gain-loss region is expected

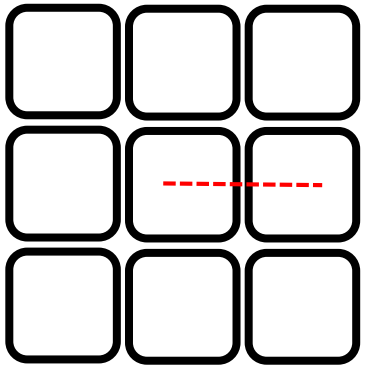
TI-LGAD Design & Simulations

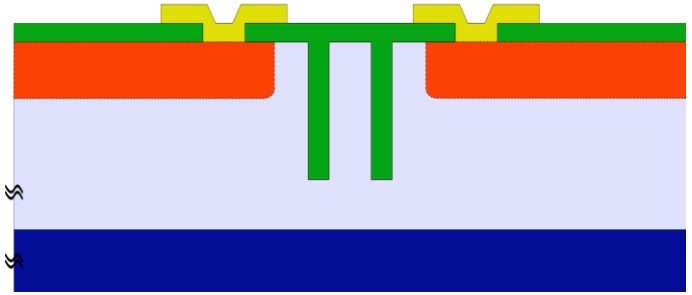
➢ **1 Trench Layout (trench grid)**





➢ **2 Trenches Layout**





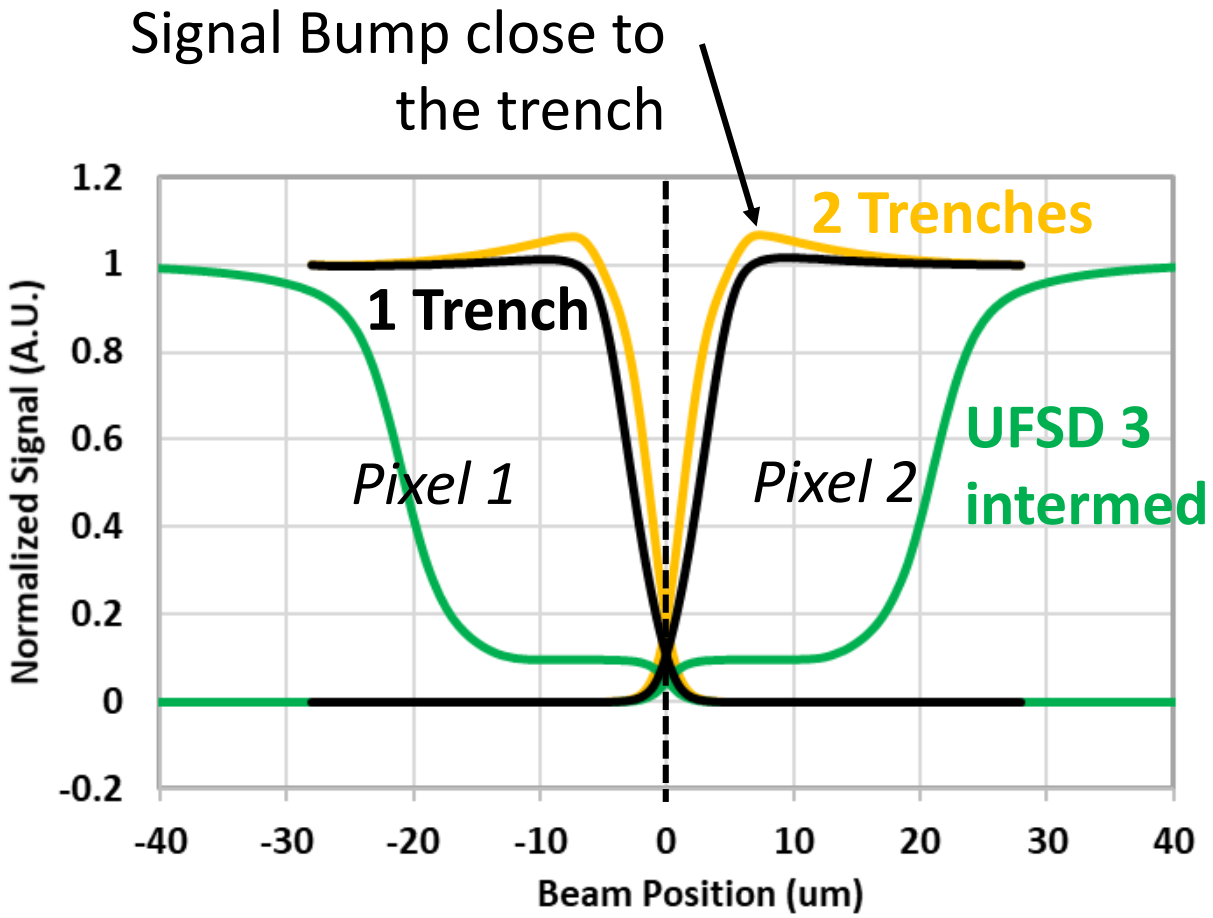
➢ **A TCAD simulations campaign** was carried out in order to optimize the TI-LGAD design in terms of:

- Trench geometry (1 trench, 2 trenches)
- Trench depth

Layout	Nominal no-gain width
1 Trench	~ 4 um
2 Trenches	~ 6 um

TI-LGAD Design & Simulations

TCAD Simulated laser scan at the inter-pixel region (1um wide IR laser spot)



Layout	Nominal no-gain	Effective gain-loss
1 Trench	~ 4 um	~6 um
2 Trenches	~ 6 um	~3 um

- Even if 2T Layout has larger nominal no-gain region the effective gain-loss width is less wrt to 1T layout
- 2T layout shows increased signals at the border (high local E-field)

Design optimization trade-off between minimization of the gain-loss region and reduction of E-field at the border.

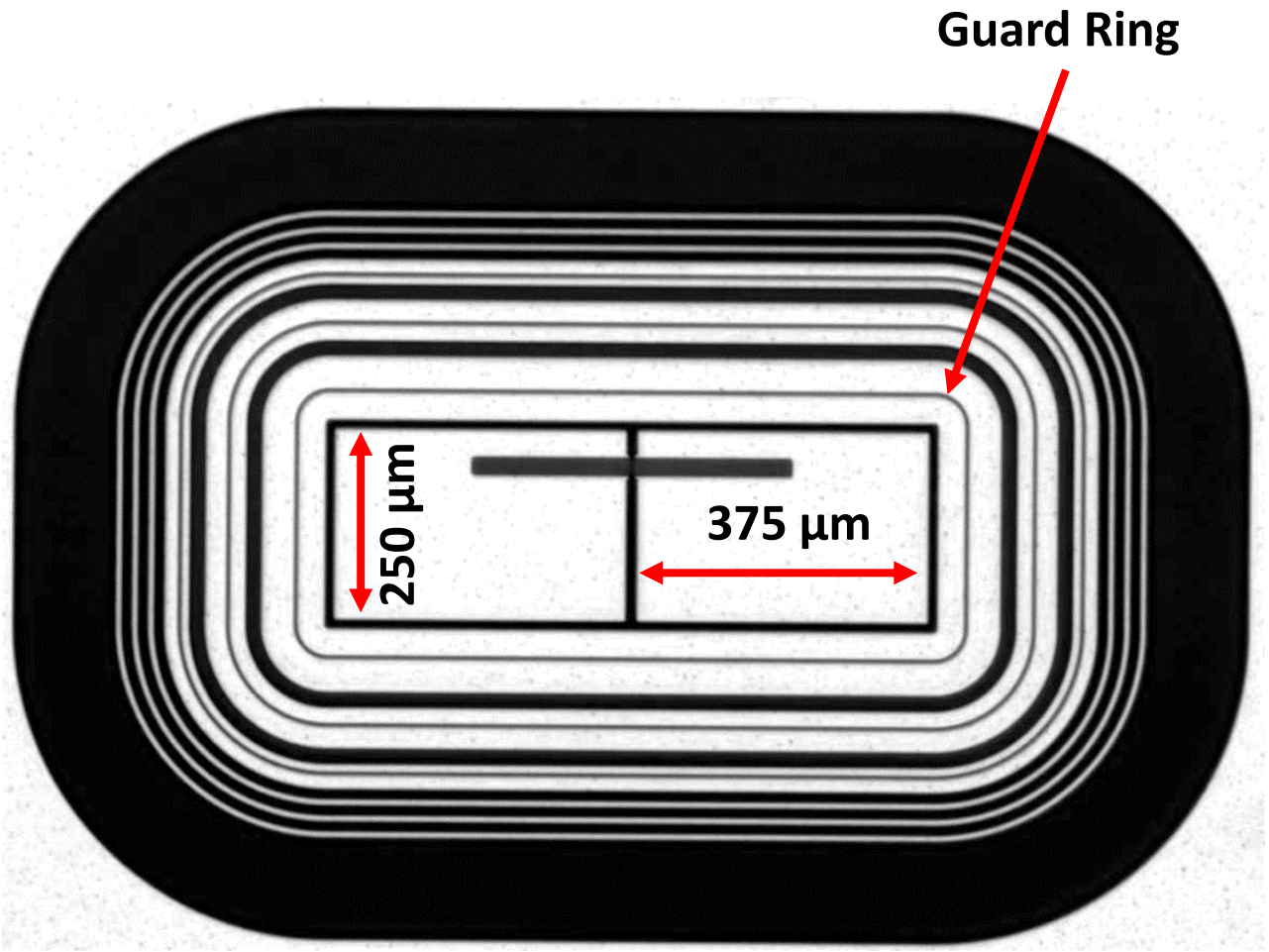
1st Test Run of TI-LGADs

First test run of TI-LGADs produced at FBK in 2019. Goals:

- Testing of the trench fabrication process
- Validating the pixel layout

Sensor geometry:

- 2x1 pixels (250 µm × 375 µm)
- 5-rings Guard Ring (the same used in standard LGADs)



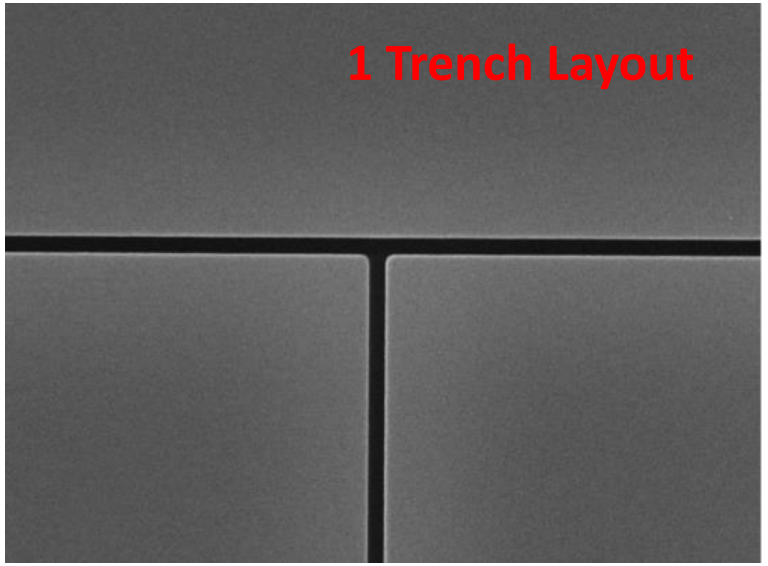
1st Test Run of TI-LGADs

Layout splits (~30):

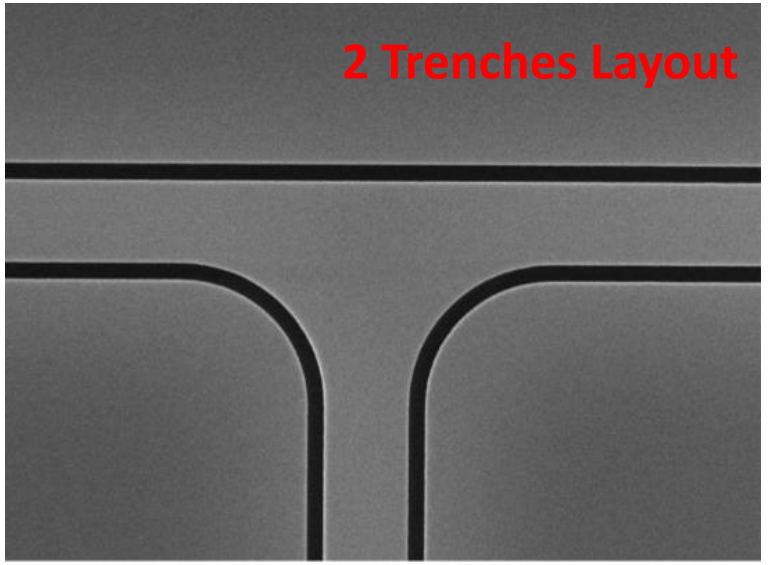
- Trench layout (1T and 2T)
- Pixel Lateral border (trench-multiplication region distance)

Process splits:

- trench fabrication process.
- Trench depth
- PGAIN implant doses



SEM images after trench etching



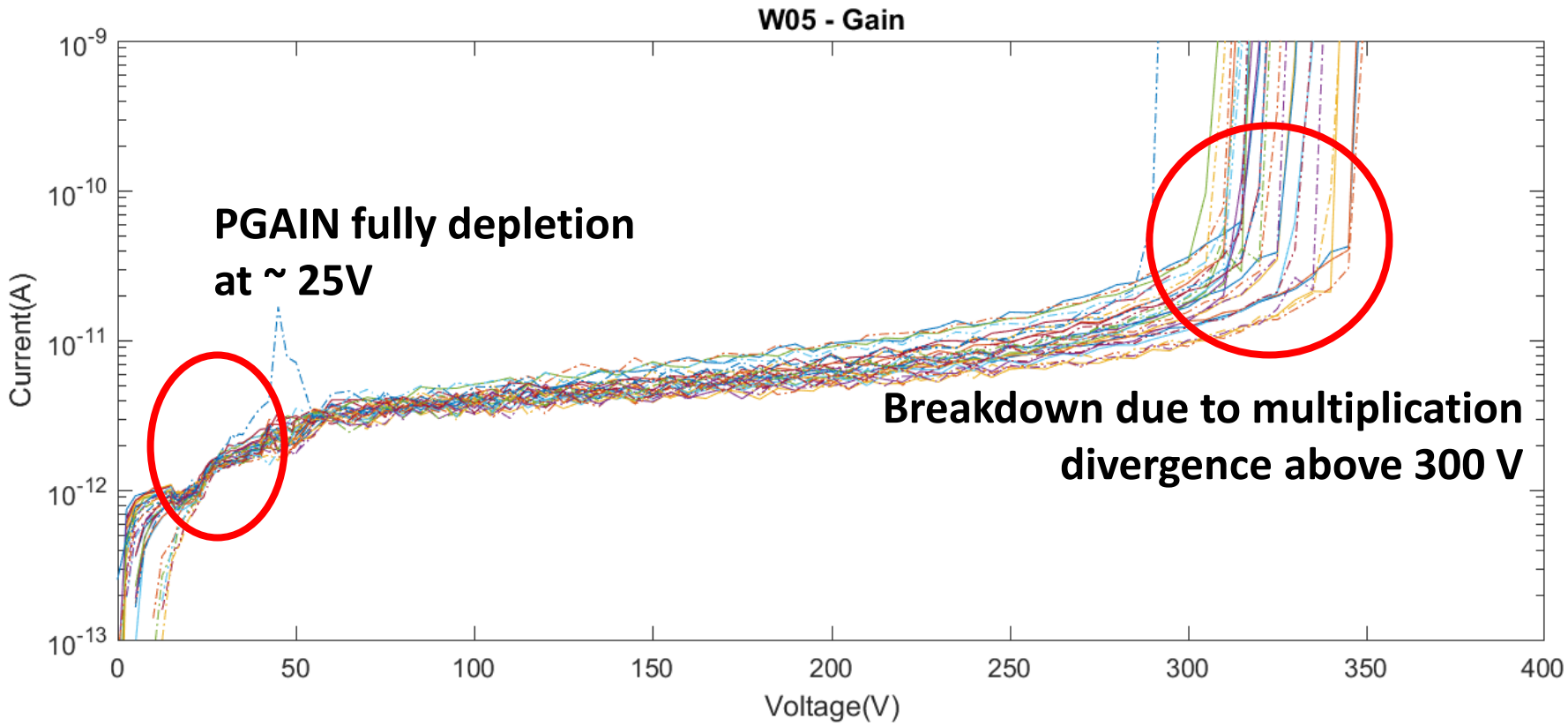
Process ISSUE: One process step of the standard process flow resulted not compatible with trench technology. **Very low yield in the first batch.**

The issue was detected and a revised process flow is now available.

TI-LGAD Parametric Characterization (IV)

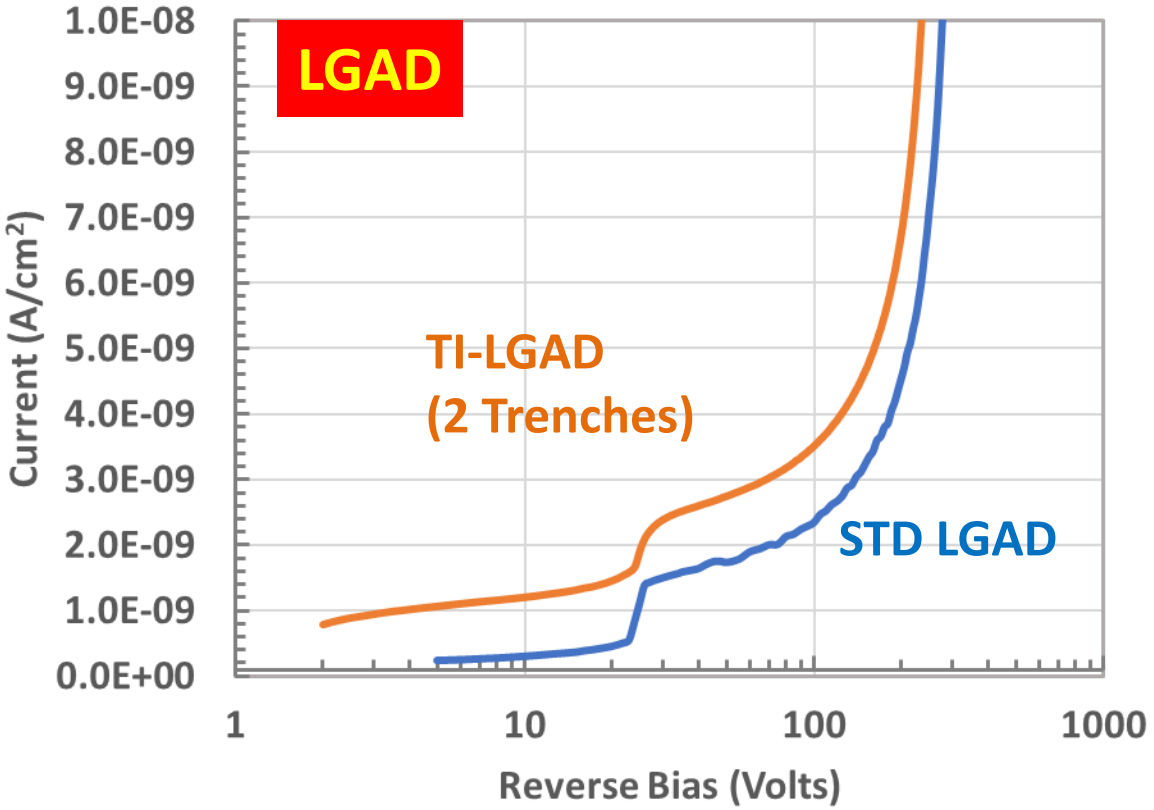
First IV curves show expected behaviour of TI-LGAD sensors:

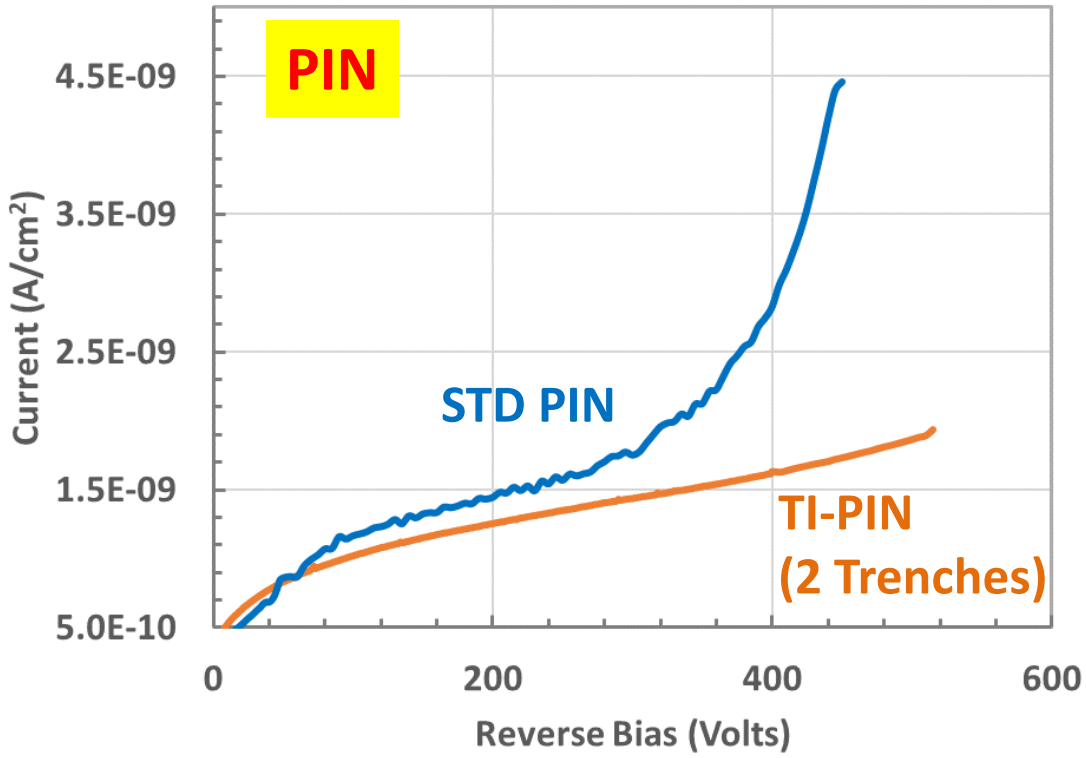
- Gain “knee” @ ~ 25 V
- Breakdown > 300 V



TI-LGAD Parametric Characterization (IV)

TI-LGAD vs STD LGADs (produced in the same batch with the same junction technology)





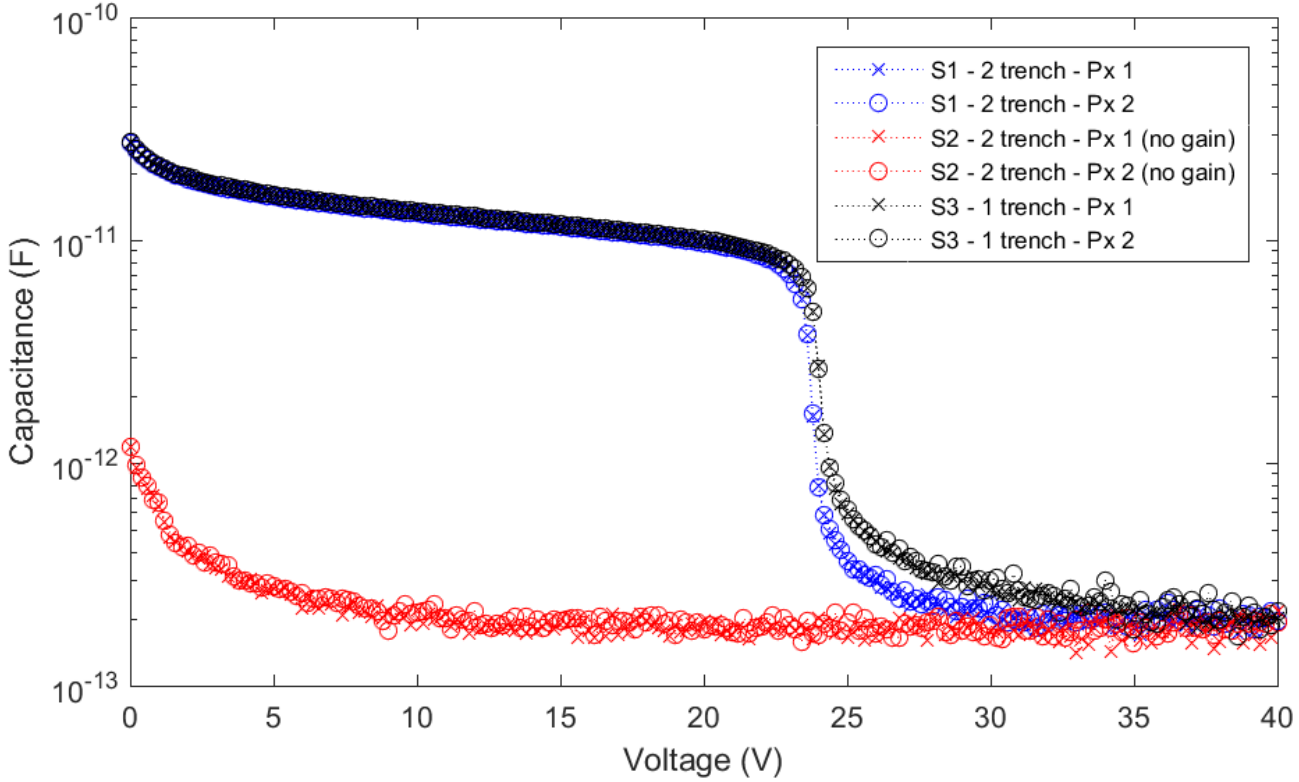
- Electrical behavior is compatible with STD LGADs
- Same knee Voltage and BD Voltage
- Difference in dark current is not significative

- STD PIN breakdown at 420 Volts (most likely at the pixel border).
- NO BD in TI-PIN up to 500V

TI-LGAD Parametric Characterization (CV)

CV curves show expected behaviour of TI-LGADs and corresponding p-i-n diodes:

- TI-LGADs : full depletion of gain layer @ ~ 24 V
- TI-LGADs : full depletion of active volume @ ~ 30 V



Functional measurements in the next talk by F. Siviero

Measurements performed in Torino Silicon Lab (University of Torino - INFN)

TI-LGAD RD50 Project

R&D Project co-funded by RD50 Collaboration

FINAL GOAL: Design and production of TI-LGAD with small pixels (<= 100 um) and high Fill Factor (> 80%)

Involved Institutes (RD50 members)

1. Fondazione Bruno Kessler
2. INFN Torino
3. KIT
4. University of Zurich
5. Paul Scherrer Institut
6. Institut "Jozef Stefan"
7. University of Birmingham
8. UC Santa Cruz

Activity	Time
Numerical simulation and structure definition	done
Characterization of the Preliminary Test RUN	Ongoing (end of Nov 19)
Layout Definition and Reticle Production	Ongoing (end of Dec 19)
Batch Production	Jan 20 – April 20
Electrical Characterization	May 2020
Dicing and sensor Shipping	June 2020

TI-LGAD RD50 Project

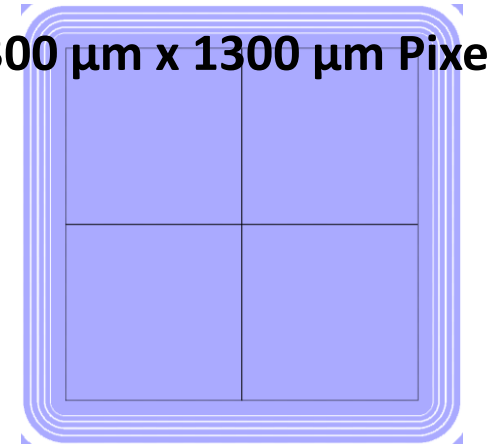
- **Layout definition is under discussion with all the partners**
  - Strip Sensors and Pixel Arrays compatible with the most common ROC (TimePix, TimeSpot, ALTIROC,….)

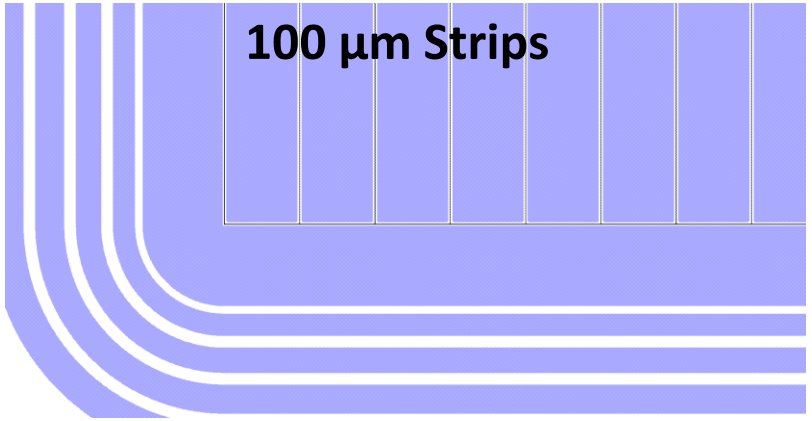
Pixel Arrays

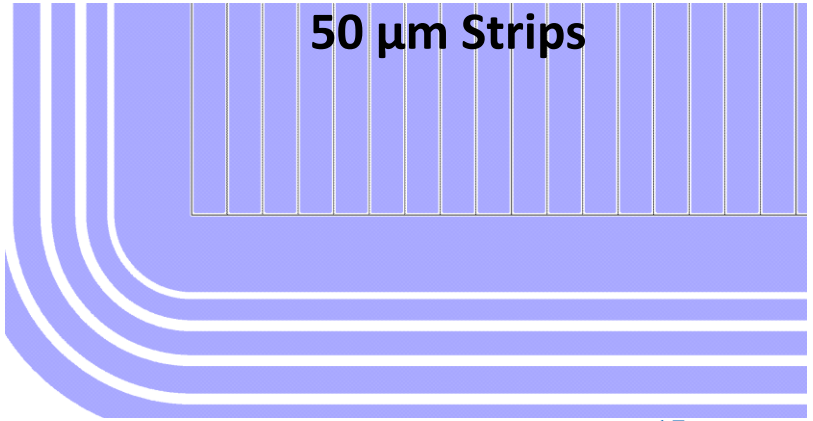
Pitch	NxM	AA Size
250 um	1 x 2	250x500
250 um	4 x 4	1000 x 1000
55 um	20 x 20	1100 x 1100
100 um	30 x 30	3000 x 3000
75 um	13 x 13	975 x 975
1300 um	2 x 2	2600 x 2600
100 um	20 x 20	2000 x 2000

Strips

Pitch	N Strip	Length	AA Size
50 um	60	3 mm	3000 x 3000
100 um	30	3 mm	3000 x 3000







Conclusions

- First Samples of Trench-isolated LGAD have been successfully produced at FBK
- Preliminary electrical measurements showed the expected behavior in terms of knee Voltage, BD voltage, and IV-CV shapes
- Numerical simulations showed that TI-LGAD could potentially reduce the gain-loss region to less than 10 µm.
- TI-LGAD RD50 project is still ongoing. New samples will be available by June 2020.

FONDAZIONE
BRUNO KESSLER

Thank you for your attention!

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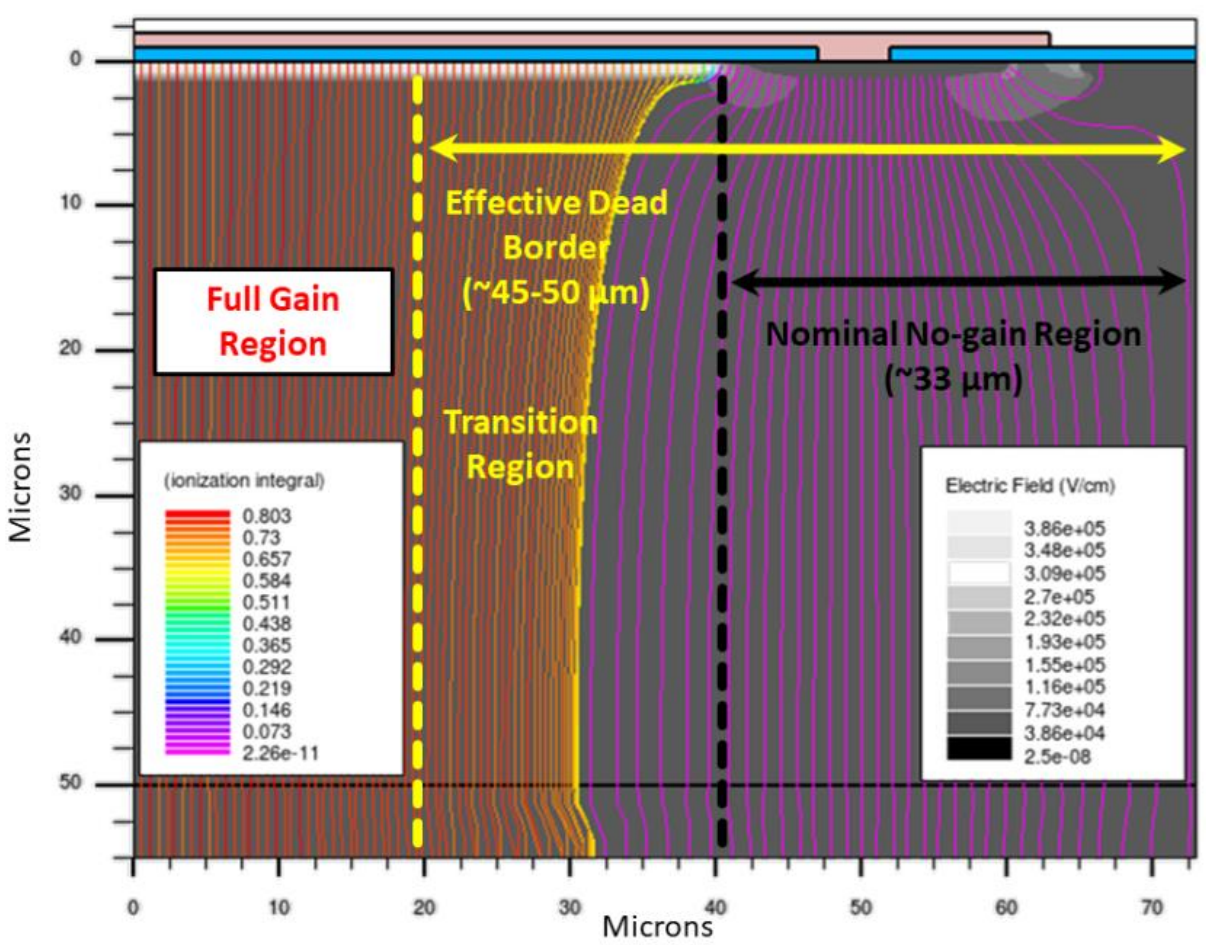
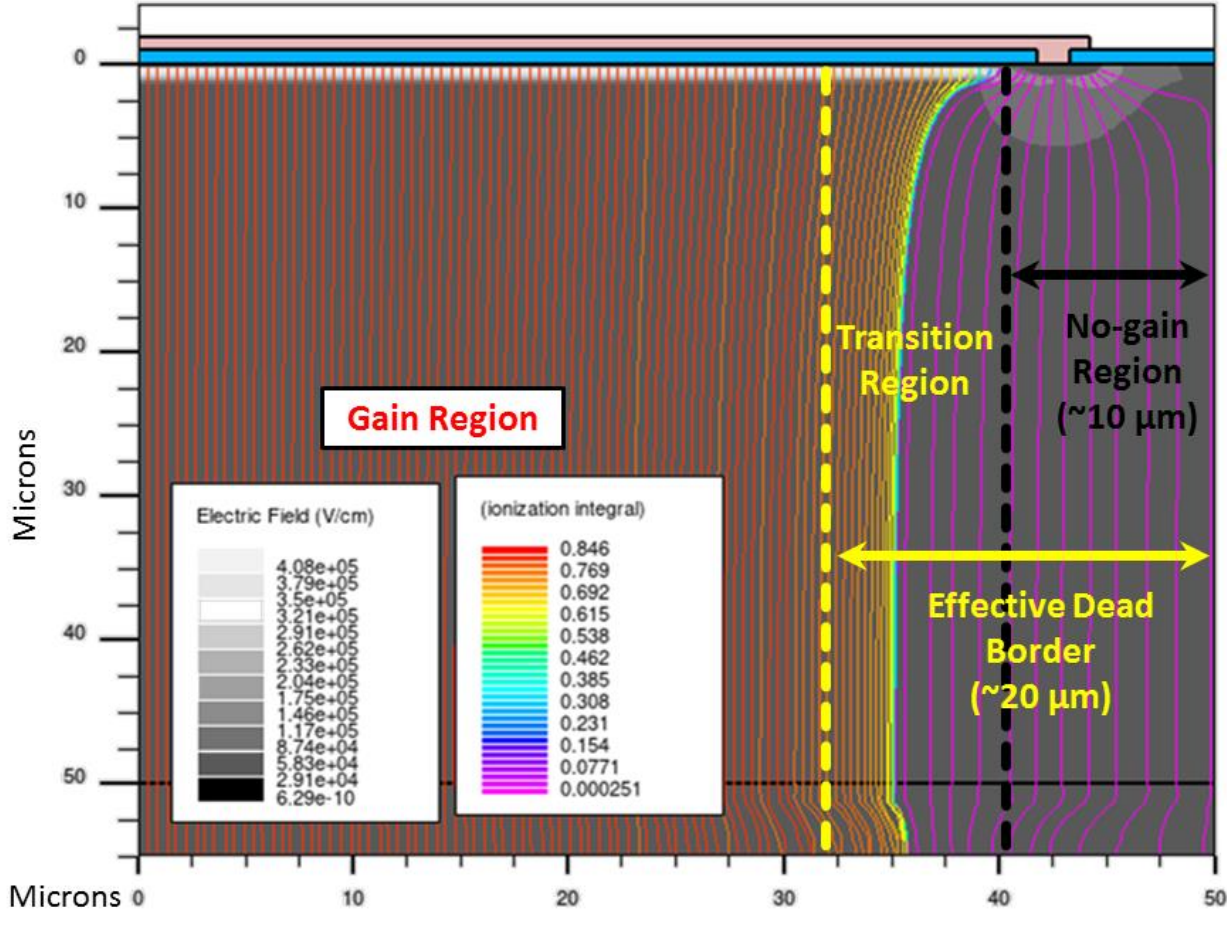
di Fisica Nucleare

We warmly thank the UFSD Torino group: R. Arcidiacono, N. Cartiglia, M. Costa, M. Ferrero, M. Mandurrino, F. Siviero, V. Sola, A. Staiano, M. Tornago for their contribution to the measurements and to the technology development

LGAD – The Segmentation Issue: Fill Factor Loss





TCAD simulation of the pixel border in a UFSD2 structure (left) and UFSD3-intermediate structure (right)