Science & Technology Facilities Council

UK Research and Innovation

Radiation damage investigation of epitaxial P-type Silicon using Schottky diodes and pn junctions

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Overview

- Project description and goals
- Design and layouts of devices
- Initial TCAD simulations
- Fabrication updates
- Test and characterization plans

Project description and goals

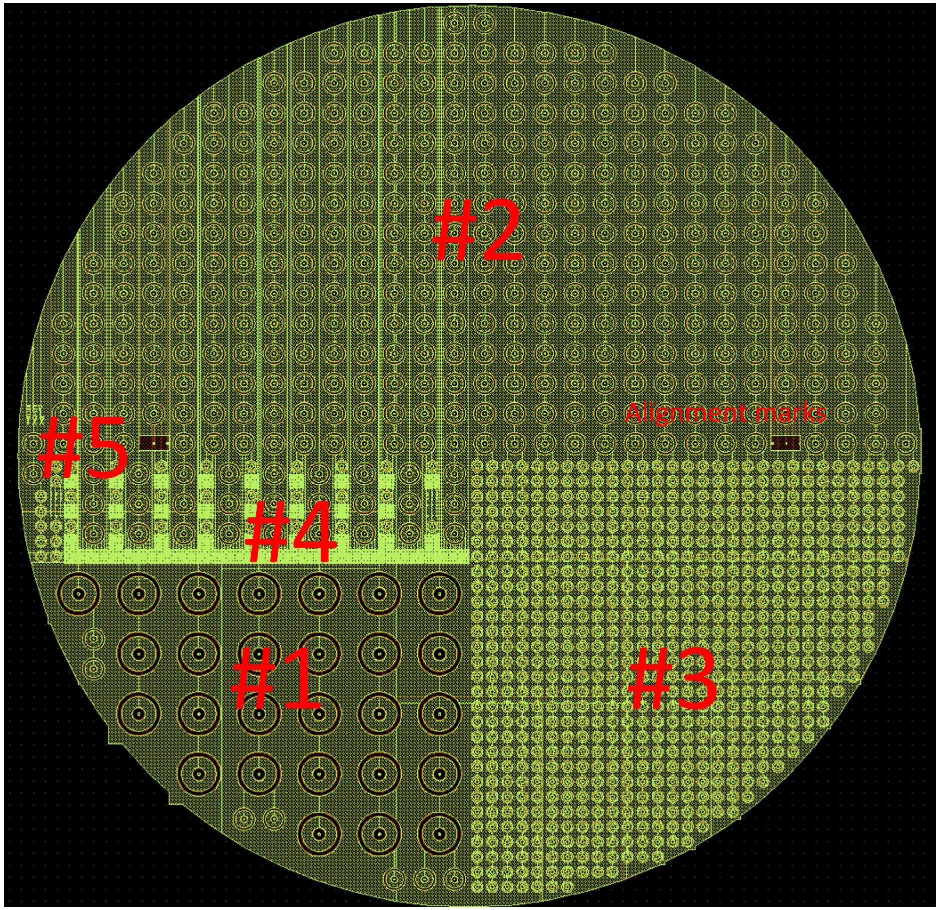
1. RAL PPD, UK
2. IHEP, China
3. JSI, Slovenia
4. Carleton University, Canada
5. University of Birmingham, UK

What: To fabricate a number of Schottky and n^+p diodes on p-type epitaxial (50µm thick) silicon wafers, of doping concentrations as they are normally found in CMOS MAPS devices

Why: The purpose is to investigate and gain a deeper understanding of radiation bulk damage in CMOS sensors. Also with a view to developing reliable damage models that can be implemented in TCAD device simulators (Synopsys or Silvaco)

How: We will purchase 6 inch wafers, 25 x 5 B-doped epitaxial levels (10^{13}, 10^{14}, 10^{15}, 10^{16} and 10^{17} cm^{-3}), total **125 wafers**. The fabrication process will happen both at ITAC (RAL) and Carleton University Microfabrication Facility (CUMFF). Tests will be carried out at RAL, Birmingham, JSI, CUMFF, IHEP.
The remaining wafers, upon agreement, could be distributed among other groups and/or RD50 institutes interested in participating in this project, whether at device design and/or at device test level

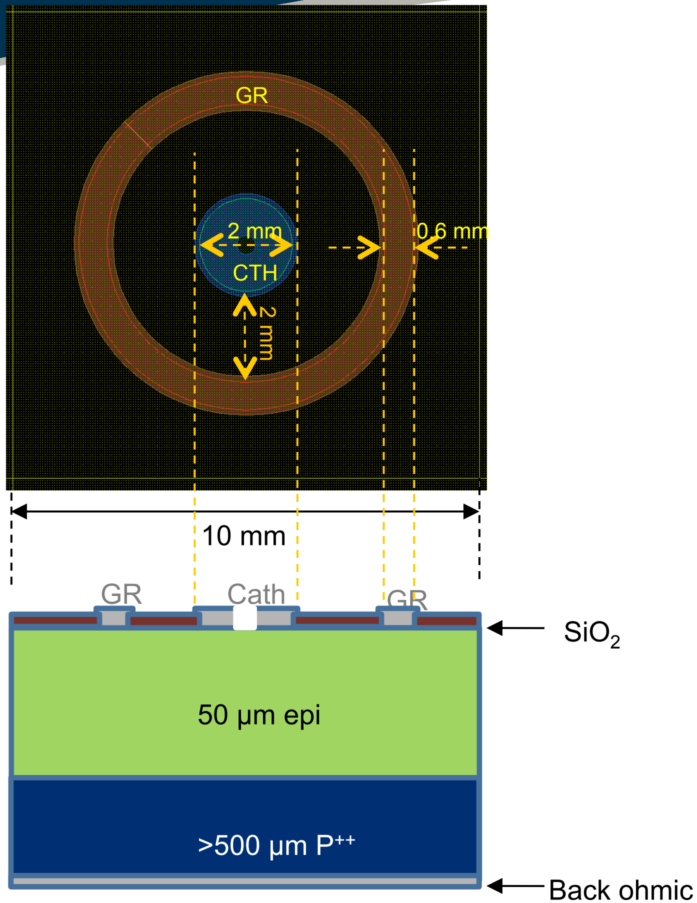
Design and layouts of devices

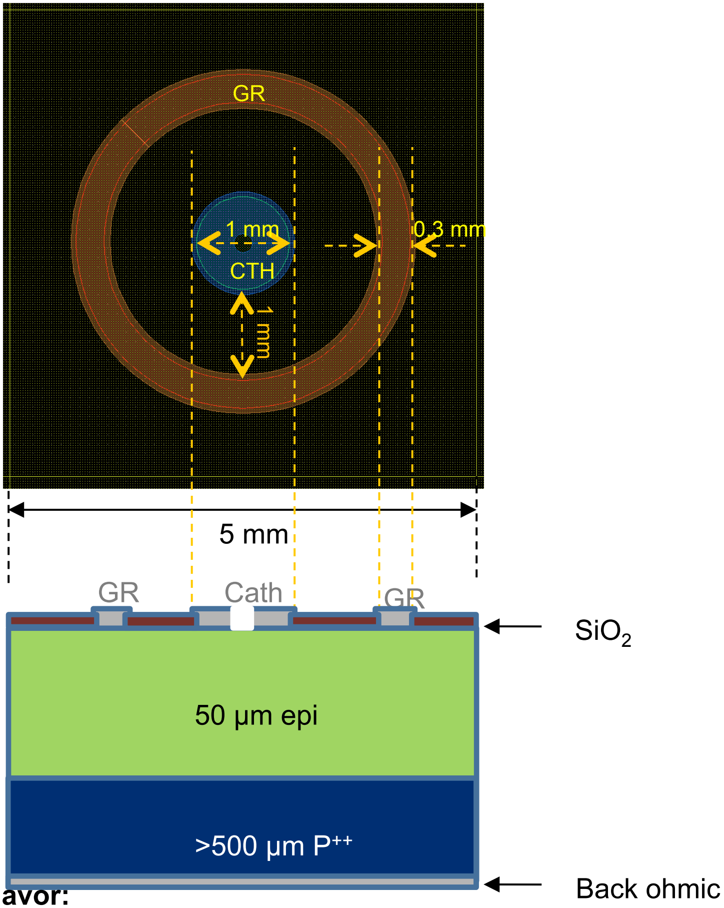


6 '' wafer:

5 type of devices proposed:

- **#1**: 2 mm ∅ cathode with 0.4 mm ∅ central hole, device inside a 10 x 10 mm2 area
  IV,BV, CV, Laser injection test
- **#2**: 1 mm ∅ cathode, 0.2 mm ∅ central hole device inside a 5 x 5 mm2 area
  IV,BV, CV, MIP Laser injection test
- **#3**: 0.5 mm ∅ cathode, no central hole device inside a 2.5 x 2.5 mm2 area
  IV,BV, CV, MIP injection & TCAD comparison
- **#4**: 0.1 mm ∅ cathode, no central hole device inside a 0.5 x 0.5 mm2 area
  IV,BV, CV, MIP injection & TCAD comparison
- 'cell' with the previous 3 flavors (2,3,4) grouped together, to exploit wafer uniformity on small area
- #5: 6 TLM points for contact and epi resistance
- 2 masks only (metal and oxide)



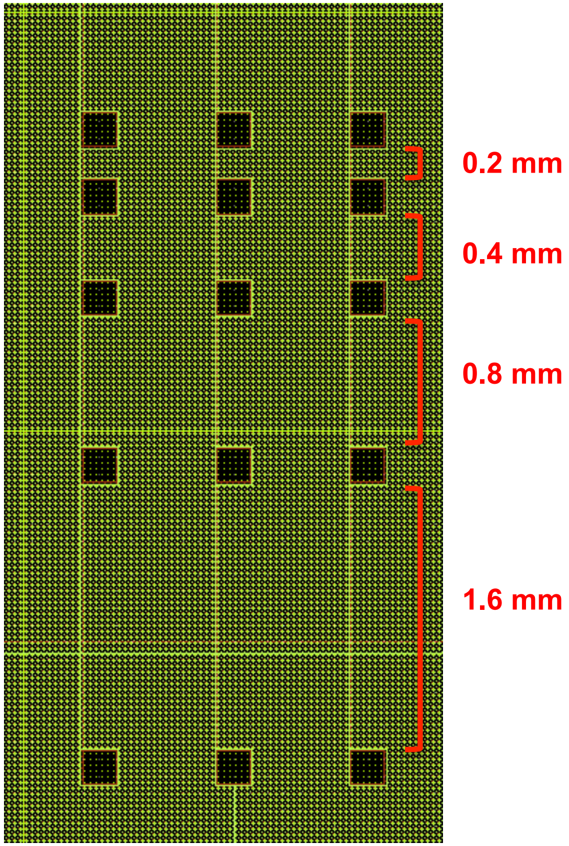


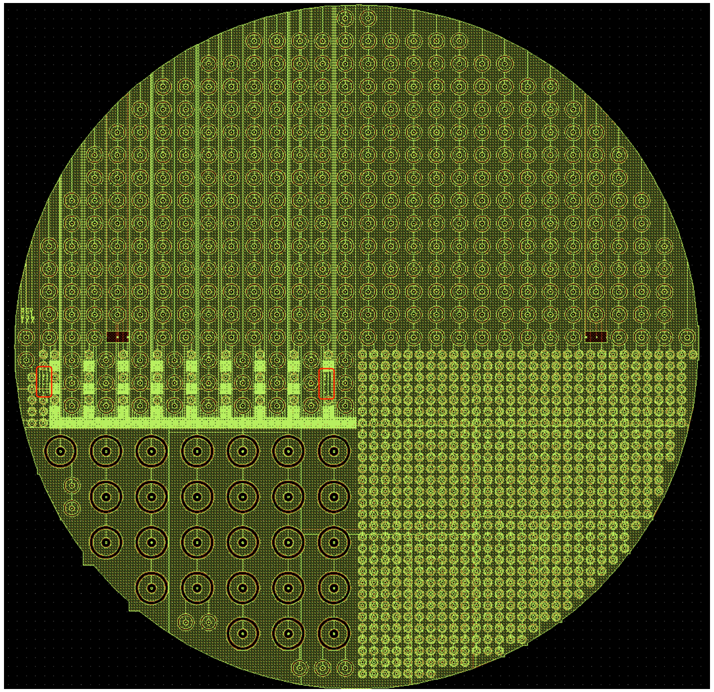
#1 Flavor:

- 10x10 mm^2 device area
- 1 mm cathode diameter (Al)
- Central hole 0.4 mm diameter
- Guard ring (Al) 2 mm from cathode
- Laser injection possible through the central hole and vertically, along the line from cathode to guard ring

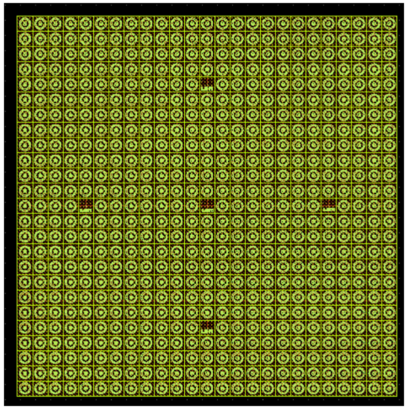
#2 Flavor:

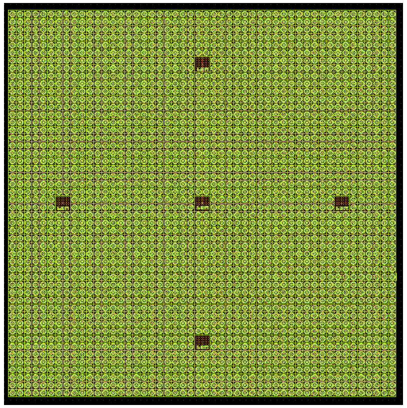
- 5x5 mm^2 device area
- 1 mm cathode diameter (Al)
- Central hole 0.2 mm diameter
- Guard ring (Al) 1 mm from cathode
- Laser injection possible through the central hole and vertically, along the line from cathode to guard ring

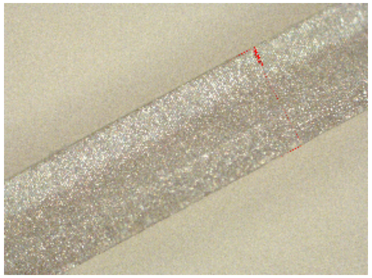




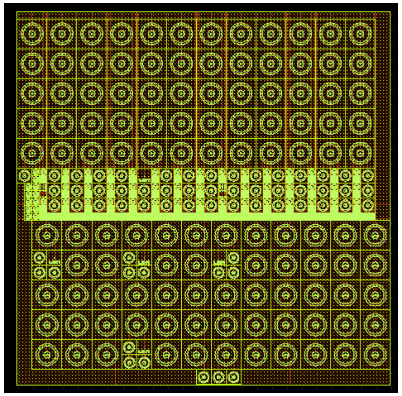
- 2 x 3 TLM points for contact and epi resistance

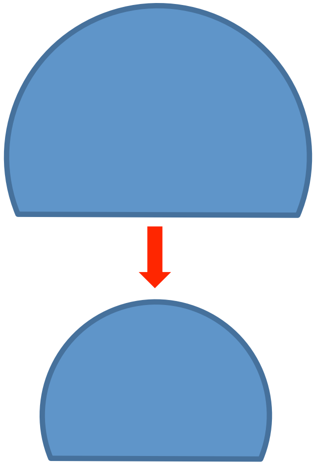






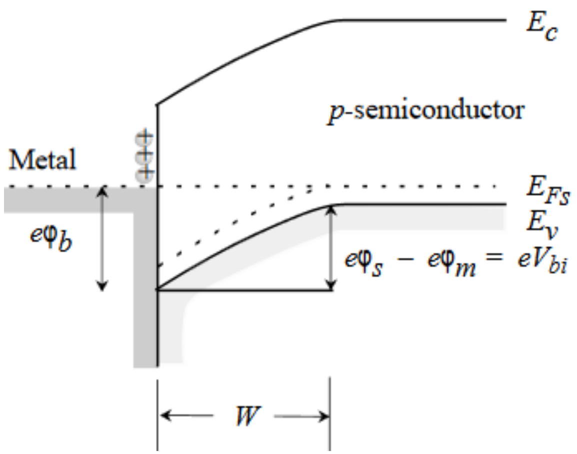
top-down view of a laser cut

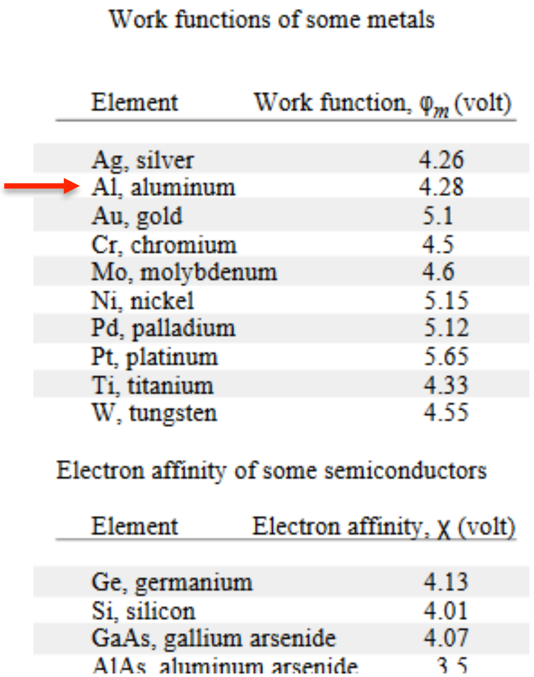




- Some of the wafers have to be laser trimmed at RAL from 6 inch to 4 inch for processing at CUMFF
- They include the same flavours as per 6 inch wafers and will have n diffusion to make PN junctions, a process already well developed at CUMFF

Initial TCAD simulations



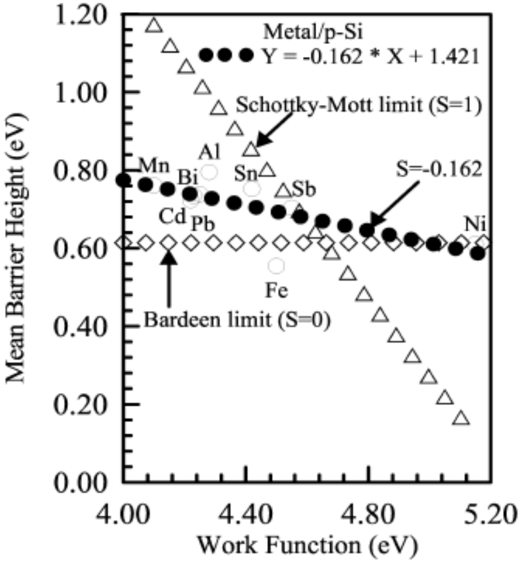


Work functions of some metals

Element	Work function, φ_m (volt)
Ag, silver	4.26
Al, aluminum	4.28
Au, gold	5.1
Cr, chromium	4.5
Mo, molybdenum	4.6
Ni, nickel	5.15
Pd, palladium	5.12
Pt, platinum	5.65
Ti, titanium	4.33
W, tungsten	4.55

Electron affinity of some semiconductors

Element	Electron affinity, χ (volt)
Ge, germanium	4.13
Si, silicon	4.01
GaAs, gallium arsenide	4.07
AlAs, aluminum arsenide	3.5

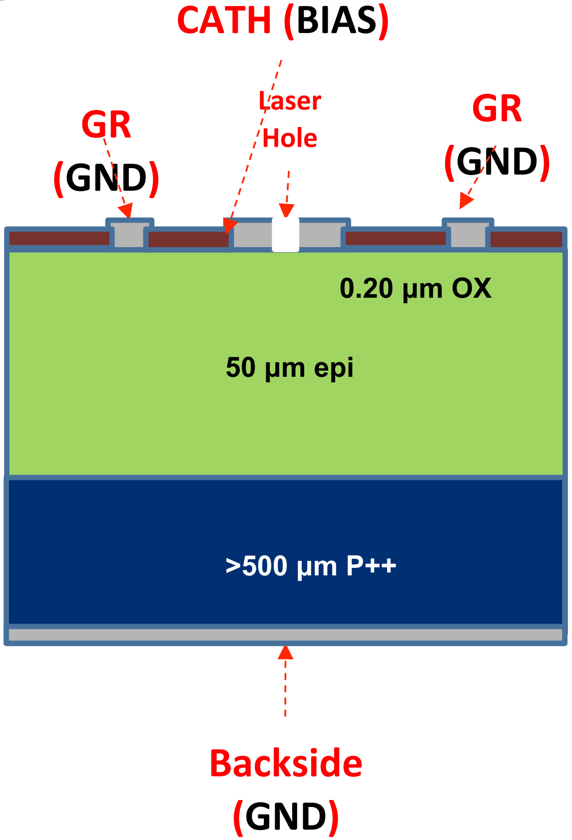


$$\phi_b = S(E_S - \phi_m) + (1 - S)\phi_{cnl},$$

On P-type Si a metal with low Φ_m is needed to have high Schottky barrier

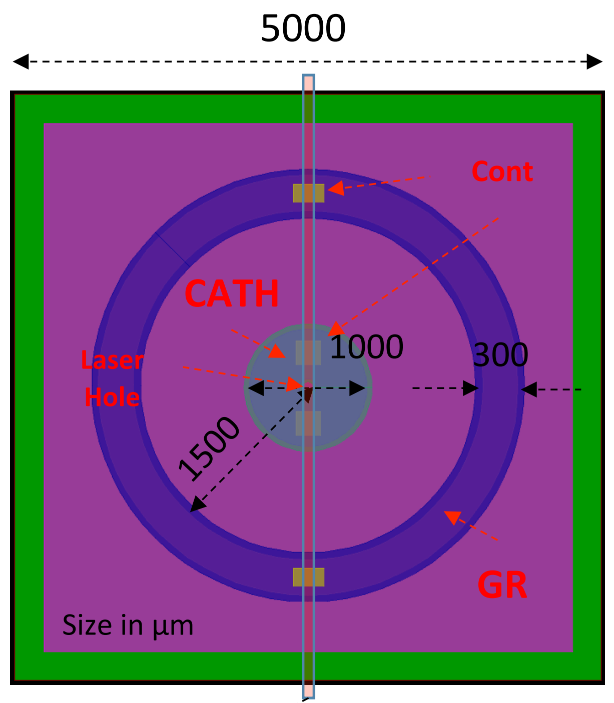
- Al seems to guarantee highest barrier height
- A real Schottky barrier will include effects due to surface states (Fermi pinning)
- Fermi pinning depends on density of surface states, very technology dependent

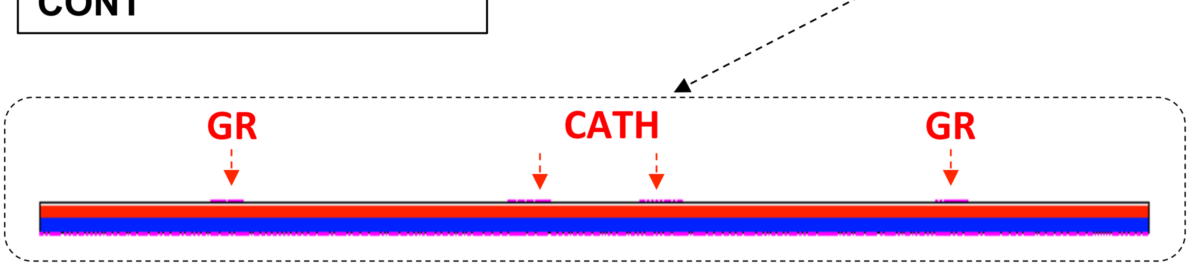
Process SIM



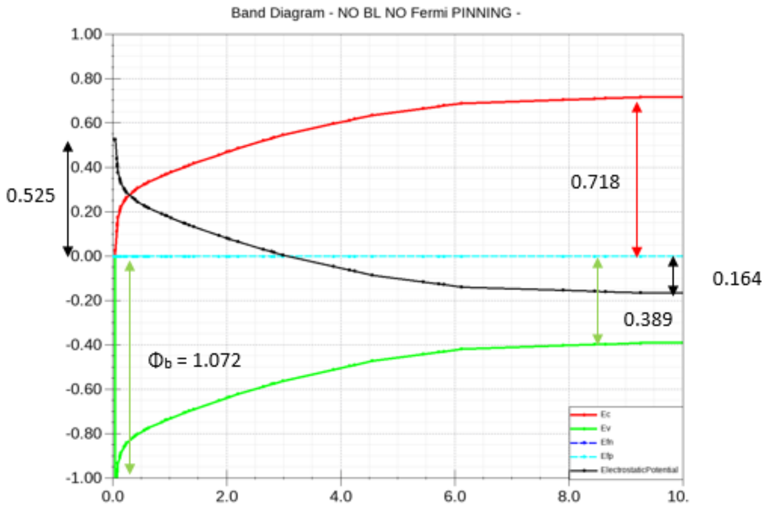
SUBS
↓
EPITAX
↓
OXID
↓
ETCH – M DEP
↓
CONT

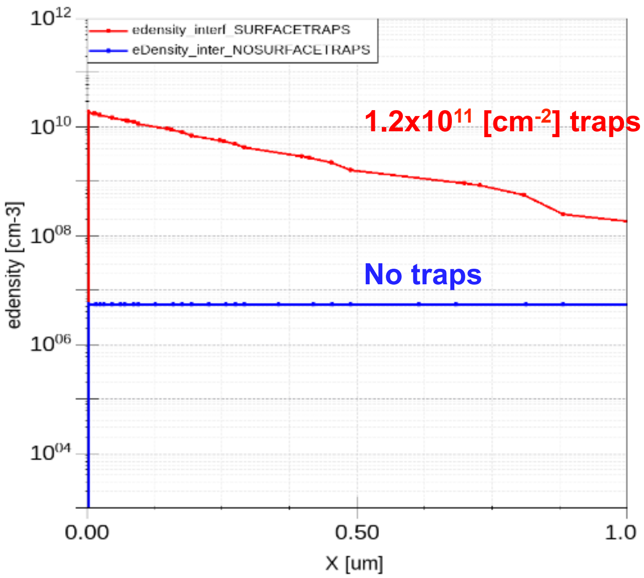
Small width 3D simulated section: 10^{-3} x 5 mm^2





- TCAD simulation on a 3D section of the above device



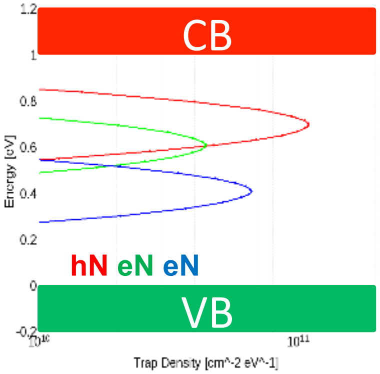


- From Al and Si {100} parameters:

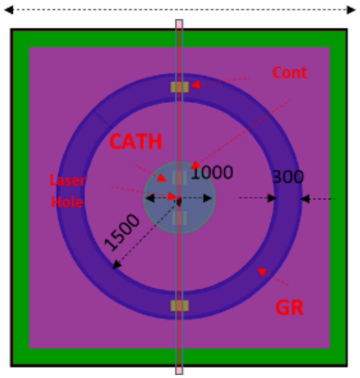
$\Phi(Al) = 4.1$ [eV], $\chi(Si)=4.05$ [eV] -> $\Phi_b=1.16-(4.1-4.05) = \mathbf{1.11}$

$V_D = \Phi_b - (E_F - E_V)/q = 1.11 - 0.389 = \mathbf{0.721}$

- Effects of interface traps on e- density
- All TCAD simulations assume T = 300 K and surface states as above (1.2 x 10^{11} ST , 10^{11} OxINT)

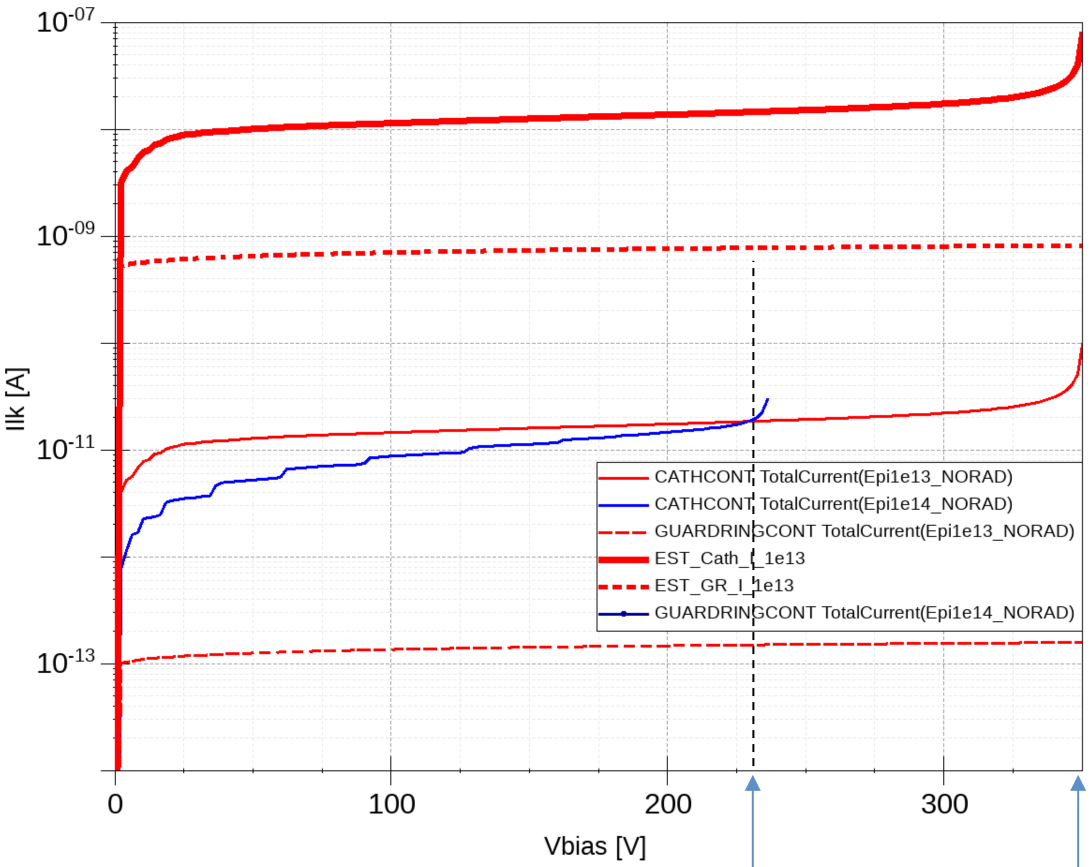


Interface Defect	Level	Concentration	σ
Acceptor	E_C-0.4 eV	40% of acceptor N_{IT} ($N_{IT}=0.85 \cdot N_{OX}$)	0.07 eV
Acceptor	E_C-0.6 eV	60% of acceptor N_{IT} ($N_{IT}=0.85 \cdot N_{OX}$)	0.07 eV
Donor	E_V+0.7 eV	100% of donor N_{IT} ($N_{IT}=0.85 \cdot N_{OX}$)	0.07 eV



Cathode ratio: ~ **785**

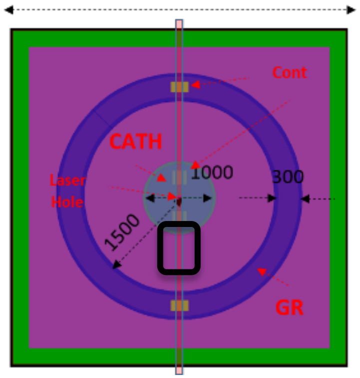
GR ratio: ~ **5183**

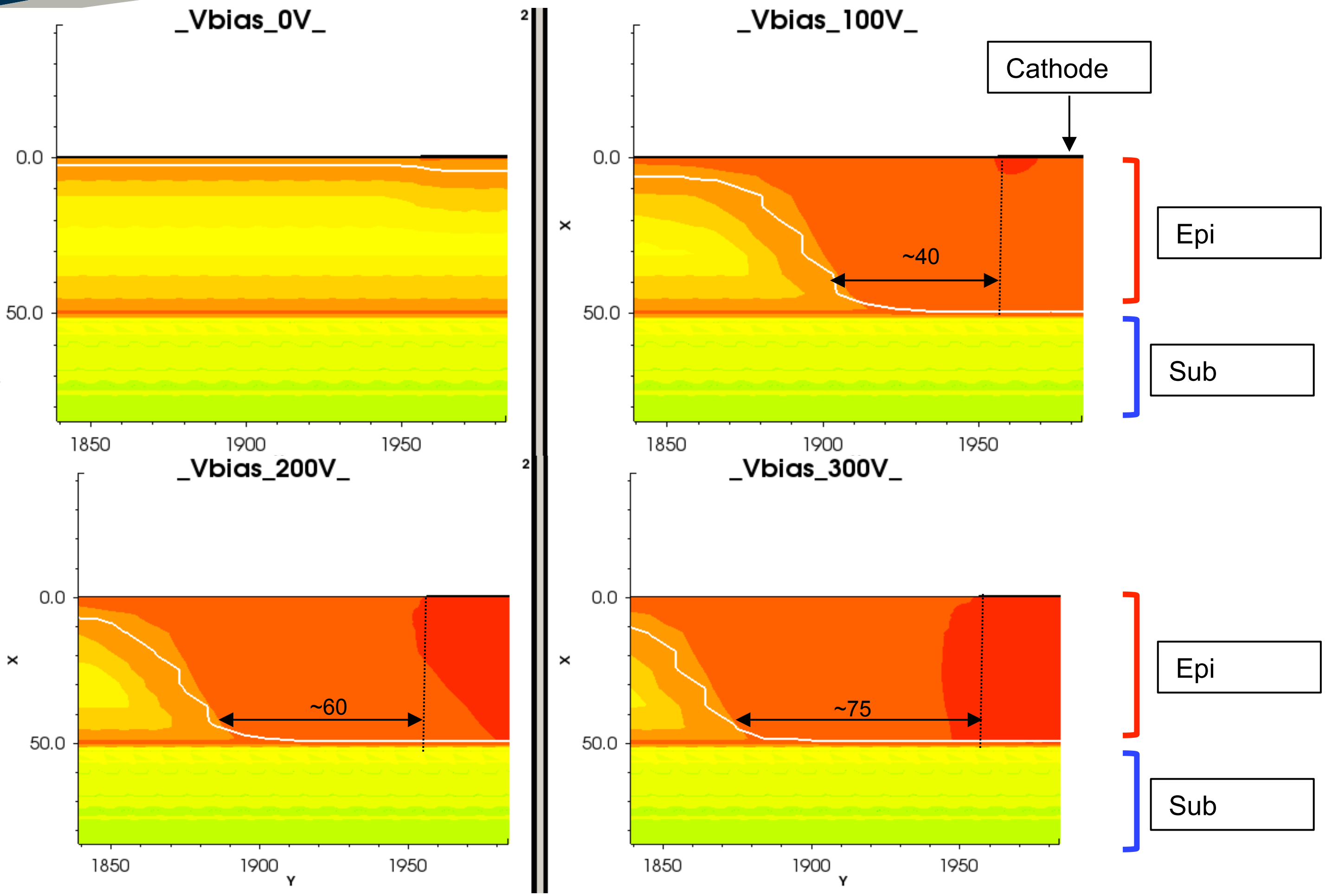


BV 10^{14} [cm^{-3}]

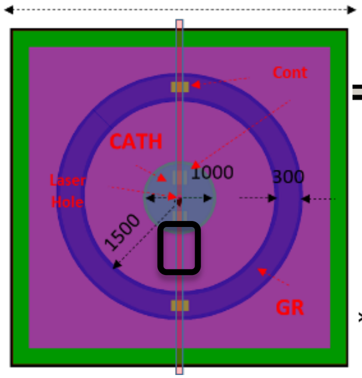
BV 10^{13} [cm^{-3}]

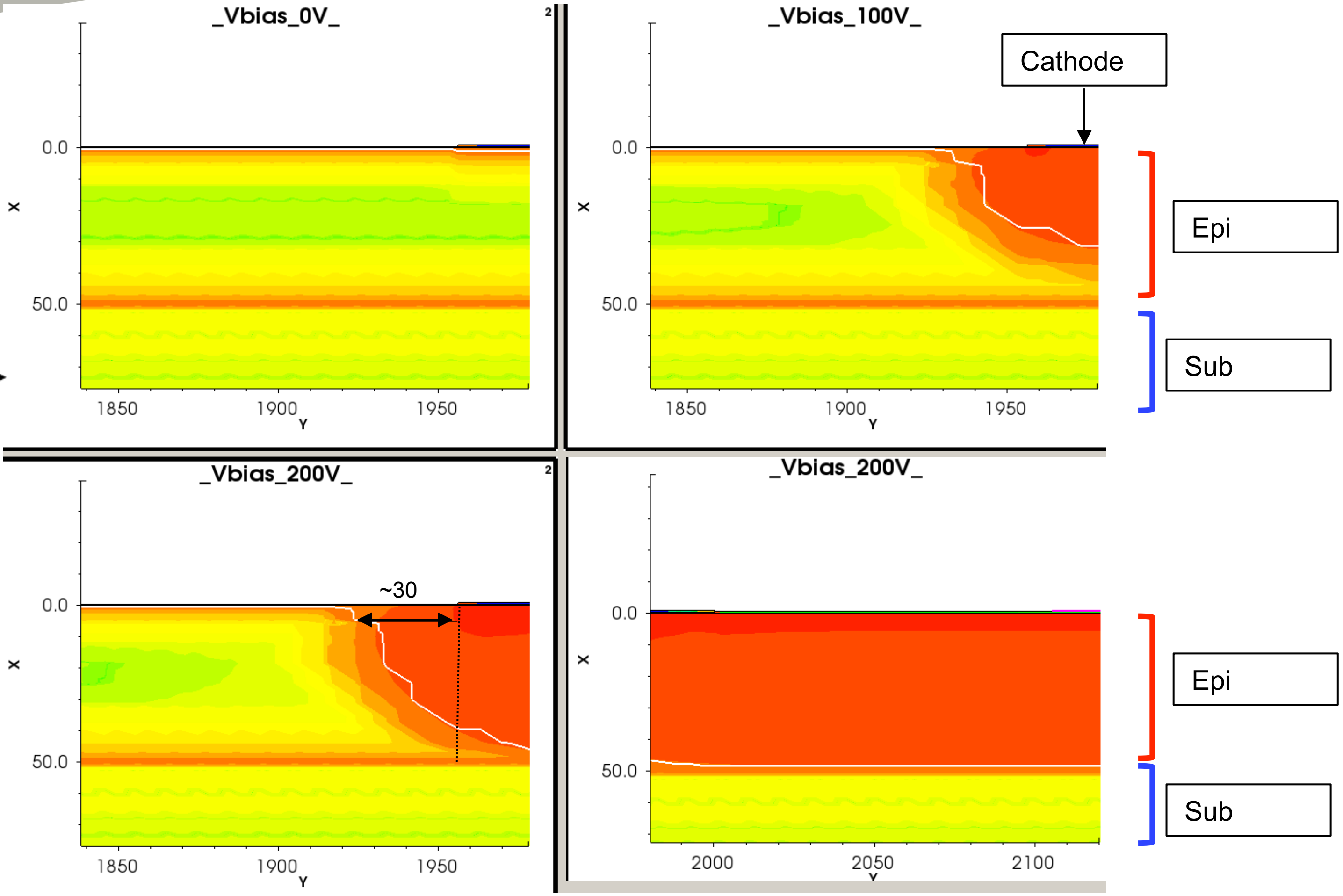
- IV plots up to BV for 10^{13}, 10^{14} cm^{-3} epi doping
- Estimated total leakage current of Cathode and GR from area factor



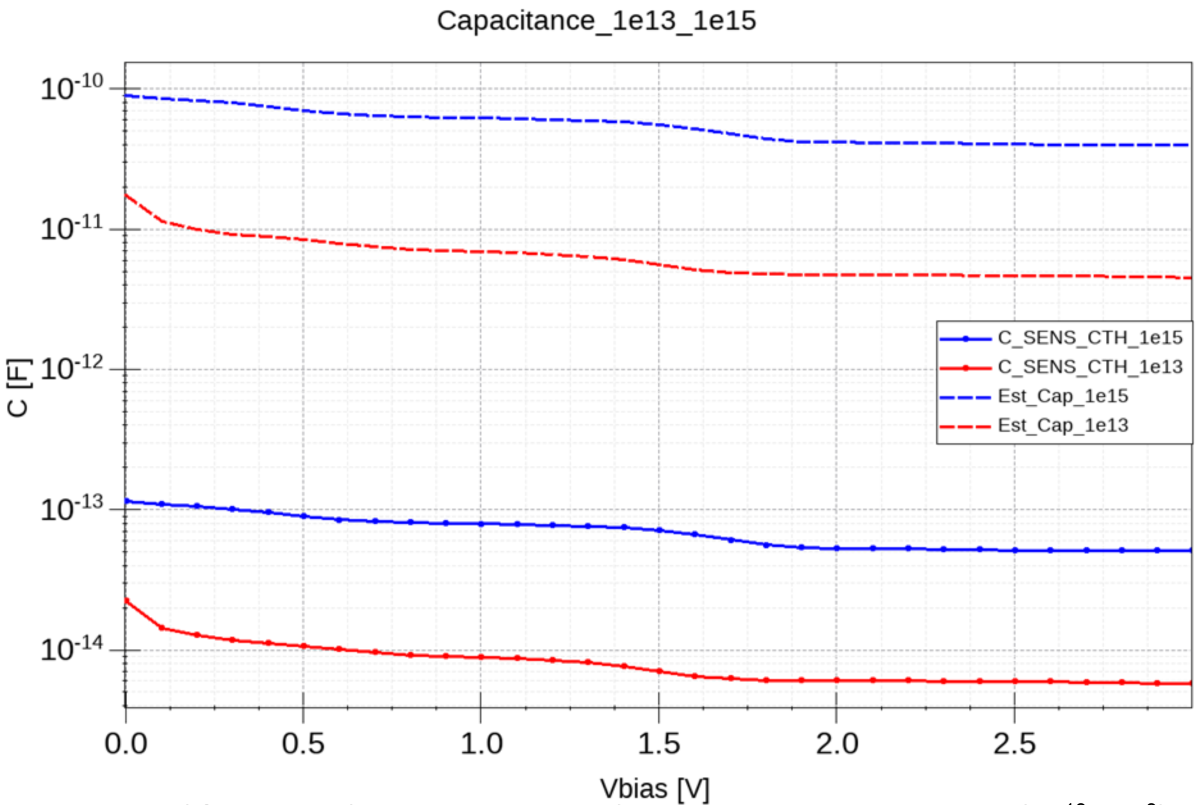


- Lateral depletion extension @ different biases 10^{13} [cm^{-3}] epi doping
- Adequate lateral extension for laser test (sizes in μm)



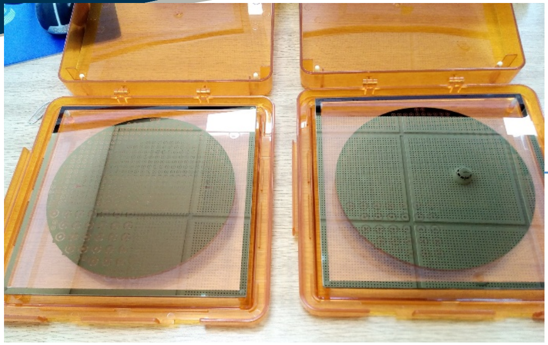


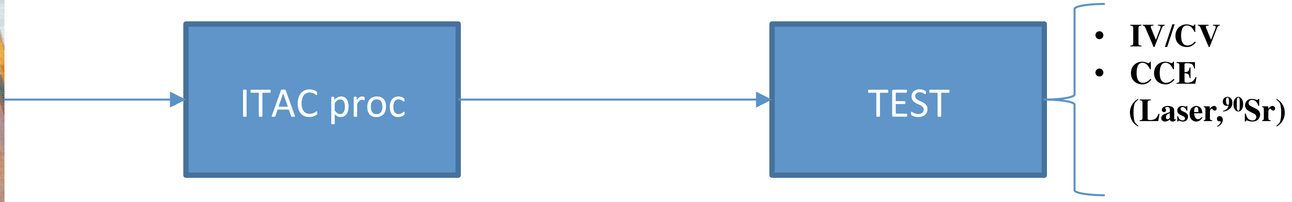
- Lateral depletion extension @ different biases 10^{14} [cm^{-3}] epi doping
- Smaller lateral extension for laser test ((sizes in μm), but still full depletion of epi before BV



- A minimum of around **3-4** pF (@ 100 kHz) can be assumed for the lowest doping device (10^{13} cm^{-3}) at nominal biasing (100V, to achieve overdepletion)
- For a 50µm thick epi , a MIP should give an average of 4000 + 500 (subs) or around 0.7 fC. On a 1pF capacitance that should give around 700µV of voltage drop.
- For example, using the A250CF charge amplifier, 113 e- RMS noise AC coupled, plus additional noise sources, around 120 e rms would be equivalent to around 2.6% noise on the MIP induced signal for non-irradiated device (we will need a proper shaper)

Fabrication updates

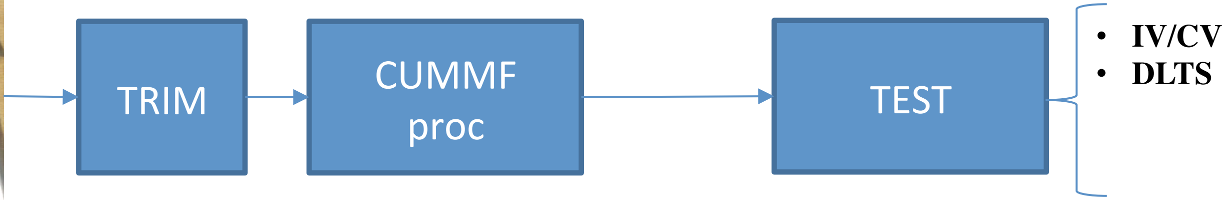




ITAC proc

TEST

- **IV/CV**
- **CCE (Laser,^{90}Sr)**



TRIM

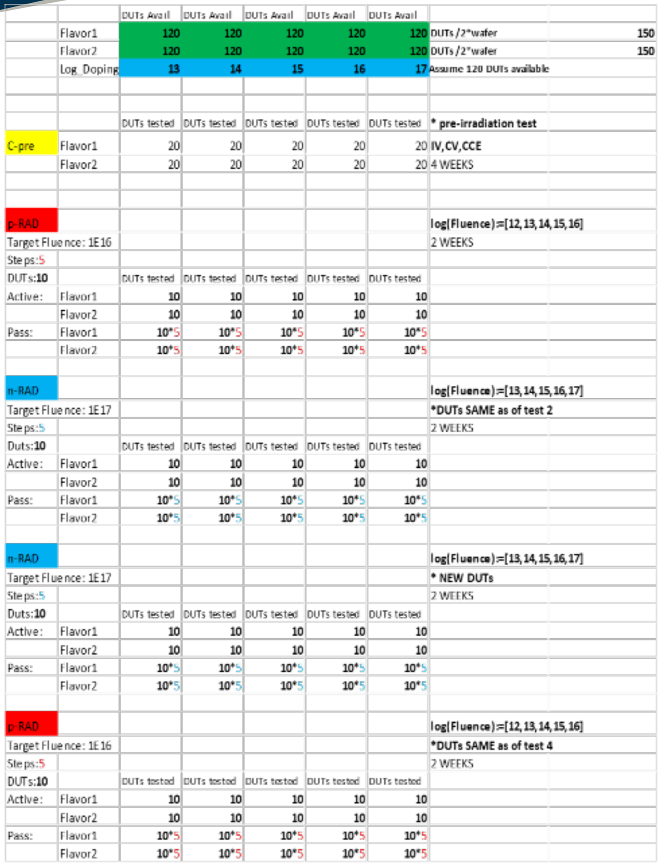
CUMMF proc

TEST

- **IV/CV**
- **DLTS**

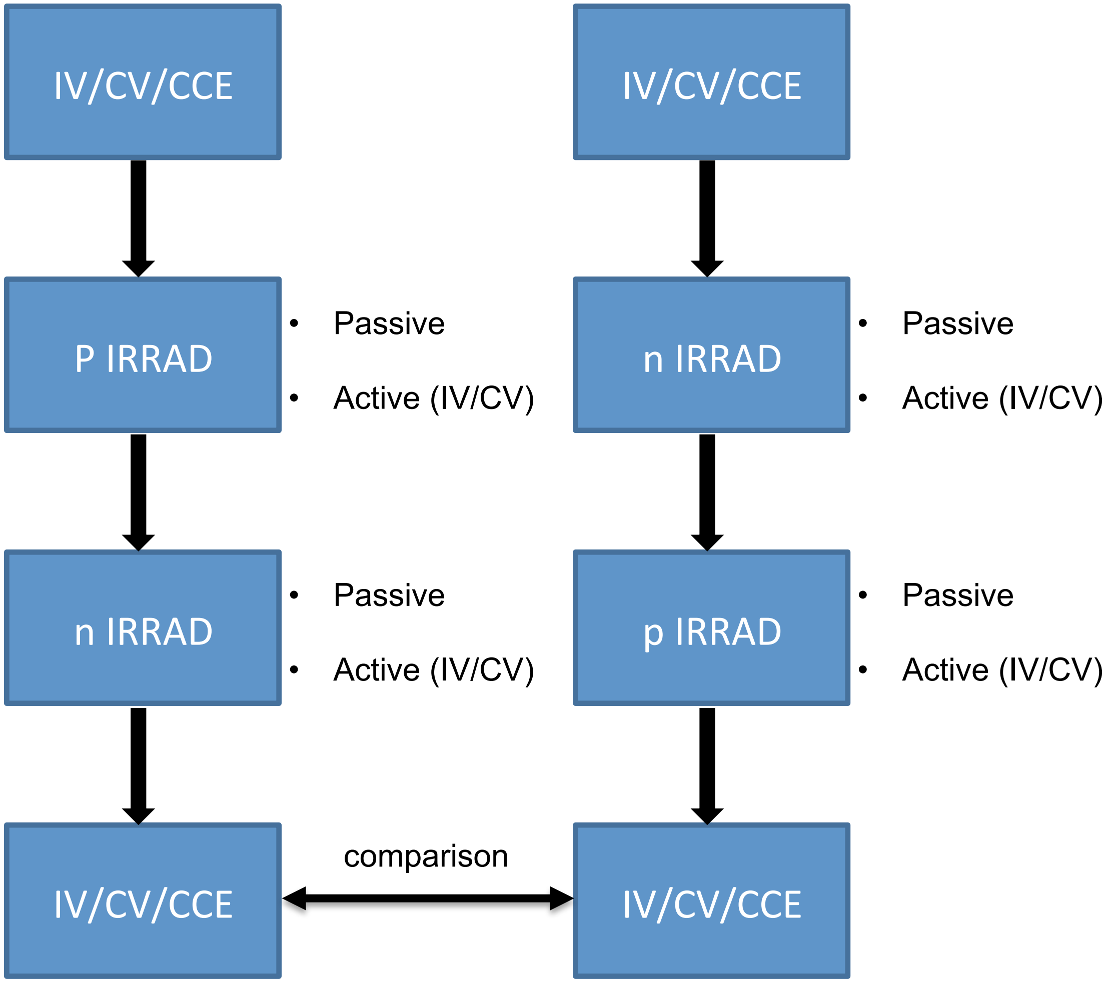
- All masks have arrived to RAL (Nov 19)
- Fabrication process on initial HR wafers planned for Dec 2019, ITAC-CUMFF
- Tests (IV/CV/CCE [Laser and ^{90}Sr]) will be done at RAL, CUMFF, IHEP
- DLTS defect investigation setting up at CUMFF/RAL. Sharing of devices if interested groups

Tests and characterization plans



		DUTs Avail	DUTs Avail	DUTs Avail	DUTs Avail	DUTs Avail		
	Flavor1	120	120	120	120	120	DUTs /2*wafer	150
	Flavor2	120	120	120	120	120	DUTs /2*wafer	150
	Log_Doping	13	14	15	16	17	Assume 120 DUTs available	
		DUTs tested	DUTs tested	DUTs tested	DUTs tested	DUTs tested	* pre-irradiation test	
C-pre	Flavor1	20	20	20	20	20	IV,CV,CCE	
	Flavor2	20	20	20	20	20	4 WEEKS	
p-RAD							log(Fluence):=[12,13,14,15,16]	
Target Fluence: 1E16							2 WEEKS	
Steps:5								
DUTs:10		DUTs tested	DUTs tested	DUTs tested	DUTs tested	DUTs tested		
Active:	Flavor1	10	10	10	10	10		
	Flavor2	10	10	10	10	10		
Pass:	Flavor1	10*5	10*5	10*5	10*5	10*5		
	Flavor2	10*5	10*5	10*5	10*5	10*5		
n-RAD							log(Fluence):=[13,14,15,16,17]	
Target Fluence: 1E17							*DUTs SAME as of test 2	
Steps:5							2 WEEKS	
Duts:10		DUTs tested	DUTs tested	DUTs tested	DUTs tested	DUTs tested		
Active:	Flavor1	10	10	10	10	10		
	Flavor2	10	10	10	10	10		
Pass:	Flavor1	10*5	10*5	10*5	10*5	10*5		
	Flavor2	10*5	10*5	10*5	10*5	10*5		
n-RAD							log(Fluence):=[13,14,15,16,17]	
Target Fluence: 1E17							* NEW DUTs	
Steps:5							2 WEEKS	
Duts:10		DUTs tested	DUTs tested	DUTs tested	DUTs tested	DUTs tested		
Active:	Flavor1	10	10	10	10	10		
	Flavor2	10	10	10	10	10		
Pass:	Flavor1	10*5	10*5	10*5	10*5	10*5		
	Flavor2	10*5	10*5	10*5	10*5	10*5		
p-RAD							log(Fluence):=[12,13,14,15,16]	
Target Fluence: 1E16							*DUTs SAME as of test 4	
Steps:5							2 WEEKS	
DUTs:10		DUTs tested	DUTs tested	DUTs tested	DUTs tested	DUTs tested		
Active:	Flavor1	10	10	10	10	10		
	Flavor2	10	10	10	10	10		
Pass:	Flavor1	10*5	10*5	10*5	10*5	10*5		
	Flavor2	10*5	10*5	10*5	10*5	10*5		

- Synopsis of radiation tests



IV/CV/CCE

P IRRAD

- Passive
- Active (IV/CV)

n IRRAD

- Passive
- Active (IV/CV)

IV/CV/CCE

IV/CV/CCE

n IRRAD

- Passive
- Active (IV/CV)

p IRRAD

- Passive
- Active (IV/CV)

IV/CV/CCE

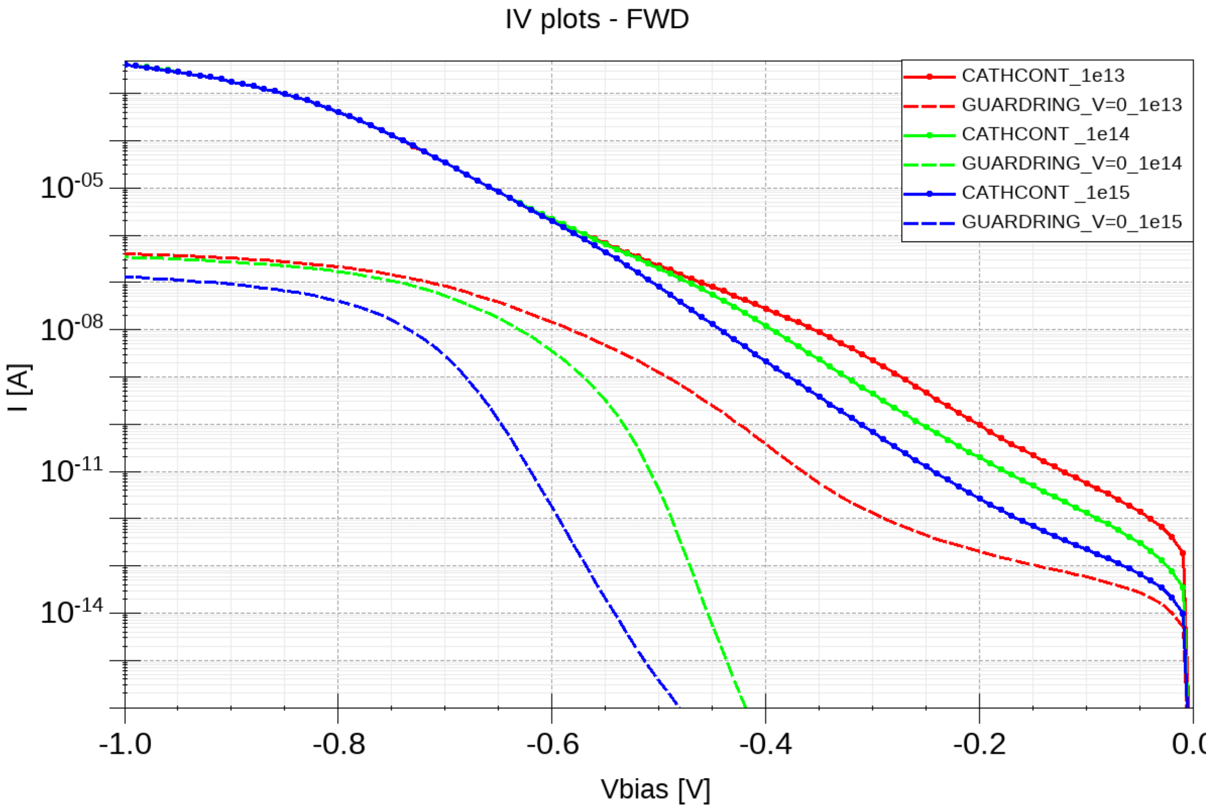
comparison

Conclusion – next steps

- Masks have arrived to RAL. HR wafers 6 inch already available. HR wafers 4 inch will be available next week
- Schottky device fabrication is planned to start at ITAC (RAL) and CUMFF in December 2019 on 2 wafers initially. Preliminary characterization by end of 2019
- Irradiation campaign with neutrons and protons planned for next spring. Devices will be tested online and passively
- Defects investigation using DLTS/TSC at CUMFF [RAL,IHEP] – interested groups please get in touch
- TCAD modelling of processed wafers and including bulk radiation damage for IV/BV/CCE

THANK YOU

BACKUP



- IV in FWD mode
- Barrier height recoverable from log(I) intercept