



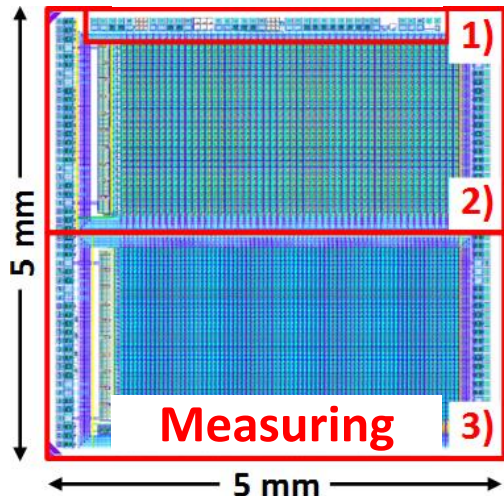
CMOS – Discussion

Eva Vilella

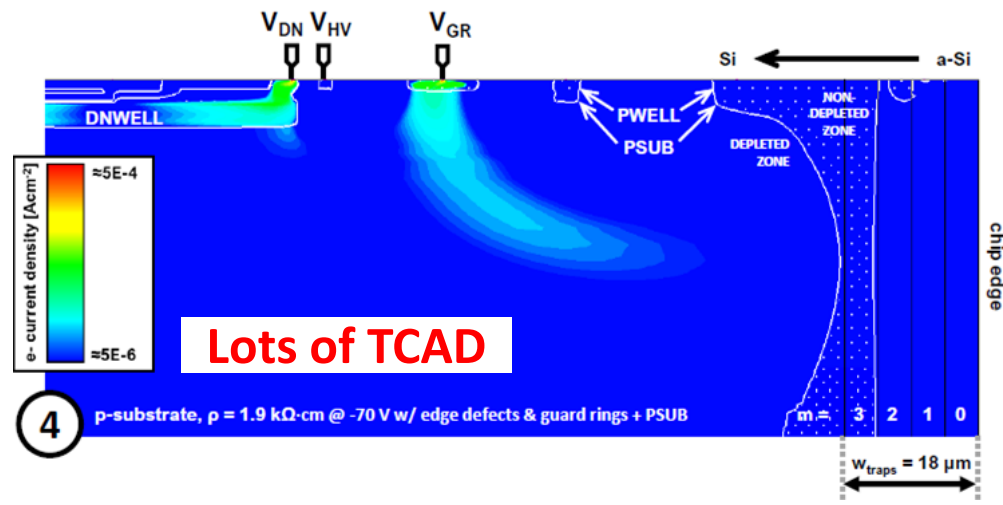
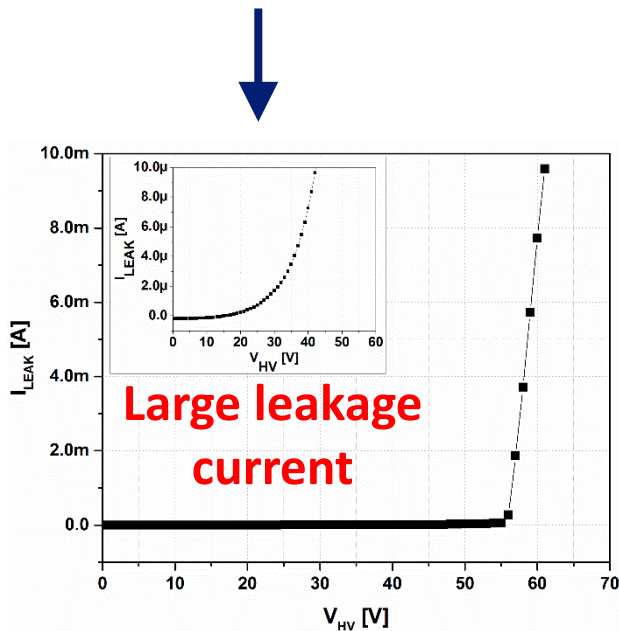
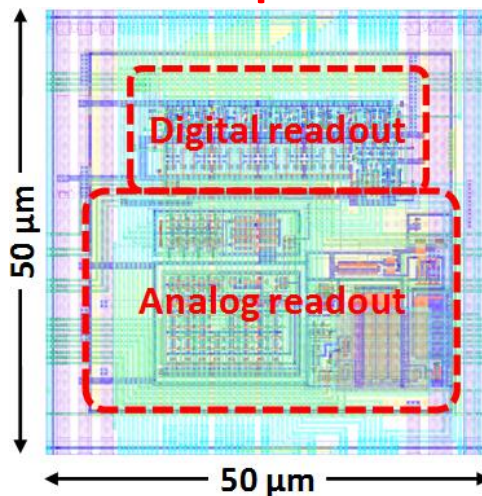
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RD50-MPW1

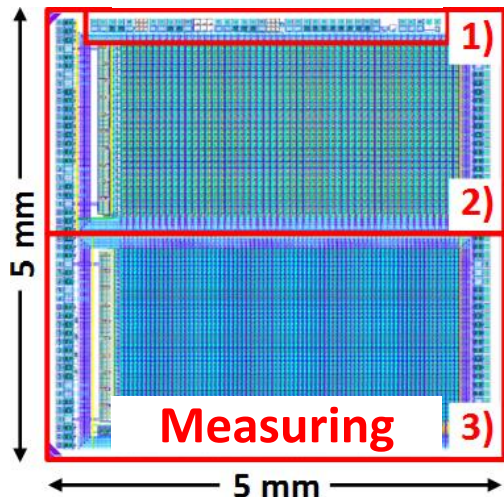


Small pixels

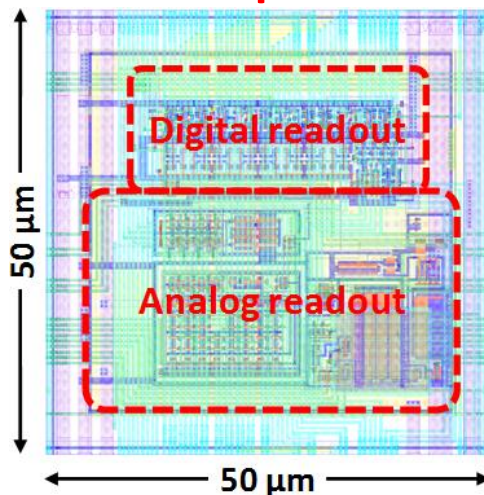




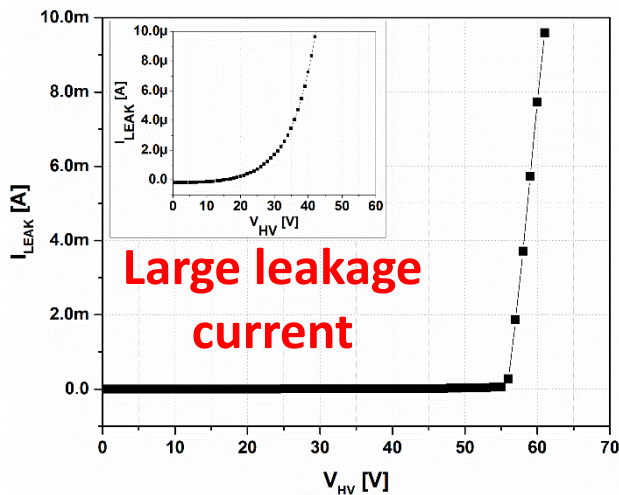
RD50-MPW1



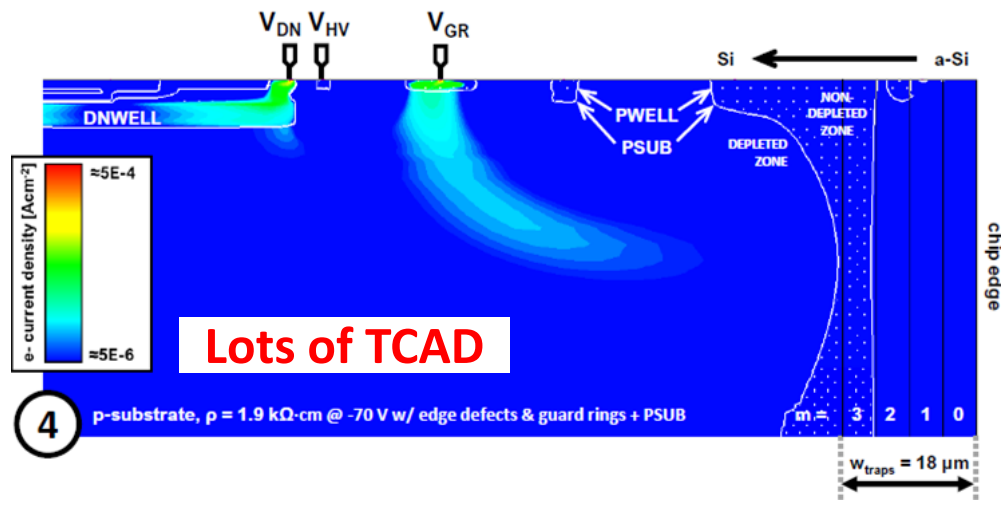
Small pixels



RD50-MPW2



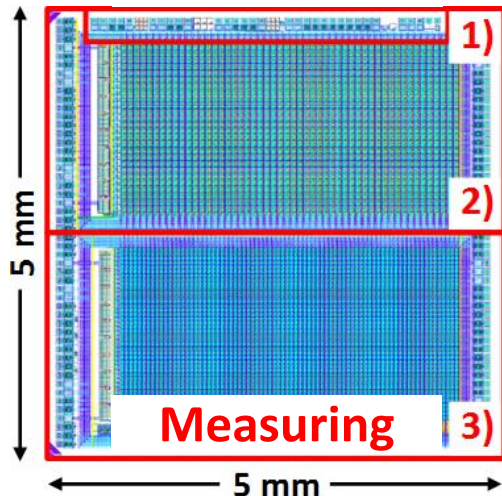
Large leakage current



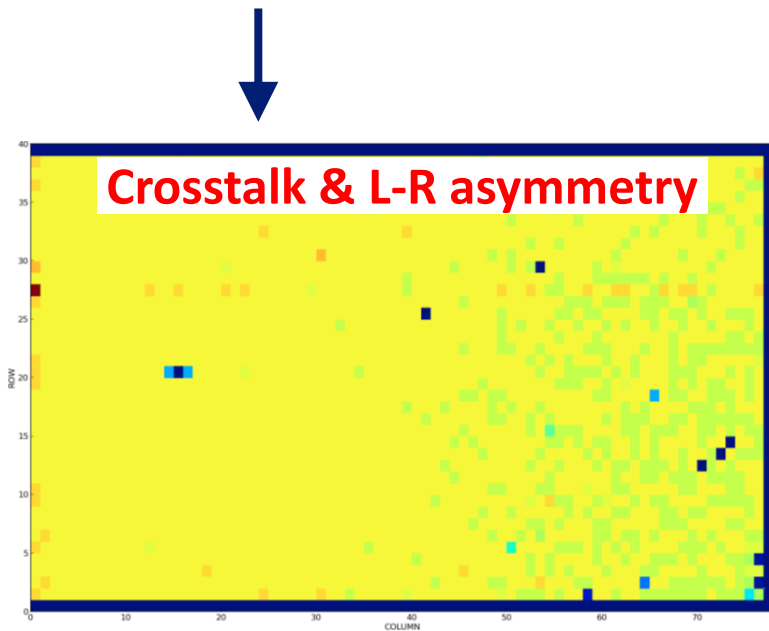
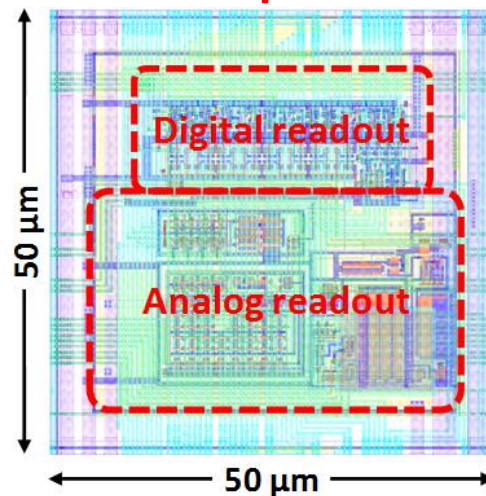
Lots of TCAD



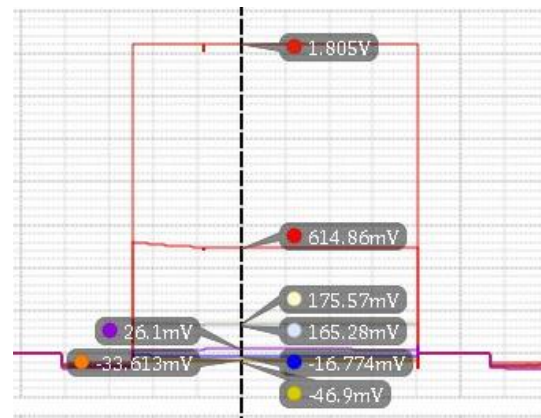
RD50-MPW1



Small pixels

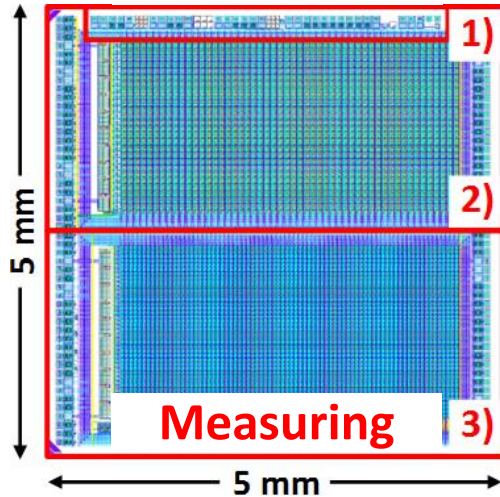


Post-layout simulations

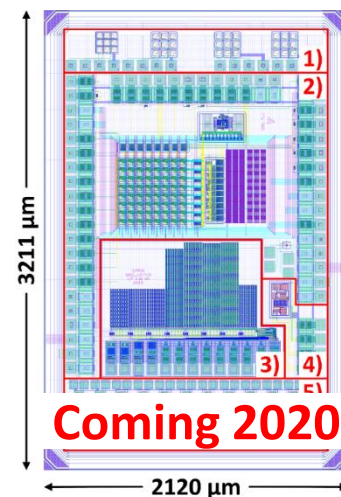




RD50-MPW1



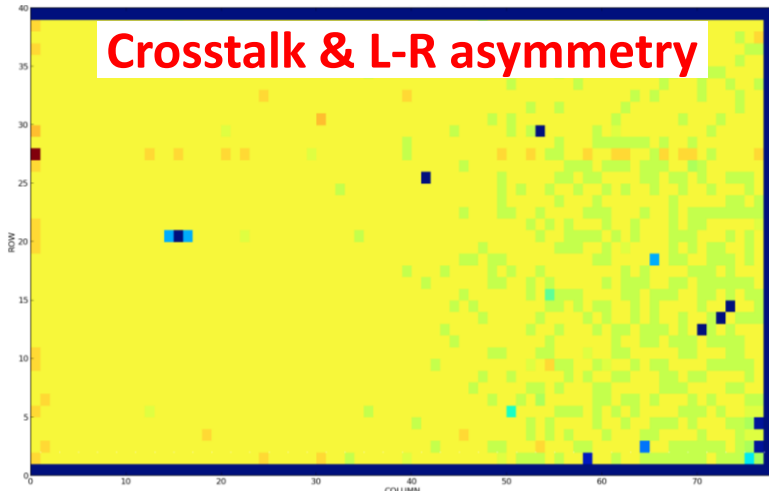
RD50-MPW2



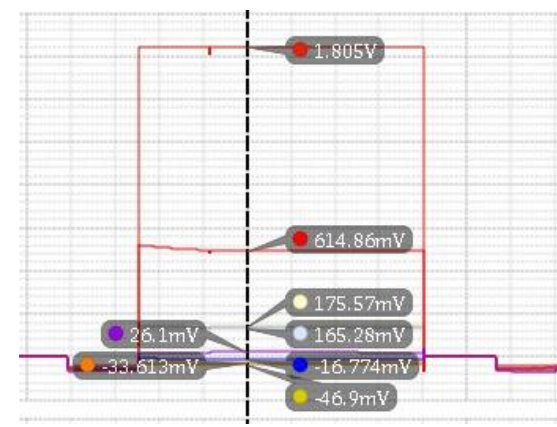
RD50-MPW3

New!

- Small pixels
- Analog + digital RO
- Small I_LEAK
- No crosstalk
- No asymmetries
 - Matrix 1 – FE-I3

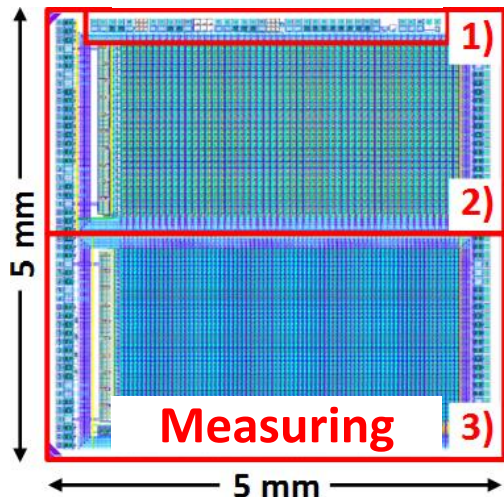


Post-layout simulations

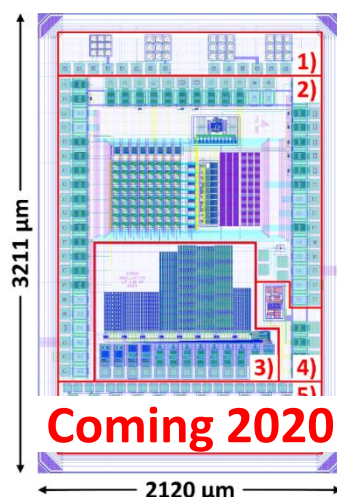




RD50-MPW1



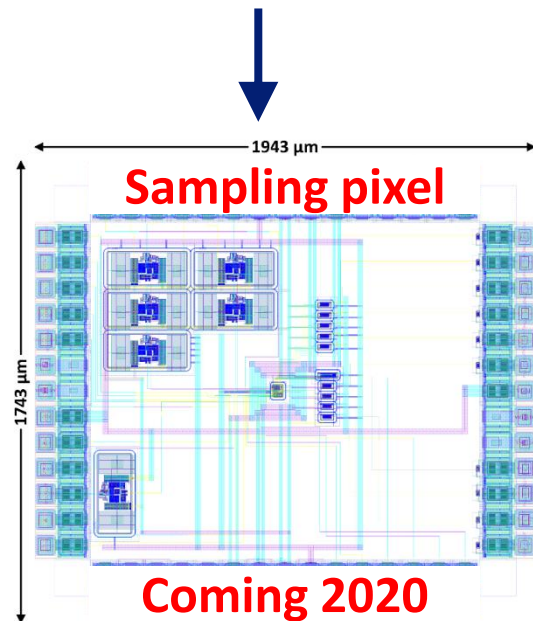
RD50-MPW2



RD50-MPW3

New!

- Small pixels
- Analog + digital RO
- Small I_LEAK
- No crosstalk
- No asymmetries
 - Matrix 1 – FE-I3
 - Matrix 2 – Sampling





- **LFoundry has improved their manufacturing system**
 - In 2019
 - The production was stopped for some time
 - It has affected the production schedule of RD50-MPW2 and of the sampling chip
- **Since October 2019, they are back to their usual volume production level**
 - RD50-MPW2 will be delivered in January 2020 and the sampling chip a bit later in the spring of 2020



- MPW schedule for 2020

LF15A		
Run ID	Tape In	Est. Ship date
C15D20	06.04.2020	02.08.2020
C15G20	20.07.2020	15.11.2020
C15K20	02.11.2020	28.02.2021

WP3.3: CMOS and monolithic devices



2019
milestones

- WP 3.3. CMOS and monolithic devices
 - **M1:** Characterization of the diodes and readout electronics of unirradiated and irradiated RD50-MPW1 samples (Q4/2018).
 - **M2:** Design and submission for fabrication of RD50-ENGRUN1 (Q4/2018).
 - **M3:** Characterization of unirradiated and irradiated RD50-ENGRUN1 samples (Q3/2019, Q3/2020).
 - **M4:** Characterization of irradiated backside biased RD50-ENGRUN1 samples for operation beyond $10^{16} n_{\text{eq}}/\text{cm}^2$ (Q4/2020).
 - **M5:** Studies of stitching process options (Q4/2021).
 - **M6:** Characterization of unirradiated and irradiated stitched samples (Q4/2022).

WP3.3: CMOS and monolithic devices



2019
milestones

• Status:

- **M1:** Characterization of the diodes and readout electronics of unirradiated and irradiated RD50-MPW1 samples (Q4/2018). → Achieved
- New intermediate milestone **M1.2:** Design and submission of RD50-MPW2 (Q1/2019). → Achieved
- New intermediate milestone **M1.3:** Characterization of unirradiated and irradiated RD50-MPW2 samples (Q4/2019, Q1/2020). → Developing DAQ at the moment
- **M2:** Design and submission for fabrication of RD50-ENGRUN1 (Q4/2018). → Ongoing
- **M3:** Characterization of unirradiated and irradiated RD50-ENGRUN1 samples (Q3/2019, Q3/2020). → Postponed
- **M4:** Characterization of irradiated backside biased RD50-ENGRUN1 samples for operation beyond $10^{16} n_{eq}/cm^2$ (Q4/2020).
- **M5:** Studies of stitching process options (Q4/2021).
- **M6:** Characterization of unirradiated and irradiated stitched samples (Q4/2022).