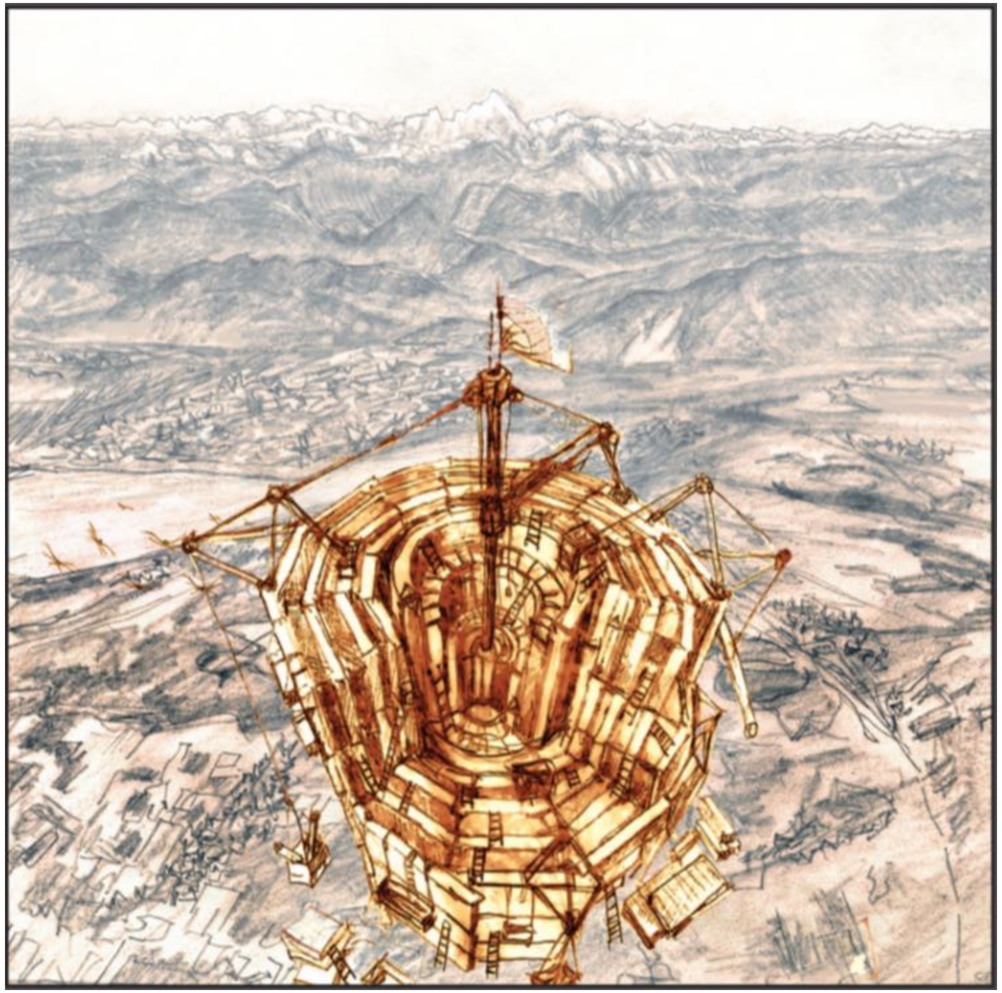
CMS HL-LHC Upgrade: Selected Highlights



LHCP 2020 M. Mannelli – CERN

On behalf of the CMS Collaboration

CMS HL-LHC Upgrade: Scope

- Aim to enable full program of Precision Measurements and Direct Searches for Rare Processes, Subtle and/or Exotic Signatures, in the search for BSM Physics, allowing for the challenging HL-LHC environment
  - The High Radiation Environment necessitates
    - The complete replacement of the Tracker and End-Cap Calorimeter systems
    - Cold operation of the Barrel ECAL (APD Noise Mitigation)
    - Major electronics overhaul and consolidation of the Barrel Calorimeters and Muon systems
  - The High Pile Up motivates
    - Improved granularity wherever possible
    - Novel approaches to in-time Pile Up mitigation: Precision Timing detectors (30ps)
  - The High Luminosity requires
    - Substantially improved L1 Trigger primitives for better selectiveness, despite the high PU
    - A complete overhaul of the Trigger and DAQ systems

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These challenges define the scope of the CMS HL-LHC upgrade program

CMS HL-LHC Upgrade: Scope

Technical proposal CERN-LHCC-2015-010 https://cds.cern.ch/record/2020886
Scope Document CERN-LHCC-2015-019 https://cds.cern.ch/record/2055167/files/LHCC-G-165.pdf

Complete replacement**

Major Electronics Upgrade/ Consolidation *

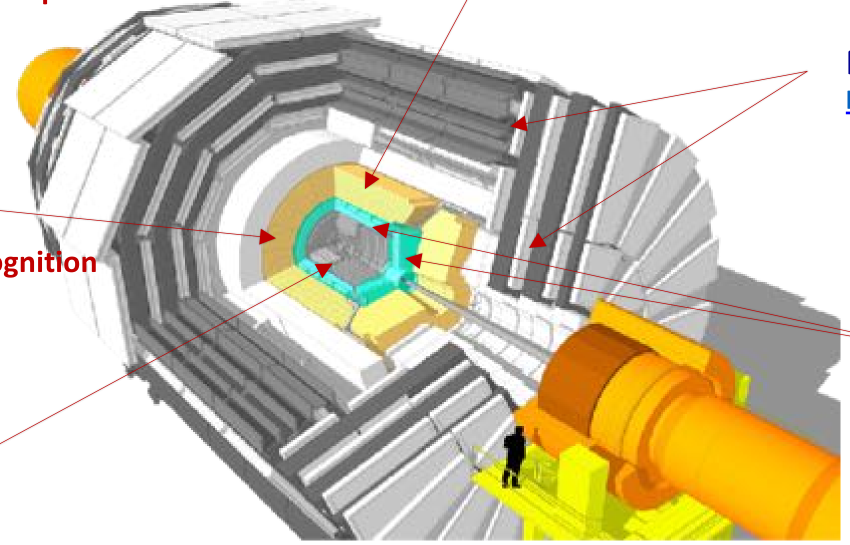
New Detector System***

L1-Trigger/HLT/DAQ**
https://cds.cern.ch/record/2283192
https://cds.cern.ch/record/2283193
- Tracks in L1-Trigger at 40 MHz
- PFlow-like selection 750 kHz output
- HLT output 7.5 kHz

Barrel Calorimeters*
https://cds.cern.ch/record/2283187
- ECAL crystal granularity readout at 40 MHz
- Precision timing for e/γ at 30 GeV, for vertex localization (H → γγ)
- ECAL and HCAL new Back-End boards

Muon systems* ***
https://cds.cern.ch/record/2283189
- Extended GEM coverage to $\eta \simeq 3$
- DT & CSC new FE/BE readout
- RPC back-end electronics
- New GEM/RPC $1.6 < \eta < 2.4$

Calorimeter Endcap**
https://cds.cern.ch/record/2293646
- 3D showers imaging for pattern recognition
- Precision timing for PU mitigation
- Si, Scint+SiPM in Pb/W-SS



MIP Timing Detector***
https://cds.cern.ch/record/2296612
- Precision timing for PU mitigation
- Barrel layer: Crystals + SiPMs
- Endcap layer: Low Gain Avalanche Diodes

Tracker**
https://cds.cern.ch/record/2272264
- P_T module design for tracking in L1-Trigger
- Extended coverage to $\eta \simeq 3.8$
- Much reduced material budget
- Si-Strip and Pixels increased granularity

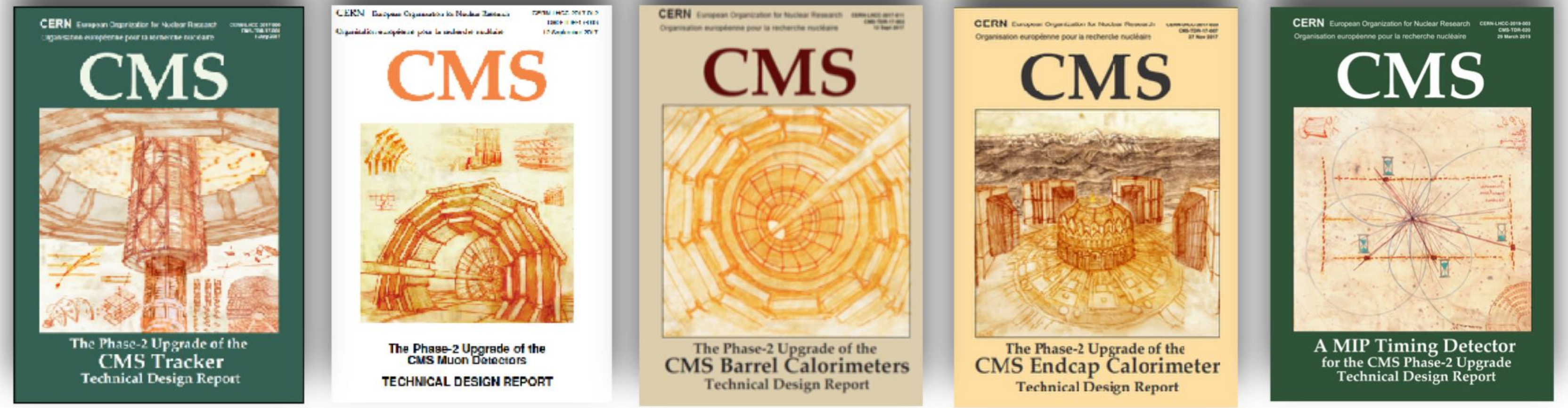
Beam Radiation Instr. and Luminosity
Common Systems and Infrastructure
https://cds.cern.ch/record/2020886

New paradigms for a HEP experiment to meet the unprecedented challenges and fully exploit the HL-LHC luminosity and physics potential

CMS HL-LHC Upgrade: from Concept towards Construction

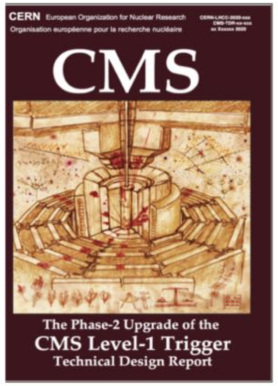
2014 → **2019**

Completed



Entering a new phase of engineering, prototyping, construction

Q1 2020



We delivered the Phase-2 L1 Trigger TDR to LHCC (350+ pages, algorithms, demonstrators, a candidate menu, ...) plus the full UCG package

Planned

DAQ/HLT

Q2 2021

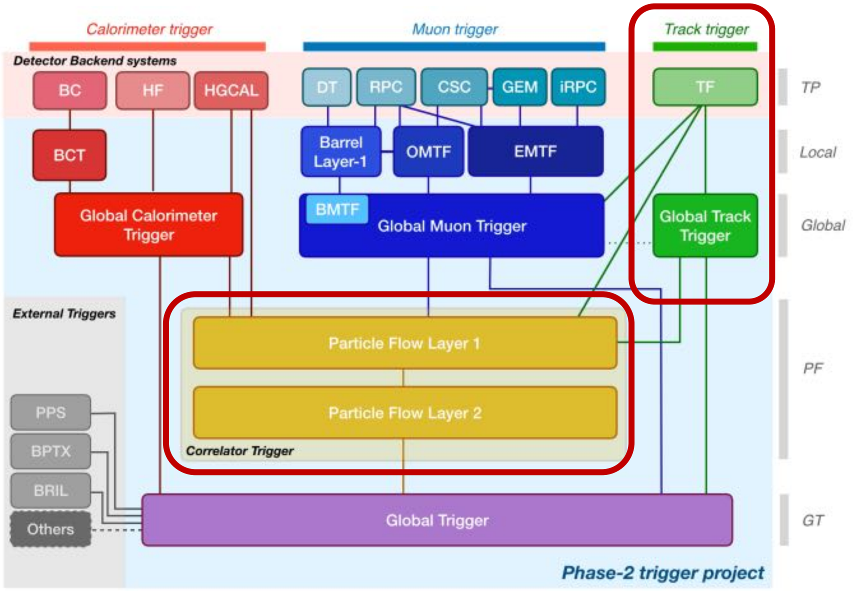
BRIL

Q2 2021

Plus

- PPS (EOI)
- Computing (2023/24)

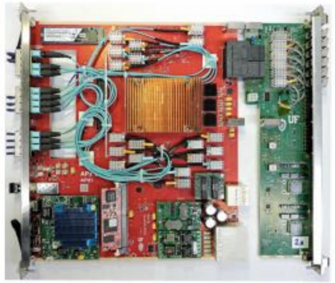
CMS HL-LHC L1 Trigger

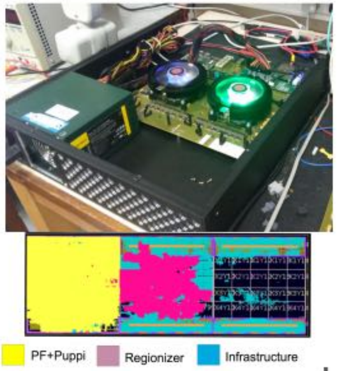


CMS is upgrading its Level-1 Trigger system to cover the HL-LHC physics program

- **Key system design**:
  - Exploit sub-detector back-end electronics: High-granularity and fully reconstructed tracks
  - Sophisticated reconstructed objects and correlations: Particle-Flow → Enhanced physics selectivity
  - Expand reach with Scouting System
- Key numbers: 12.5 us latency, 750 kHz

- **Key features**:
  - **Global Triggers** providing standalone objects for triggering including displaced signals.
  - **Correlator Trigger**: Particle-Flow
- **Instrumentation:** ATCA boards
  - FPGA (VU9P) / 28 Gb/s links
  - HLS for firmware design
  - Flexible, Robust and Modular architecture

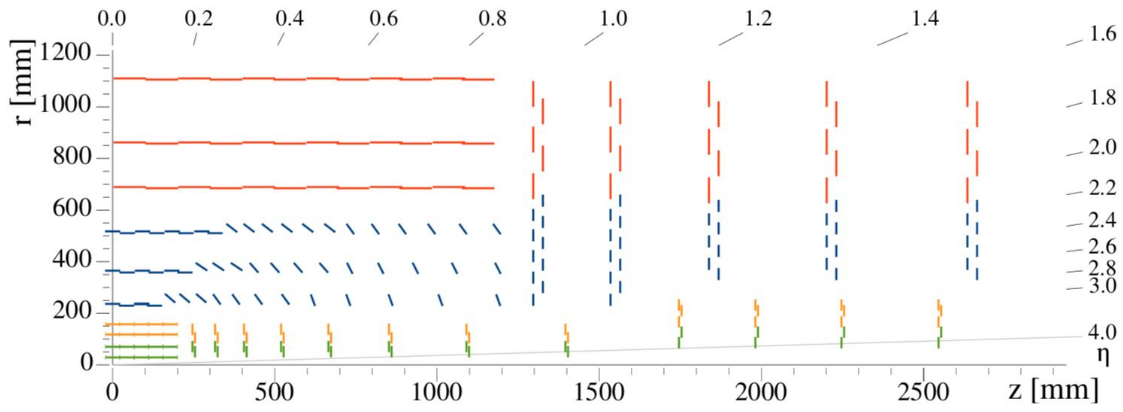




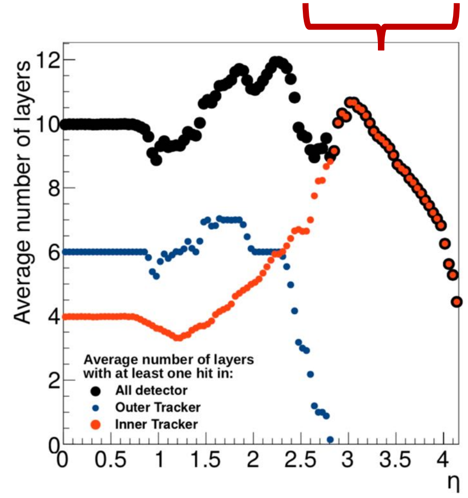
Advanced and powerful generic processing engine, particle-flow fully demonstrated in FPGA

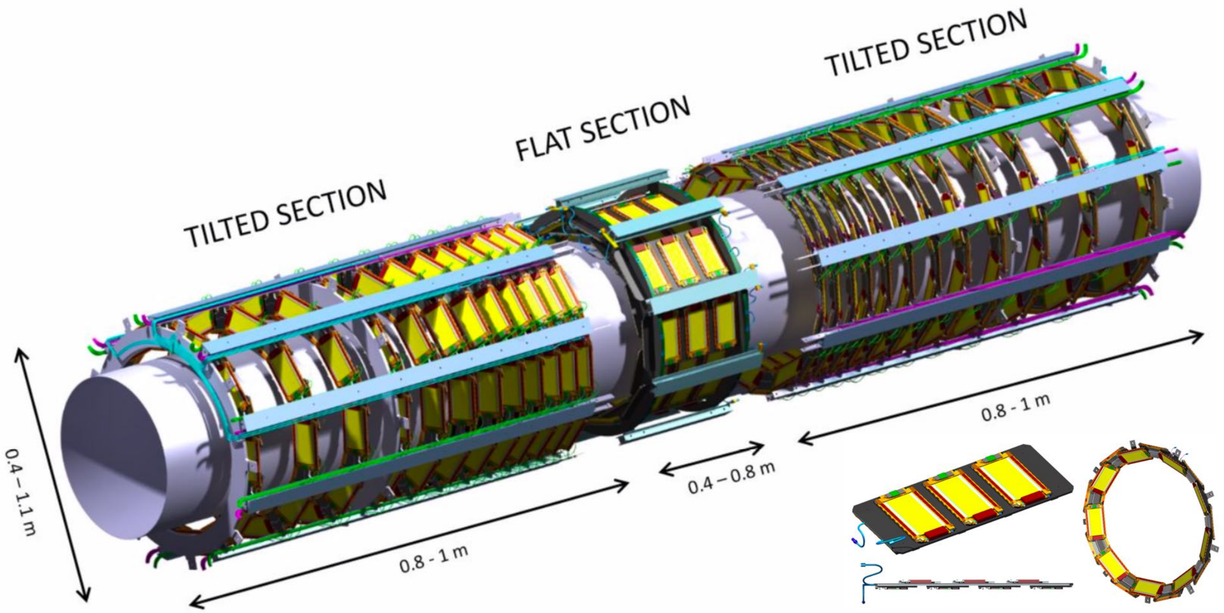
TDR under LHCC review

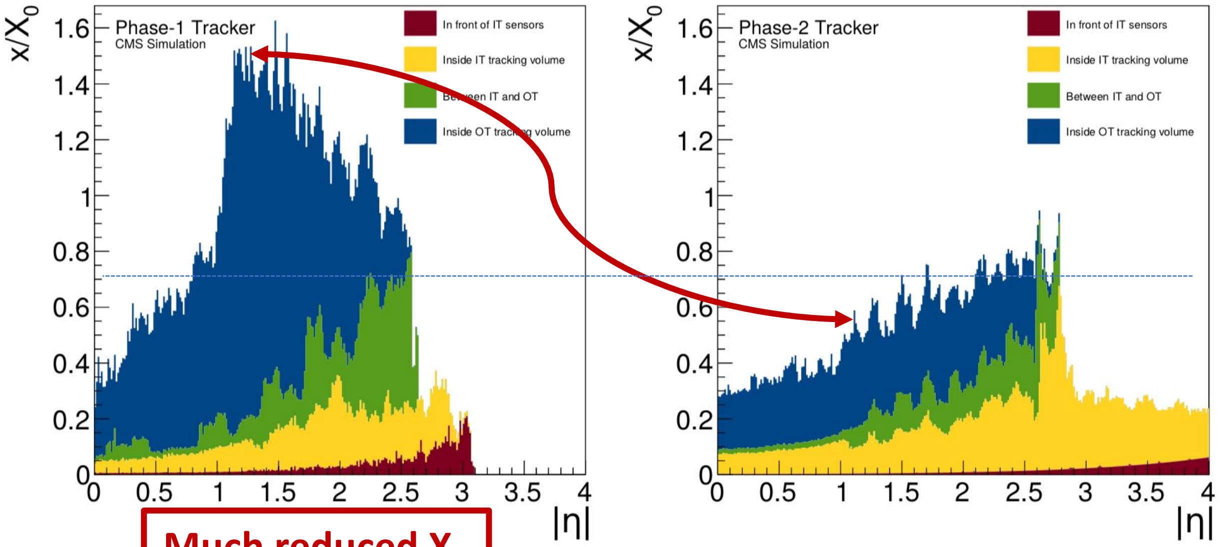
CMS HL-LHC Tracker: Layout and Material Budget



Extended η coverage

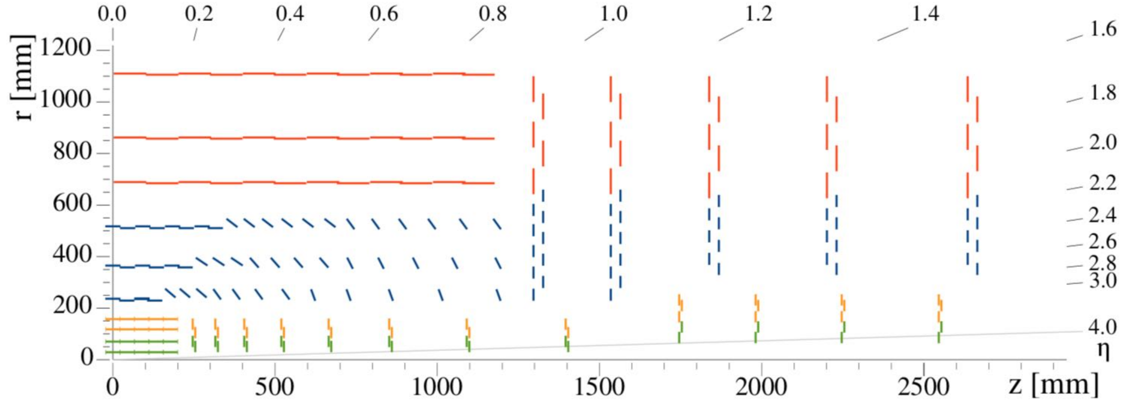


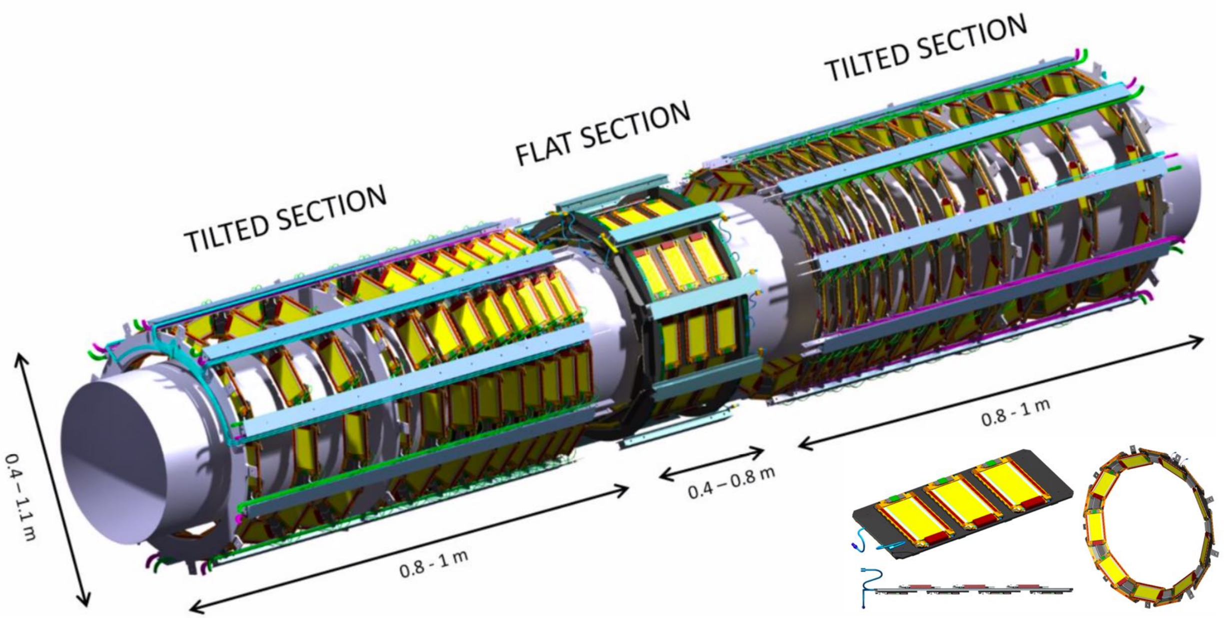


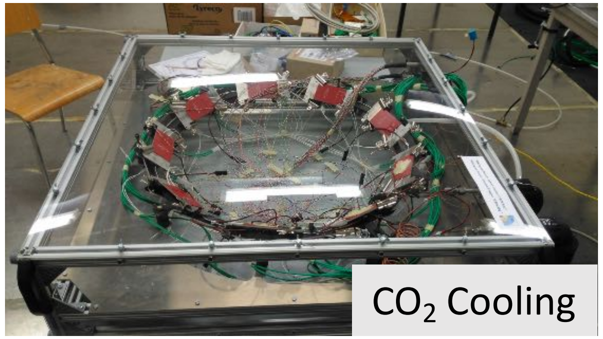


Much reduced X_0

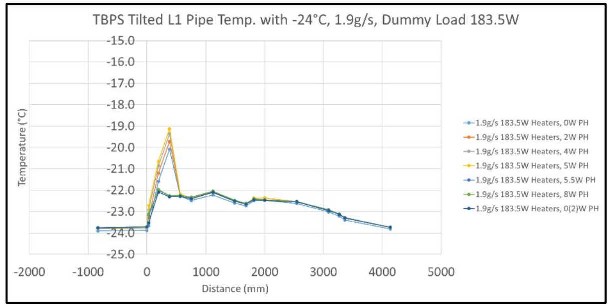
CMS HL-LHC Tracker: engineering for low mass







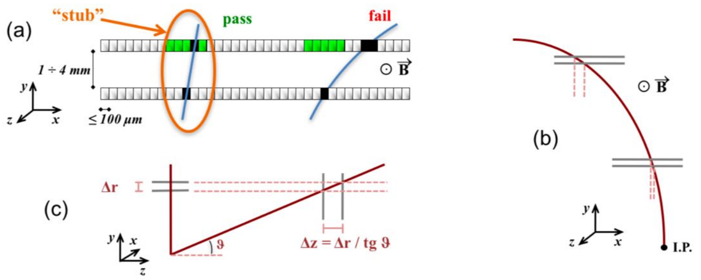
CO_2 Cooling

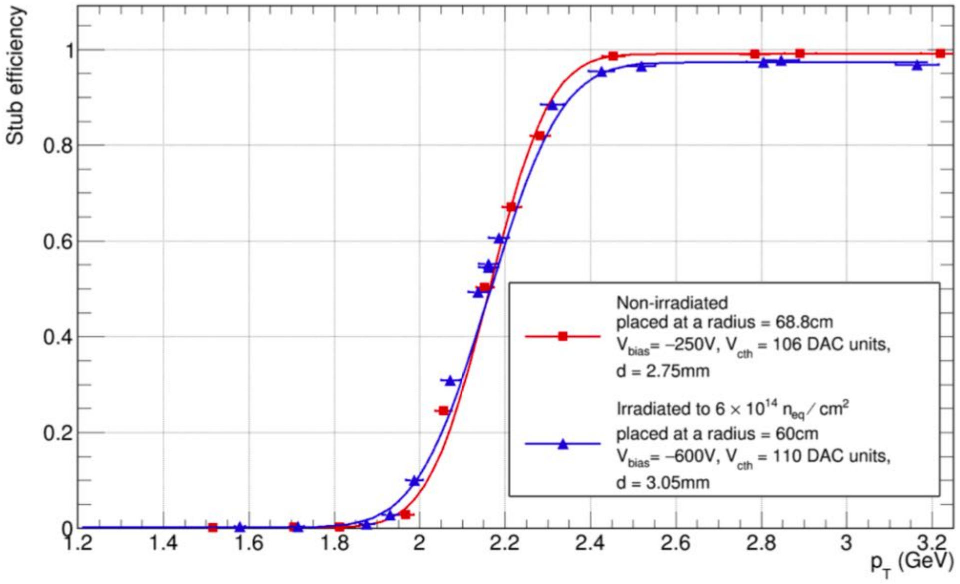


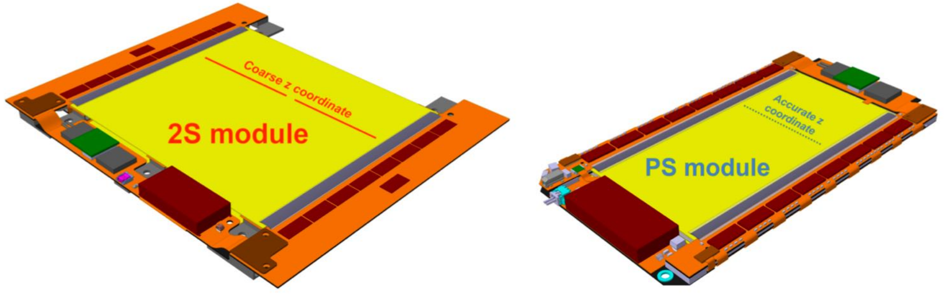
Much reduced X_0

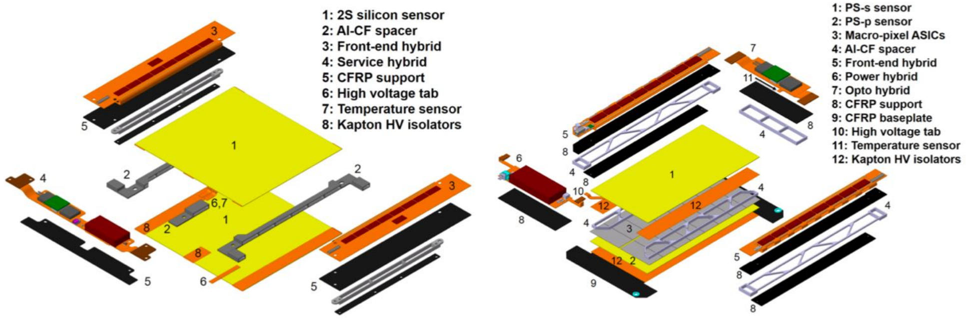
CMS HL-LHC Tracker: p_T Module Design

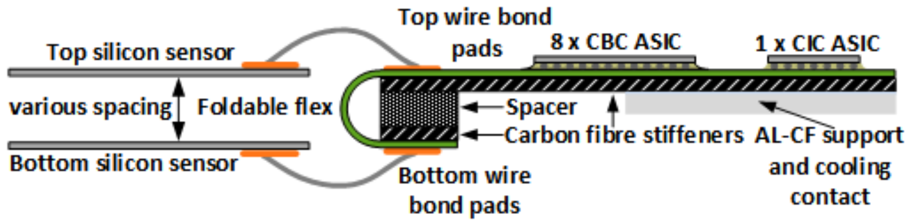
p_T Modules
select pair of hits (Stubs) compatible with track p_T > 2GeV
=> local data reduction for L1 Tracking Trigger @ 40MhZ



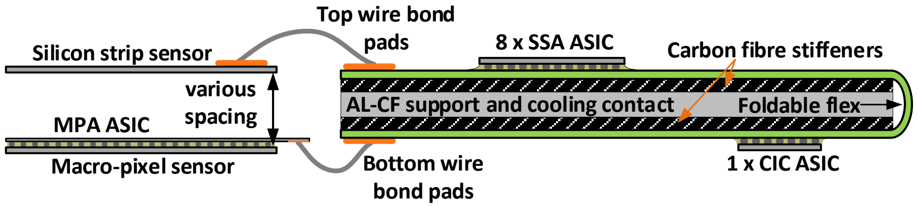






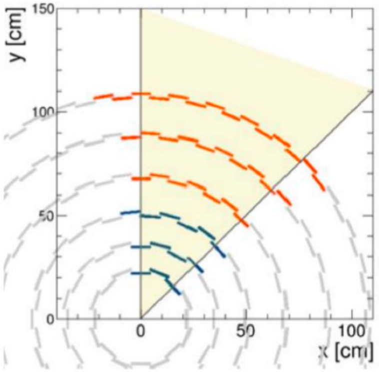


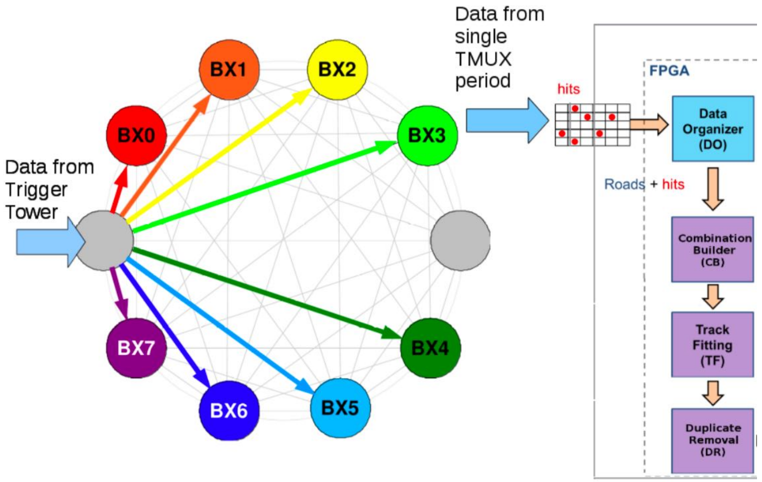
2S

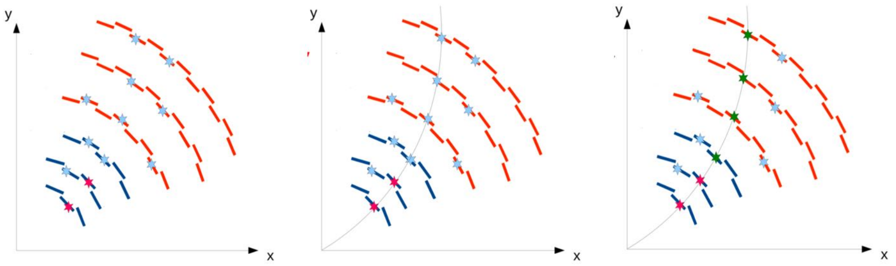


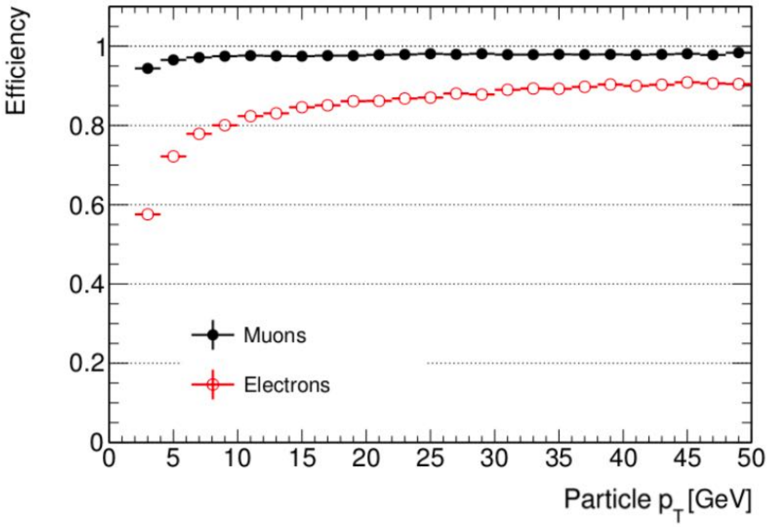
PS

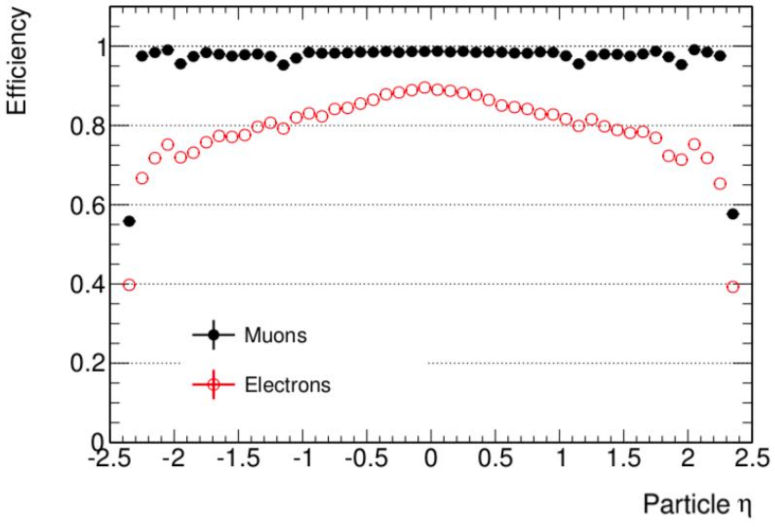
CMS HL-LHC Tracker: from Stubs to L1 Tracks @ 40MHz

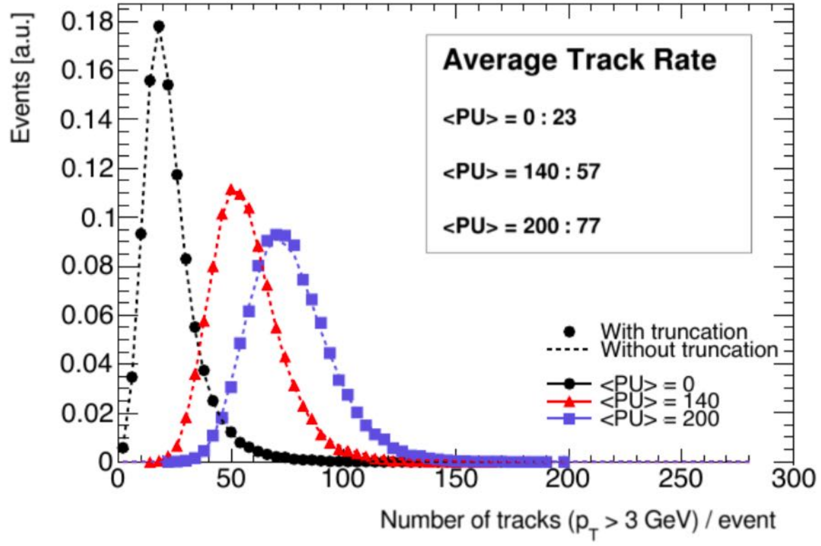




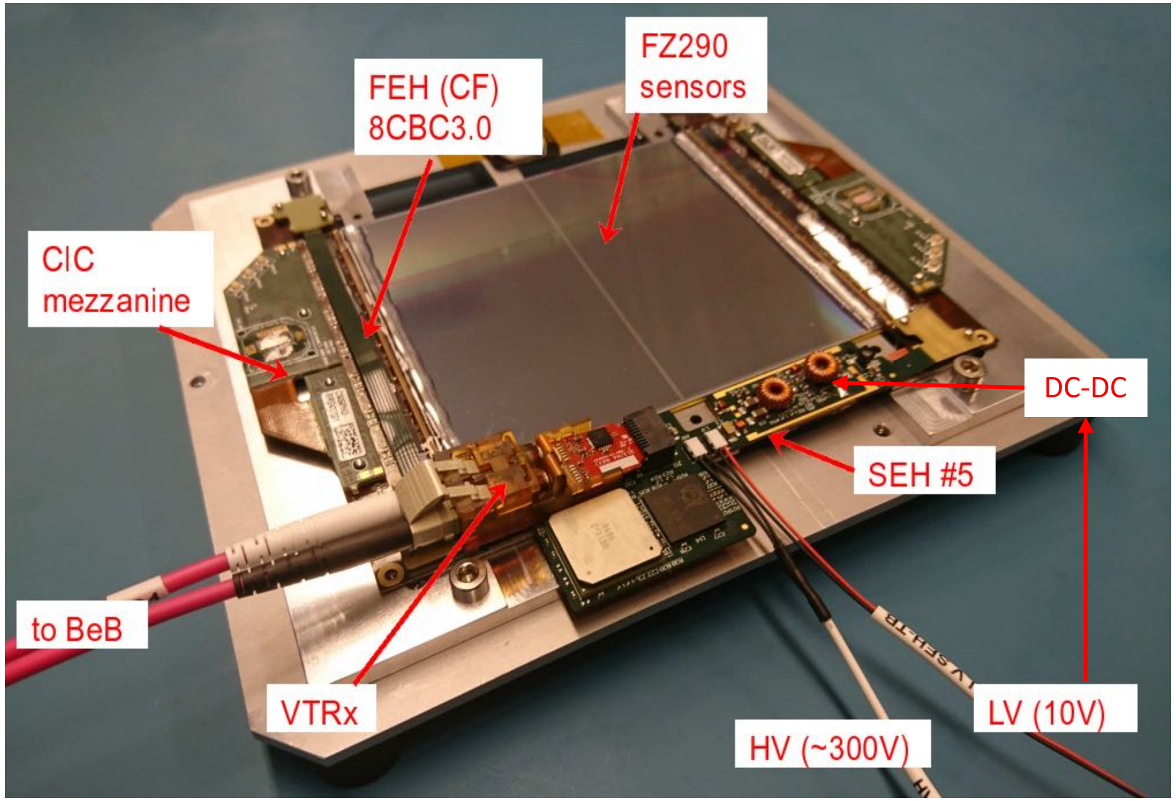


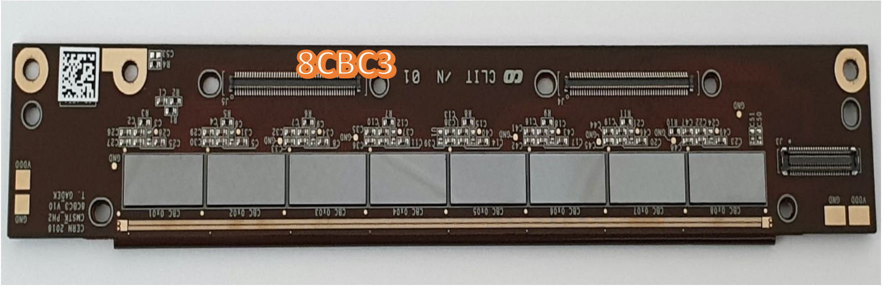




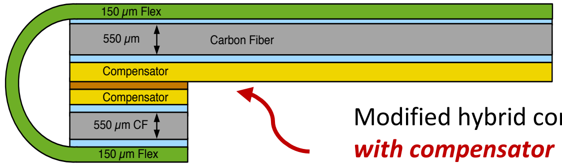


CMS HL-LHC Tracker: p_T Module Development

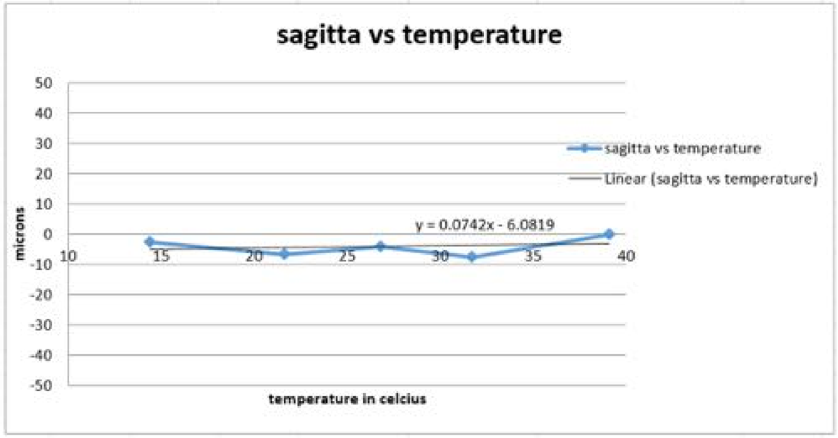




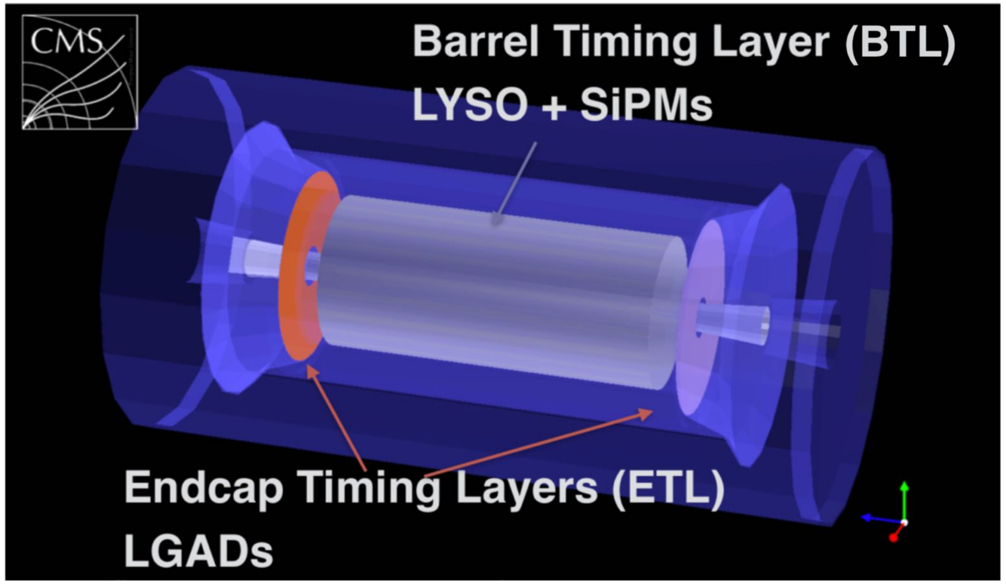
- 4 Layers flexible circuits, carbon fibre stiffened.
- High density interconnect: 42.5 µm tracks width and spacing.
- Laser copper filled microvias on all layers: 25 µm laser drills, 120 µm capture pads.
- Tight fold.
- High pin-count 250 µm pitch flip chips: CBC3, SSA, CIC.
- High speed 90 Ω differential pairs in 150 µm thin flex.



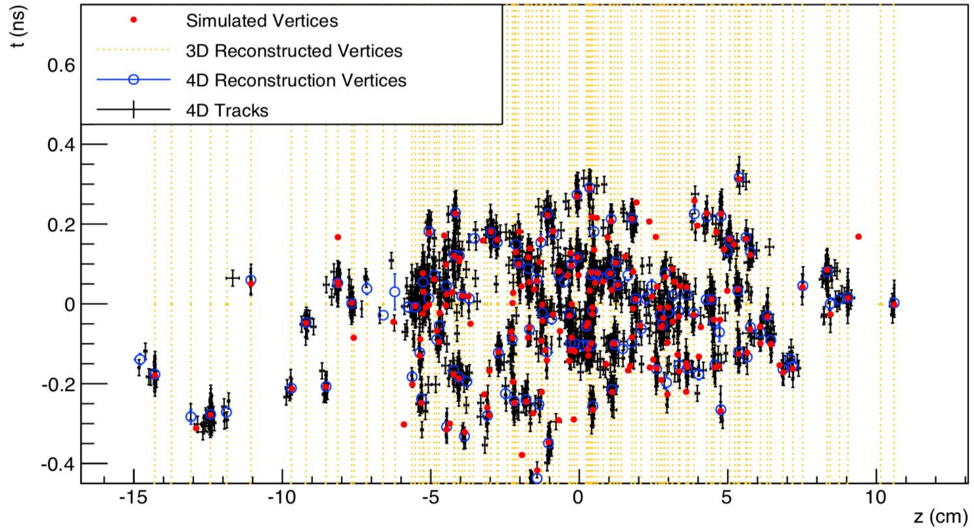
Modified hybrid construction
with compensator

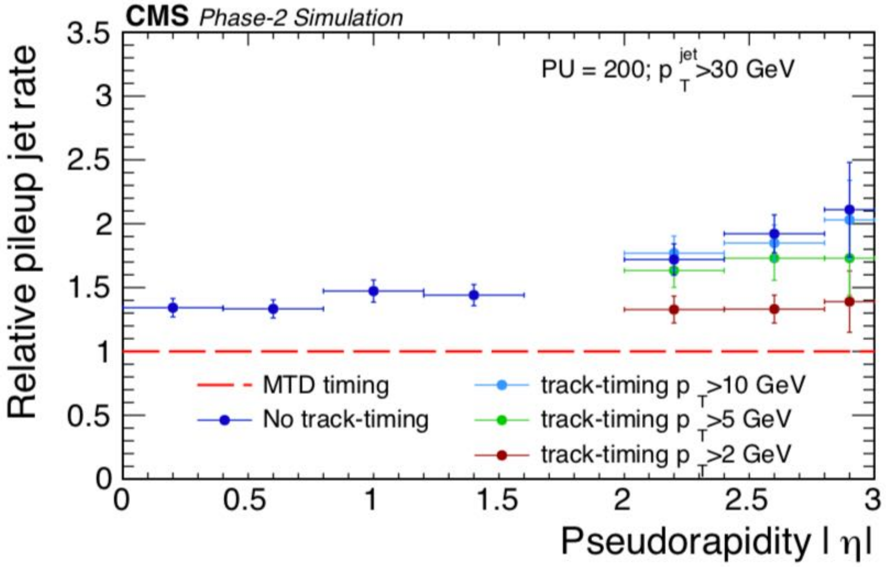


CMS HL-LHC MIP Timing Detector - MTD



Signal	Physics measurement	MTD impact
$H \to \gamma\gamma$ and H→4 leptons	+15 − −25% (statistical) precision on the cross section → Improve coupling measurements	Isolation and Vertex identification
VBF→H→ $\tau\tau$	+30% (statistical) precision on cross section → Improve coupling measurements	Isolation VBF tagging, p_T^{miss}
HH	+20% gain in signal yield → Consolidate searches	Isolation b-tagging
EWK SUSY	+40% background reduction → 150 GeV increase in mass reach	MET b-tagging
Long-lived particles (LLP)	Peaking mass reconstruction → Unique discovery potential	β_{LLP} from timing of displaced vertices





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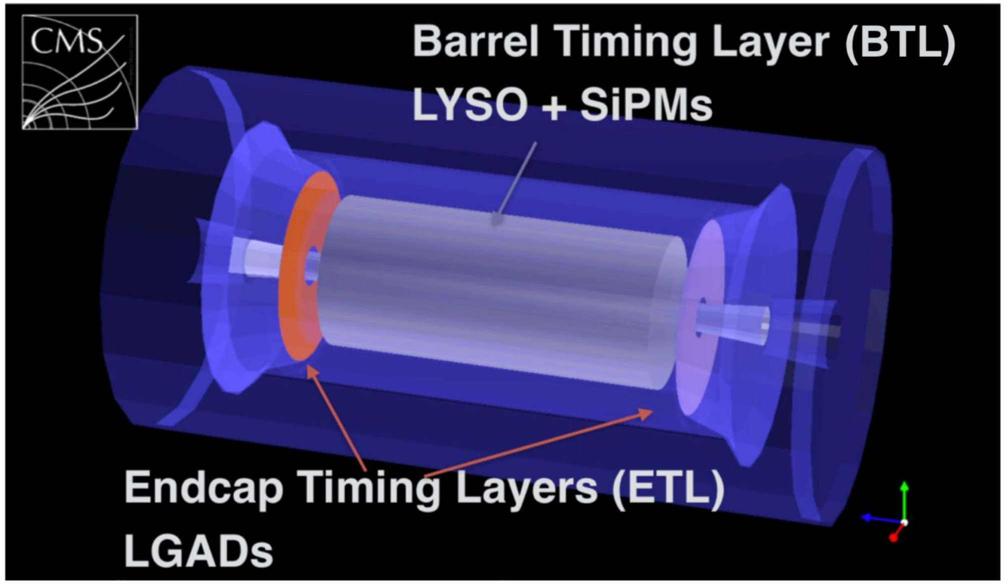

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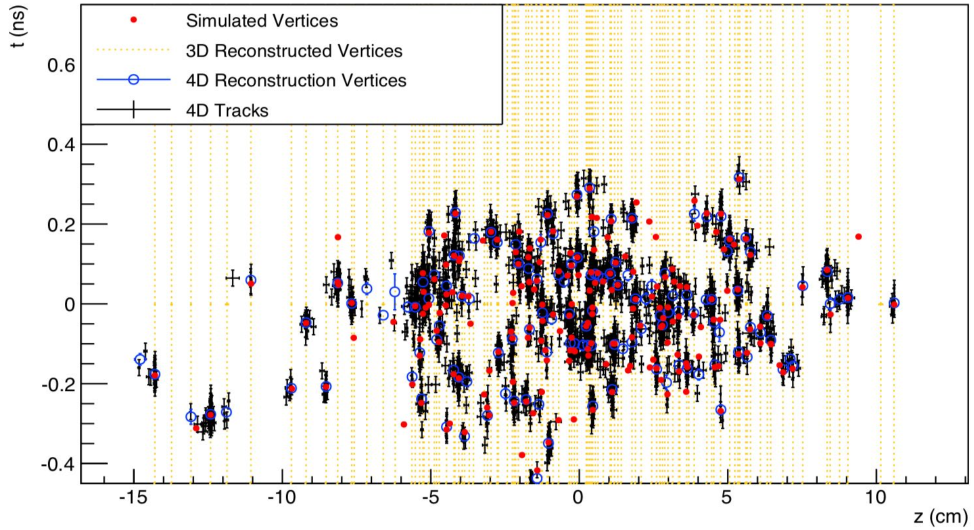

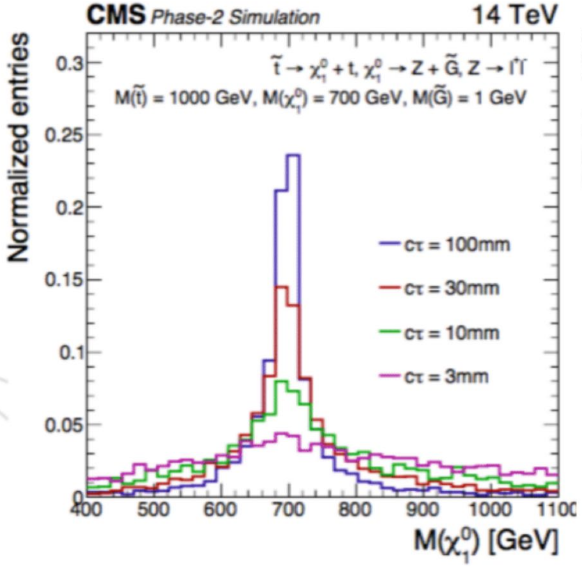

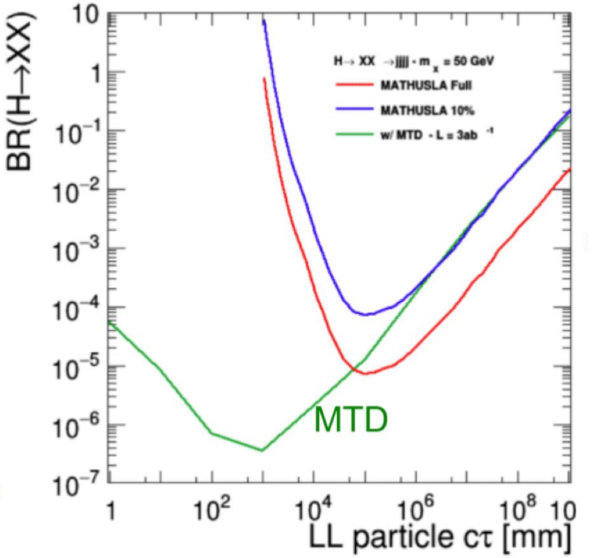

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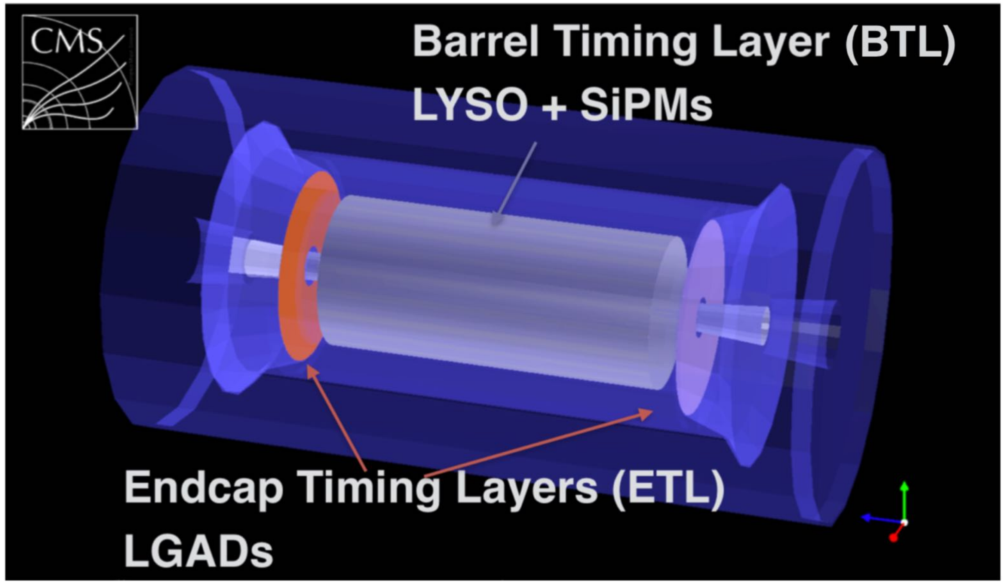

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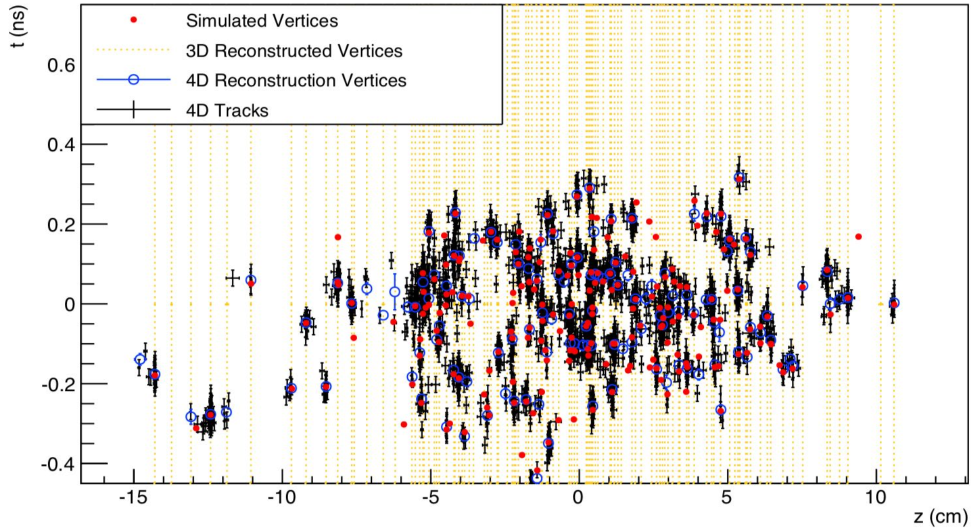

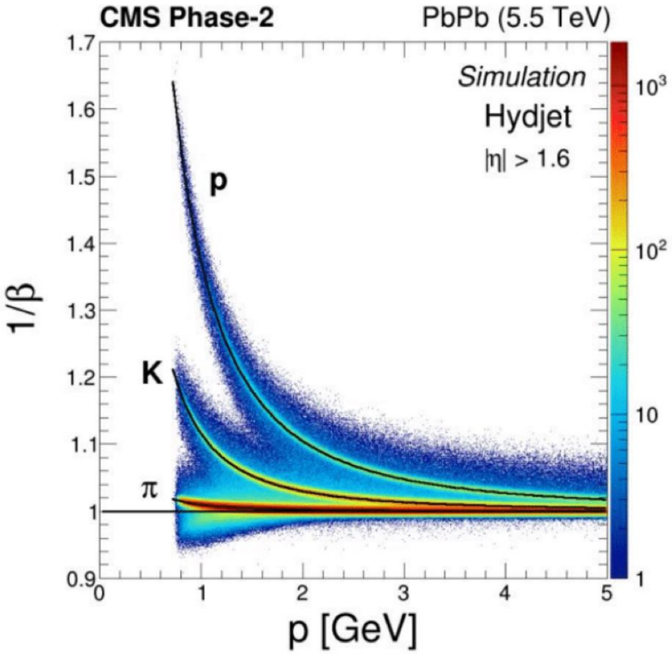

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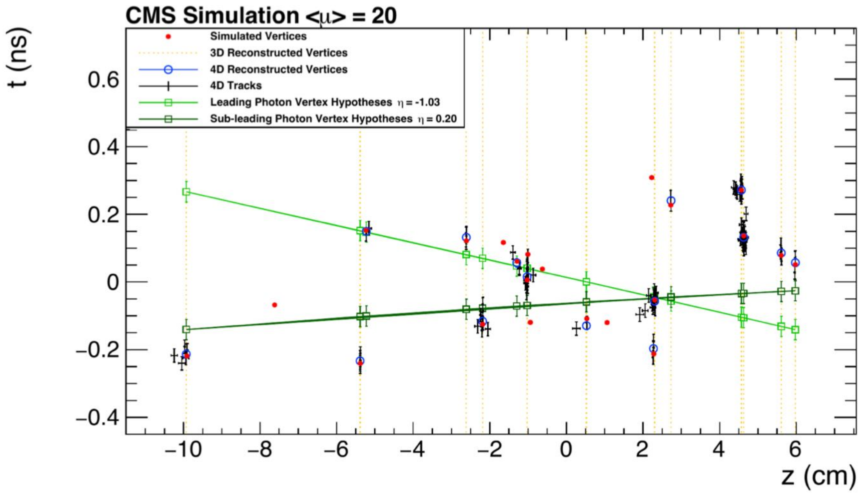

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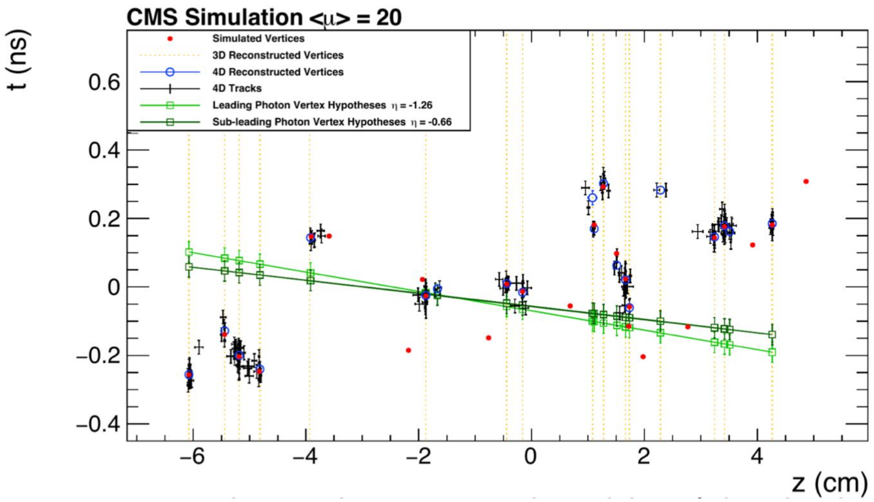
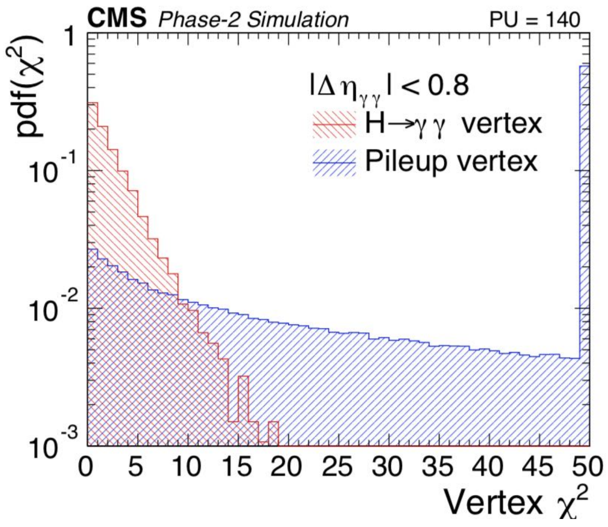
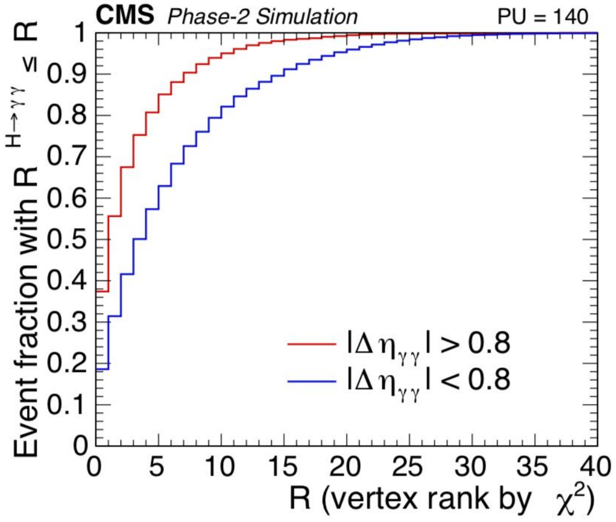


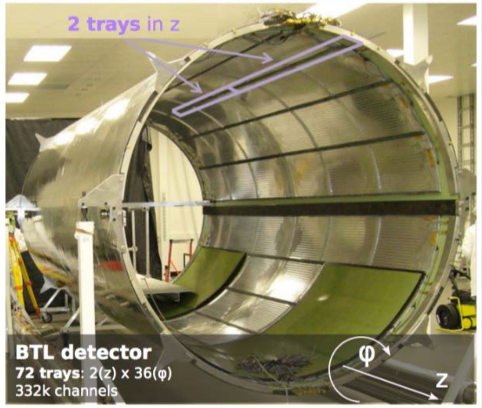




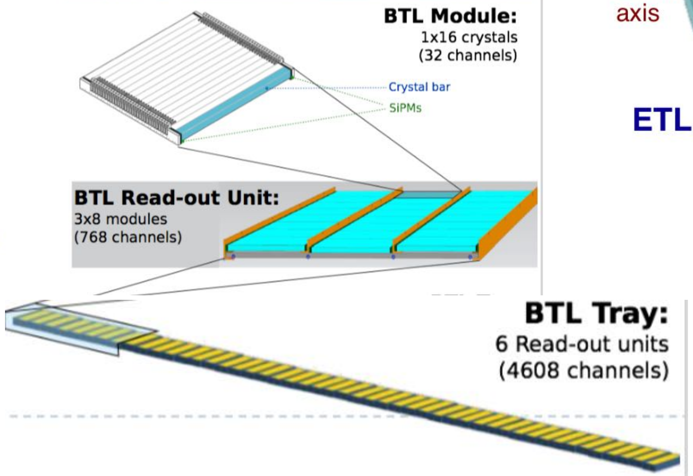
CMS HL-LHC MIP Timing Detector - MTD

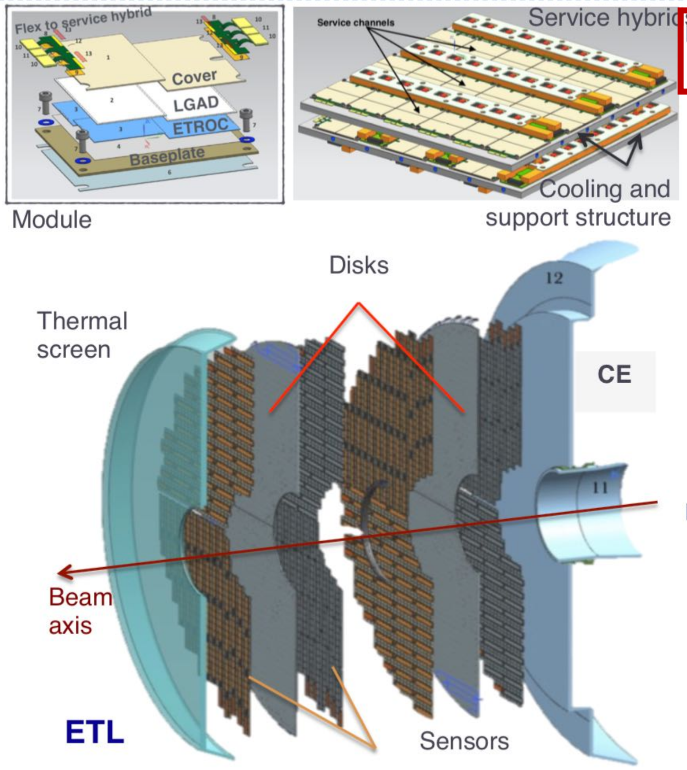
Barrel - BTL

- **LYSO crystals with dual-end SiPM readout**
  - Basic unit: 16x1 array of crystals (~ 3 x 3 x 57 mm^3)
  - Arranged in trays (segmented in readout units)
    - Mounted on the inner surface of the Tracker Support Tube (same cold volume as Tracker)
  - Coverage: $|\eta|<1.45$, surface ~38 m^2; 332k channels
  - Nominal fluence: **1.9×10^{14} n_{eq}/cm^2** (3000 fb^{-1})



- **Recent progress:**
  - LYSO qualification and procurement
  - SiPM characterization and procurement
  - ASIC and front-end prototyping and testing
  - System tests with front-end / back-end integration
  - Mechanics design



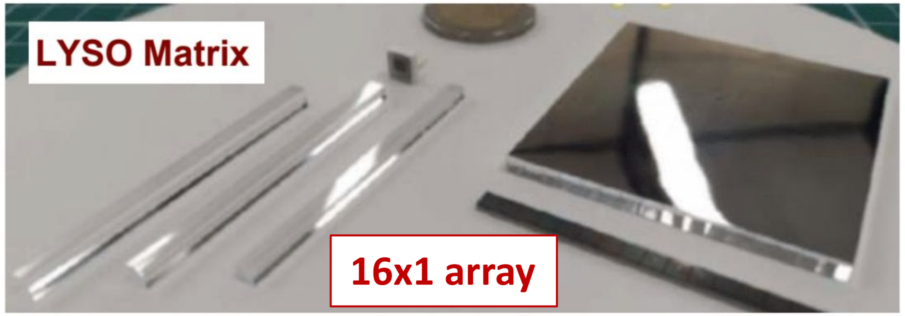


- **Low Gain Avalanche Detectors (LGADs)**
  - Basic unit: Module (4x6 cm^2)
    - LGADs bump-bonded to ETROC ASICs mounted on two sides of cooling plates
  - Two disks per endcap mounted on the HGC nose (independent volume)
  - Coverage: $1.6 < |\eta| < 3.0$, surface ~14 m^2; ~8.5 M channels
  - Nominal fluence: **1.6×10^{15} n_{eq}/cm^2** (3000 fb^{-1})

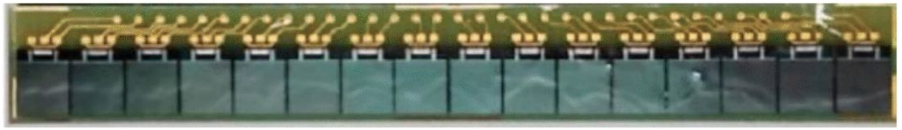
- **Recent progress:**
  - LGAD characterization,
  - ASIC prototyping,
  - System & mechanical design/ prototyping

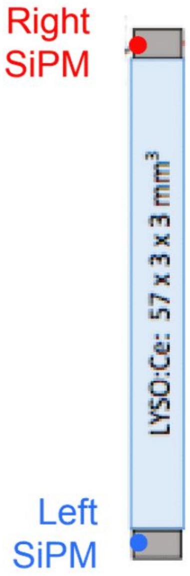
End-Cap - ETL

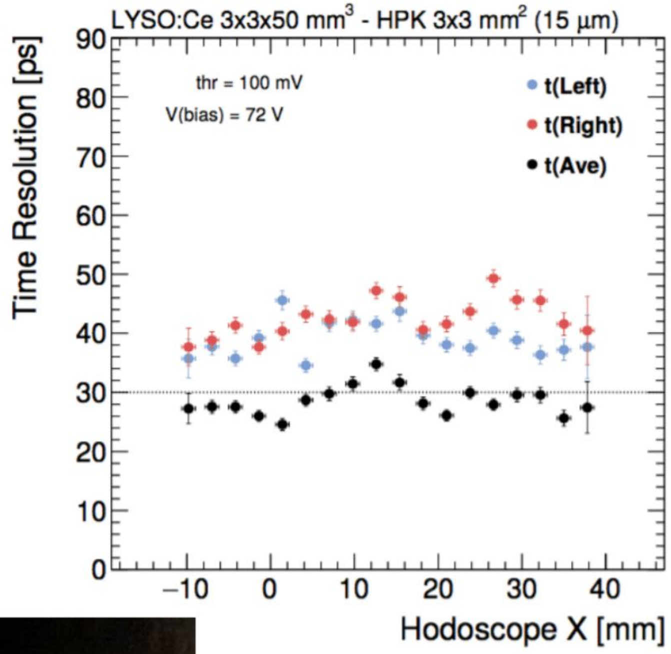
CMS HL-LHC MTD: BTL sensor response

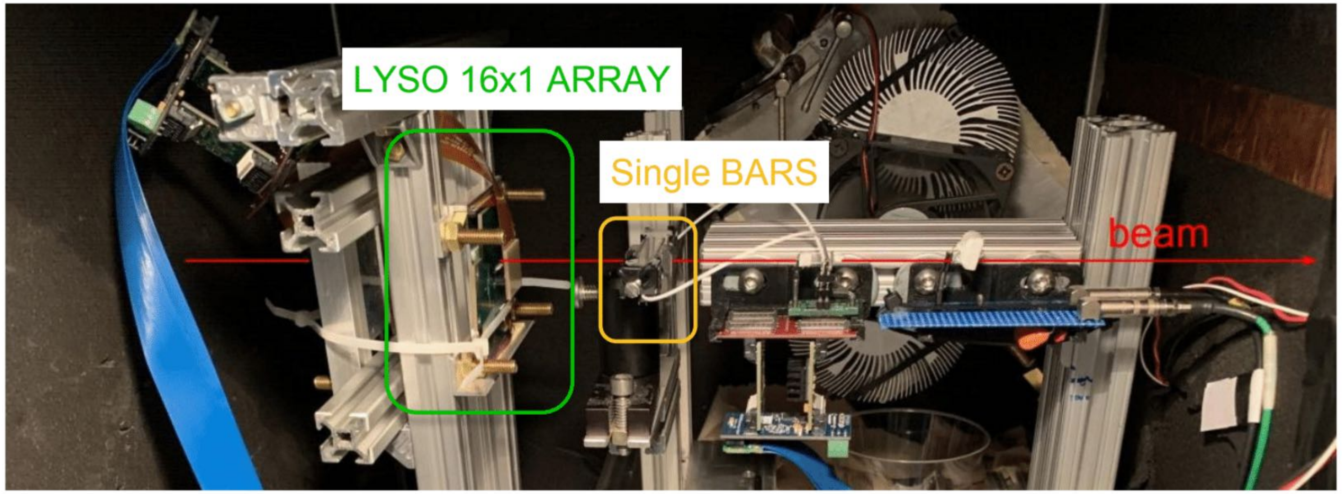


SiPM Array prototype



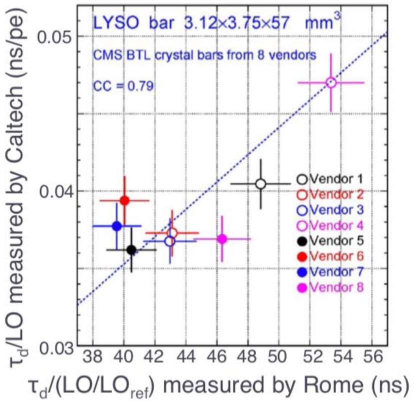


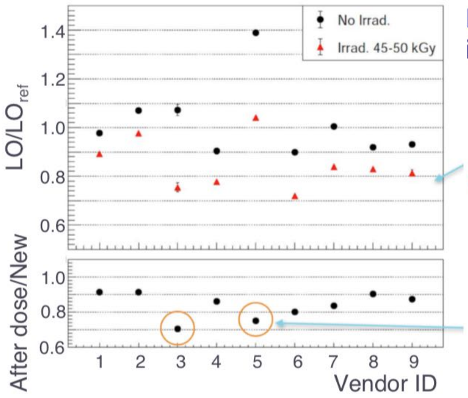




CMS HL-LHC MTD: BTL LYSO-SiPM Module Development

- **Crystals from 9 different vendors fully characterized in lab during 2019**
  - Test stand and testing procedures established; good reproducibility
  - Parameters to control the production quality identified
  - Specifications refined for the procurement process



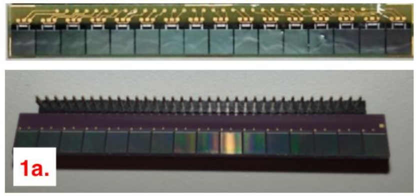


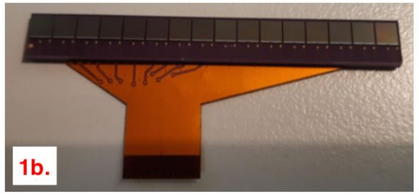
Light output after irradiation by vendor

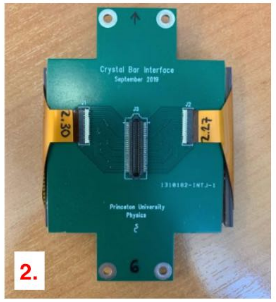
45–50 kGy (1.5 x nominal dose)

$BaSO_4$ wrapping not rad-hard ESR foils requested

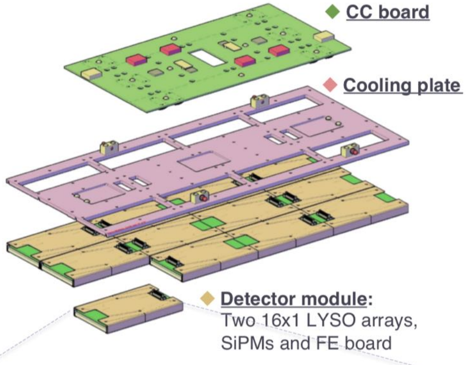
- **Thorough study of integration aspects and signal routing from SiPMs to ASIC**
  1. a) PIN+flex vs b) Flex on array
  2. Module integration (flex robustness, bending radius, noise pickup)
  3. Thermal test of the substrate conductivity
  4. Encapsulation thickness

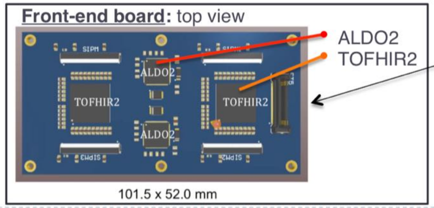


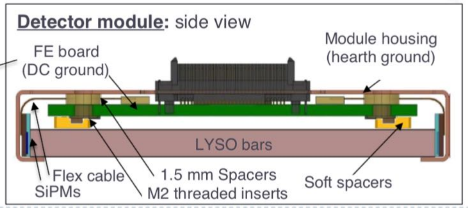


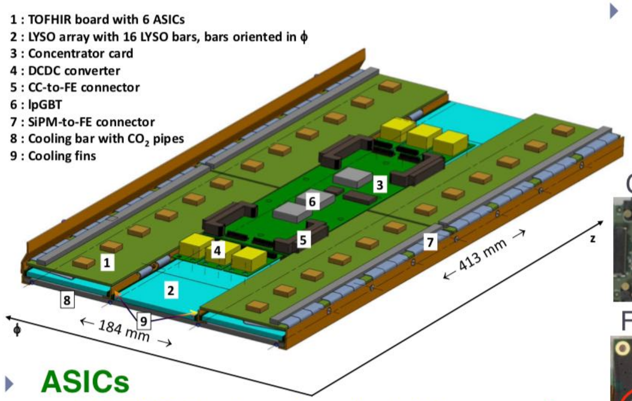


- **TOM (TOFHIR on Module) model**
  - Shortest possible signal path
  - Copper housing provides thermal coupling and electromagnetic shielding
- **Additional functionalities (RUProto2)**
  - SiPM bias voltage regulation
    - TOFHIR DACs and ALDO2
  - Selection of the clock source (redundancy)
  - Redundancy of the links to backend
    - Saclay fan-out ASICs
- **Different form factor for the boards**
  - 12 FE boards / CC (2 ASICs each)









- **Readout unit – 768 channels**
  - Four **Front-End** cards
  - One **Concentrator Card** (CC)
  - Two **Power Control Cards** (PCC)

CC and PCC prototypes

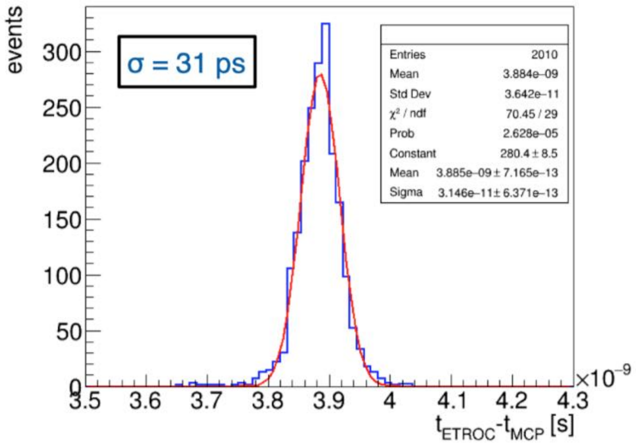
Front end board prototypes

- **ASICs**
  - TOFHIR front-end readout chip
  - ALDO1 LV and SiPM bias regulator
- **Prototype FE boards**

CMS HL-LHC MTD: ETL LGAD Sensor response

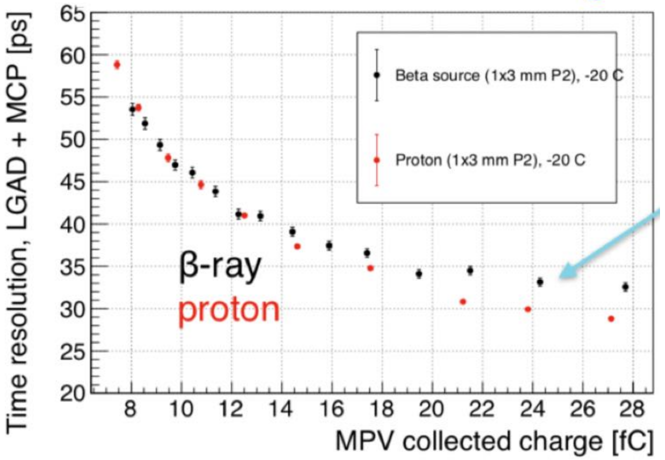
- **LGADs prototype v1 shown to satisfy all requirements for ETL**
  - Timing resolution of 30 ps
  - Radiation tolerance to the end of HL-LHC
  - Wafer process control adequate for production of larger sensors (2x4 cm^2)
- **Next round of prototypes are potentially the final sensor design**
  - Expect slight improvement in radiation hardness
  - Joint order with ATLAS
  - Delivery COVID19-delayed by ~1 months (both vendors)
  - Do not expect impact on the long term schedule
  - Still one additional prototype iteration allocated in schedule

Test beam results (Feb 2020)
LGAD v1 + ETROC0 with
pre-amp waveform analysis

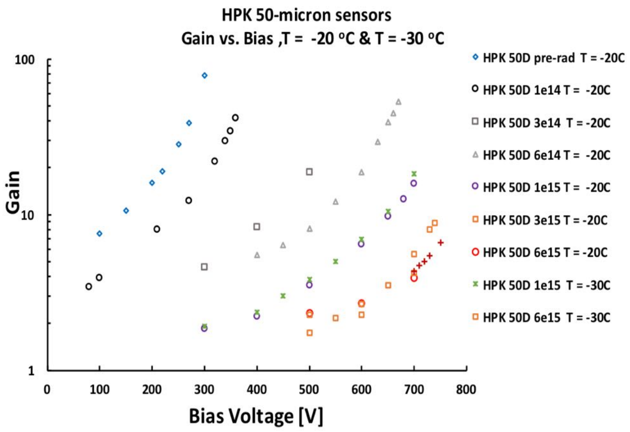


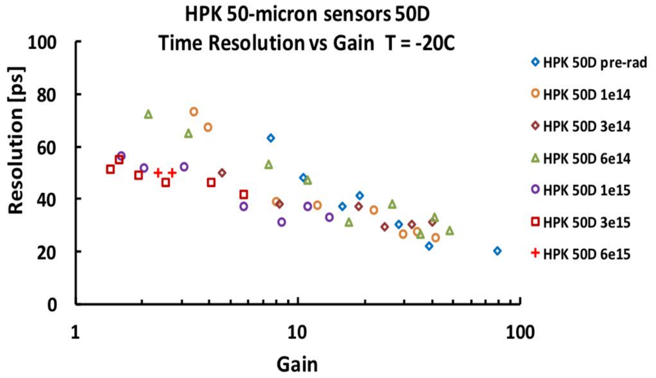
- **Developed mature sensor characterization facilities that enable large sample testing**
  - Key links established between beam, Sr-90 β-rays, and probe station measurements
  - Interpret probe information based on correspondence with beta/beam test
    - CV measurements with probe stations will play a key role in QA/QC
  - **Uniformity sufficient to produce working full-sized sensors (2 x 4 cm^2)**

LGAD resolution versus charge



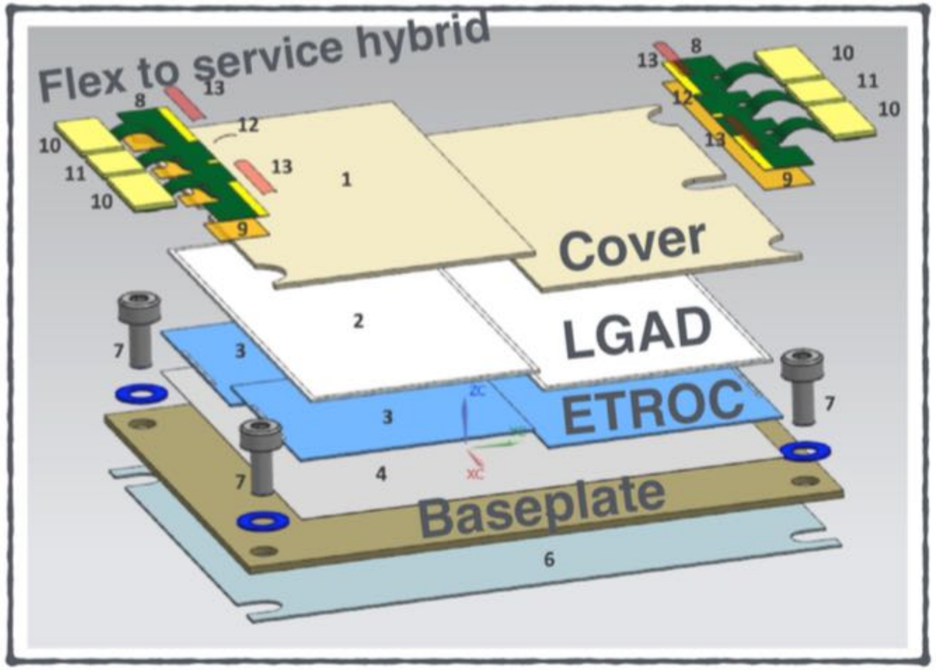
LGAD response vs n fluence

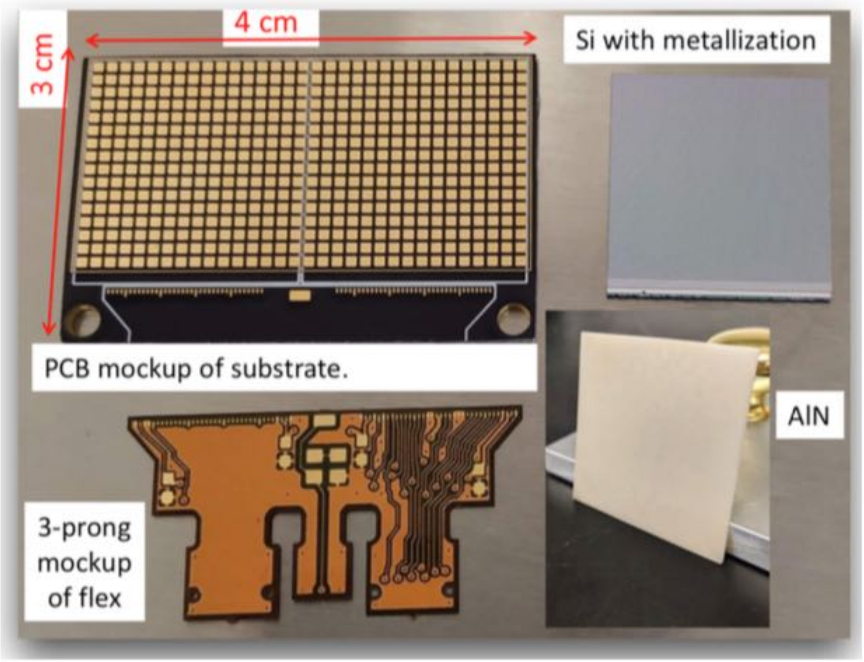




CMS HL-LHC MTD: ETL LGAD Module Development

- **Rugged and simple to assemble modules**
  - Bump-bonded ETROC to LGADs
  - Will assemble 9k modules: considering both gantry and jig workflows.
- **Practicing assembly using mechanical mockups**
- **Preparing for thermal & electrical testing**





1.3x1.3mm² LGAD sensor granularity

CMS HL-LHC HGCAL

HGCAL Parameters

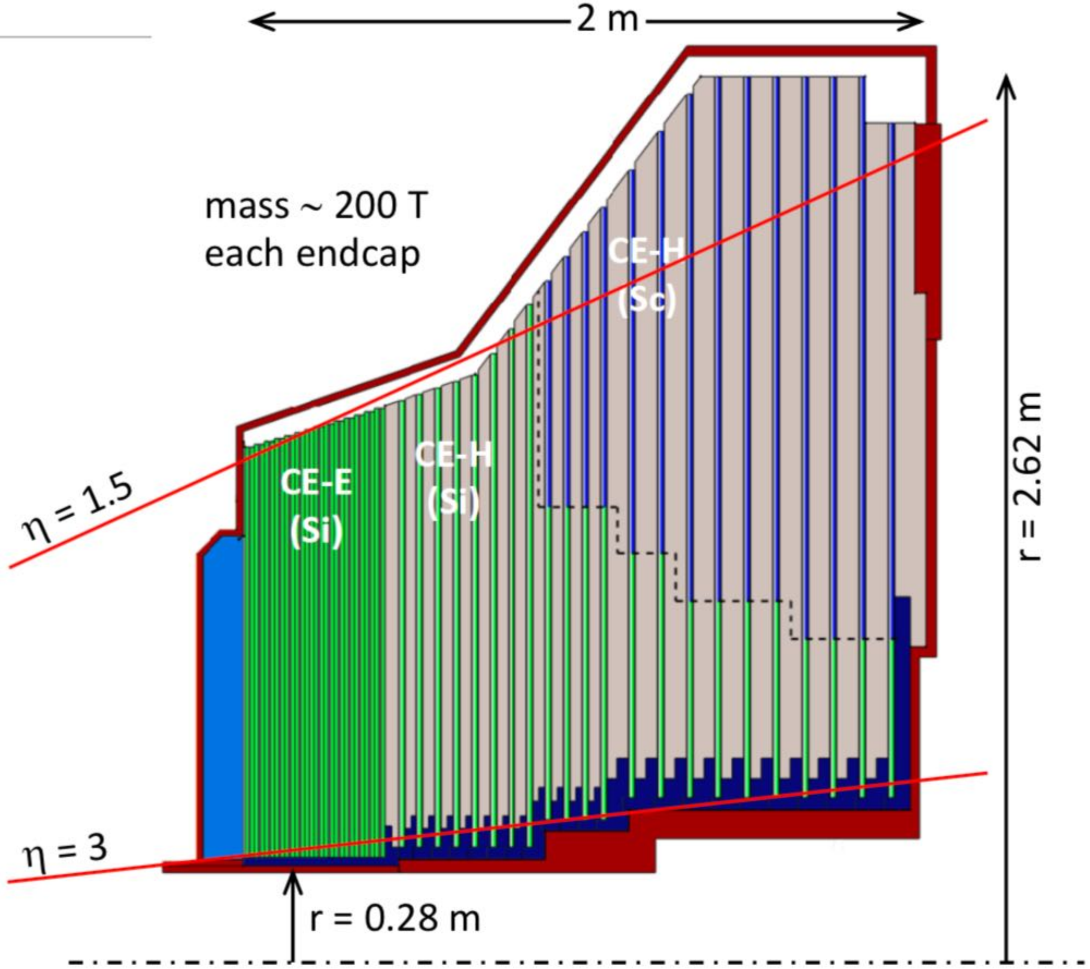
Key Parameters (updated from the TDR):

- HGCAL covers 1.5 < η < 3.0
- **Full system maintained at -30°C**
- **~640 m²** of silicon sensors
- **~370 m²** of scintillators
- 6.1M Si channels, 0.5 or 1.1 cm² cell size (*6M*)
  240k scint-tile channels (η–ϕ)
  - Data readout from all layers
  - Trigger readout from alternate layers in CE-E and all in CE-H
- ~31000 Si modules (incl. spares) 8" Si Sensors

Active Elements:

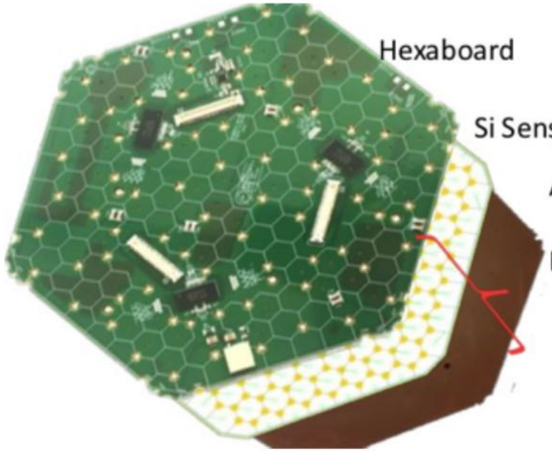
- Si sensors (full and partial hexagons) in CE-E and high-radiation region of CE-H.
- SiPM-on-Scintillating tiles in low-radiation region of CE-H

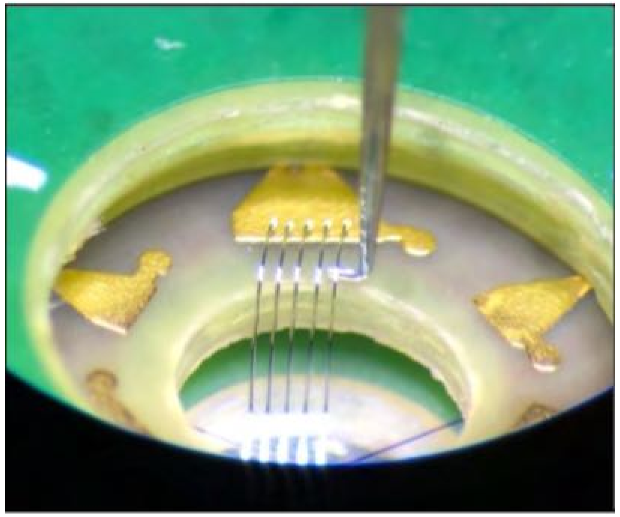
Electromagnetic calorimeter (**CE-E**): **Si**, Cu/CuW/Pb absorbers, 28 layers, 25.5 X_0 & ~1.7λ
Hadronic calorimeter (**CE-H**): **Si** & **scintillator**, steel absorbers, 22 layers, ~9.5λ (including CE-E)

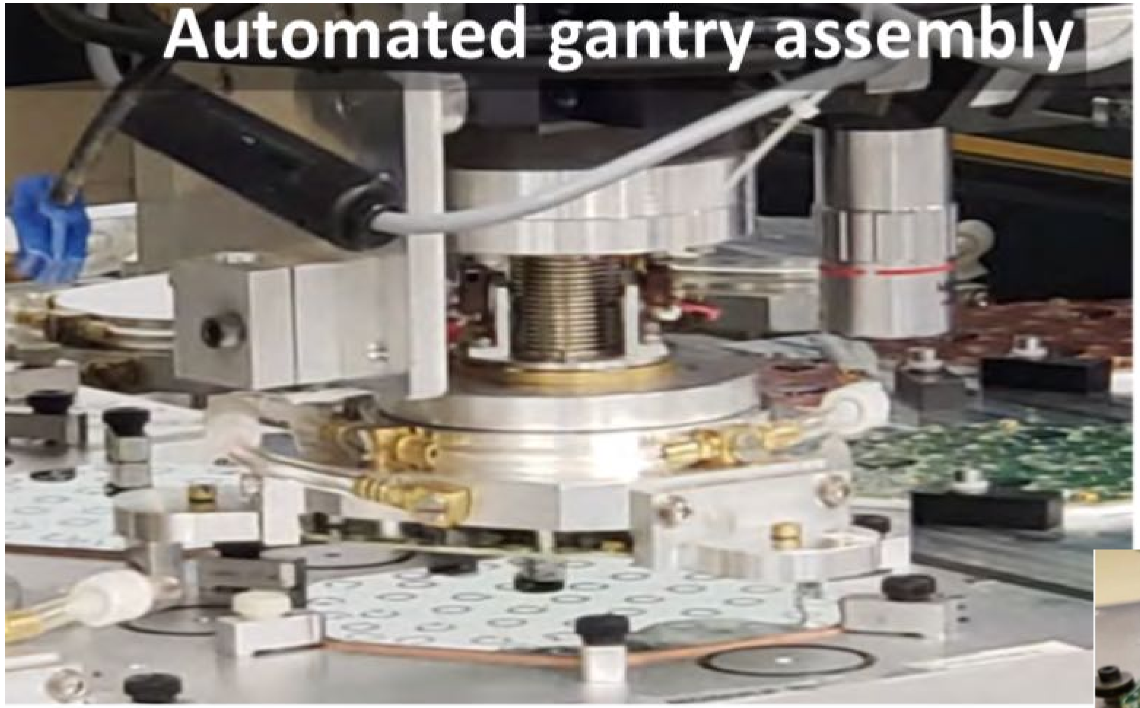


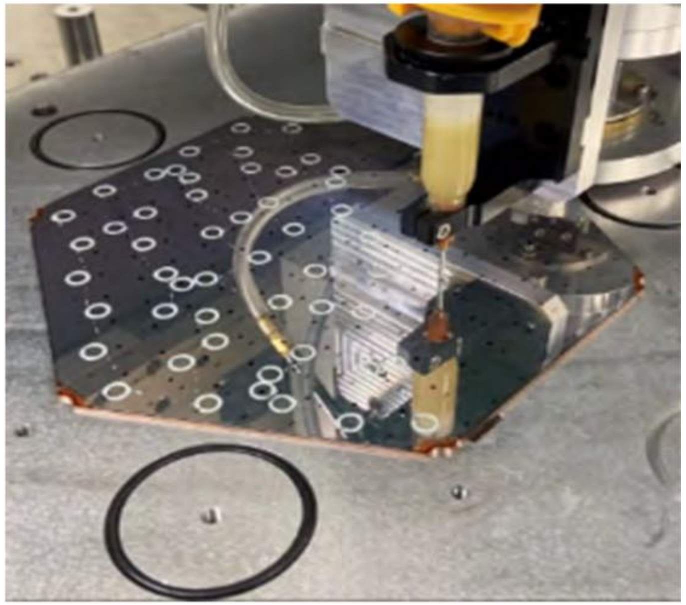
CMS HGCAL: Silicon Sensor Module Development

Silicon Sensor Modules





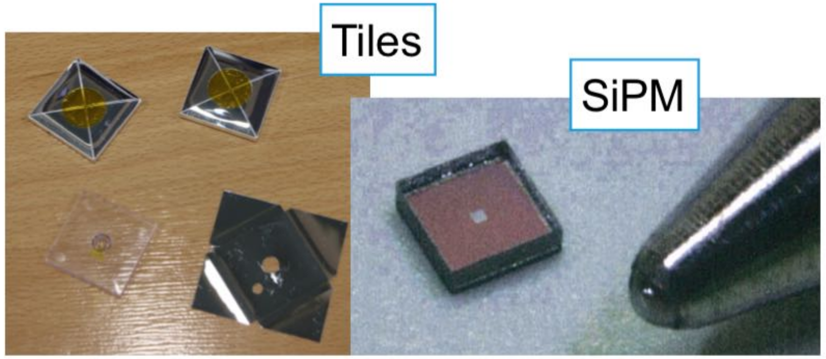


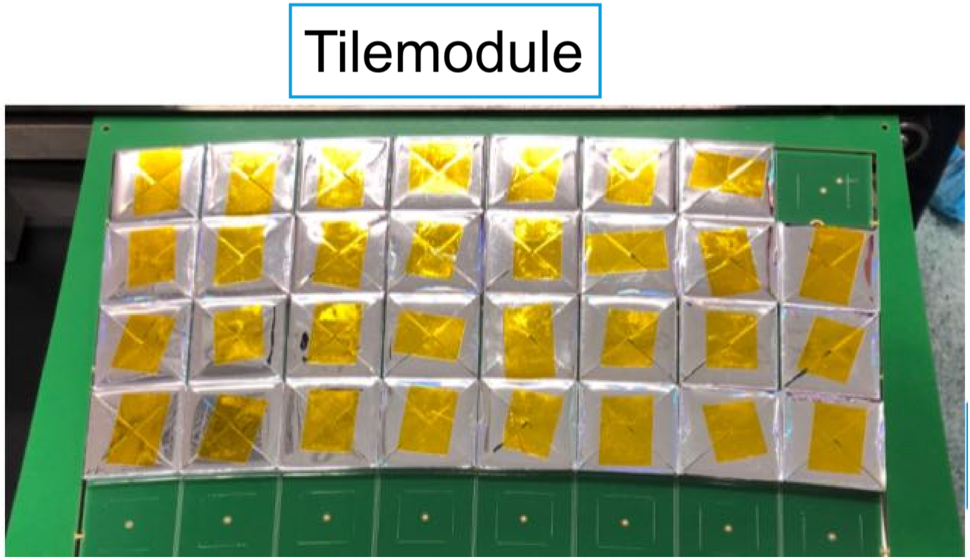


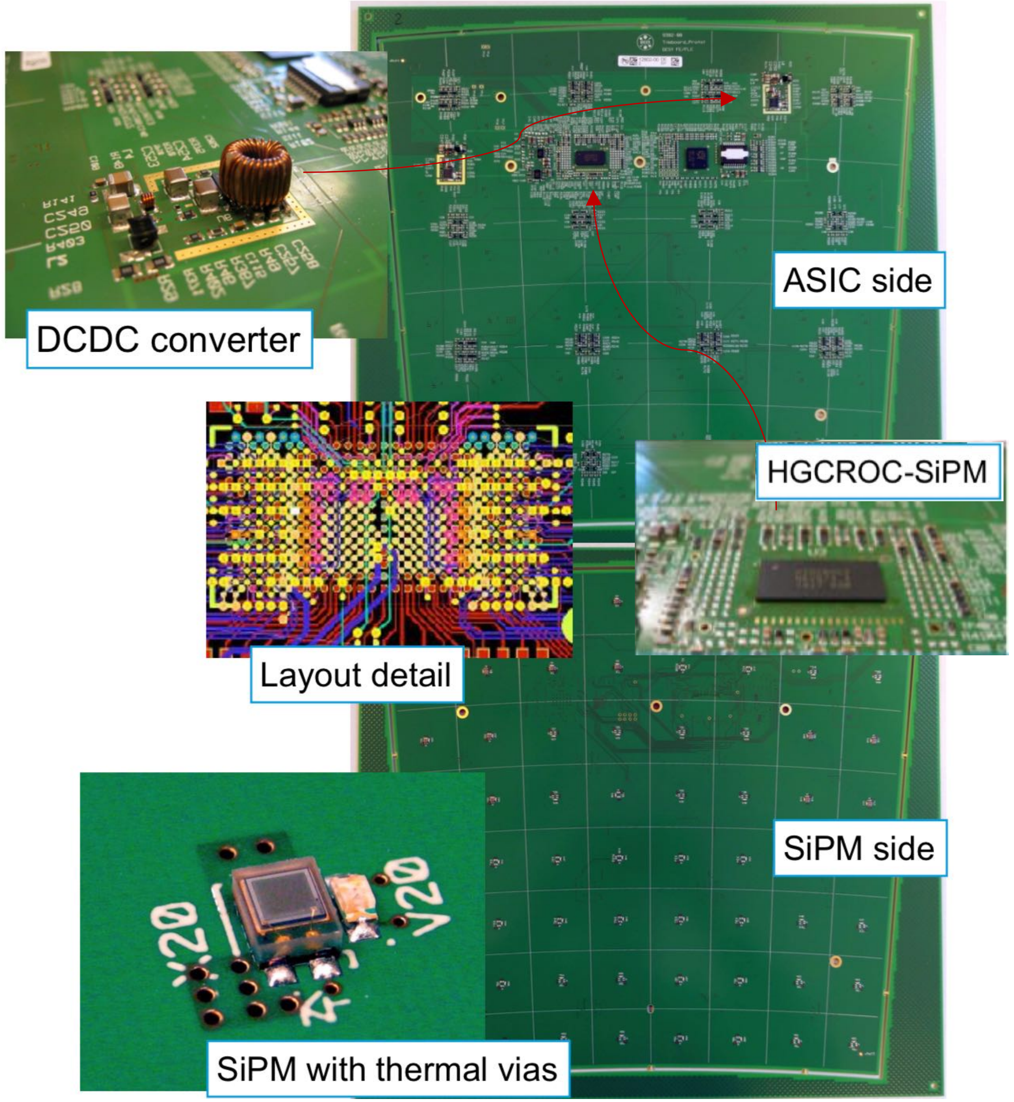
8" Silicon Sensors

CMS HGCAL: SiPM-on-Tile Module Development

SiPM-on-Tile Modules







CMS HGCAL: HGCROC Development

Front-End Electronics

HGCROC2

HGCROC2 is the full size in terms of channels.
It has most of the analog functionality.

The digital part does not include the L1 Buffer.
It is also not fully designed for SEE in this prototype.

Overall chip divided in two symmetrical parts
- 1 half is made of:
  - 39 channels: 18 ch, CM0, Calib, CM1, 18 ch (78 channels in total)
  - Bandgap, voltage reference close to the edge
  - Bias, ADC reference, Master TDC in the middle
  - Main digital block and 3 differential outputs (2x Trigger, 1x Data)

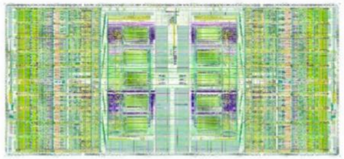
Measurements
- Charge
  - ADC (AGH): peak measurement, 10 bits @ 40 MHz, dynamic range defined by preamplifier gain
  - TDC (IRFU): TOT (Time over Threshold), 12 bits (LSB = 50ps)
  - ADC: 0.2 fC resolution. TOT: 2.5 fC resolution
- Time
  - TDC (IRFU): TOA (Time of Arrival), 10 bits (LSB = 25ps)

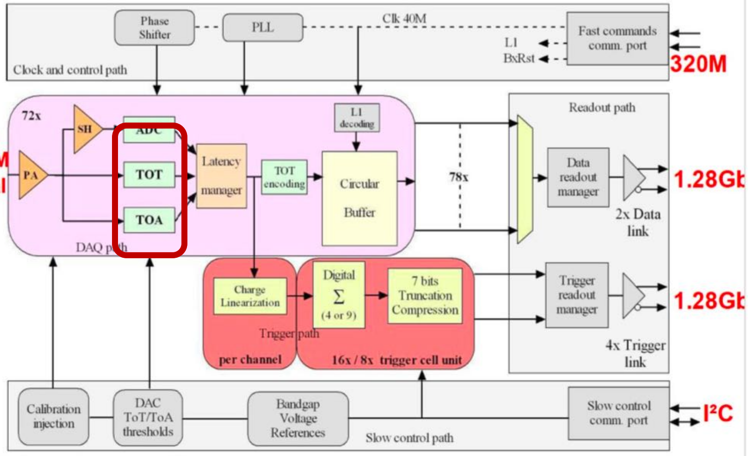
Two data flows
- DAQ path
  - 512 depth DRAM (CERN), circular buffer
  - Store the ADC, TOT and TOA data
  - 2 DAQ 1.28 Gbps links
- Trigger path
  - Sum of 4 (9) channels, linearization, compression over 7 bits
  - 4 Trigger 1.28 Gbps links

Control
- Fast commands
  - 320 MHz clock and 320 MHz commands
  - A 40 MHz extracted, 5 implemented fast commands
- I2C protocol for slow control

Ancillary blocks
- Bandgap (CERN)
- 10-bits DAC for reference setting
- 11-bits Calibration DAC for characterization and calibration
- PLL (IRFU)
- Adjustable phase for mixed domain

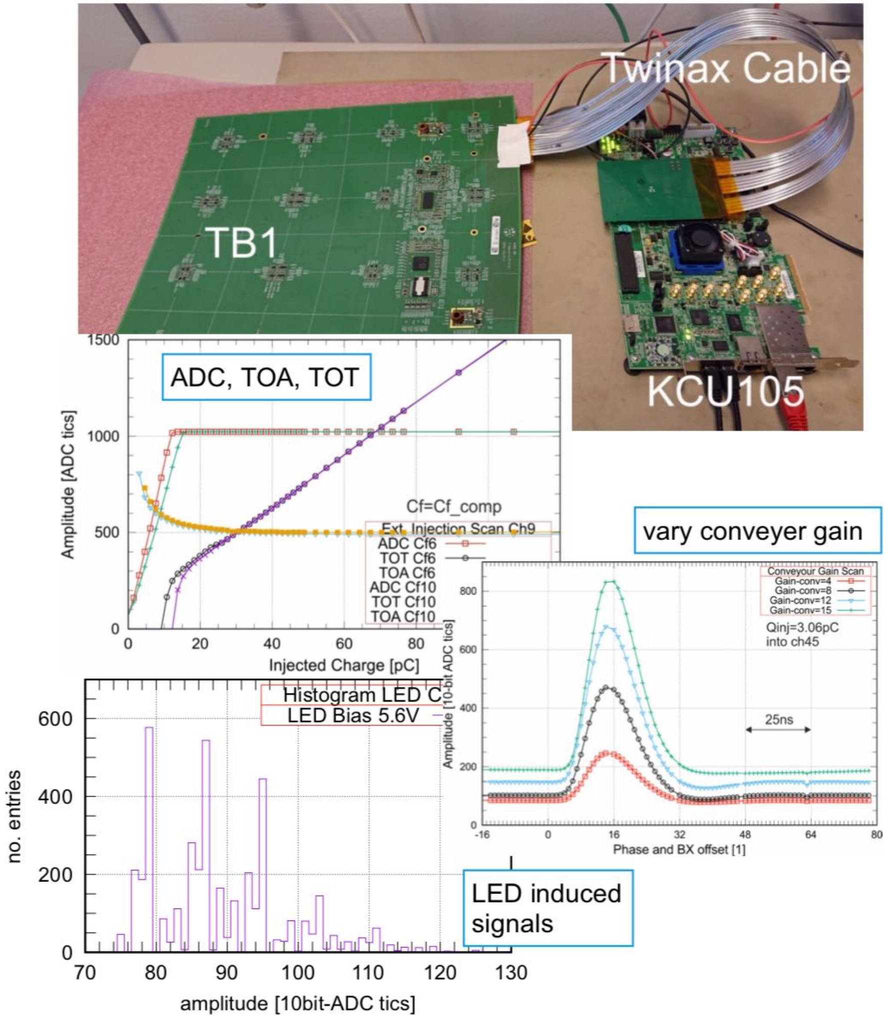
AGH
Irfu
CERN
ΩMEGA Microelectronics





HGCROC2 is currently under-going intensive testing
HGCROC1 principle concerns (digital coupling degrading noise and very limited radiation tolerance) largely resolved in HGCROC2.
HGCROC2 analog performance mostly correct with some minor areas for improvement.

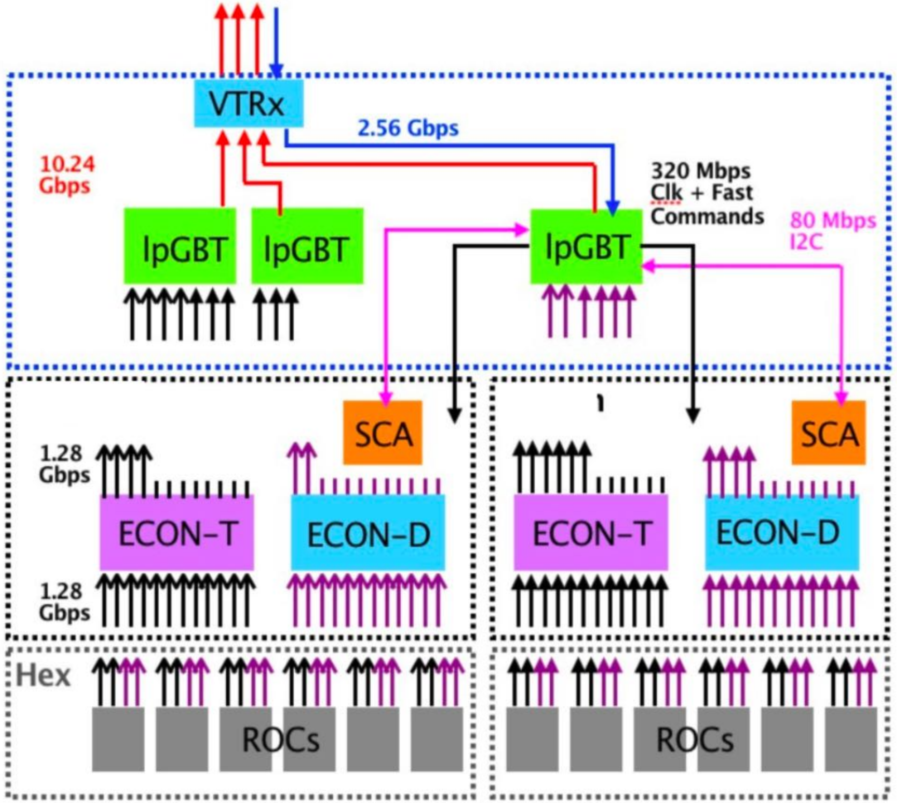
16bits effective dynamic range => ADC +TOT
Precision timing => TOA (25ps lsb)

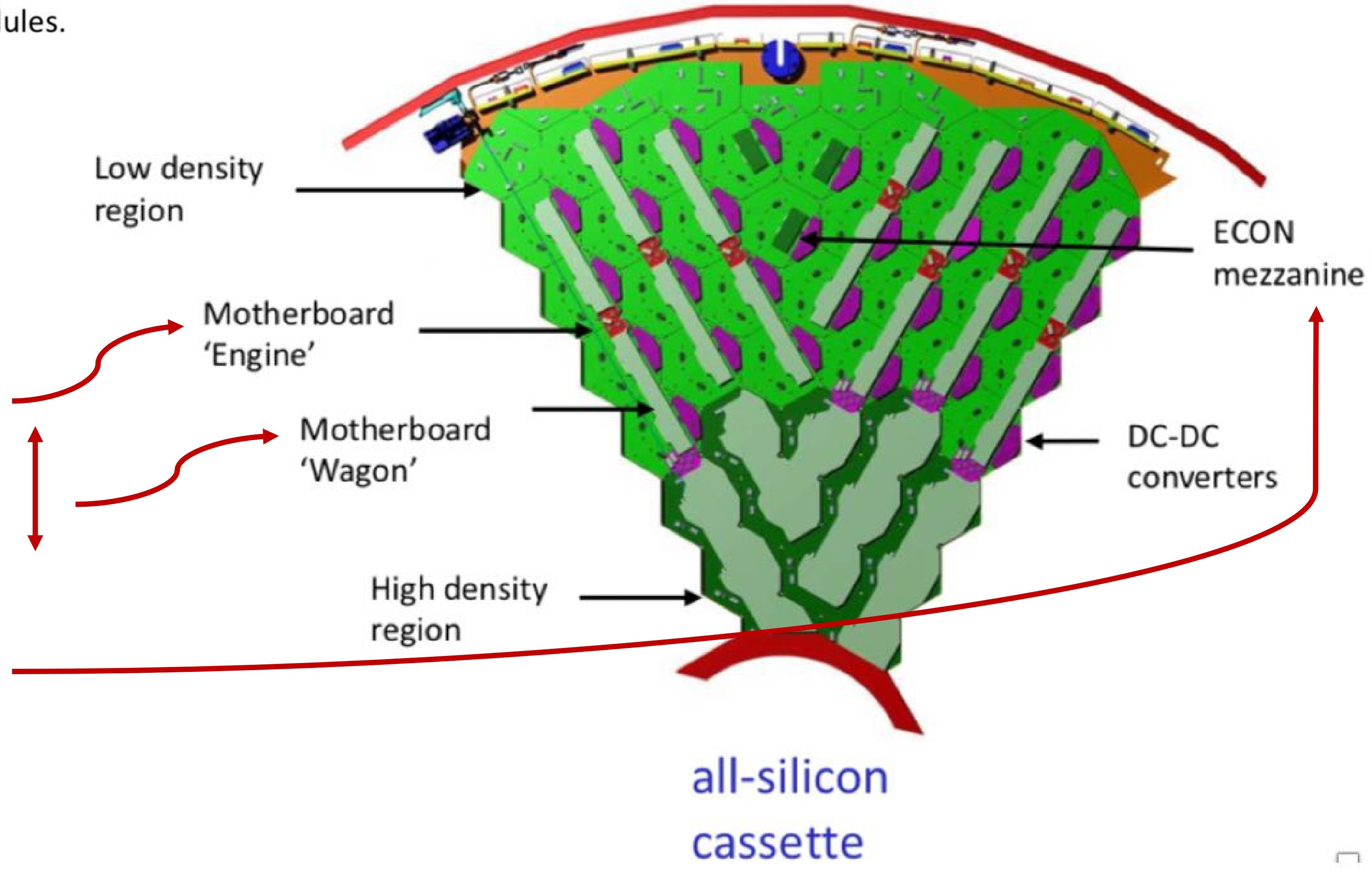


CMS HGCAL: Front-End Electronics Architecture

Front-End Electronics

Active detector organized into **cassettes**
comprised of a cooling plate with silicon and scintillator modules.
Front-end electronics on the modules
Readout and control through motherboards
Powering via DCDC converters now located at the front-end





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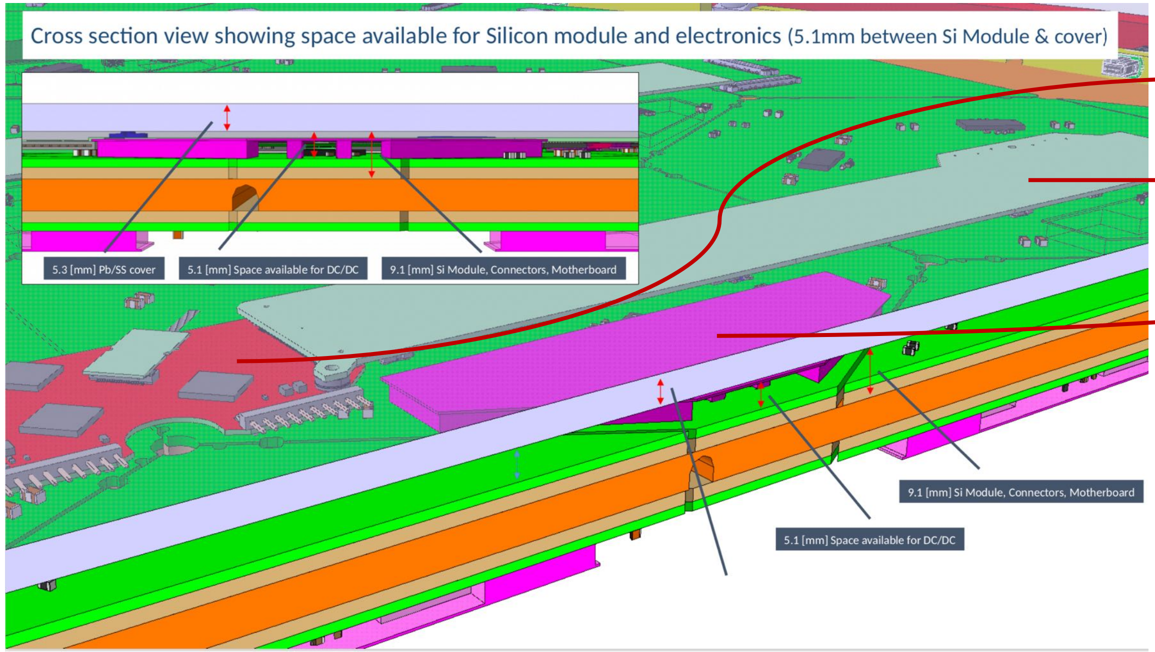

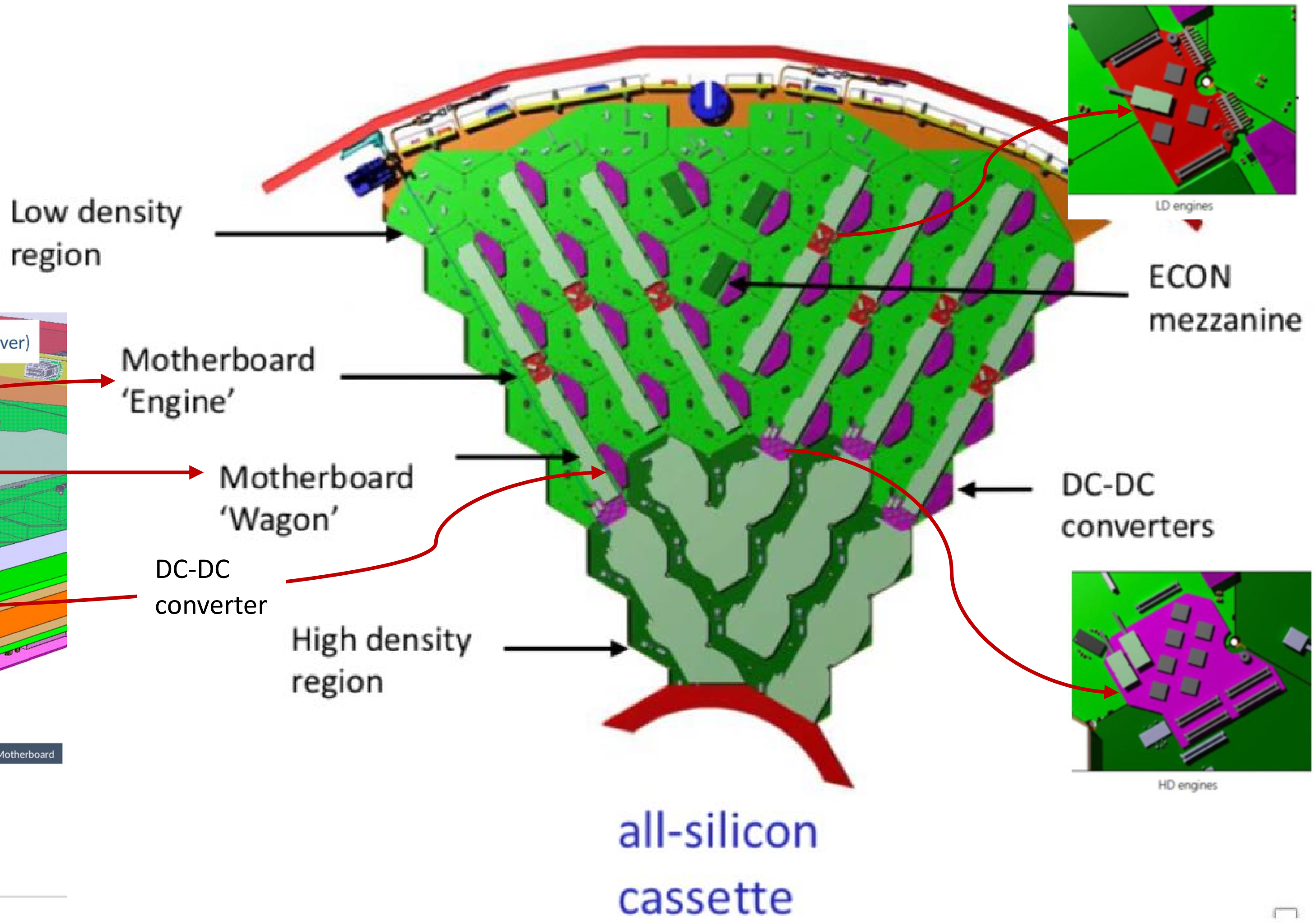

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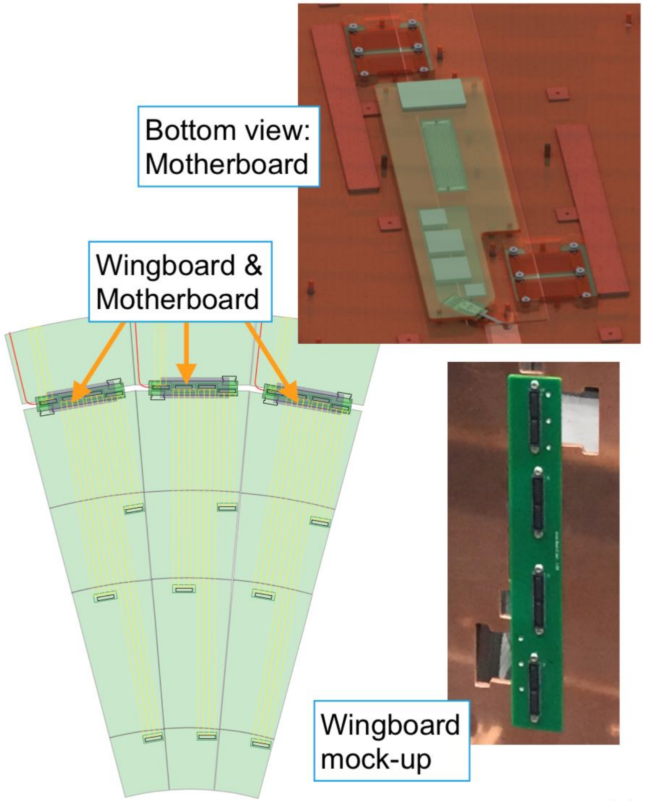
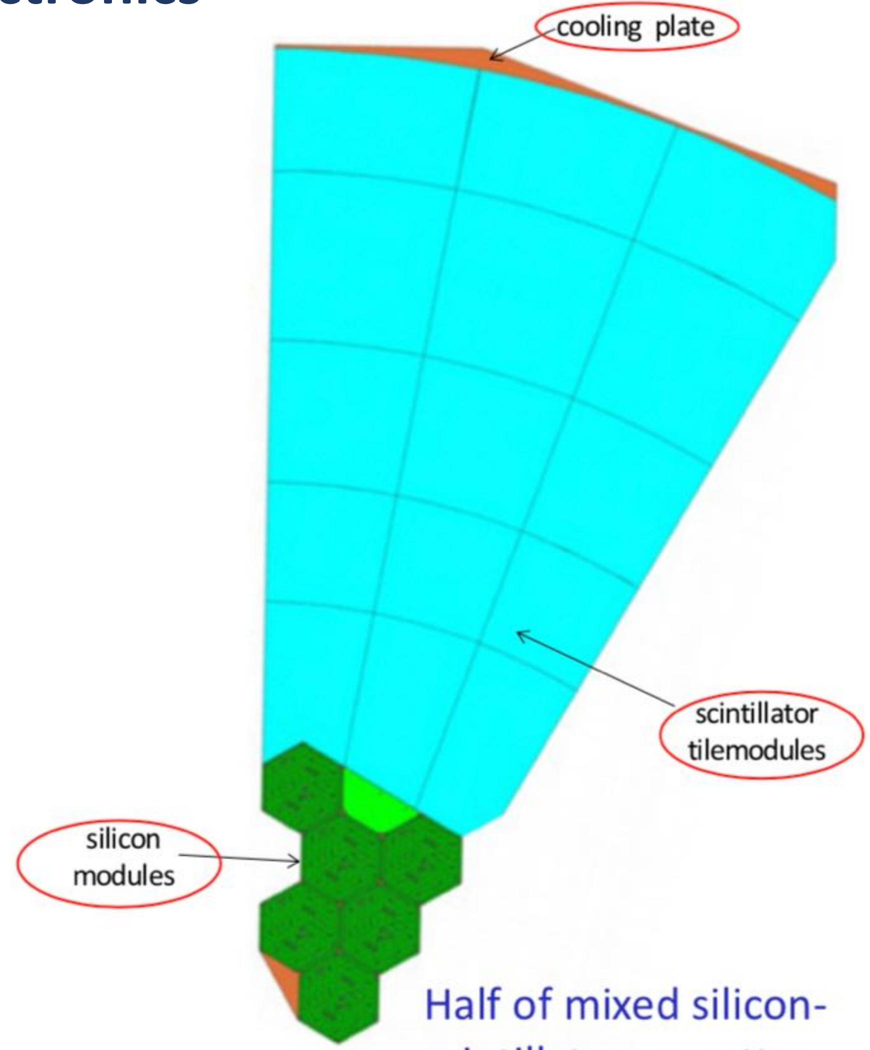
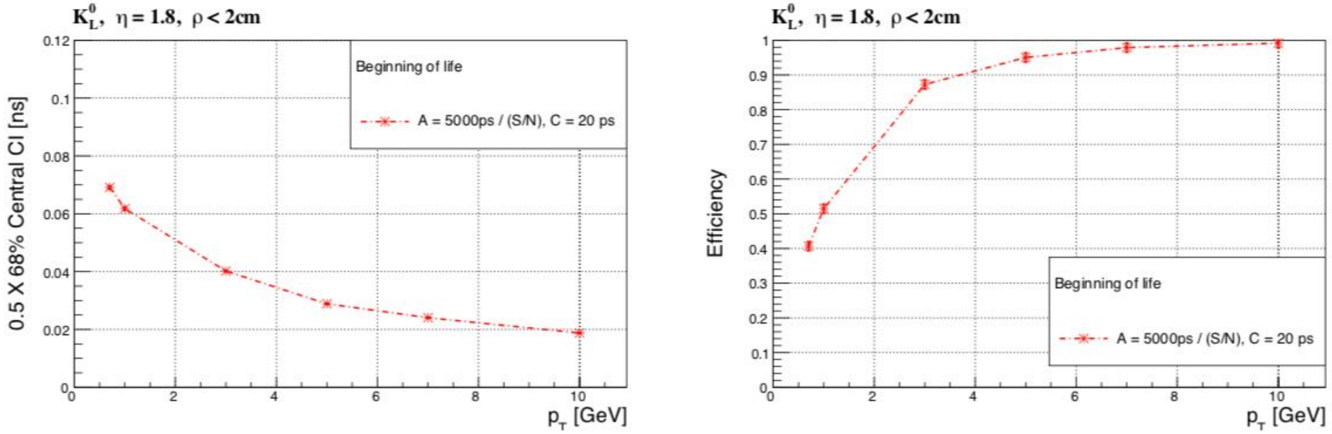


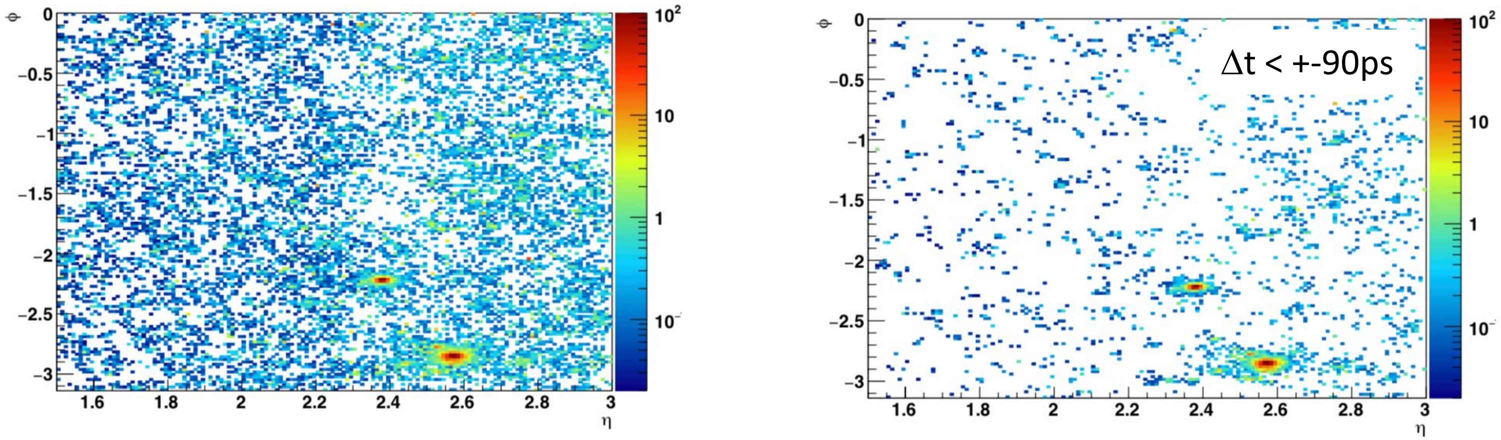


Half of mixed silicon-scintillator cassette

HGCAL Precision Timing and PU mitigation



HGCAL Timing response for neutral hadrons

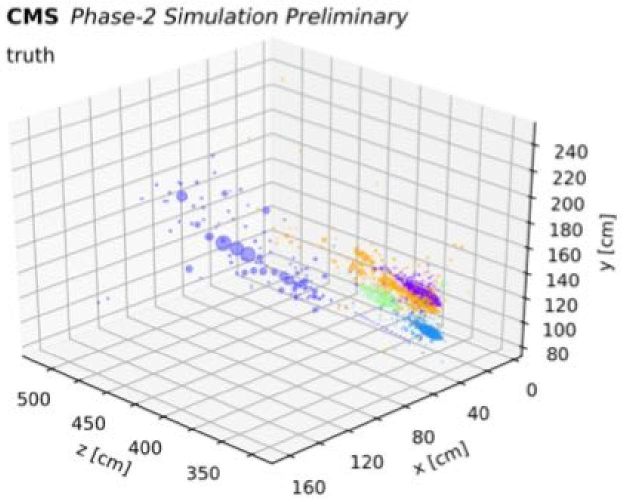


HGCAL PU mitigation with Precision Timing H -> $\gamma\gamma$, PU = 200

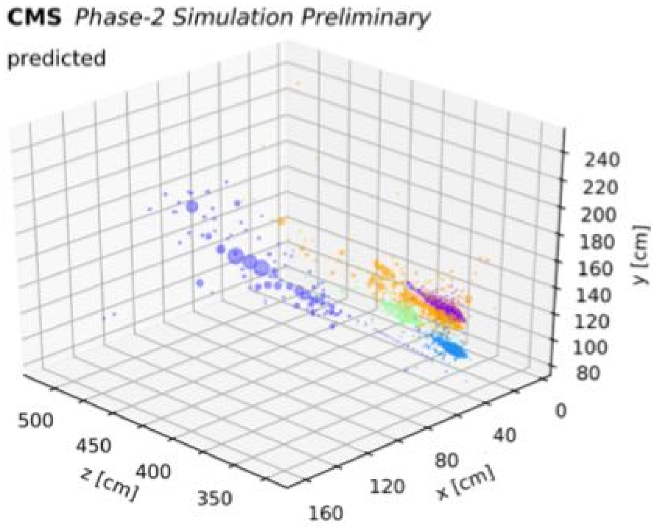
CMS HGCAL: Pattern Recognition and Reconstruction

ML Exploration: Dynamic Graph Networks

- Using graph neural networks for reconstruction arxiv:1801.07829v2
- Developed dedicated dynamic space transformation networks: GravNet arxiv:1902.07987

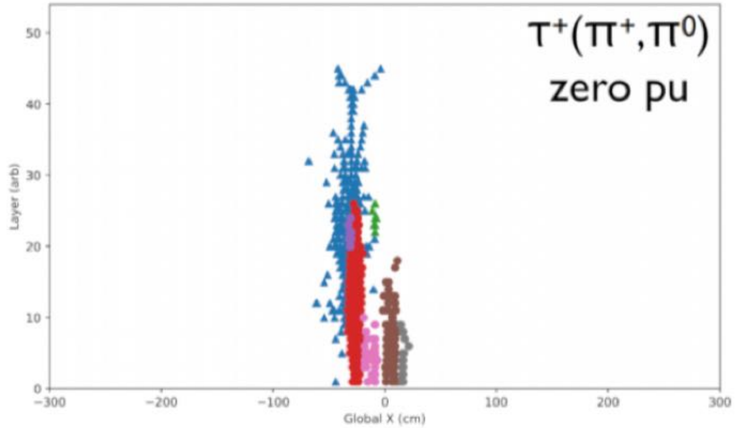


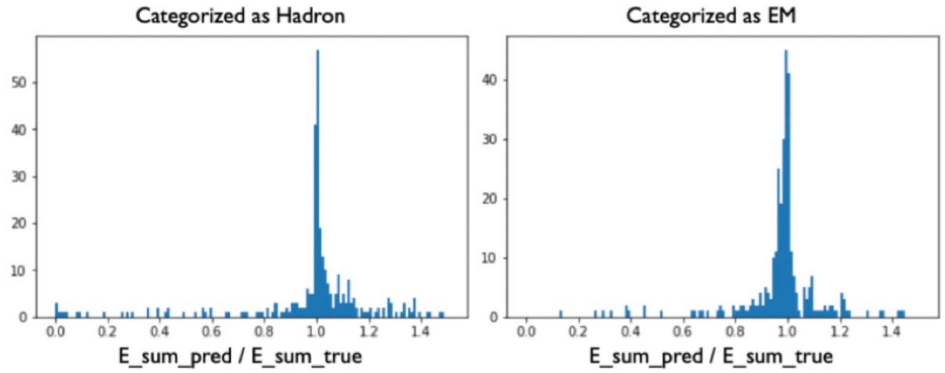
GravNet Results



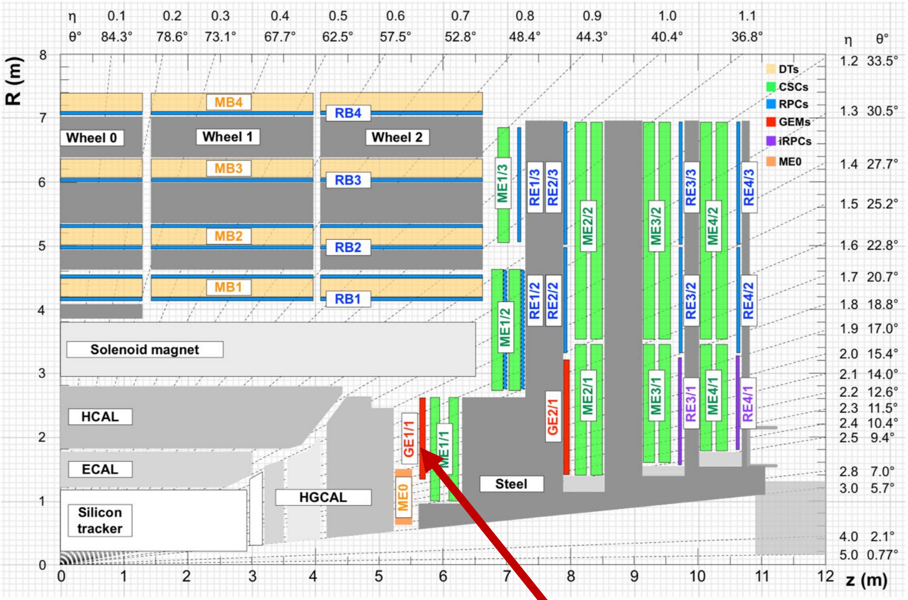
Edge Classifier Results

- Edges are used to group together points of the same particle type
  - Individual decay products of taus clearly separable (triangles - hadron, circles - EM)
  - Good reconstruction of reconstructable energy (E_sum_true) using these clusters
- Accurate separation of EM vs. HAD energy across multiple clusters

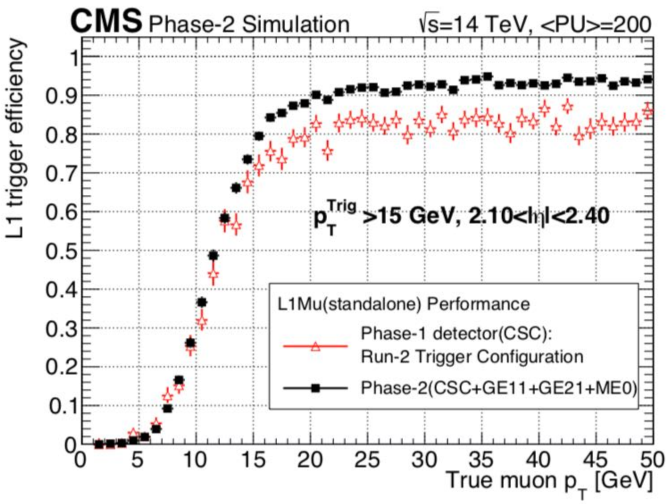


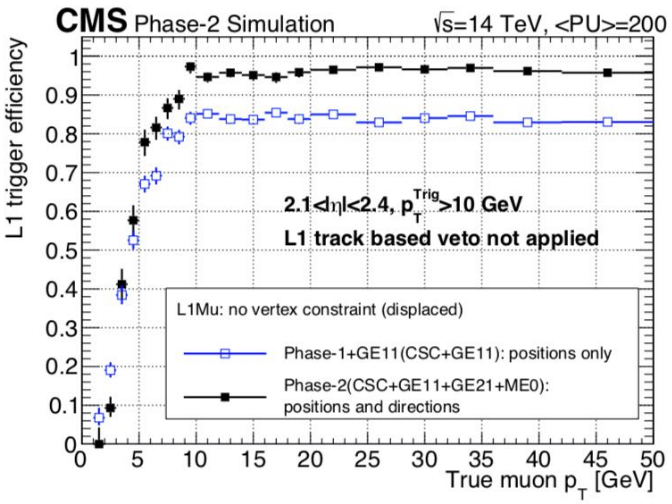


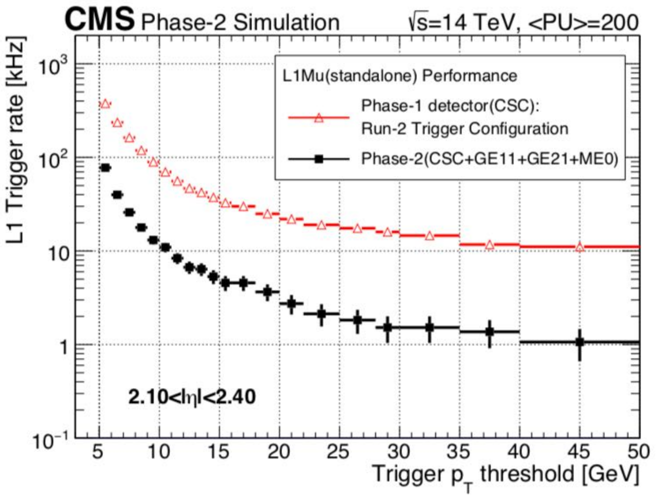
CMS HL-LHC Muon System: GE1/1

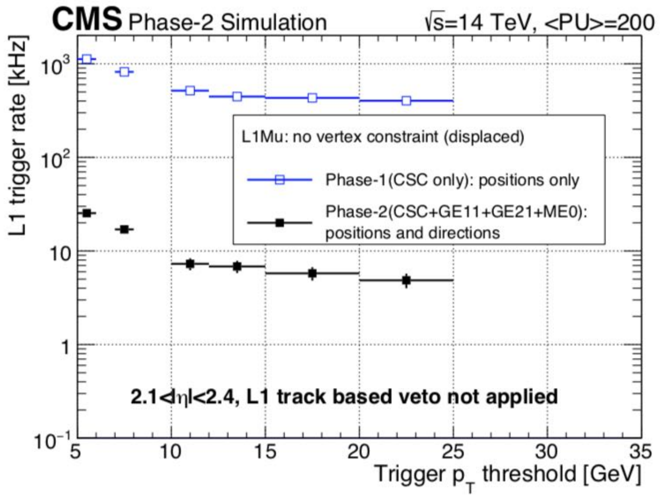


GE1/1



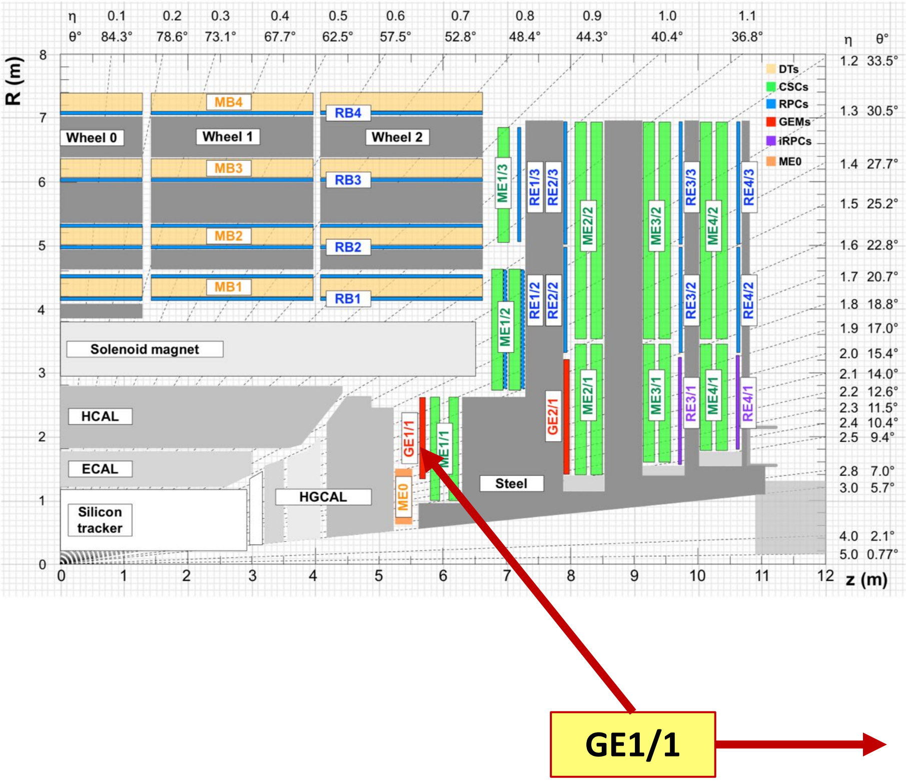






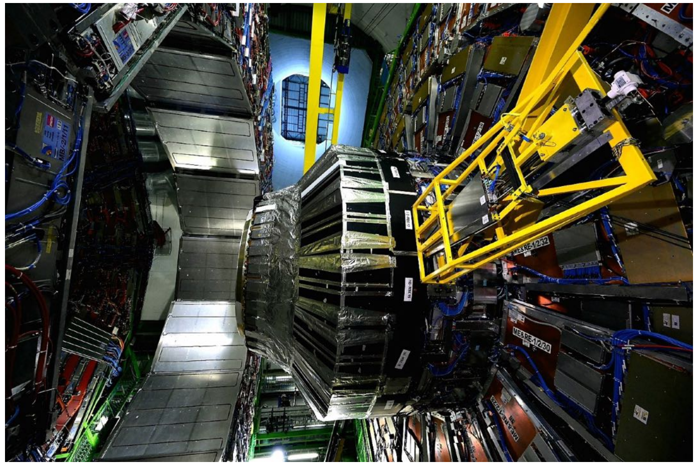
Improved L1 μ Trigger
in challenging EndCap region:
O(10) rate reduction AND improved efficiency

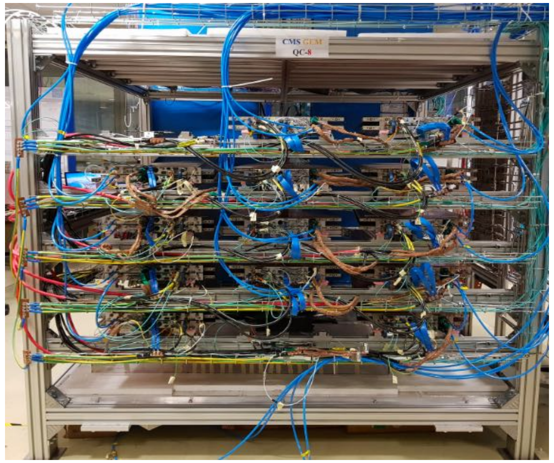
CMS HL-LHC Muon System: GE1/1



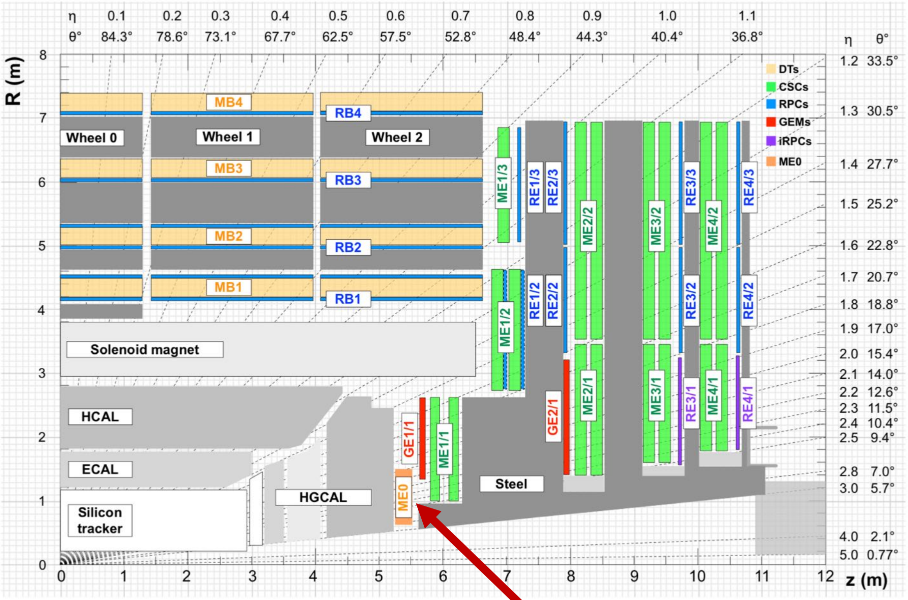
Improved L1 μ Trigger
in challenging EndCap region:
O(10) rate reduction AND improved efficiency

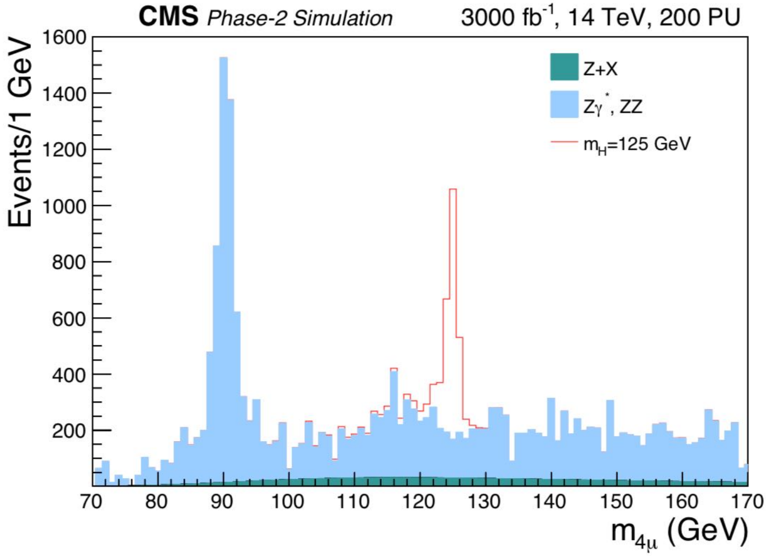
- **Installation of the first full disc (negative side) ended on Oct 24th**
  - After connection of services commissioning started
  - Second GE1/1 disc (positive side) was planned for Summer 2020, GEM super-chambers are in the final cosmic test stand
- **This will be the first new Phase-2 detector installed in CMS**





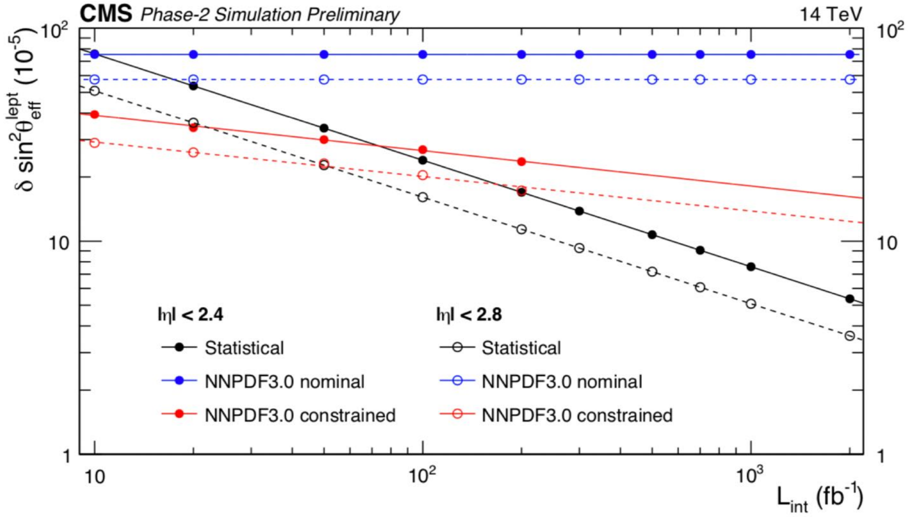
CMS HL-LHC Muon System: ME0



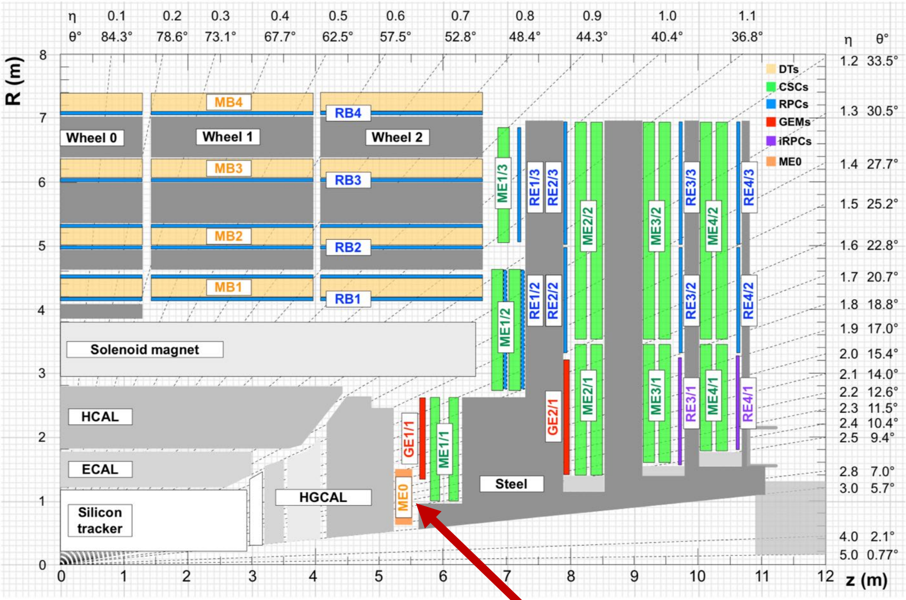


ME0

Extended μ coverage, up to η=3
In combination with extended Tracker coverage
And profiting from denser, more compact, HGCAL



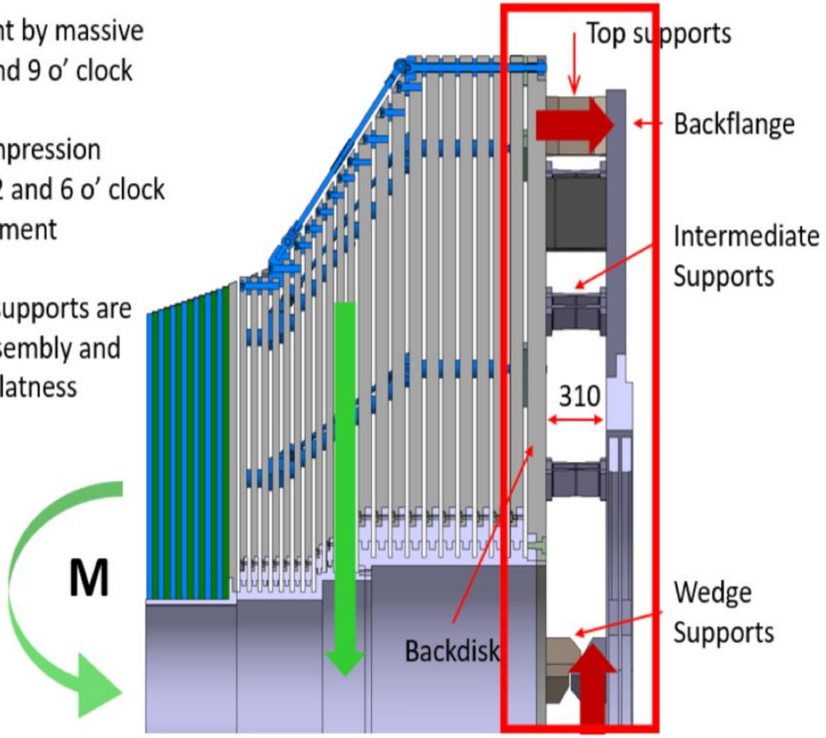
CMS HL-LHC Muon System: ME0

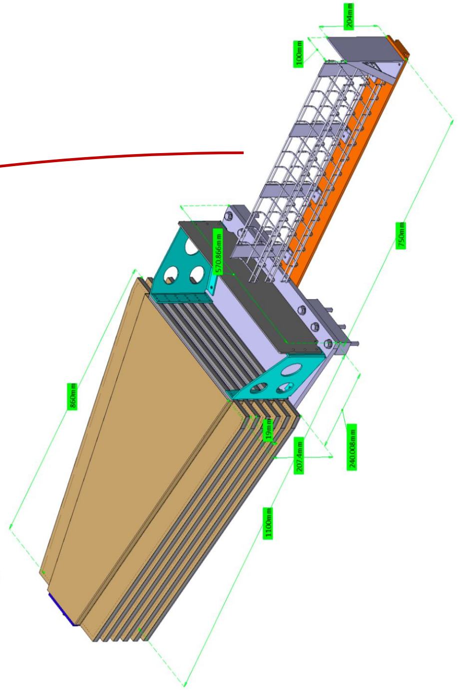


ME0

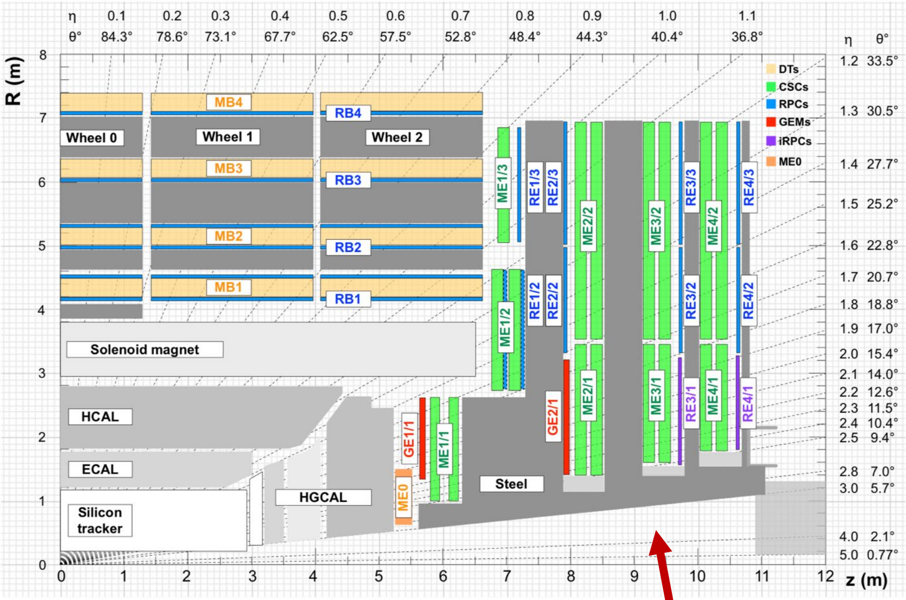
Extended μ coverage, up to η=3
In combination with extended Tracker coverage
And profiting from denser, more compact, HGCAL

1. Take the weight by massive wedges at 3 and 9 o' clock
2. Tension & Compression reactions at 12 and 6 o' clock due to the moment
3. Intermediate supports are needed for assembly and to guarantee flatness



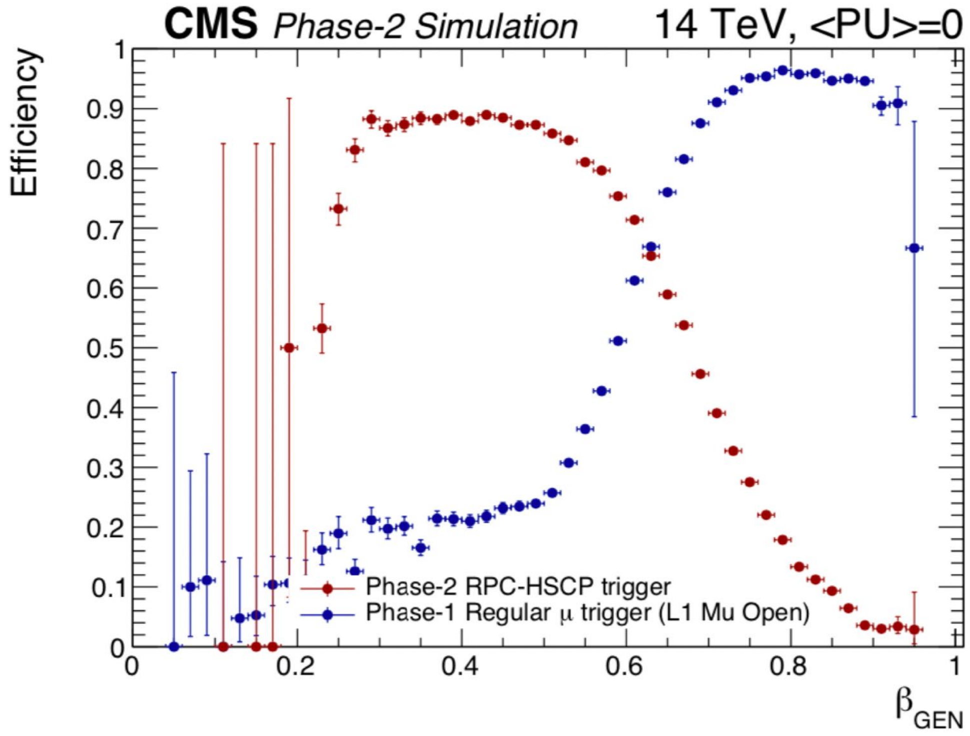


CMS HL-LHC Muon System: RPC Timing



RPC Timing

Improved redundancy with new RE3/1 & RE4/1 RPC
Fully exploit intrinsic timing resolution => eg HSCP @ L1



CMS HL-LHC Upgrade: ASICS

Common ASISCS: CERN

ASICS	HGCAL	Tracker	MTD	BCAL	Muons
IpGBT	x	x	x	x	x
VTRx+	x	x	x	x	x
BPOL12V	x	x	x		
BPOL2V5	x	x	x		
FEAST				x	x
GTB-SCA	x		x	x	
RD53B		x			

System Specific ASISCS: Collaboration Institutes with CERN Support

Systems					
Tracker	*CBC*	***SSA***	***MPA***	***CIC***	
BCAL	**LiTE-DTU**	*CATIA*			
HGCAL	*HGROC*	**ECON-D**	***ECON-T***	ALDO	LDO
MTD	*TOFHIR*	**ETROC**	ALDO*		
MUON	*VFAT*	*PETIROC*			

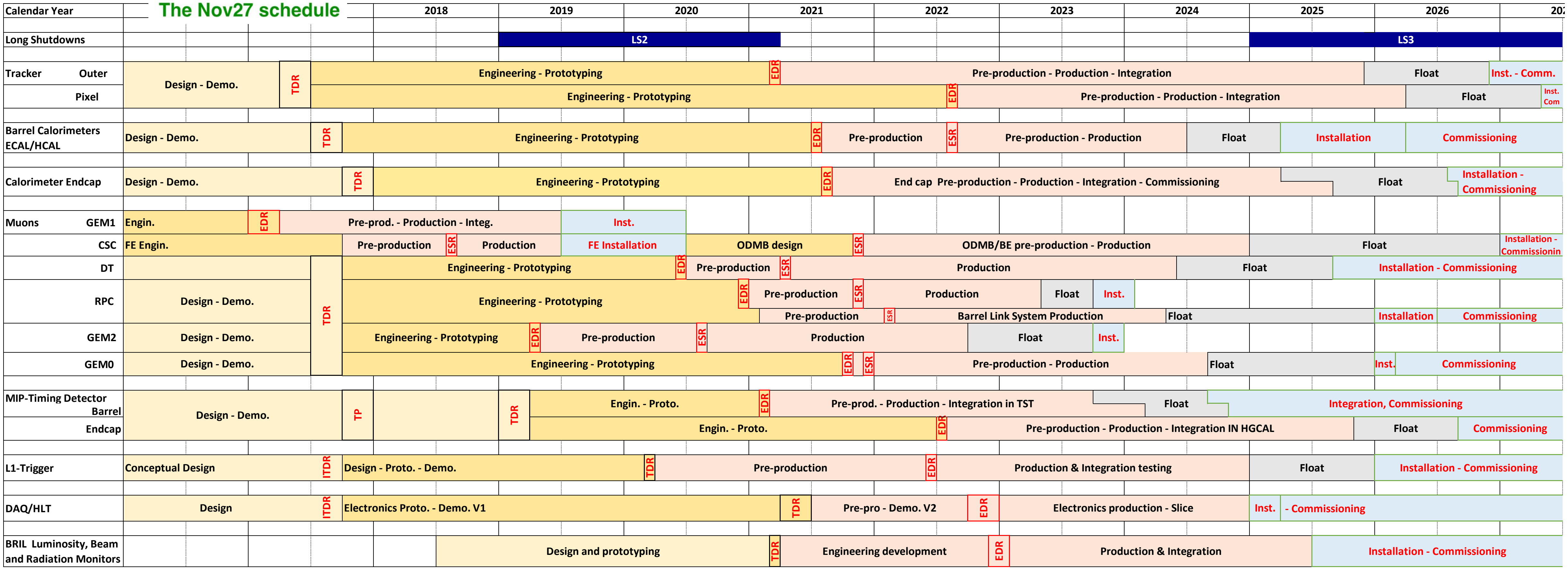
65nm *130nm*

CMS HL-LHC Upgrade: Schedule

CMS Phase-2 schedule, taking into account the additional year reflected CERN's November 27th schedule

→ no Covid-19 correction

Most of the additional year used to increase the overall float, a fraction invested for risk mitigation



CMS HL-LHC Upgrade: Summary and Outlook

In view of the unprecedented challenges of the HL-LHC environment and physics program

- the CMS Upgrade program introduces new paradigms
  - p_T modules for L1 Trigger Tracking, HGCAL, and Precision Timing for PU mitigation
- breaks new ground in detector technology
  - very large scale deployment of 8” Silicon Sensors, radiation hard SiPMs, LGADs, GEMs
- TDAQ and computing

- The Upgrade program is underpinned by a broad ASICs development program for both common applications
  - lpGBT, VTRx+, BPOL12V, BPOL2V5, FEAST, GBT-SCA, RD53
- and detector specific designs

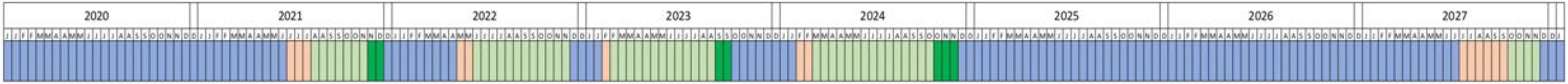
CMS HL-LHC Upgrade: Summary and Outlook

- The CMS HL-LHC upgrade program is by necessity ambitious, and many challenges still lie ahead
- With the completion of the TDRs for the major detectors, and the submission of the Trigger TDR, the CMS upgrade projects are now advancing well in the development phase and preparation for production
- The additional year foreseen in the "November 17" CERN schedule allows to
  - set aside more time as necessary to mitigate technical risks
  - while restoring a ~ 12 month master float for contingency
- This, together with the commitment and support of CERN and of all the Collaborating Funding Agencies and Institutes, provides a solid footing for successful completion of the HL-LHC Upgrade and physics program

Backup Material

CMS HL-LHC Upgrade: from Concept towards Construction

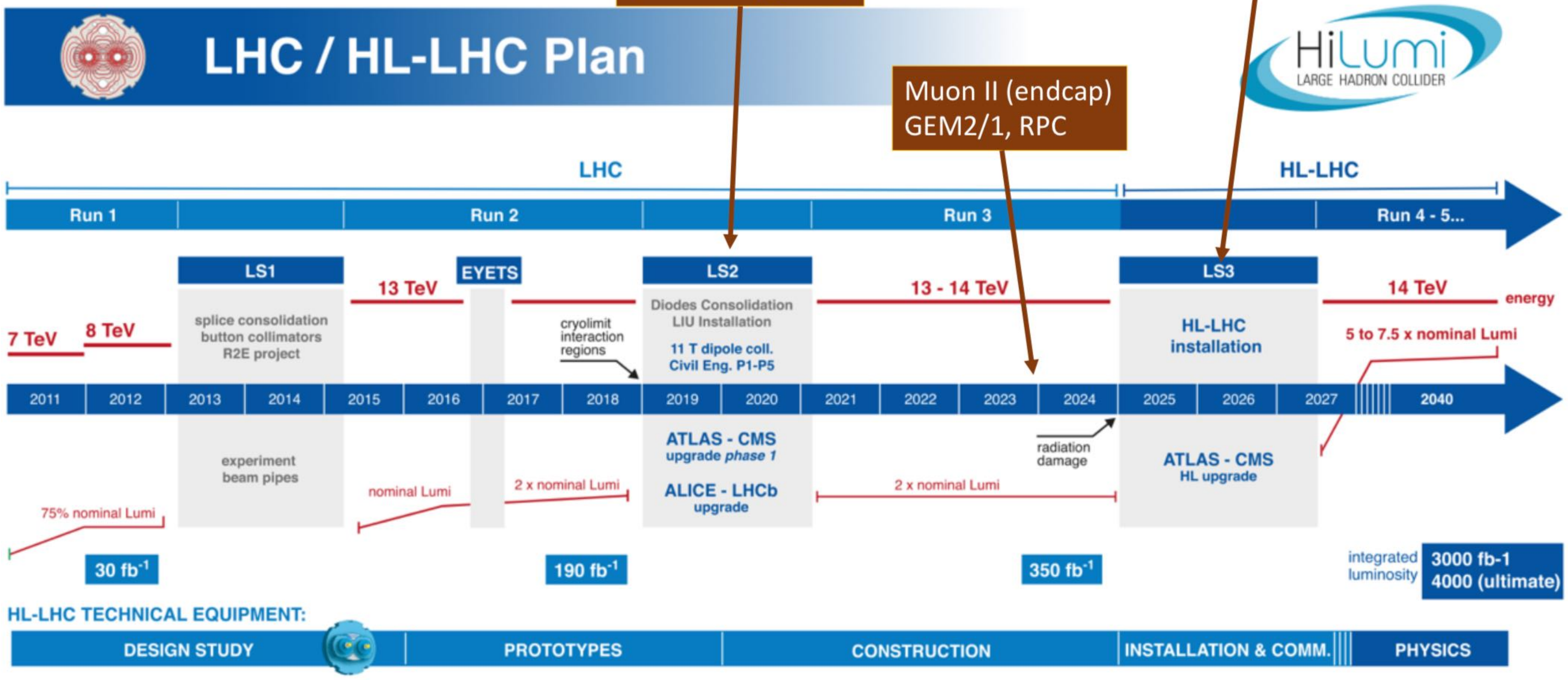
The Nov27 schedule



Muon I (endcap)
CSC, GEM1/1
(Phase-2 upgrade)

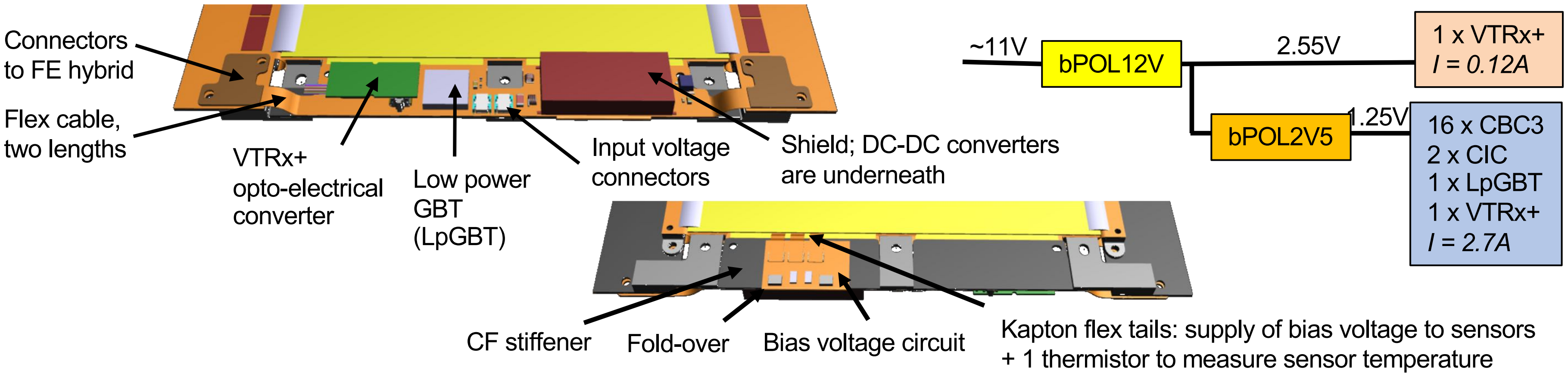
BCAL, Tracker, HGCAL,
MTD, Muon III (barrel), ME0

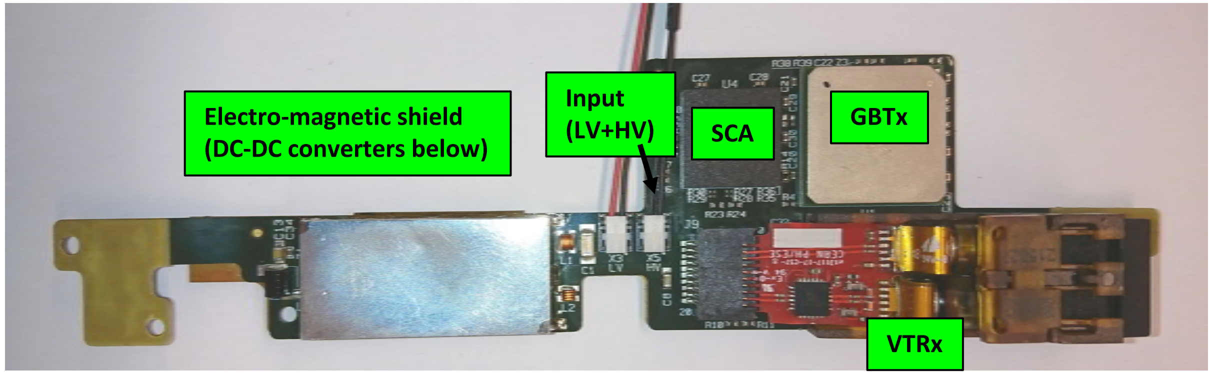
Muon II (endcap)
GEM2/1, RPC



CMS HL-LHC Tracker: p_T Module Development

2S SEH: Powers the module hybrids and transmits the readout data



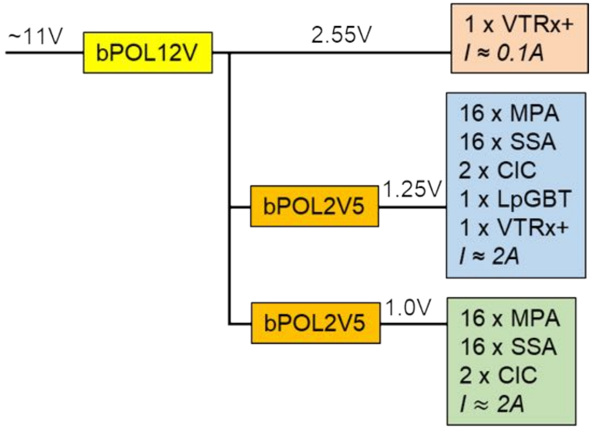


Demonstrator prototype

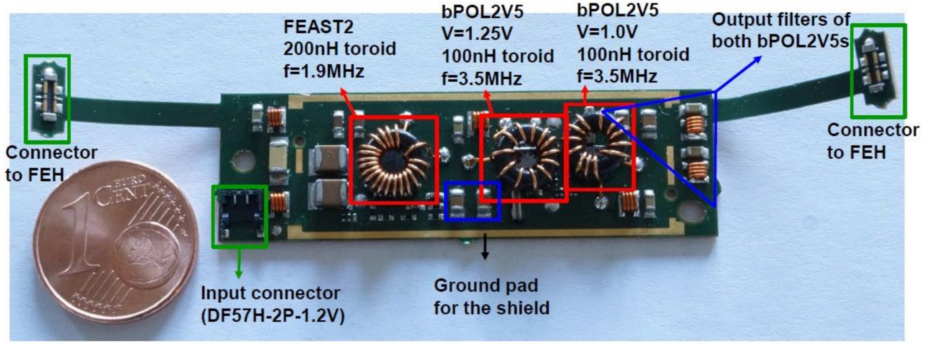
- **Features full functionality, but uses predecessors of final active components:**
  - **GBTx + SCA, VTRx, FEAST2.1, commercial DC-DC converter**
- **Used for DAQ and hybrid test system development, module assembly tests, system tests and test beam experiments**

CMS HL-LHC Tracker: p_T Module Development

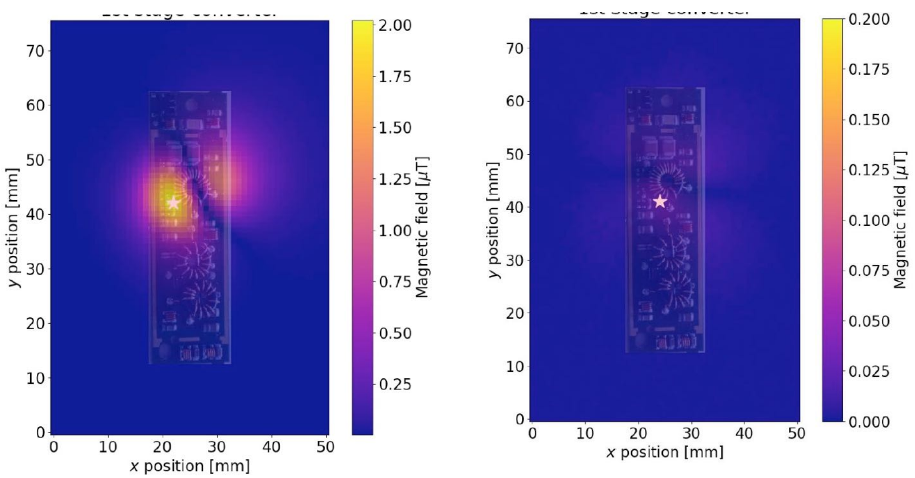
PS Power Hybrid (POH)



- **First prototype of the POH, using FEAST2.1 (1st stage) and 2 x bPOL2V5 (2nd stage)**



Magnetic field scans of 1st DC-DC stage: effect of shield



CMS HL-LHC MTD: BTL sensor response

Figure 2.4: Top left: Set of 11 × 11 × 3 mm^3 LYSO:Ce crystals with depolished lateral faces, before and after Teflon wrapping. Bottom left: 6 × 6 mm^2 HPK SiPMs glued on LYSO crystals. Right: Crystal+SiPM sensors plugged on the NINO board used for test beam studies.

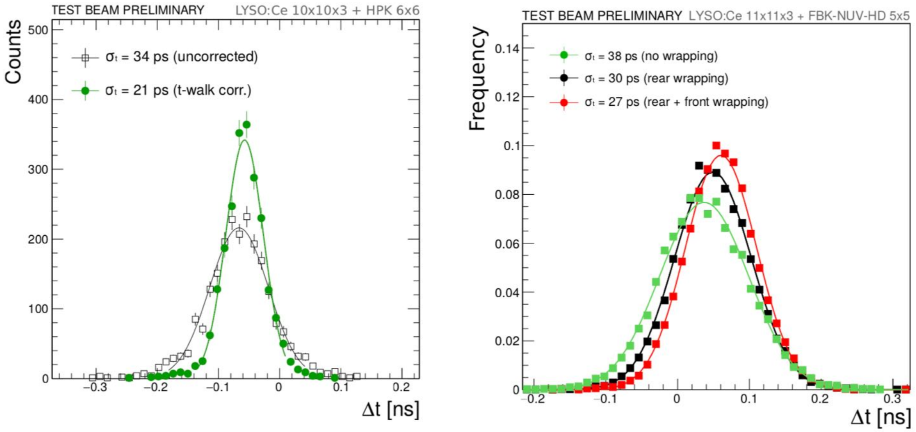


Figure 2.5: Distribution of the time difference in a pair of LYSO:Ce tiles exposed to a 3 mm wide beam of MIPs hitting the centre of the tiles. Left: Results before and after time walk correction for 10 × 10 × 3 mm^3 crystals read out with 6 × 6 mm^2 HPK SiPMs. Right: Results for 11 × 11 × 3 mm^3 crystals read out with 5 × 5 mm^2 FBK SiPMs under different wrapping configurations.

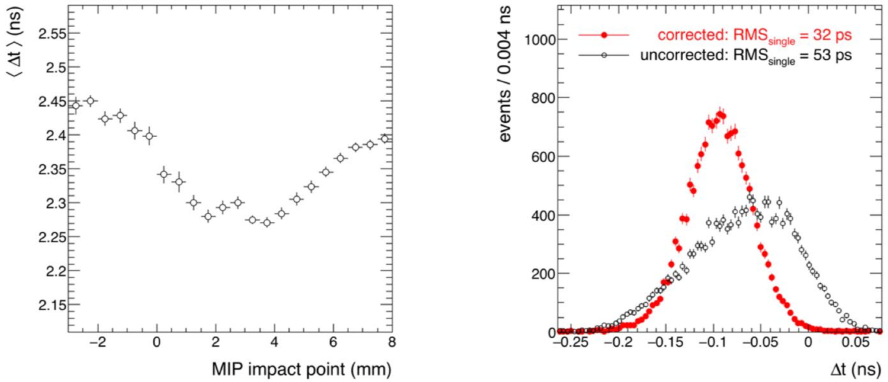
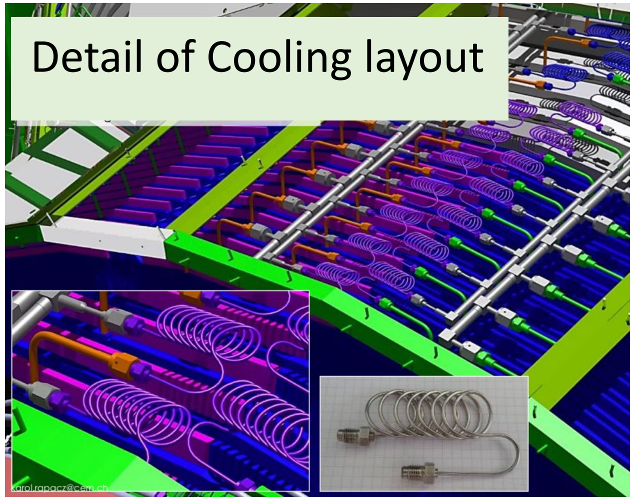
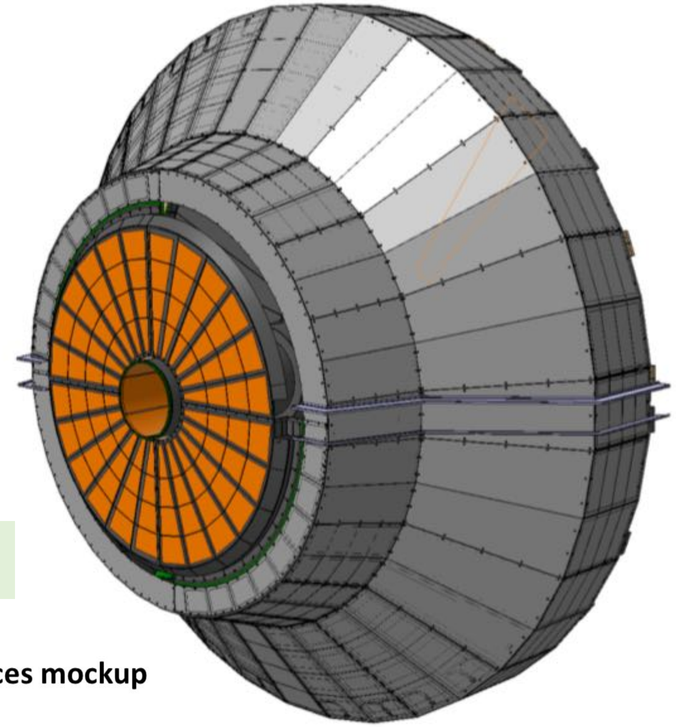


Figure 2.6: Left: Difference between the time measurements in a 11 × 11 × 3 mm^3 tile with a 5 × 5 mm^2 FBK SiPM and in a reference MCP as a function of the MIP impact point on the crystal surface. Right: Time resolution before and after the application of a position dependent correction.

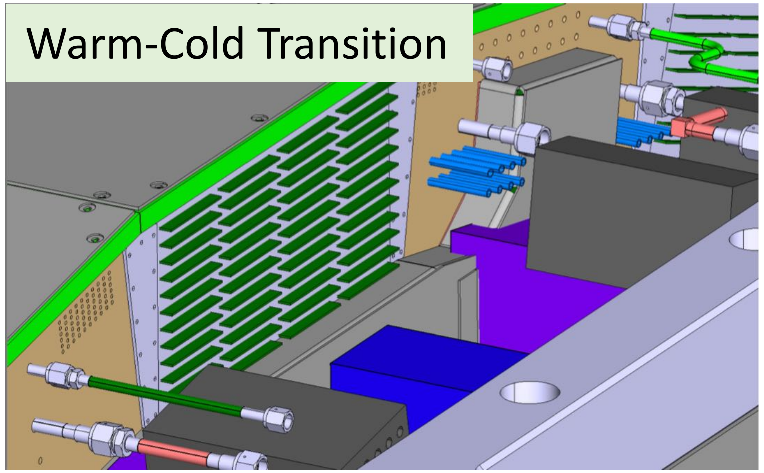
CMS HGCAL: Engineering and Integration

Detail of Cooling layout





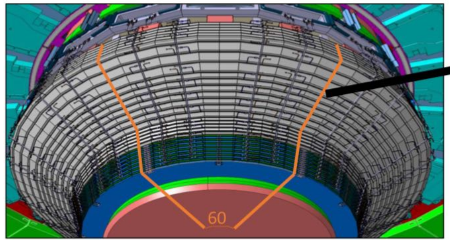
Warm-Cold Transition



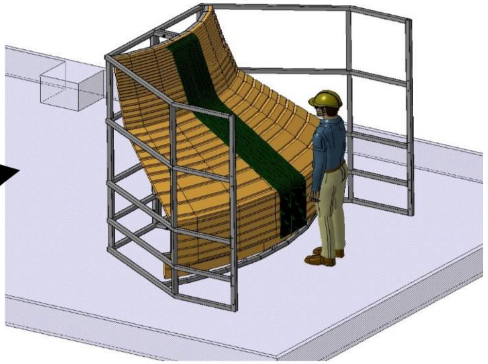
Services Integration inside Cold Volume:

Scope of the Mock-up:

-Investigate the services installation sequence within thermal screen (services thickness, cable paths)
-Choice of connectors and passage through thermal screen feedthrough
-Understand services behaviour in different orientations
-Study feedthroughs and routing services away from HGCAL
-Thermal screen design validation



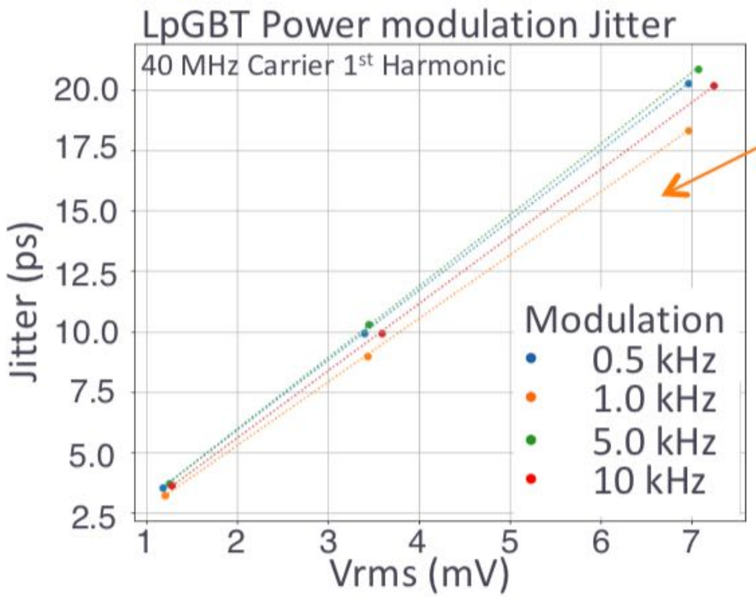
60 degree 1:1 services mockup



Services Integration over EndCap

lpGBT clock distribution studies for precision timing

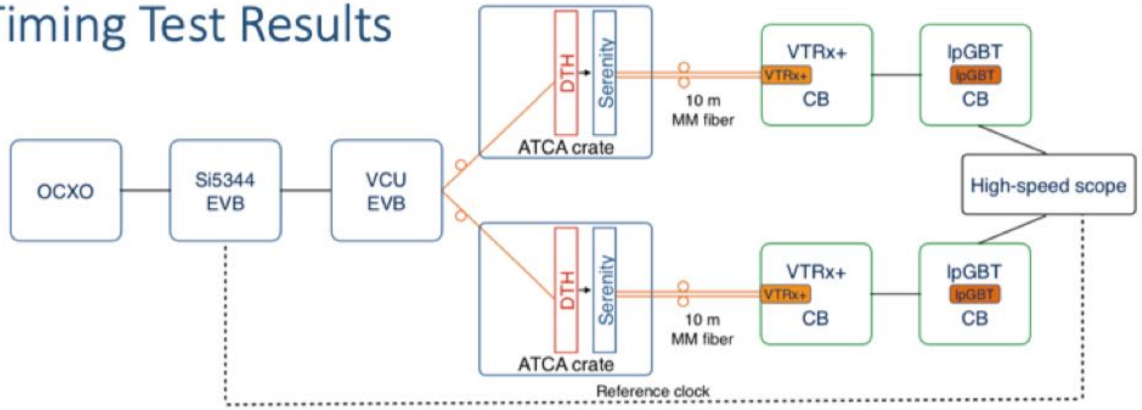
- **lpGBTv1 clock studies with a test board**
  - Two independent links through DTH + Serenity + VTRx + and lpGBTv1 test board (*):
    - Time jitter: **4 / 11 ps at 40 / 160 MHz** (ETROC / TOFHIR sampling rate)
  - Clock stability vs temperature (3 ps/^{0}C) and power voltage (3 ps/mV) → specs for FE boards
- **Clock tests with BTL RUProto1**
  - Routing of clock to FE boards show jitter within specifications (6 ps RMS at 160 MHz)
  - Full-system clock distribution tests (DTH →BE →BTL FE) after COVID lockdown



Saclay at al

lpGBT clock distribution studies for precision timing

Timing Test Results



Milestone:
CE.EL.6 Precision clock distribution scheme tested with lpGBT

- Two ATCA crates with separate power supplies are used for the tests.
- Two DTH and Serenity boards with the same configurations:
  - We have observed some differences between two lpGBTs.

- The link-to-link jitter of
  - e-clock at 40 MHz : 4 ps RMS
  - e-clock at 320 MHz : 11.9 ps RMS are observed (these are mostly due to the deterministic jitter contribution).

HGCAL specification in TDR : Clock distribution precision of 10–15 ps (RMS jitter)

Summary

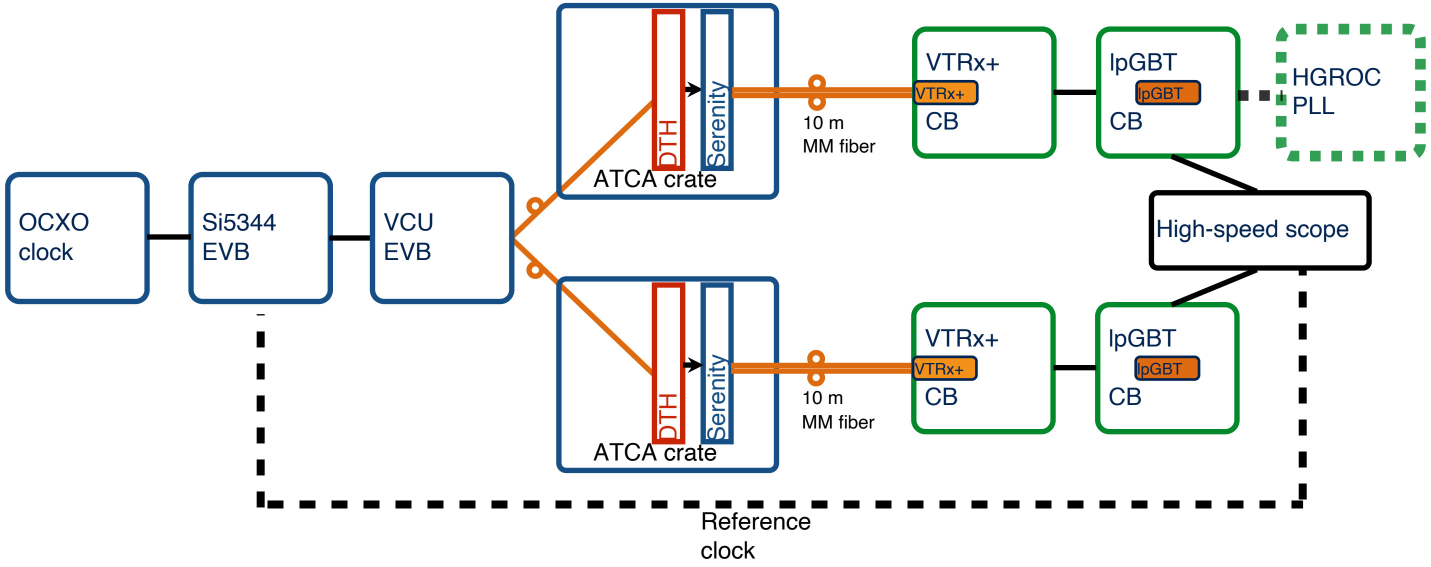
No significant jitter contribution to the clock distribution @ 40MHz, The performance at 320MHz is within HGCAL specification but with room for further improvement.

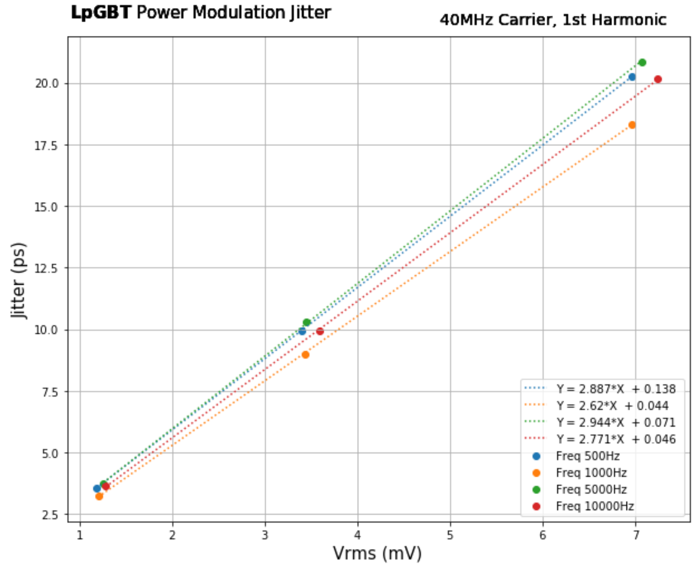
Two strong possibilities for further improvement:
- The 320MHz performance could be better after the next generation of lpGBT.
- There is also the possibility of clock cleaning via the HGCROC PLL (but this is still to be proven).

Next tests to include HGCROC2

Saclay at al

Clock distribution studies

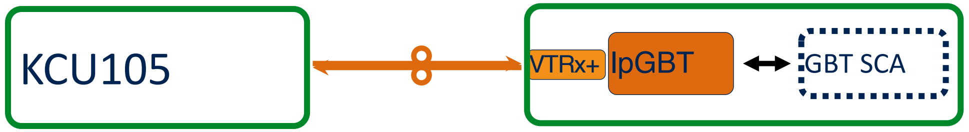


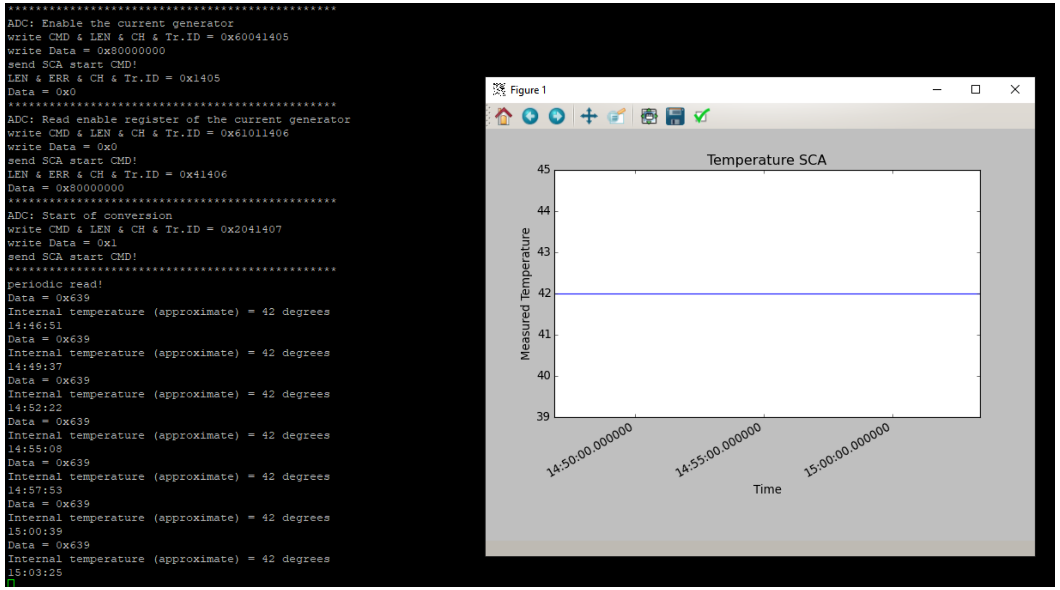


- Measurement of the clock distribution network with two independently powered ATCA crates (with two DTH boards and two Serenity boards) and two lpGBT characterization boards:
  - 12 ps RMS jitter for 320 MHz reference clock.
- In addition to the module specific tests, HGROC PLL will be included in the chain (connected to lpGBT eClocks) after the COVID19 shut down is over.
- FE motherboards and hexaboards will be added as soon as they are available.

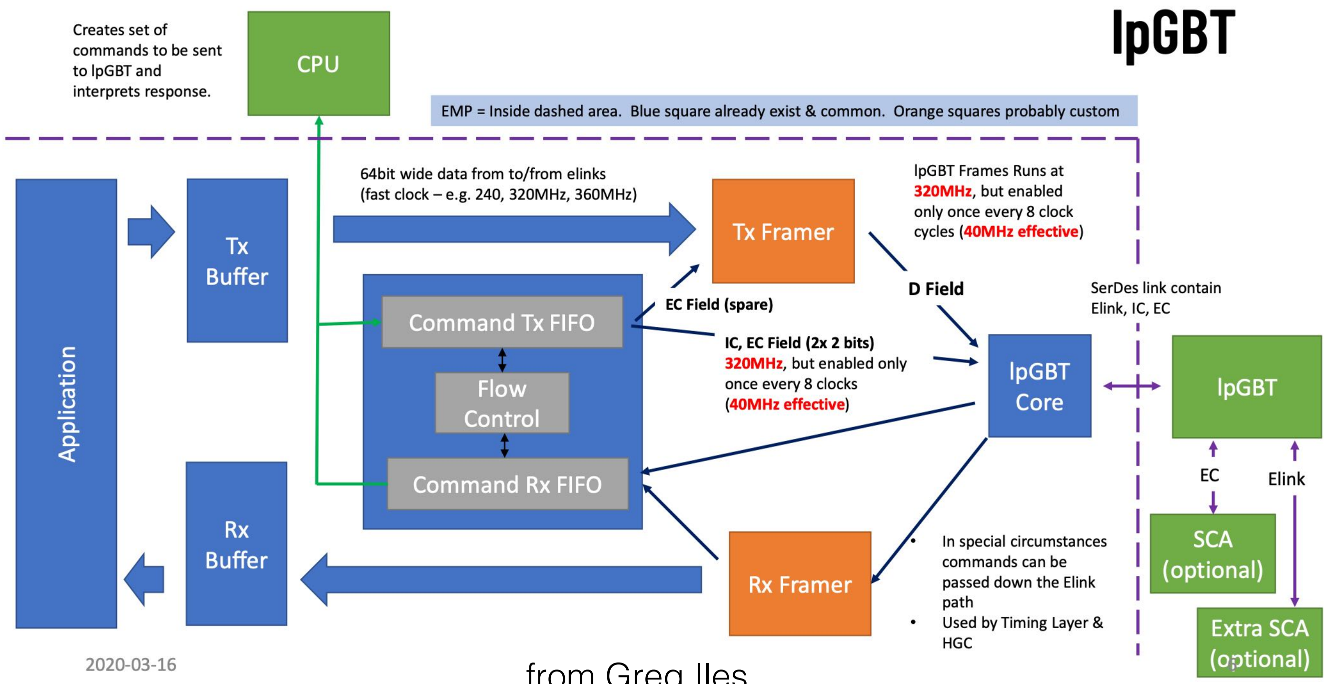
- The impact of the power modulation on the lpGBT clock distribution jitter is measured.
  - 3 ps/mV RMS is observed.
- Similar tests will be performed once the FE motherboard with lpGBT is available for these tests.
- We are also investigating techniques to monitor such shifts from the backend DAQ system via offline simulation studies, which will be embedded into the Serenity firmware (together with the HPTD timing IP).

Firmware studies





Özgür Sahin (Saclay), Kirika Uchida (Imperial) & Alexey Kozyrev (Novosibirsk)



from Greg Iles

- A slow control logic block is developed to communicate with lpGBT EC and IC control lanes.
  - The communication with GBT-SCA is successfully tested with the Xilinx KCU105 board.
  - The temperature monitoring can be performed using GBT-SCA.
- The logic is being integrated into EMP framework (Serenity firmware),
- We are also working on a fast diagnosis and response system to detect possible link issues and take automated actions in the firmware via the fast controls.