Contribution ID: **268** Type: **Experimental poster**

The ATLAS Hardware Track Trigger performance studies for the HL-LHC

Thursday 28 May 2020 18:45 (1 hour)

For the High-Luminosity LHC, planned to start in 2027, the ATLAS experiment will be equipped with the Hardware Tracking for the Trigger (HTT) system, a dedicated hardware system able to reconstruct tracks in the silicon detectors with short latency. The evolved TDAQ system design consists of a two-level hardware trigger in which the HTT is used in a low-latency mode (L1Track), providing tracks in regions of ATLAS at a rate of up to 4 MHz, with a latency of a few tens of micro-seconds. Different readout scenarios for the silicon pixel layers of the inner detector at 4 MHz are under study. While the full, bit-level simulation of the HTT is under development, a fast simulation was produced using parametrized track resolutions, to study the impact of L1Track reconstruction on physics benchmark channels. In this paper we describe the status of the ongoing HTT performance studies for the HL-LHC trigger menu, covering the impact on b-tagging and on muti-jets and leptonic signatures.

Author: CARVALHO, Ana Luisa (LIP (PT))

Presenter: CARVALHO, Ana Luisa (LIP (PT))

Session Classification: Poster Session (I)

Track Classification: Upgrade & Future