Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Liquid Argon Calorimeter

- Sampling calorimeter using liquid argon as active medium [1]
- EM barrel and EM end-cap are accordion geometry lead absorber plates
- Hadronic endcap calorimeters use conventional parallel plate copper electrodes
- Forward calorimeters use copper and tungsten absorbers
- Data-path:
  - Calorimeter Pulse → Preamplifier-Shaper → ADC → Off-detector FPGA
  - For HL-LHC, full readout chain—calibration, front-end, off-detector electronics—will be upgraded

Preamplifier-Shaper ASIC

- Preamplifier-Shaper amplifies and shapes pulses into two overlapping gain scales
- CR-RC² shaping and summing of four calorimeter channels across two gains
- Two proposed ASICs have been developed—LAUROC and ALFE
- Final pre-prototypes of both ASICs under study

ADC ASIC

- Several ASIC options under investigation to meet the stringent specifications
- Design requirements:
  - Sampling frequency: 40 MSPS
  - Dynamic range: 14 bits
  - Precision: 11 ENOB (effective number of bits)
  - Power: <100 mW per channel
  - Radiation hardness requirements [2]:

> | Parameter | Value |
> |-----------|-------|
> | ADC 1.36 | (2.15) |
> | 3.7 × 10⁶ | (2) |
> | 2.0 × 10⁵ | (2) |

A possible option: COLUTA ADC

- Eight digitizer channels—four DRE+SAR blocks, four MDAC+SAR blocks
- Dynamic Range Enhancer (DRE) with two gain modes (1x, 4x) to reach 14-bits
- Multiplying DAC (MDAC) is an alternative to the DRE
- 12-bit pipeline Successive Approximation Register (SAR) ADC
- Received first chips in December 2019, calibration and testing in progress

How to measure performance?

- Input a sine wave and digitize the signal at 40 MSPS
- Perform a Fast Fourier Transform (FFT—example on the left) to calculate the strength of the signal (power spectral density)
- Calculate the purity of the signal (SNDR) and extract ADC resolution (ENOB)

Calibration ASIC

- Delivers a calorimeter pulse with precisely known amplitude and shape close to calorimeter ionization to calibrate readout electronics
- Cover the 16-bit dynamic range with non-linearity < 0.1%
- CLAROC ASIC, a 16-bit DAC with four high-frequency switches with slow control chip configuration, has been developed to achieve necessary range and precision

FEB2 Prototype Boards

Analog Testboard (2019):
- Consists of two preamplifier-shaper (LAUROCV1) chips, two COLUTAV2 ADC chips, and one lpGBTv1 chip
- Provides two-channel readout, each with high/low gains
- Designed to be standalone, including on-board pulse generation
- First attempt at integrating and testing the front-end electronics

Slice Testboard (2020):
- Represents a “slice” of the final FEB2
- Goal: Demonstrate multi-channel performance, control links and radiation tolerant power
- Integrate components to read up to 32 calorimeter cells

Off-detector electronics

Lar Signal Processor (LASP):
- Receives the digitized waveforms, applies digital filtering, buffers and transmits data to the trigger and data acquisition (DAQ) systems
- Layout and design of the test board in progress

Lar Timing System (LATS):
- Distributes Trigger, Timing and Control based on lpGBT protocol
- Configures and monitors FEB2 and calibration boards
- Designed a development board to test communication links, estimate FPGA resources

References


Devanshu Panchal (University of Texas at Austin) on behalf of the ATLAS Collaboration