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picoTDC: A 3ps bin bize 64 channel TDC for HEP experiments

We present the ASIC development and test results of the picoTDC, a 64 channel time tagging Time-to-Digital Converter (TDC) with 3ps bin size. The ASIC runs from a single 40MHz reference clock, can be configured very flexible. Reference clock is fed to a PLL generating an internal 1.28GHz, then split into 256 phases through a 64 element DLL and a resistive interpolation resulting in the 3.05ps bin size. These clock phases then drive the capture registers of the 64 channels. To reduce the power consumption, the resistive interpolation can be disabled resulting in a bin size of 12.2ps. The digital logic of the ASIC is clocked at 320 MHZ thus it supports hit rates of up to 320MHz per channel, internal buffering and trigger matching as well as TOT measurements. The readout interface consists of four eight bit parallel interfaces with up to 320MHz data rate, resulting in a maximum readout rate of 10GBit/s or 320 million hits per second for the whole ASIC. In order to reduce the required readout bandwidth, a trigger functionality is implemented to read out only the interesting hits. Where this is not feasible, the data can also be read out triggerless. The TDC has been prototyped in a 65nm CMOS technology. First test results show an effective single-shot RMS resolution better than the bin size (3ps, including measurement jitter), but a higher mismatch between bins than expected. For the submission of the final production version the mismatch will be improved. Detailed measurements and functional tests of the final version will be available at the time of the conference.

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